19-0406; Rev 1; 12/05

EVALUATION KIT AVAILABLE

バックプレーンおよびケーブル用 1Gbps～12.5Gbpsパッシブイコライザ

概要

MAX3787は、FR4およびケーブルで発生する伝送媒体損失を補償する1Gbps～12.5Gbpsの等化回路です。この等化回路は受動部品のみで構成され、8b/10bまたはスクランブル信号にも同様に適切に機能します。MAX3787は1.5mm x 1.5mmの小型チップスケールパッケージ(UCSP™)で提供され、伝送媒体の途中の任意の場所に配置して高速相互接続のジッタマージンを増大することができます。MAX3787は0603部品2個とほぼ同じサイズで、容易かつ柔軟に配置と配線を行うことができます。

8.5Gbpsで、MAX3787は最長18インチのFR4と7mのケーブルの距離を補償します。12.5Gbpsで、MAX3787は最長12インチのFR4と3mのケーブルの距離を補償します。入力および出力インピーダンスは100Ω差動です。MAX3787は電源不要で、-40℃～+125℃の温度範囲で動作します。

アプリケーション

バックプレーン相互接続補償

ケーブル相互接続補償

チップ間リンク拡張

Ethernetおよびファイバチャネルシリアルモジュール

シャーシ寿命延長

UCSPはMaxim Integrated Products, Inc.の商標です。

特長

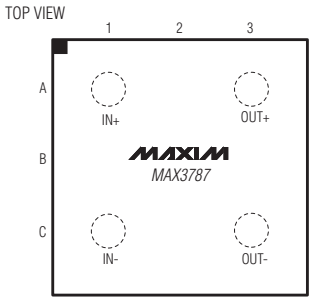
- ♦ 電源不要
- ♦ 1.5mm x 1.5mmの小型チップスケールパッケージ
- ♦ 受動等化によってISIを低減
- ♦ 1Gbps～12.5Gbpsで動作
- ♦ ボードリンクを延長
- ♦ ケーブルリンクを延長
- ♦ コーディングに無関係、8b/10b、またはスクランブル

型番

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX3787ABL	-40°C to +125°C	4 UCSP-4	AET
MAX3787ABL+	-40°C to +125°C	4 UCSP-4	AET

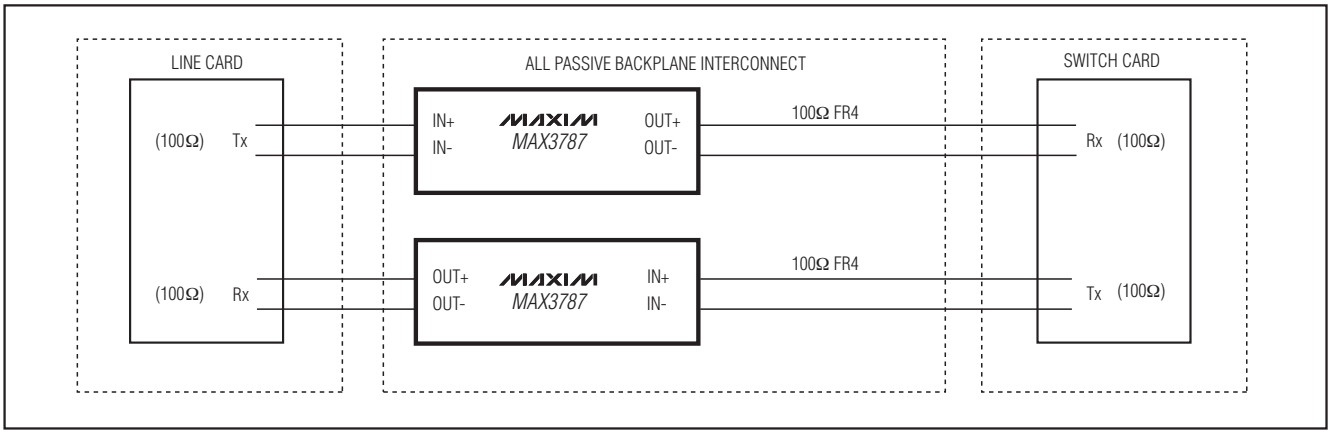
+は鉛フリーパッケージを示します。

ピン配置



UCSP

標準動作回路



標準動作回路はデータシートの最後に続いています。

ABSOLUTE MAXIMUM RATINGS

Voltage between (IN+ and OUT+) or (IN- and OUT-).....+2V
Voltage between (IN+ and IN-) or (OUT+ and OUT-).....+4V
Voltage between (IN+ and OUT-) or (IN- and OUT+).....+4V

Continuous Power Dissipation (T_A = +70°C)
4-Bump UCSP (derate 3.0mW/°C above +70°C).....238mW
Operating Junction Temperature.....+150°C
Storage Ambient Temperature Range .....-55°C to +150°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Ambient Temperature	T_A		-40	+25	+125	°C
Bit Rate		NRZ data	1		12.5	Gbps
CID Tolerance		Consecutive identical digits			100	Bits

ELECTRICAL CHARACTERISTICS

(Specifications guaranteed over specified operating conditions. Typical values measured at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current				0.0		mA
Input Swing		Measured differentially at point A in Figure 1			3600	mV_{P-P}
Compensation		5GHz relative to 100MHz		6		dB
Input Impedance		Differential, Z_{LOAD} = 100Ω		100		Ω
Output Impedance		Differential, Z_{SOURCE} = 100Ω		100		Ω
Through Response		Relative to ideal load, see Figure 2 for setup		See Figure 3 for limits		
Input Return Loss		100MHz to 6GHz		15		dB
Output Return Loss		100MHz to 6GHz		15		dB
Resistance IN+ to IN- and OUT+ to OUT-		No load, high impedance on all ports	112		152	Ω
Resistance IN+ to OUT+ and IN- to OUT-		No load, high impedance on all ports	32		44	Ω
Resistance IN+ to OUT- and IN- to OUT+		No load, high impedance on all ports	112		152	Ω
DC Gain (OUT/IN)		Z_{LOAD} = 100Ω		0.5		
Residual Deterministic Jitter (Table 1, Notes 1, 2)		3.125Gbps and 6.25Gbps, 18in of 6mil microstrip FR4		0.05		UI
		8.5Gbps, 10.0Gbps, and 12.5Gbps, 18in of 6mil microstrip FR4		0.10		

Note 1: Signal applied differentially at point A as shown in Figure 1. The deterministic jitter at point B is from media-induced loss, not from clock-source modulation. Deterministic jitter is measured at the 50% vertical level of the signal at point C.

Note 2: Difference in deterministic jitter between reference points A and C in Figure 1. Stress pattern: 2^7 PRBS, 100 zeros, 1, 0, 1, 0, 27 PRBS, 100 ones, 0, 1, 0, 1.

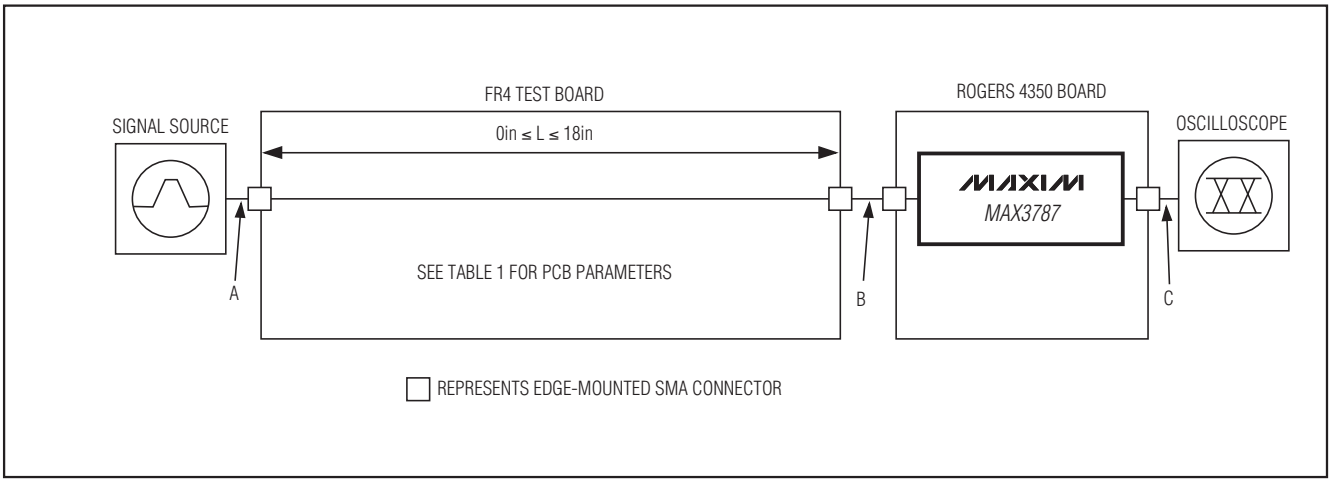


図1. 残留確定ジッタの試験回路

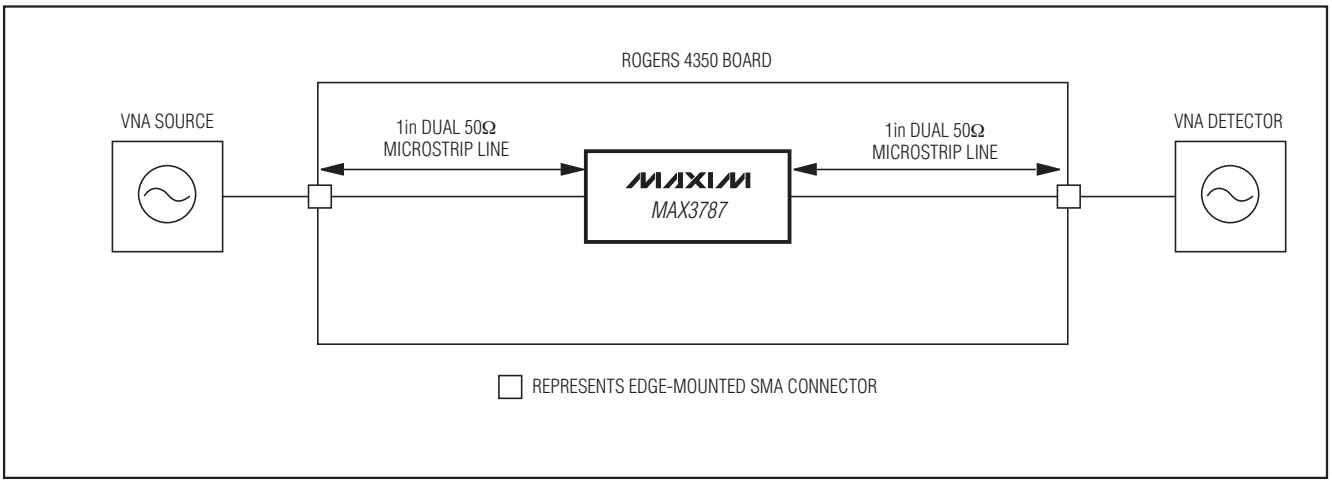


図2. ベクトルネットワークアナライザ(VNA)による周波数応答試験回路

FREQUENCY	MIN (dB)	TYP (dB)	MAX (dB)
100MHz	-8.2	-7.4	-6.8
200MHz	-7.9	-7.0	-6.4
300MHz	-7.5	-6.6	-6.0
500MHz	-6.8	-6.0	-5.3
1.0GHz	-5.5	-4.8	-4.2
2.0GHz	-4.2	-3.2	-2.5
3.0GHz	-3.1	-2.2	-1.5
4.0GHz	-2.3	-1.5	-0.8
5.0GHz	-2.1	-1.3	-0.5
5.5GHz	-2.4	-1.6	-0.6
6.0GHz	-2.9	-2.1	-1.1
6.5GHz	—	-2.6	—
7.0GHz	—	-3.1	—
7.5GHz	—	-3.6	—
8.0GHz	—	-4.1	—
8.5GHz	—	-4.7	—
9.0GHz	—	-5.5	—
9.5GHz	—	-7.0	—
10.0GHz	—	-9.0	—

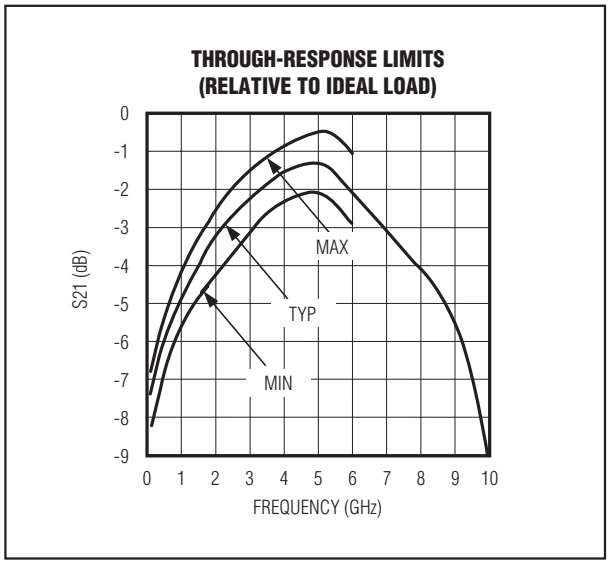


図3. スルー応答制限値

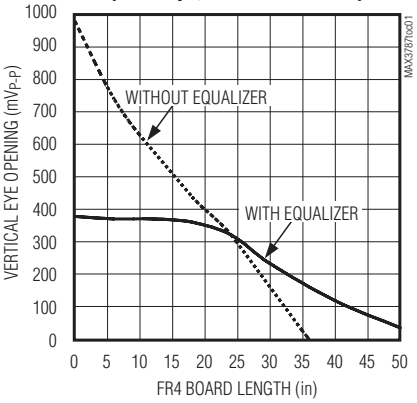
表1. PCBの仮定条件(ボード材はFR4)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Transmission Line	Edge-coupled microstrip line		6		mil
Relative Permittivity at 1GHz	FR4 or similar		4.0		—
Loss Tangent	FR4 or similar		0.02		—
Metal Thickness	1oz copper		1.4		mil
Impedance	Differential	90	100	110	Ω

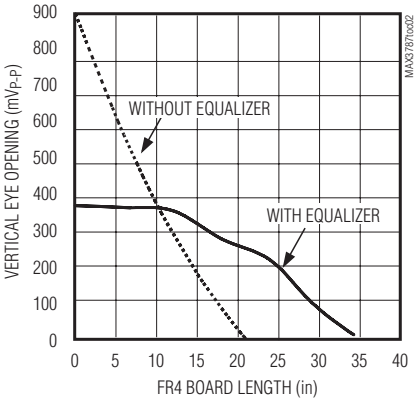
標準動作特性

(T_A = +25°C, unless otherwise noted. All measurements were done with $1V_{P-P}$ at the source. Stress pattern: 2^7 PRBS, 100 zeros, 1, 0, 1, 0, 2^7 PRBS, 100 ones, 0, 1, 0, 1. Residual deterministic jitter graphs were measured using Tektronix's FrameScan®. Deterministic jitter of the system was subtracted from the measured value. Eye diagrams acquired by FrameScan include deterministic jitter of the system (approximately 9ps) but not random jitter. Twin-ax cable: Amphenol Spectra-Strip® Skewclear® 100Ω 24AWG.)

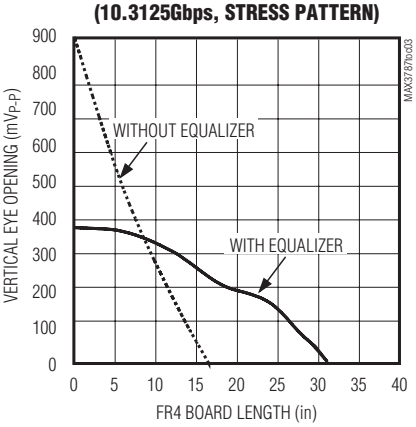
VERTICAL EYE OPENING vs. LENGTH (4.25Gbps, STRESS PATTERN)



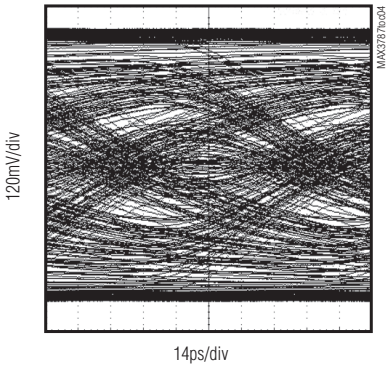
VERTICAL EYE OPENING vs. LENGTH (8.5Gbps, STRESS PATTERN)



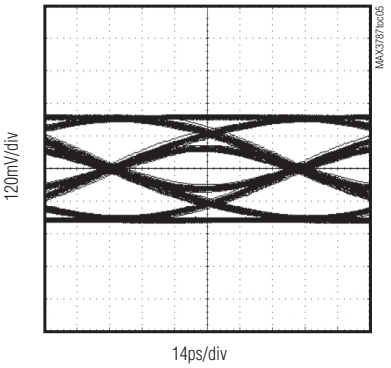
VERTICAL EYE OPENING vs. LENGTH (10.3125Gbps, STRESS PATTERN)



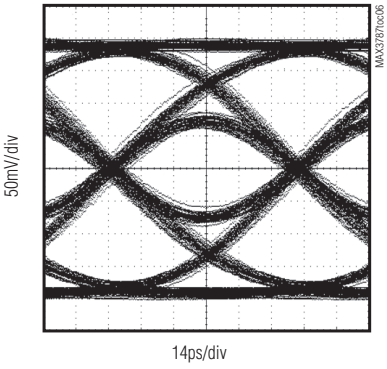
EYE DIAGRAM OF UNEQUALIZED SIGNAL (18in FR4, 12.5Gbps, STRESS PATTERN)



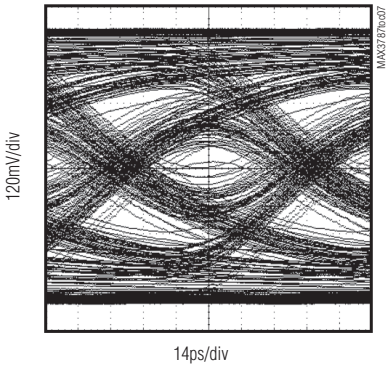
EYE DIAGRAM OF EQUALIZED SIGNAL (18in FR4, 12.5Gbps, STRESS PATTERN)



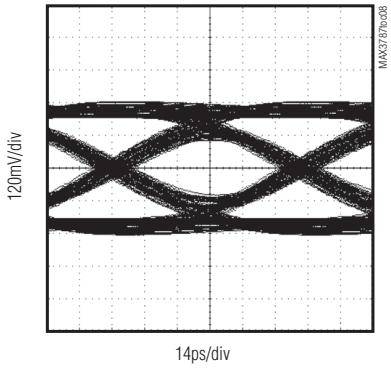
EYE DIAGRAM OF EQUALIZED SIGNAL (ZOOM) (18in FR4, 12.5Gbps, STRESS PATTERN)



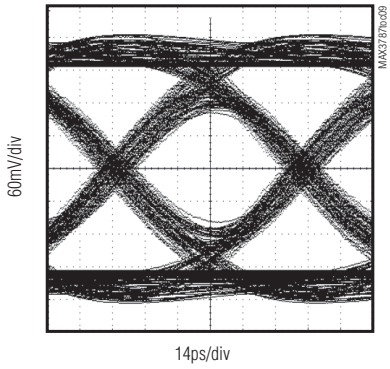
EYE DIAGRAM OF UNEQUALIZED SIGNAL (12in FR4, 12.5Gbps, STRESS PATTERN)



EYE DIAGRAM OF EQUALIZED SIGNAL (12in FR4, 12.5Gbps, STRESS PATTERN)



EYE DIAGRAM OF EQUALIZED SIGNAL (ZOOM) (12in FR4, 12.5Gbps, STRESS PATTERN)



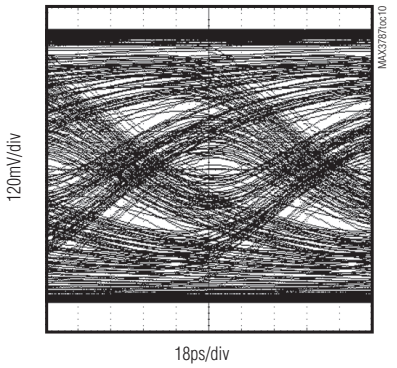
FrameScanはTektronixの登録商標です。

Spectra-StripおよびSkewclearは、Amphenolの登録商標です。

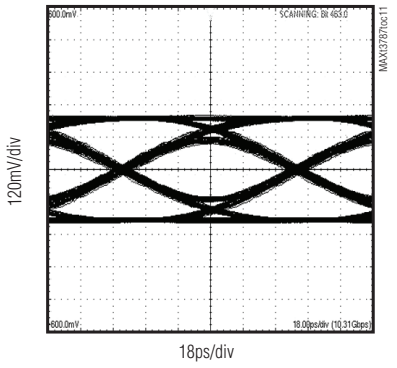
標準動作特性(続き)

(T_A = +25°C, unless otherwise noted. All measurements were done with $1V_{P-P}$ at the source. Stress pattern: 2^7 PRBS, 100 zeros, 1, 0, 1, 0, 2^7 PRBS, 100 ones, 0, 1, 0, 1. Residual deterministic jitter graphs were measured using Tektronix's FrameScan®. Deterministic jitter of the system was subtracted from the measured value. Eye diagrams acquired by FrameScan include deterministic jitter of the system (approximately 9ps) but not random jitter. Twin-ax cable: Amphenol Spectra-Strip® Skewclear® 100Ω 24AWG.)

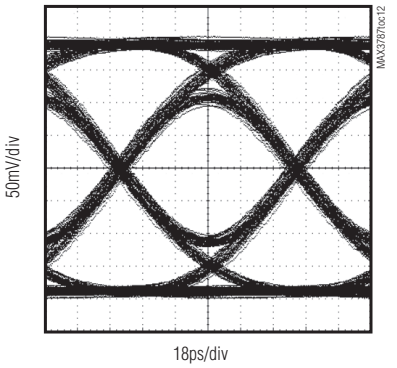
EYE DIAGRAM OF UNEQUALIZED SIGNAL (18in FR4, 10.3125Gbps, STRESS PATTERN)



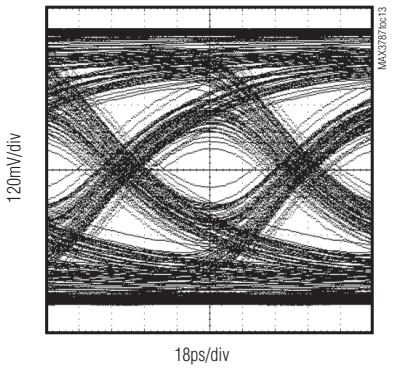
EYE DIAGRAM OF EQUALIZED SIGNAL (18in FR4, 10.3125Gbps, STRESS PATTERN)



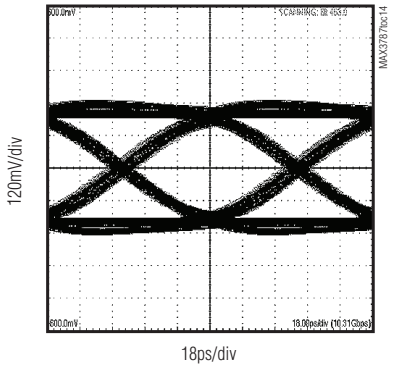
EYE DIAGRAM OF EQUALIZED SIGNAL (ZOOM) (18in FR4, 10.3125Gbps, STRESS PATTERN)



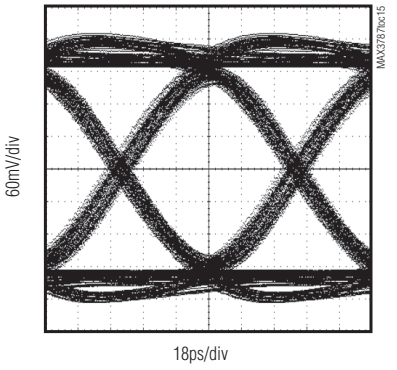
EYE DIAGRAM OF UNEQUALIZED SIGNAL (12in FR4, 10.3125Gbps, STRESS PATTERN)



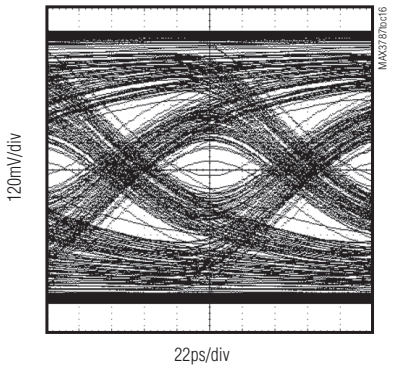
EYE DIAGRAM OF EQUALIZED SIGNAL (12in FR4, 10.3125Gbps, STRESS PATTERN)



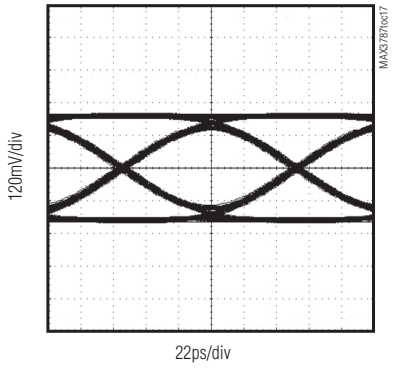
EYE DIAGRAM OF EQUALIZED SIGNAL (ZOOM) (12in FR4, 10.3125Gbps, STRESS PATTERN)



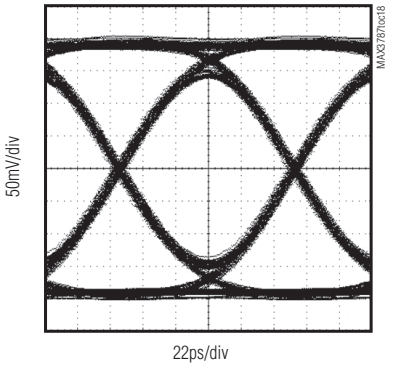
EYE DIAGRAM OF UNEQUALIZED SIGNAL (18in FR4, 8.5Gbps, STRESS PATTERN)



EYE DIAGRAM OF EQUALIZED SIGNAL (18in FR4, 8.5Gbps, STRESS PATTERN)



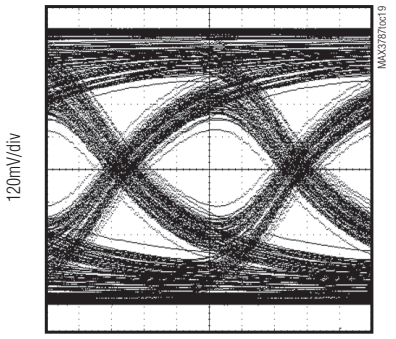
EYE DIAGRAM OF EQUALIZED SIGNAL (ZOOM) (18in FR4, 8.5Gbps, STRESS PATTERN)



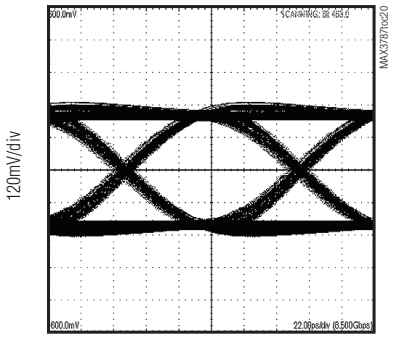
標準動作特性(続き)

(T_A = +25°C, unless otherwise noted. All measurements were done with $1V_{P-P}$ at the source. Stress pattern: 2^7 PRBS, 100 zeros, 1, 0, 1, 0, 2^7 PRBS, 100 ones, 0, 1, 0, 1. Residual deterministic jitter graphs were measured using Tektronix's FrameScan®. Deterministic jitter of the system was subtracted from the measured value. Eye diagrams acquired by FrameScan include deterministic jitter of the system (approximately 9ps) but not random jitter. Twin-ax cable: Amphenol Spectra-Strip® Skewclear® 100Ω 24AWG.)

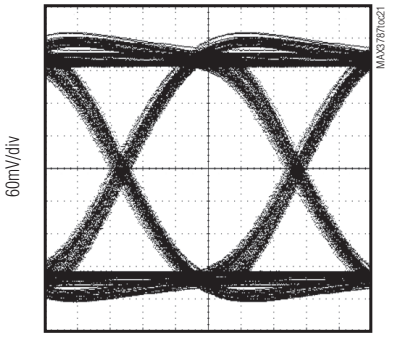
EYE DIAGRAM OF UNEQUALIZED SIGNAL (12in FR4, 8.5Gbps, STRESS PATTERN)



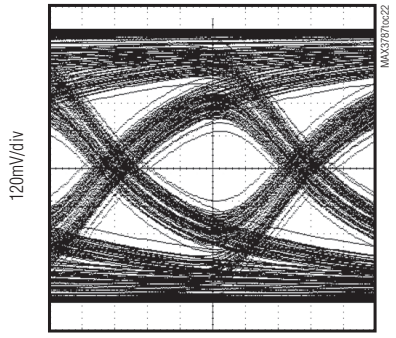
EYE DIAGRAM OF EQUALIZED SIGNAL (12in FR4, 8.5Gbps, STRESS PATTERN)



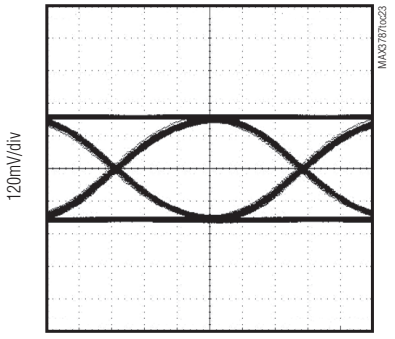
EYE DIAGRAM OF EQUALIZED SIGNAL (ZOOM) (12in FR4, 8.5Gbps, STRESS PATTERN)



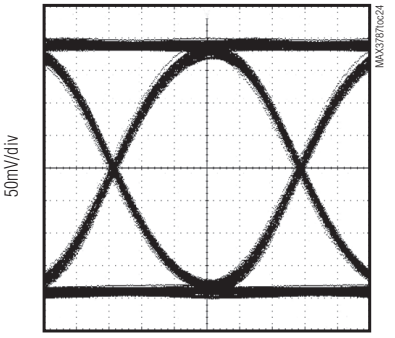
EYE DIAGRAM OF UNEQUALIZED SIGNAL (18in FR4, 6.25Gbps, STRESS PATTERN)



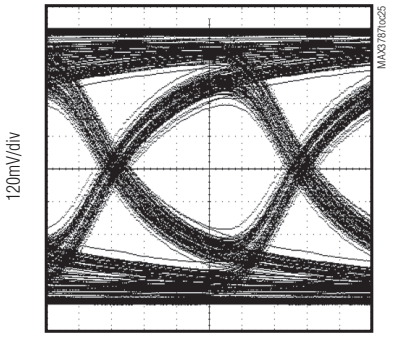
EYE DIAGRAM OF EQUALIZED SIGNAL (18in FR4, 6.25Gbps, STRESS PATTERN)



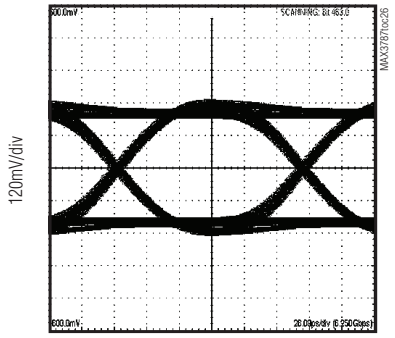
EYE DIAGRAM OF EQUALIZED SIGNAL (ZOOM) (18in FR4, 6.25Gbps, STRESS PATTERN)



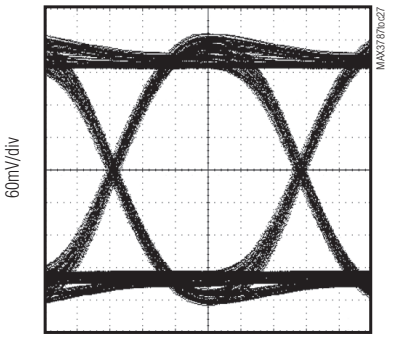
EYE DIAGRAM OF UNEQUALIZED SIGNAL (12in FR4, 6.25Gbps, STRESS PATTERN)



EYE DIAGRAM OF EQUALIZED SIGNAL (12in FR4, 6.25Gbps, STRESS PATTERN)



EYE DIAGRAM OF EQUALIZED SIGNAL (ZOOM) (12in FR4, 6.25Gbps, STRESS PATTERN)

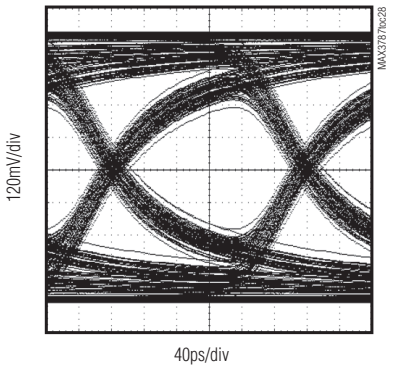


バックプレーンおよびケーブル用 1Gbps～12.5Gbpsパッシブイコライザ

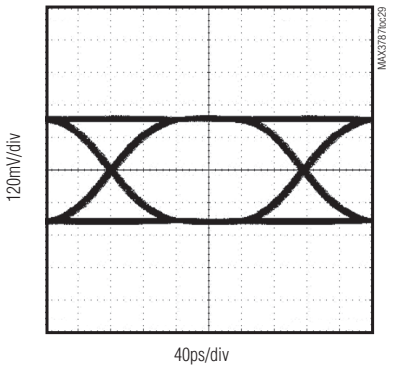
標準動作特性(続き)

(T_A = +25°C, unless otherwise noted. All measurements were done with $1V_{P-P}$ at the source. Stress pattern: 2^7 PRBS, 100 zeros, 1, 0, 1, 0, 2^7 PRBS, 100 ones, 0, 1, 0, 1. Residual deterministic jitter graphs were measured using Tektronix's FrameScan®. Deterministic jitter of the system was subtracted from the measured value. Eye diagrams acquired by FrameScan include deterministic jitter of the system (approximately 9ps) but not random jitter. Twin-ax cable: Amphenol Spectra-Strip® Skewclear® 100Ω 24AWG.)

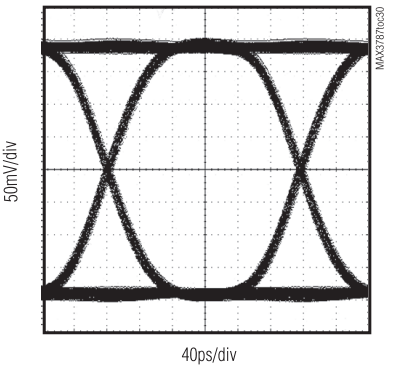
EYE DIAGRAM OF UNEQUALIZED SIGNAL (18in FR4, 4.25Gbps, STRESS PATTERN)



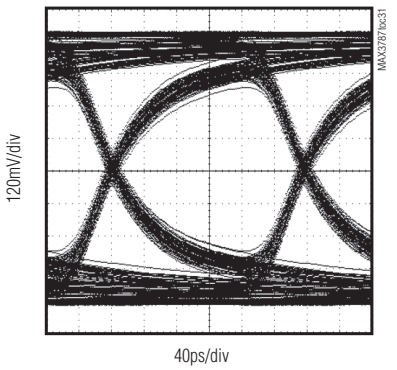
EYE DIAGRAM OF EQUALIZED SIGNAL (18in FR4, 4.25Gbps, STRESS PATTERN)



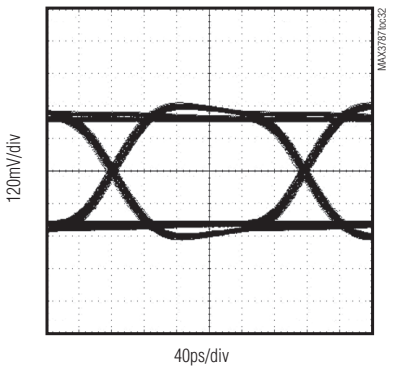
EYE DIAGRAM OF EQUALIZED SIGNAL (ZOOM) (18in FR4, 4.25Gbps, STRESS PATTERN)



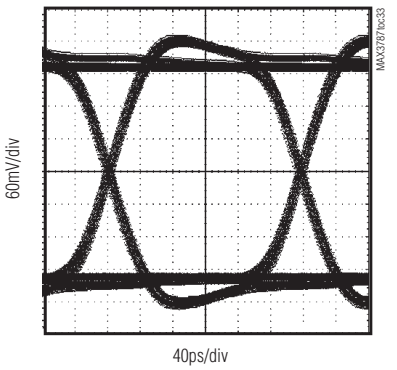
EYE DIAGRAM OF UNEQUALIZED SIGNAL (12in FR4, 4.25Gbps, STRESS PATTERN)



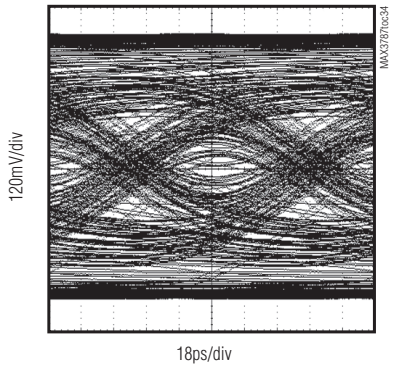
EYE DIAGRAM OF EQUALIZED SIGNAL (12in FR4, 4.25Gbps, STRESS PATTERN)



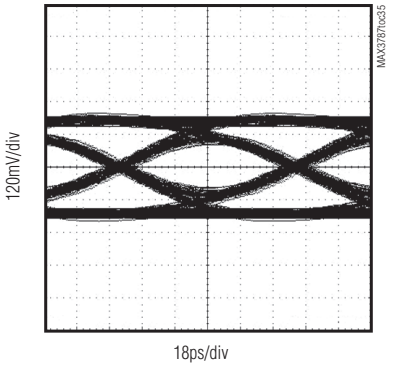
EYE DIAGRAM OF EQUALIZED SIGNAL (ZOOM) (12in FR4, 4.25Gbps, STRESS PATTERN)



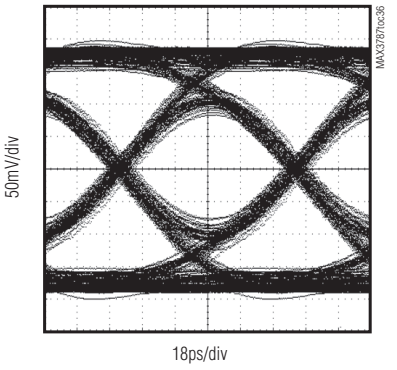
EYE DIAGRAM OF UNEQUALIZED SIGNAL (5m TWIN-AX CABLE, 10.3125Gbps, STRESS PATTERN)



EYE DIAGRAM OF EQUALIZED SIGNAL (5m TWIN-AX CABLE, 10.3125Gbps, STRESS PATTERN)



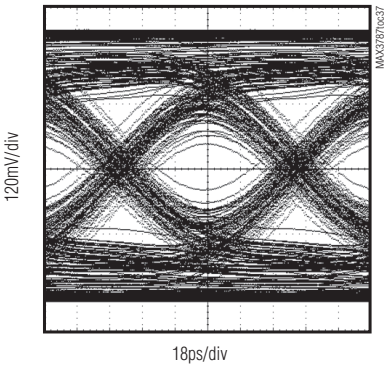
EYE DIAGRAM OF EQUALIZED SIGNAL (ZOOM) (5m TWIN-AX CABLE, 10.3125Gbps, STRESS PATTERN)



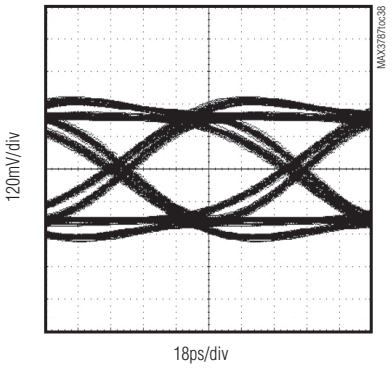
標準動作特性(続き)

(T_A = +25°C, unless otherwise noted. All measurements were done with $1V_{P-P}$ at the source. Stress pattern: 2^7 PRBS, 100 zeros, 1, 0, 1, 0, 2^7 PRBS, 100 ones, 0, 1, 0, 1. Residual deterministic jitter graphs were measured using Tektronix's FrameScan®. Deterministic jitter of the system was subtracted from the measured value. Eye diagrams acquired by FrameScan which include deterministic jitter of the system (approximately 9ps) but not random jitter. Twin-ax cable: Amphenol Spectra-Strip® Skewclear® 100Ω 24AWG.)

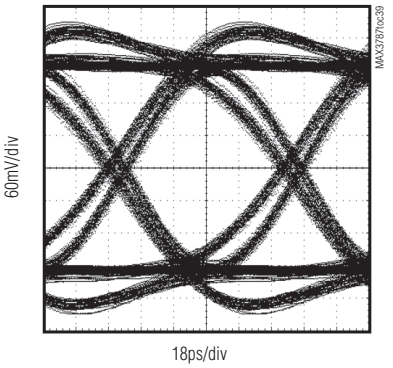
EYE DIAGRAM OF UNEQUALIZED SIGNAL (3m TWIN-AX CABLE, 10.3125Gbps, STRESS PATTERN)



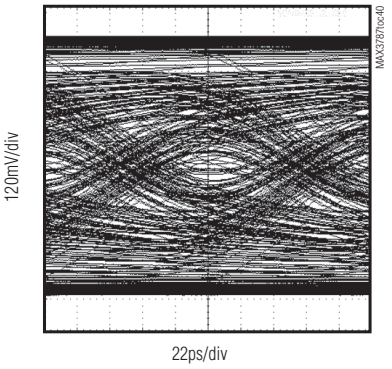
EYE DIAGRAM OF EQUALIZED SIGNAL (3m TWIN-AX CABLE, 10.3125Gbps, STRESS PATTERN)



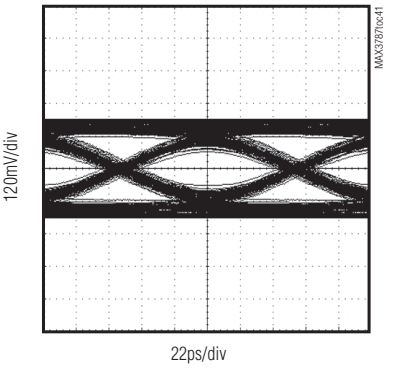
EYE DIAGRAM OF EQUALIZED SIGNAL (ZOOM) (3m TWIN-AX CABLE, 10.3125Gbps, STRESS PATTERN)



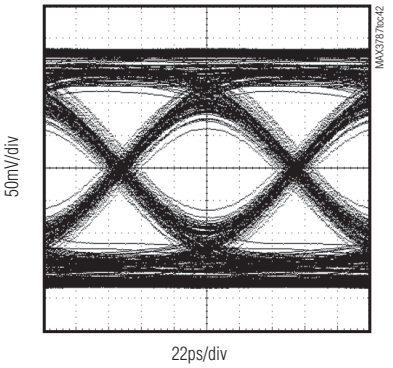
EYE DIAGRAM OF UNEQUALIZED SIGNAL (7m TWIN-AX CABLE, 8.5Gbps, STRESS PATTERN)



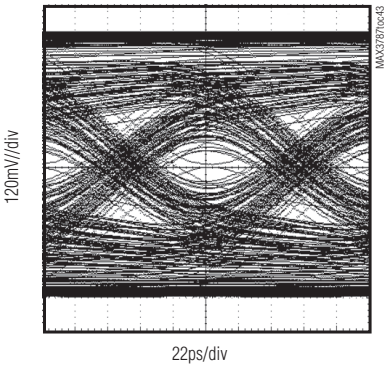
EYE DIAGRAM OF EQUALIZED SIGNAL (7m TWIN-AX CABLE, 8.5Gbps, STRESS PATTERN)



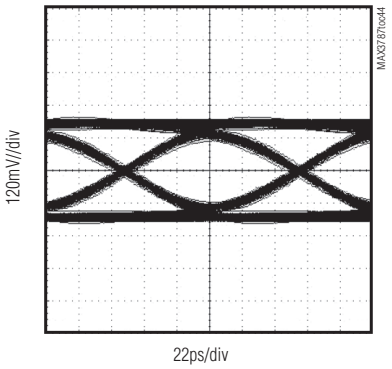
EYE DIAGRAM OF EQUALIZED SIGNAL (ZOOM) (7m TWIN-AX CABLE, 8.5Gbps, STRESS PATTERN)



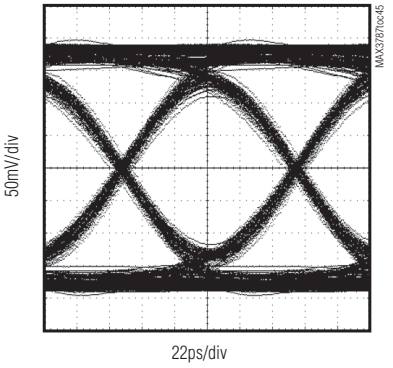
EYE DIAGRAM OF UNEQUALIZED SIGNAL (5m TWIN-AX CABLE, 8.5Gbps, STRESS PATTERN)



EYE DIAGRAM OF EQUALIZED SIGNAL (5m TWIN-AX CABLE, 8.5Gbps, STRESS PATTERN)



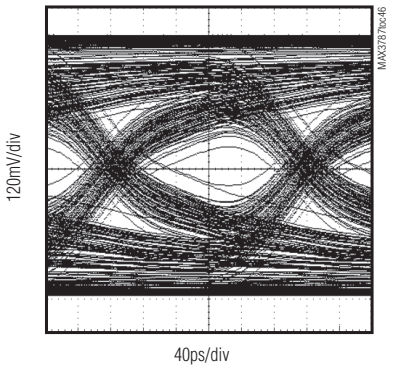
EYE DIAGRAM OF EQUALIZED SIGNAL (ZOOM) (5m TWIN-AX CABLE, 8.5Gbps, STRESS PATTERN)



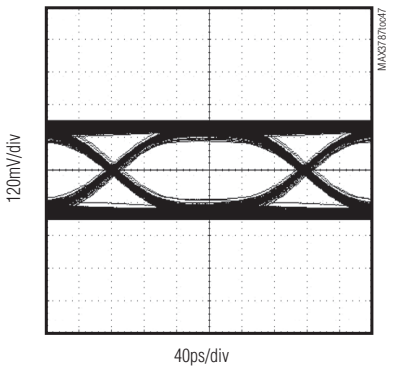
標準動作特性(続き)

(T_A = +25°C, unless otherwise noted. All measurements were done with $1V_{P-P}$ at the source. Stress pattern: 2^7 PRBS, 100 zeros, 1, 0, 1, 0, 2^7 PRBS, 100 ones, 0, 1, 0, 1. Residual deterministic jitter graphs were measured using Tektronix's FrameScan®. Deterministic jitter of the system was subtracted from the measured value. Eye diagrams acquired by FrameScan include deterministic jitter of the system (approximately 9ps) but not random jitter. Twin-ax cable: Amphenol Spectra-Strip® Skewclear® 100Ω 24AWG.)

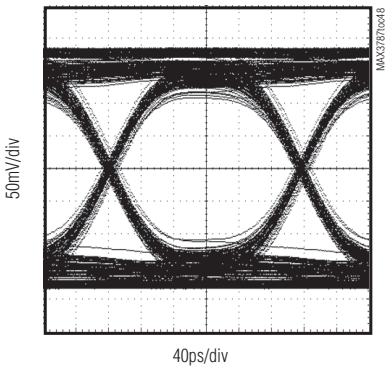
EYE DIAGRAM OF UNEQUALIZED SIGNAL (7m TWIN-AX CABLE, 4.25Gbps, STRESS PATTERN)



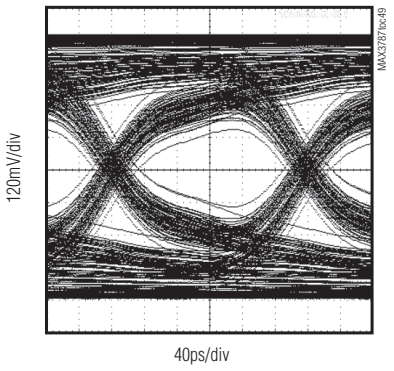
EYE DIAGRAM OF EQUALIZED SIGNAL (7m TWIN-AX CABLE, 4.25Gbps, STRESS PATTERN)



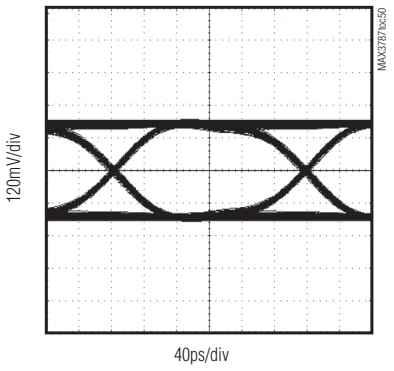
EYE DIAGRAM OF EQUALIZED SIGNAL (ZOOM) (7m TWIN-AX CABLE, 4.25Gbps, STRESS PATTERN)



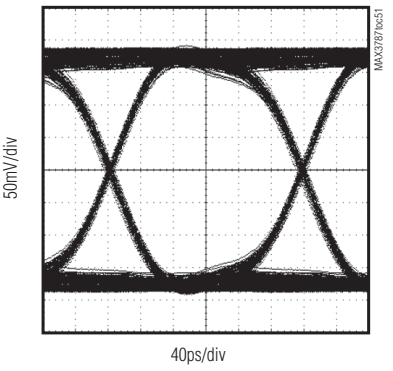
EYE DIAGRAM OF UNEQUALIZED SIGNAL (5m TWIN-AX CABLE, 4.25Gbps, STRESS PATTERN)



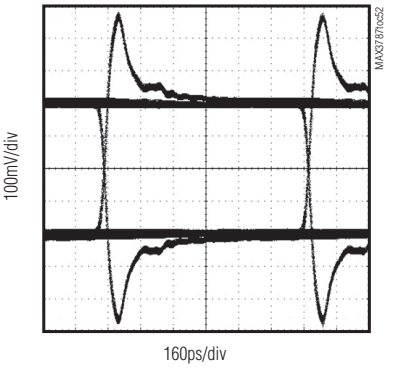
EYE DIAGRAM OF EQUALIZED SIGNAL (5m TWIN-AX CABLE, 4.25Gbps, STRESS PATTERN)



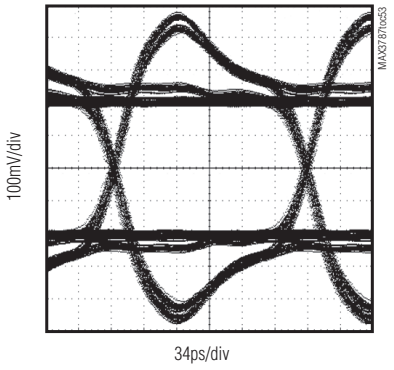
EYE DIAGRAM OF EQUALIZED SIGNAL (ZOOM) (5m TWIN-AX CABLE, 4.25Gbps, STRESS PATTERN)



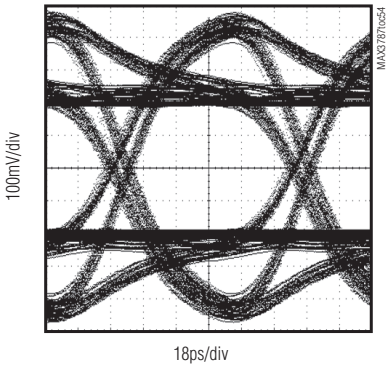
EYE DIAGRAM OF EQUALIZED SIGNAL (0in FR4, 1Gbps, STRESS PATTERN)



EYE DIAGRAM OF EQUALIZED SIGNAL (0in FR4, 5Gbps, STRESS PATTERN)



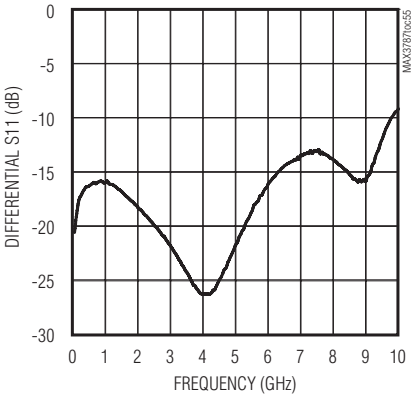
EYE DIAGRAM OF EQUALIZED SIGNAL (0in FR4, 10Gbps, STRESS PATTERN)



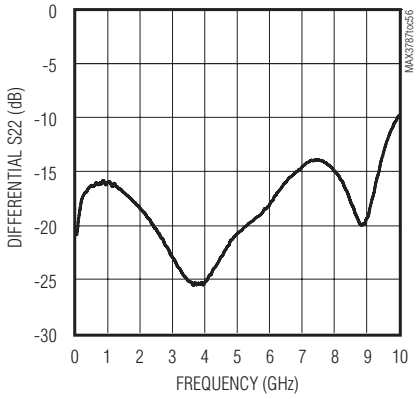
標準動作特性(続き)

(T_A = +25°C, unless otherwise noted. All measurements were done with $1V_{P-P}$ at the source. Stress pattern: 2^7 PRBS, 100 zeros, 1, 0, 1, 0, 2^7 PRBS, 100 ones, 0, 1, 0, 1. Residual deterministic jitter graphs were measured using Tektronix's FrameScan®. Deterministic jitter of the system was subtracted from the measured value. Eye diagrams acquired by FrameScan include deterministic jitter of the system (approximately 9ps) but not random jitter. Twin-ax cable: Amphenol Spectra-Strip® Skewclear® 100Ω 24AWG.)

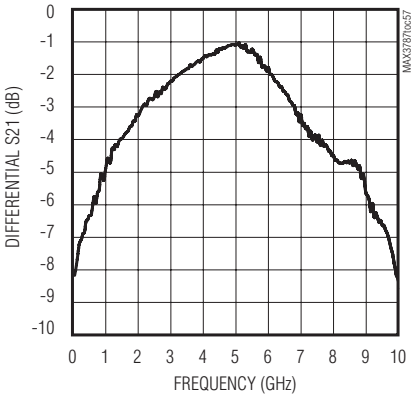
DIFFERENTIAL S11 vs. FREQUENCY



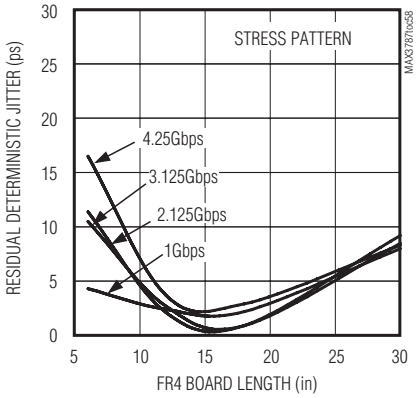
DIFFERENTIAL S22 vs. FREQUENCY



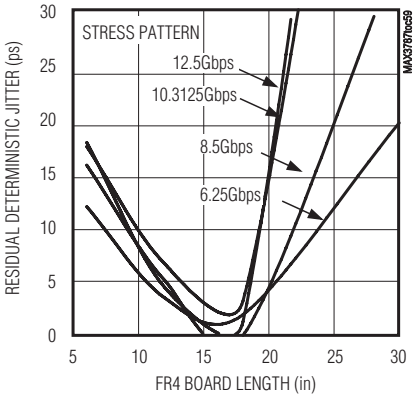
DIFFERENTIAL S21 vs. FREQUENCY



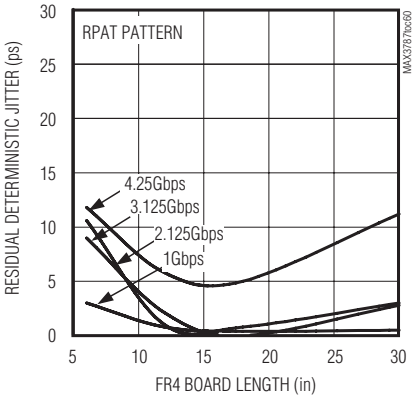
RESIDUAL DETERMINISTIC JITTER vs. FR4 BOARD LENGTH



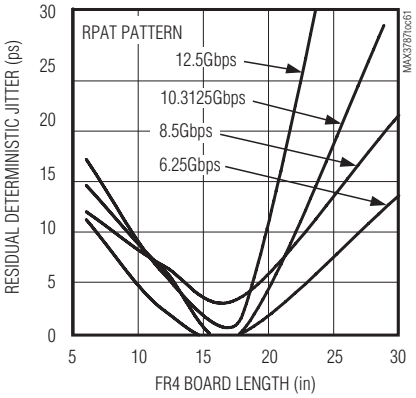
RESIDUAL DETERMINISTIC JITTER vs. FR4 BOARD LENGTH



RESIDUAL DETERMINISTIC JITTER vs. FR4 BOARD LENGTH



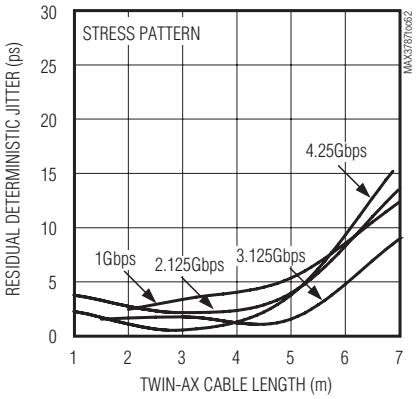
RESIDUAL DETERMINISTIC JITTER vs. FR4 BOARD LENGTH



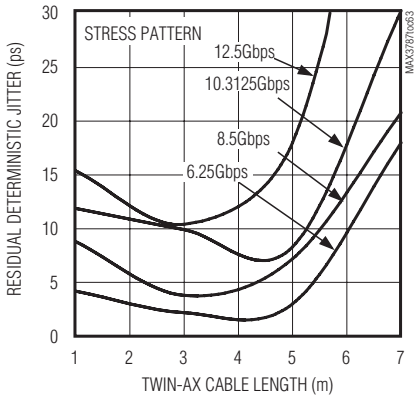
標準動作特性(続き)

(T_A = +25°C, unless otherwise noted. All measurements were done with $1V_{P-P}$ at the source. Stress pattern: 2^7 PRBS, 100 zeros, 1, 0, 1, 0, 2^7 PRBS, 100 ones, 0, 1, 0, 1. Residual deterministic jitter graphs were measured using Tektronix's FrameScan®. Deterministic jitter of the system was subtracted from the measured value. Eye diagrams acquired by FrameScan include deterministic jitter of the system (approximately 9ps) but not random jitter. Twin-ax cable: Amphenol Spectra-Strip® Skewclear® 100Ω 24AWG.)

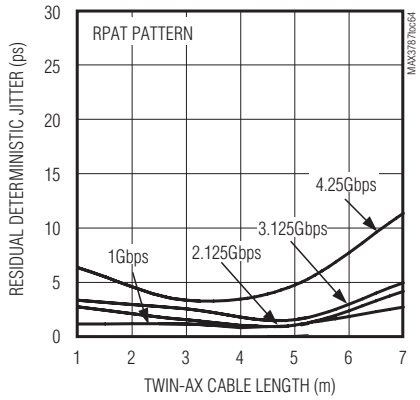
RESIDUAL DETERMINISTIC JITTER vs. TWIN-AX CABLE LENGTH



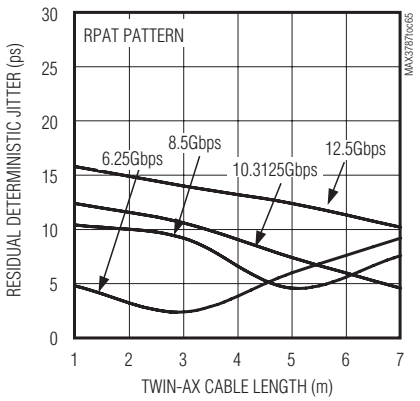
RESIDUAL DETERMINISTIC JITTER vs. TWIN-AX CABLE LENGTH



RESIDUAL DETERMINISTIC JITTER vs. TWIN-AX CABLE LENGTH



RESIDUAL DETERMINISTIC JITTER vs. TWIN-AX CABLE LENGTH



端子説明

端子	名称	機能
A1	IN+	正データ入力
A3	OUT+	正データ出力
C1	IN-	負データ入力
C3	OUT-	負データ出力

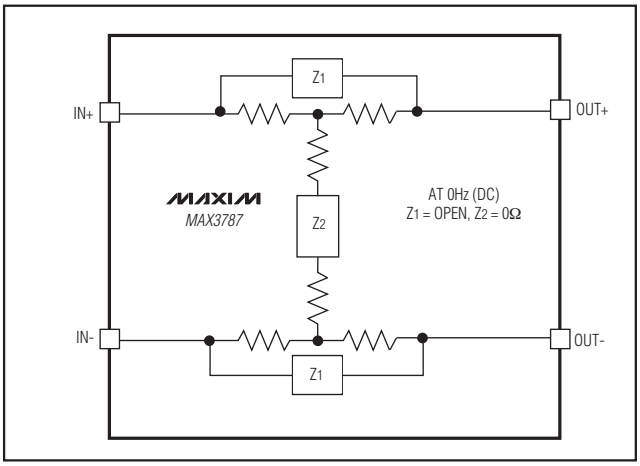


図4. ファンクションダイアグラム

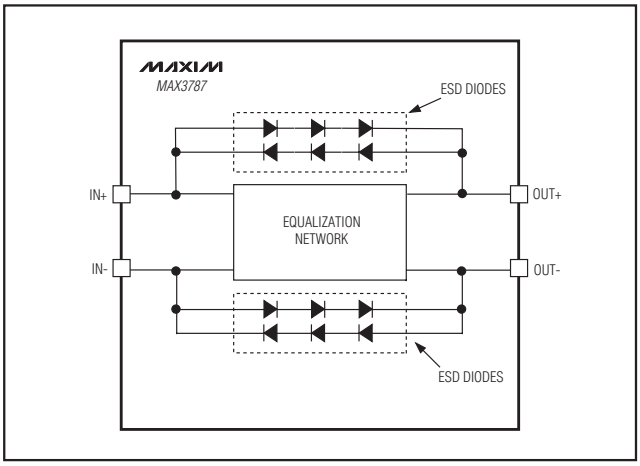


図5. ESD保護ダイオード

詳細

MAX3787は、抵抗成分と無効分から構成される完全受動回路です(図4)。ハイパス特性用のバイパスを備える2つの対称T型回路を使って、差動対称H型回路を構築します。回路全体は、FR4およびケーブルで発生する伝送媒体損失を補償するように特に調整されたフィルタとして機能します。

入力および出力終端

MAX3787の入力インピーダンスは、出力を100Ω差動負荷に接続した100Ω差動です。回路は100Ωバランス差動信号用に設計され、シングルエンド伝送用ではありません。

ESD保護ダイオード

MAX3787は、静電放電の場合に等化回路をバイパスするESDダイオードを内蔵しています(図5)。

アプリケーション情報

イコライザの統合および配置

MAX3787は1.5mm x 1.5mmの小型UCSPパッケージで提供され、伝送媒体の途中の任意の場所に配置することができます。サイズが小型であるため、柔軟に配置し、配線することができます。

等化回路が対称であるため、信号はINからOUT、またはOUTからINに同じ補償で通過することができます。また、イコライザは伝送媒体の先頭か末尾に配置され、同じ補償を受信回路で提供することができます。たとえば、送信パス用と受信パス用の2つのイコライザを1つのトランシーバモジュールに配置することができます(「標準動作回路」を参照)。

UCSPアセンブリに関して

UCSP構成、寸法、テープキャリア情報、PCB技術、バンプパッドレイアウト、および推奨リフロー温度プロファイルに関する最新アプリケーションの詳細、ならびに信頼性試験結果に関する最新情報については、マキシムのウェブサイト(japan.maxim-ic.com/ucsp)に掲載されたアプリケーションノート：「UCSP—ウェハレベルチップスケールパッケージ」を参照してください。

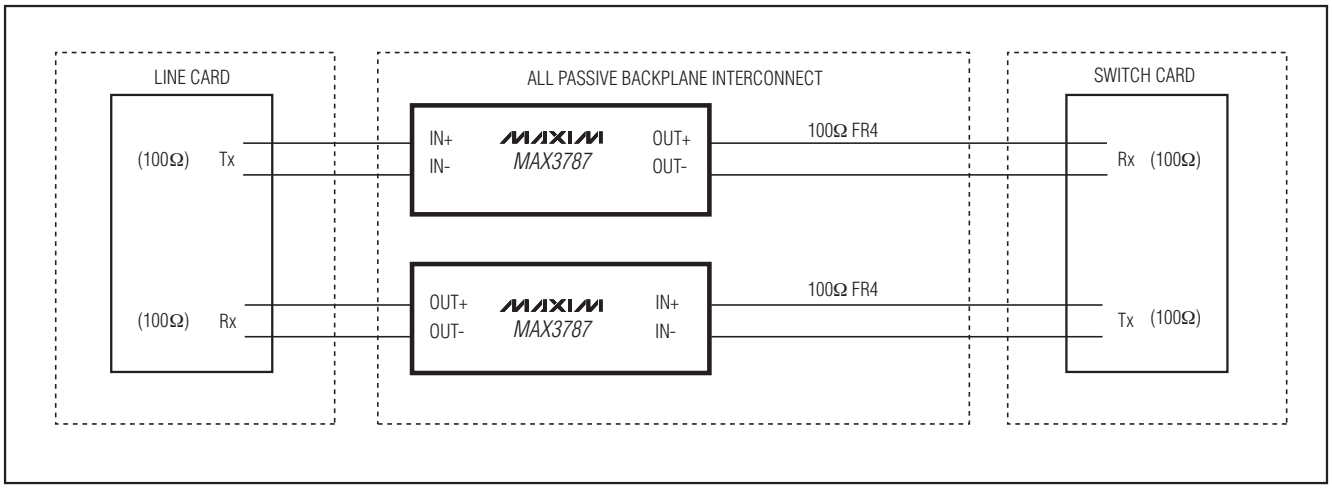
チップ情報

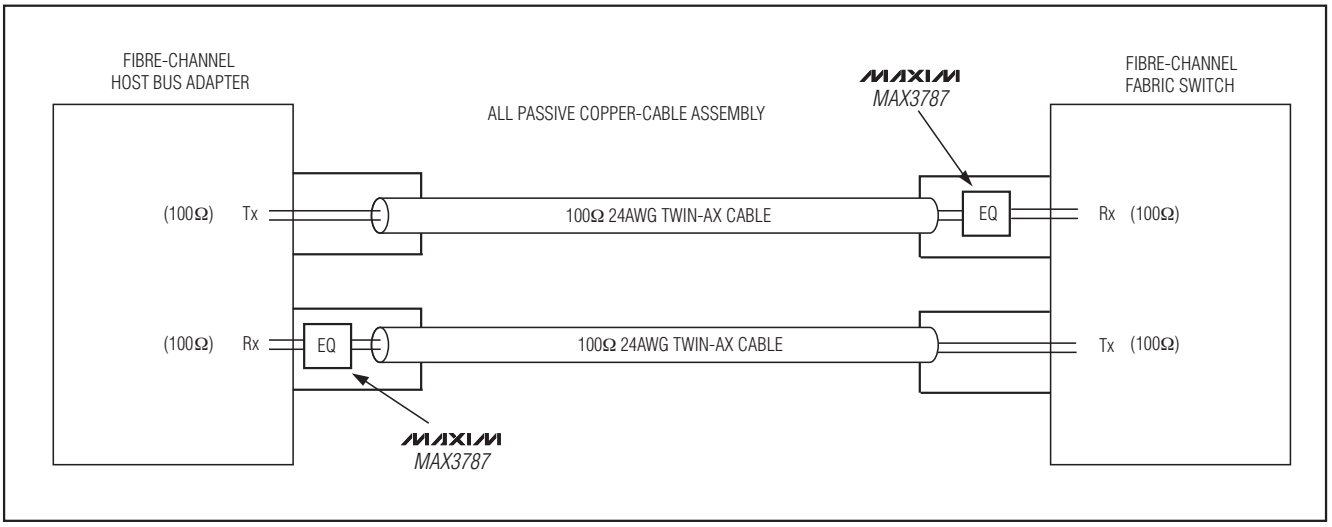
TRANSISTOR COUNT: 0

PROCESS: SiGe Bipolar

バックプレーンおよびケーブル用 1Gbps～12.5Gbpsパッシブイコライザ

標準動作回路(続き)

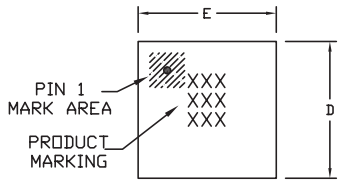




パッケージ

(このデータシートに掲載されているパッケージ仕様は、最新版が反映されているとは限りません。最新のパッケージ情報は、**japan.maxim-ic.com/packages**をご参照下さい。)

9LUCSP, 3x3.EPS

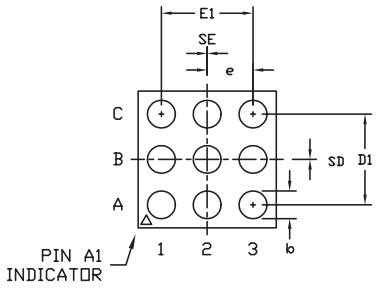


TOP VIEW

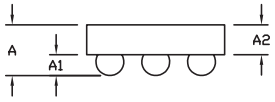
COMMON DIMENSIONS	
A	0.62+0.05-0.08
A1	0.29±0.02
A2	0.33 REF.
b	ø0.35±0.03
D1	1.00 BASIC
E1	1.00 BASIC
e	0.50 BASIC
SD	0.00 BASIC
SE	0.00 BASIC

PKG. CODE	VARIABLE DIMENSIONS		DEPOPULATED SOLDER BALLS
	D	E	
B9-1	1.52±0.05	1.52±0.05	NONE
B9-2	1.52±0.05	1.52±0.05	B2
B9-3	1.52±0.05	1.52±0.05	B1, B2, B3
B9-4	1.60±0.05	1.60±0.05	NONE
B9-5	1.60±0.05	1.60±0.05	B2
B9-6	1.60±0.05	1.60±0.05	B1, B2, B3
B9-7	1.52±0.05	1.52±0.05	A2, B1, B2, B3, C2

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. PRODUCT MARKING: NUMBER OF CHARACTERS AND LINES VARY PER PRODUCT.



BOTTOM VIEW



SIDE VIEW

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 3x3 UCSP

APPROVAL	DOCUMENT CONTROL NO.	REV.	
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