

## Microstrip and Stripline Design

### INTRODUCTION

Much has been written about terminating PCB traces in their characteristic impedance, to avoid signal reflections. However, it may not be clear when transmission line techniques are appropriate.

A good guideline to determine when the transmission line approach is necessary for logic signals is as follows:

*Terminate the transmission line in its characteristic impedance when the one-way propagation delay of the PCB track is equal to or greater than one-half the applied signal rise/fall time (whichever edge is faster).*

For example, a 2 inch microstrip line over an  $E_r = 4.0$  dielectric would have a delay of about 270 ps. Using the above rule strictly, termination would be appropriate whenever the signal rise time is less than approximately 500 ps.

*A more conservative rule is to use a 2 inch (PCB track length)/nanosecond (rise/fall time) rule. If the signal trace exceeds this trace-length/speed criterion, then termination should be used.*

For example, PCB tracks for high-speed logic with rise/fall time of 5 ns should be terminated in their characteristic impedance if the track length is equal to or greater than 10 inches (where measured length *includes* meanders).

In the analog domain, it is important to note that this same 2 inch/nanosecond guideline should also be used with op amps and other circuits, to determine the need for transmission line techniques. For instance, if an amplifier must output a maximum frequency of  $f_{\max}$ , then the equivalent risetime  $t_r$  is related to this  $f_{\max}$ . This limiting risetime,  $t_r$ , can be calculated as:

$$t_r = 0.35/f_{\max} \quad \text{Eq. 1}$$

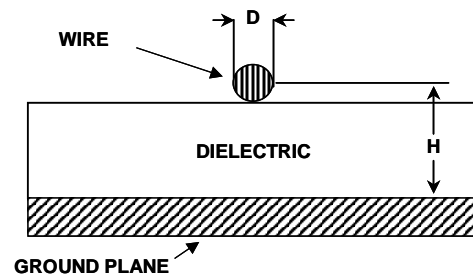
The maximum PCB track length is then calculated by multiplying  $t_r$  by 2 inch/nanosecond. For example, a maximum frequency of 100 MHz corresponds to a risetime of 3.5 ns, so a 7-inch or more track carrying this signal should be treated as a transmission line.

### DESIGNING CONTROLLED IMPEDANCES TRACES ON PCBs

A variety of trace geometries are possible with controlled impedance designs, and they may be either integral to or allied to the PCB pattern. In the discussions below, the basic patterns follow those of the IPC, as described in standard 2141A (see Reference 1).

Note that the figures below use the term "ground plane". It should be understood that this plane is in fact a large area, low impedance *reference* plane. In practice it may actually be either a ground plane or a power plane, both of which are assumed to be at zero ac potential.

The first of these is the simple wire-over-a-plane form of transmission line, also called a *wire microstrip*. A cross-sectional view is shown in Figure 1. This type of transmission line might be a signal wire used within a breadboard, for example. It is composed simply of a discrete insulated wire spaced a fixed distance over a ground plane. The dielectric would be either the insulation wall of the wire, or a combination of this insulation and air.



**Figure 1: A Wire Microstrip Transmission Line With Defined Impedance is Formed by an Insulated Wire Spaced From a Ground Plane**

The impedance of this line in ohms can be estimated with Eq. 2. Here  $D$  is the conductor diameter,  $H$  the wire spacing above the plane, and  $\epsilon_r$  the dielectric constant.

$$Z_0 (\Omega) = \frac{60}{\sqrt{\epsilon_r}} \ln \left[ \frac{4H}{D} \right]. \quad \text{Eq. 2}$$

For patterns integral to the PCB, there are a variety of geometric models from which to choose, single-ended and differential. These are covered in some detail within IPC standard 2141A (see Reference 1), but information on two popular examples is shown here.

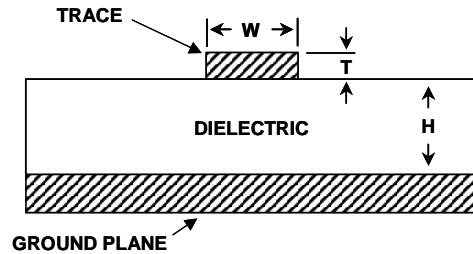
Before beginning any PCB-based transmission line design, it should be understood that there are abundant equations, all claiming to cover such designs. In this context, "Which of these are accurate?" is an extremely pertinent question. The unfortunate answer is, *none are perfectly so!* All of the existing equations are approximations, and thus accurate to varying degrees, depending upon specifics. The best known and most widely quoted equations are those of Reference 1, but even these come with application caveats.

Reference 2 has evaluated the Reference 1 equations for various geometric patterns against test PCB samples, finding that predicted accuracy varies according to target impedance. The equations quoted below are from Reference 1, and are offered here as a starting point for a design, subject to further analysis, testing and design verification. The bottom line is, study carefully, and take PCB trace impedance equations with a proper dose of salt.

**MICROSTRIP PCB TRANSMISSION LINES**

For a simple two-sided PCB design where one side is a ground plane, a signal trace on the other side can be designed for controlled impedance. This geometry is known as a *surface microstrip*, or more simply, *microstrip*.

A cross-sectional view of a two-layer PCB illustrates this microstrip geometry as shown in Figure 2.



**Figure 2: A Microstrip Transmission Line with Defined Impedance is Formed by a PCB Trace of Appropriate Geometry, Spaced from a Ground Plane**

For a given PCB laminate and copper weight, note that all parameters will be predetermined except for W, the width of the signal trace. Eq. 3 can then be used to design a PCB trace to match the impedance required by the circuit. For the signal trace of width W and thickness T, separated by distance H from a ground (or power) plane by a PCB dielectric with dielectric constant  $\epsilon_r$ , the characteristic impedance is:

$$Z_o(\Omega) = \frac{87}{\sqrt{\epsilon_r + 1.41}} \ln \left[ \frac{5.98H}{(0.8W + T)} \right] \tag{Eq. 3}$$

Note that in these expressions, measurements are in common dimensions (mils).

These transmission lines will have not only a characteristic impedance, but also capacitance. This can be calculated in terms of pF/in as shown in Eq. 4.

$$C_o(\text{pF/in}) = \frac{0.67(\epsilon_r + 1.41)}{\ln[5.98H/(0.8W + T)]} \tag{Eq. 4}$$

As an example including these calculations, a 2-layer board might use 20-mil wide (W), 1 ounce (T=1.4) copper traces separated by 10-mil (H) FR-4 ( $\epsilon_r = 4.0$ ) dielectric material. The resulting impedance for this microstrip would be about 50  $\Omega$ . For other standard impedances, for example the 75- $\Omega$  video standard, adjust "W" to about 8.3 mils.

## SOME MICROSTRIP GUIDELINES

This example touches an interesting and quite handy point. Reference 2 discusses a useful guideline pertaining to microstrip PCB impedance. For a case of dielectric constant of 4.0 (FR-4), it turns out that when  $W/H$  is 2/1, the resulting impedance will be close to  $50 \Omega$  (as in the first example, with  $W = 20$  mils).

Careful readers will note that Eq. 3 predicts  $Z_o$  to be about  $46 \Omega$ , generally consistent with accuracy quoted in Reference 2 (>5%). The IPC microstrip equation is most accurate between  $50 \Omega$  and  $100 \Omega$ , but is substantially less so for lower (or higher) impedances.

The propagation delay of the microstrip line can also be calculated, as per Eq. 5. This is the one-way transit time for a microstrip signal trace. Interestingly, for a given geometry model, *the delay constant in ns/ft is a function only of the dielectric constant, and not the trace dimensions* (see Reference 6). Note that this is quite a convenient situation. It means that, with a given PCB laminate (and given  $\epsilon_r$ ), the propagation delay constant is fixed for various impedance lines.

$$t_{pd}(\text{ns/ft}) = 1.017\sqrt{0.475\epsilon_r + 0.67} \quad \text{Eq. 5}$$

This delay constant can also be expressed in terms of ps/in, a form which will be more practical for smaller PCBs. This is:

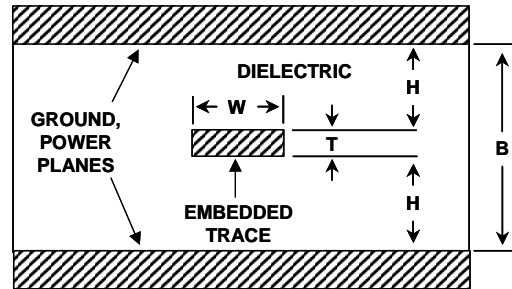
$$t_{pd}(\text{ps/in}) = 85\sqrt{0.475\epsilon_r + 0.67} \quad \text{Eq. 6}$$

Thus for an example PCB dielectric constant of 4.0, it can be noted that a microstrip's delay constant is about 1.63 ns/ft, or 136 ps/in. These two additional rules-of-thumb can be useful in designing the timing of signals across PCB trace runs.

## SYMMETRIC STRIPLINE PCB TRANSMISSION LINES

A method of PCB design preferred from many viewpoints is a multi-layer PCB. This arrangement *embeds* the signal trace between a power and a ground plane, as shown in the cross-sectional view of Figure 3. The low-impedance ac-ground planes and the embedded signal trace form a *symmetric stripline* transmission line.

As can be noted from the figure, the return current path for a high frequency signal trace is located directly above and below the signal trace on the ground/power planes. The high frequency signal is thus contained entirely inside the PCB, minimizing emissions, and providing natural shielding against incoming spurious signals.



**Figure 3: A Symmetric Stripline Transmission Line With Defined Impedance is Formed by a PCB Trace of Appropriate Geometry Embedded Between Equally Spaced Ground and/or Power Planes**

The characteristic impedance of this arrangement is again dependent upon geometry and the  $\epsilon_r$  of the PCB dielectric. An expression for  $Z_0$  of the stripline transmission line is:

$$Z_0(\Omega) = \frac{60}{\sqrt{\epsilon_r}} \ln \left[ \frac{1.9(B)}{(0.8W + T)} \right] \quad \text{Eq. 7}$$

Here, all dimensions are again in mils, and B is the spacing between the two planes. In this symmetric geometry, note that B is also equal to  $2H + T$ . Reference 2 indicates that the accuracy of this Reference 1 equation is typically on the order of 6%.

Another handy guideline for the symmetric stripline in an  $\epsilon_r = 4.0$  case is to make B a multiple of W, in the range of 2 to 2.2. This will result in an stripline impedance of about 50  $\Omega$ . Of course this rule is based on a further approximation, by neglecting T. Nevertheless, it is still useful for ballpark estimates.

The symmetric stripline also has a characteristic capacitance, which can be calculated in terms of pF/in as shown in Eq. 8.

$$C_0(\text{pF/in}) = \frac{1.41(\epsilon_r)}{\ln[3.81H/(0.8W + T)]} \quad \text{Eq. 8}$$

The propagation delay of the symmetric stripline is shown in Eq. 9.

$$t_{pd}(\text{ns/ft}) = 1.017\sqrt{\epsilon_r} \quad \text{Eq. 9}$$

or, in terms of ps:

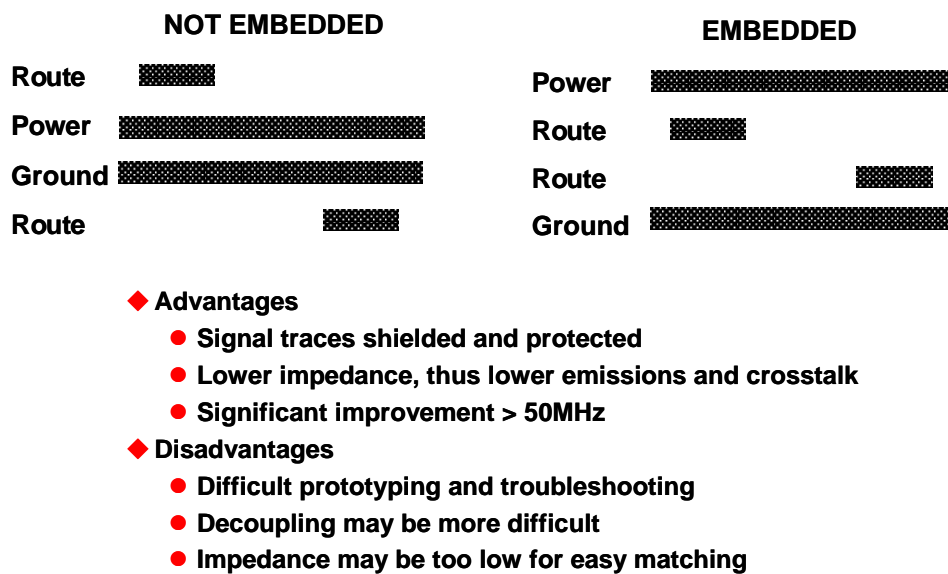
$$t_{pd}(\text{ps/in}) = 85\sqrt{\epsilon_r} \quad \text{Eq. 10}$$

For a PCB dielectric constant of 4.0, it can be noted that the symmetric stripline's delay constant is almost exactly 2 ns/ft, or 170 ps/in.

### SOME PROS AND CONS OF EMBEDDING TRACES

The above discussions allow the design of PCB traces of defined impedance, either on a surface layer or embedded between layers. There of course are many other considerations beyond these impedance issues.

Embedded signals do have one major and obvious disadvantage—the debugging of the hidden circuit traces is difficult to impossible. Some of the pros and cons of embedded signal traces are summarized in Figure 4.



**Figure 4: The Pros and Cons of Not Embedding Vs. the Embedding of Signal Traces in Multi-Layer PCB Designs**

Multi-layer PCBs can be designed *without* the use of embedded traces, as is shown in the left-most cross-sectional example. This embedded case could be considered as a doubled two-layer PCB design (i.e., four copper layers overall). The routed traces at the top form a microstrip with the power plane, while the traces at the bottom form a microstrip with the ground plane. In this example, the signal traces of both outer layers are readily accessible for measurement and troubleshooting purposes. But, the arrangement does nothing to take advantage of the shielding properties of the planes.

This non embedded arrangement will have greater emissions and susceptibility to external signals, vis-a-vis the embedded case at the right, which uses the embedding, and does take full advantage of the planes. As in many other engineering efforts, the decision of embedded vs. not-embedded for the PCB design becomes a tradeoff, in this case one of reduced emissions vs. ease of testing.

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