

Electrostatic Discharge (ESD)

OUT-OF-CIRCUIT OVERVOLTAGE PROTECTION FROM ESD

Linear ICs such as op amps, in-amps, and data converters be protected prior to the time that they are mounted to a printed circuit board. That is an *out-of-circuit* state. In such a condition, ICs are completely at the mercy of their environment as to what stressful voltage surges they may see. Most often the harmful voltage surges come from *electrostatic discharge*, or, as more commonly referenced, ESD. This is a single, fast, high current transfer of electrostatic charge resulting from one of two conditions. These conditions are:

1. Direct contact transfer between two objects at different potentials (sometimes called contact discharge)
2. A high electrostatic field between two objects when they are in close proximity (sometimes called air discharge)

The prime sources of static electricity are mostly insulators and are typically synthetic materials, e.g., vinyl or plastic work surfaces, insulated shoes, finished wood chairs, Scotch tape, bubble pack, soldering irons with ungrounded tips, etc. Voltage levels generated by these sources can be extremely high since their charge is not readily distributed over their surfaces or conducted to other objects. The generation of static electricity caused by rubbing two substances together is called the *triboelectric* effect. Some common examples of ordinary acts producing significant ESD voltages are shown in Figure 1.

- ◆ **Walking Across a Carpet**
1000V - 1500V
- ◆ **Walking Across a Vinyl Floor**
150V - 250V
- ◆ **Handling Material Protected by Clear Plastic Covers**
400V - 600V
- ◆ **Handling Polyethylene Bags**
1000V - 2000V
- ◆ **Pouring Polyurethane Foam Into a Box**
1200V - 1500V
- ◆ **Note: Above Assumes 60% RH. For Low RH (30%), Voltages Can Be > 10 Times**

Figure 1: ESD Voltages Generated By Various Ordinary Circumstances

ICs can be damaged by the high voltages and high peak currents generated by ESD. Precision analog circuits, often featuring very low bias currents, are more susceptible to damage than common digital circuits, because traditional input-protection structures which protect against ESD damage increase input leakage—and thus can't be used.

For the design engineer or technician, the most common manifestation of ESD damage is a catastrophic failure of the IC. However, exposure to ESD can also cause increased leakage or degrade other parameters. If a device appears to not meet a data sheet specification during evaluation, the possibility of ESD damage should be considered. Figure 2 outlines some relevant points on ESD induced failures.

◆ **ESD Failure Mechanisms:**

- **Dielectric or junction damage**
- **Surface charge accumulation**
- **Conductor fusing**

◆ **ESD Damage Can Cause:**

- **Increased leakage**
- **Degradation in performance**
- **Functional failures of ICs**

◆ **ESD Damage is often Cumulative:**

- **For example, each ESD "zap" may increase junction damage until, finally, the device fails.**

Figure 2: Understanding ESD damage

All ESD-sensitive devices are shipped in protective packaging. ICs are usually contained in either conductive foam or antistatic shipping tubes, and the container is then sealed in a static-dissipative plastic bag. The sealed bag is marked with a distinctive sticker, such as in Figure 3, which outlines the appropriate handling procedures.

The presence of outside package notices such as those shown in Figure 3 is notice to the user that device handling procedures appropriate for ESD protection are necessary.

In addition, data sheets for ESD-sensitive ICs generally have a bold statement to that effect, as shown in Figure 4.

All static sensitive devices are sealed in protective packaging and marked with special handling instructions



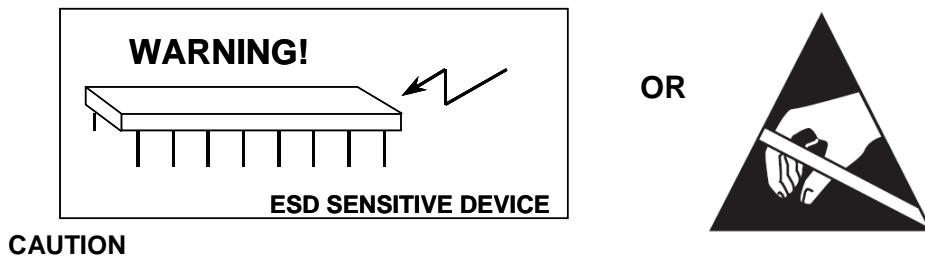
CAUTION

SENSITIVE ELECTRONIC DEVICES SENSITIVE ELECTRONIC DEVICES

DO NOT SHIP OR STORE NEAR STRONG ELECTROSTATIC, ELECTROMAGNETIC, MAGNETIC, OR RADIOACTIVE FIELDS

DO NOT OPEN EXCEPT AT APPROVED FIELD FORCE PROTECTIVE WORK STATION

Figure 3: Recognizing ESD-Sensitive Devices by Package and Labeling



CAUTION

ESD (Electrostatic Discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADXXX features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Figure 4: ESD Data Sheet Statement for Linear ICs

Once ESD-sensitive devices are identified, protection is relatively easy. Obviously, keeping ICs in their original protective packages as long as possible is a first step. A second step is discharging potentially damaging ESD sources before IC damage occurs. Discharging such voltages can be done quickly and safely, through a high impedance.

A key component required for ESD-safe IC handling is a workbench with a static-dissipative surface, shown in the workstation of Figure 5. The surface is connected to ground through a $1\text{ M}\Omega$ resistor, which dissipates any static charge, while protecting the user from electrical

ground fault shock hazards. If existing bench tops are nonconductive, a static-dissipative mat should be added, along with the discharge resistor.

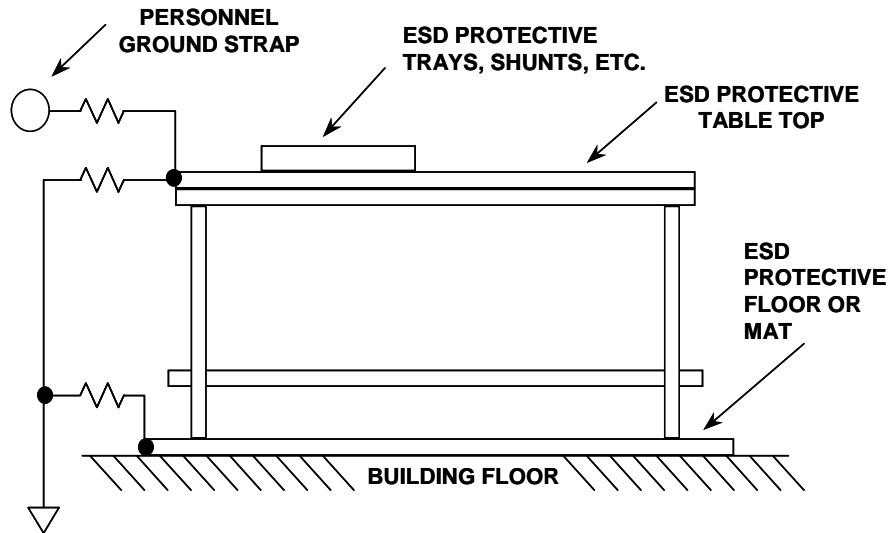


Figure 5: A Workstation Environment Suitable for Handling ESD-Sensitive ICs

Note that the surface of the workbench has a moderately high sheet resistance. It is neither necessary nor desirable to use a low-resistance surface (such as a sheet of copper-clad PC board) for the work surface. Remember, a high peak current may flow if a charged IC is discharged through a low impedance. This is precisely what happens when a charged IC contacts a grounded copper clad board. When the same charged IC is placed on the high impedance surface of Figure 5 however, the peak current isn't high enough to damage the device.

Several personnel handling techniques are keys to minimizing ESD-related damage. At the workstation, a conductive wrist strap is recommended while handling ESD-sensitive devices. The wrist strap ensures that normal tasks, such as peeling tape from packages, won't cause IC damage. Again, a $1\text{ M}\Omega$ resistor, from the wrist strap to ground, is required for safety. When building prototype breadboards or assembling PC boards which contain ESD-sensitive ICs, all passive components should be inserted and soldered before the ICs. This minimizes the ESD exposure of the sensitive devices. The soldering iron must, of course, have a grounded tip.

Protecting ICs from ESD requires the participation of both the IC manufacturer and the customer. IC manufacturers have a vested interest in providing the highest possible level of ESD protection for their products. IC circuit designers, process engineers, packaging specialists and others are constantly looking for new and improved circuit designs, processes, and packaging methods to withstand or shunt ESD energy.

A complete ESD protection plan, however, requires more than building ESD protection into ICs. The users of ICs must also provide their employees with the necessary knowledge of and training

in ESD handling procedures, so that protection can be built in at all key points along the way, as outlined in Figure 6.

ANALOG DEVICES:

- **Circuit Design and Fabrication -**
 - ↓ **Design and manufacture products with the highest level of ESD protection consistent with required analog and digital performance.**

- **Pack and Ship -**
 - ↓ **Pack in static dissipative material. Mark packages with ESD warning.**

CUSTOMERS:

- **Incoming Inspection -**
 - ↓ **Inspect at grounded workstation. Minimize handling.**

- **Inventory Control -**
 - ↓ **Store in original ESD-safe packaging. Minimize handling.**

- **Manufacturing -**
 - ↓ **Deliver to work area in original ESD-safe packaging. Open packages only at grounded workstation. Package subassemblies in static dissipative packaging.**

- **Pack and Ship -**
 - Pack in static dissipative material if required. Replacement or optional boards may require special attention.**

Figure 6: ESD Protection Requires a Partner Relationship Between ADI and the End Customer With Control at Key Points

Special care should be taken when breadboarding and evaluating ICs. The effects of ESD damage can be cumulative, so repeated mishandling of a device can eventually cause a failure. Inserting and removing ICs from a test socket, storing devices during evaluation, and adding or removing external components on the breadboard should all be done while observing proper ESD precautions. Again, if a device fails during a prototype system development, repeated ESD stress may be the cause.

The key word to remember with respect to ESD is *prevention*. There is no way to undo ESD damage, or to compensate for its effects.

ESD MODELS AND TESTING

Some applications have higher sensitivity to ESD than others. ICs which are located on a PC board surrounded by other circuits are generally much less susceptible to ESD damage than circuits which must interface with other PC boards or the outside world. These ICs are generally not specified or guaranteed to meet any particular ESD specification (with the exception of MIL-STD-883 Method 3015 classified devices). A good example of an ESD-sensitive interface is the RS-232 interface port ICs on a computer, which can easily be exposed to excess voltages. In

order to guarantee ESD performance for such devices, the test methods and limits must be specified.

A host of test waveforms and specifications have been developed to evaluate the susceptibility of devices to ESD. The three most prominent of these waveforms currently in use for semiconductor or discrete devices are: The Human Body Model (HBM), the Machine Model (MM), and the Charged Device Model (CDM). Each of these models represents a fundamentally different ESD event, consequently, correlation between the test results for these models is minimal.

Since 1996, all electronic equipment sold to or within the European Community must meet Electromechanical Compatibility (EMC) levels as defined in specification IEC1000-4-x. Note that this does not apply to individual ICs, *but to the end equipment*. These standards are defined along with test methods in the various IEC1000 specifications, and are listed in Figure 7.

IEC1000-4-2 specifies compliance testing using two coupling methods, *contact discharge* and *air-gap discharge*. Contact discharge calls for a direct connection to the unit being tested. Air-gap discharge uses a higher test voltage, but does not make direct contact with the unit under test. With air discharge, the discharge gun is moved toward the unit under test, developing an arc across the air gap, hence the term air discharge. This method is influenced by humidity, temperature, barometric pressure, distance and rate of closure of the discharge gun. The contact-discharge method, while less realistic, is more repeatable and is gaining acceptance in preference to the air-gap method.

- ◆ **IEC1000-4 Electromagnetic Compatibility EMC**
- ◆ **IEC1000-4-1 Overview of Immunity Tests**
- ◆ **IEC1000-4-2 Electrostatic Discharge Immunity (ESD)**
- ◆ **IEC1000-4-3 Radiated Radio-Frequency Electromagnetic Field Immunity**
- ◆ **IEC1000-4-4 Electrical Fast Transients (EFT)**
- ◆ **IEC1000-4-5 Lightening Surges**
- ◆ **IEC1000-4-6 Conducted Radio Frequency Disturbances above 9kHz**
- ◆ **Compliance Marking: CE**

Figure 7: A Listing of the IEC Standards Applicable to ESD Specifications and Testing Procedures

Although very little energy is contained within an ESD pulse, the extremely fast risetime coupled with high voltages can cause failures in unprotected ICs. Catastrophic destruction can occur immediately as a result of arcing or heating. Even if catastrophic failure does not occur immediately, the device may suffer from parametric degradation, which may result in degraded performance. The cumulative effects of continuous exposure can eventually lead to complete failure.

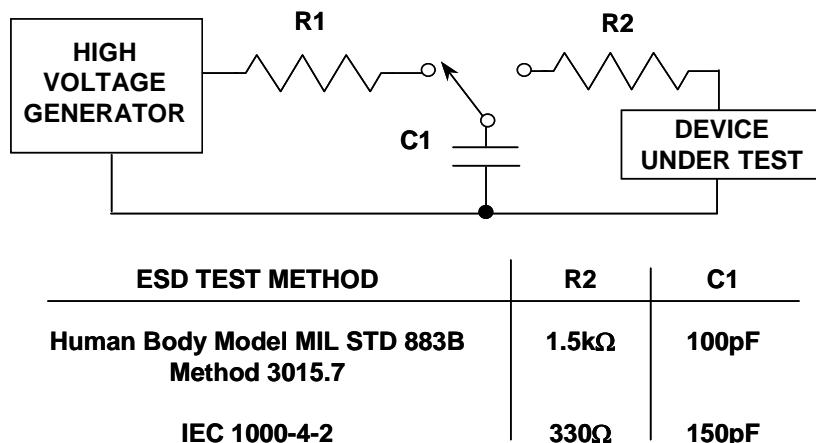
I/O lines are particularly vulnerable to ESD damage. Simply touching or plugging in an I-O cable can result in a static discharge that can damage or completely destroy the interface product connected to the I/O port (such as RS-232 line drivers and receivers).

Traditional ESD test methods such as MIL-STD-883B Method 3015.7 do not fully test a product's susceptibility to this type of discharge. This test was intended to test a product's susceptibility to ESD damage during handling. Each pin is tested with respect to all other pins. There are some important differences between the MIL-STD-883B Method 3015.7 test and the IEC test, noted as follows:

1. The IEC test is much more stringent in terms of discharge energy. The peak current injected is over four times greater.
2. The current risetime is significantly faster in the IEC test.
3. The IEC test is carried out while power is applied to the device.

It is possible that ESD discharge could induce latch-up in the device under test. This test is therefore more representative of a real-world I-O discharge where the equipment is operating normally with power applied. For maximum confidence, however, both tests should be performed on interface devices, thus ensuring maximum protection both during handling, and later, during field service.

A comparison of the test circuit values for the IEC1000-4-2 model versus the MIL-STD-883B Method 3015.7 Human Body Model is shown in Figure 8.



NOTE: CONTACT DISCHARGE VOLTAGE SPEC FOR IEC 1000-4-2 IS ±8kV

Figure 8: ESD Test Circuits and Values

The ESD waveforms for the MIL-STD-883B, METHOD 3015.7 and IEC 1000-4-2 tests are compared in Figure 9, left and right, respectively.

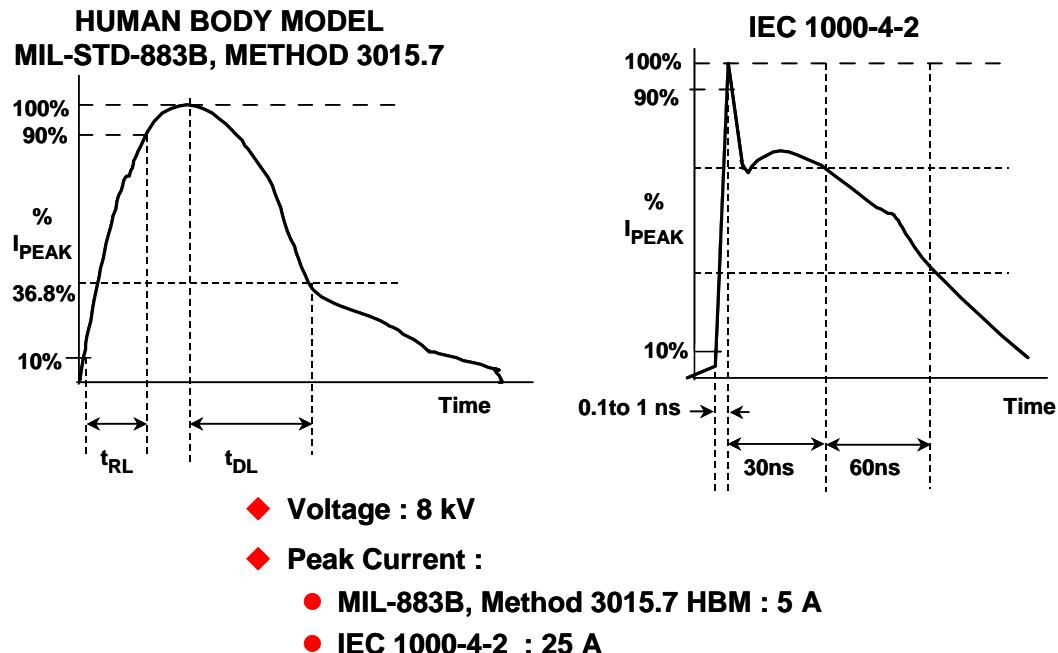


Figure 9: ESD Test Waveforms

Suitable ESD-protection design measures are relatively easy to incorporate, and most of the overvoltage protection methods already discussed in this section will help. Additional protection can also be obtained. For RS-232 and RS-485 drivers and receivers, the ADMXXX-E series is supplied with guaranteed 15-kV (HBM) ESD specifications. For more general uses, the addition of TransZorbs at appropriate places in a system can provide protection against ESD (See Reference 9).

Figure 10 summarizes the major points about ESD prevention, from both an out-of-circuit as well as an in-circuit perspective.

- ◆ Observe all Absolute Maximum Ratings on Data Sheet!
- ◆ Read ADI AN-397 (See Reference 6)
- ◆ Purchase ESD-Specified Digital Interface Devices
 - ADMXXX-E Series of RS-232 / RS-485 Drivers / Receivers (See Reference 8)
- ◆ Follow General Over-voltage Protection Recommendations
 - Add Series Resistance to Limit Currents
 - Add Zeners or Transient Voltage Suppressors (TVS) for Extra Protection (See Reference 9)

Figure 10: A Summary of ESD Points

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4. ESD Association Standard S5.2 for "Electrostatic Discharge (ESD) Sensitivity Testing -Machine Model (MM)- Component Level." Available from the [ESD Association, Inc.](#), 200 Liberty Plaza, Rome, NY 13440.
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