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## Using Op Amps As Comparators

Even though op amps and comparators may seem interchangeable at first glance there are some important differences. Comparators are designed to work open-loop, they are designed to drive logic from their outputs, and they are designed to work at high speed with minimal instability. Op amps are not designed for use as comparators, they may saturate if over-driven which may cause it to recover comparatively slowly. Many have input stages which behave in unexpected ways when used with large differential voltages, in fact, in many cases, the differential input voltage range of the op amp is limited. And op amp outputs are rarely compatible with logic.

Yet many people still try to use op amps as comparators. While this may work at low speeds and low resolutions, many times the results are not satisfactory. Not all of the issues involved with using an op amp as a comparator can be resolved by reference to the op amp data sheet, since op amps are not intended for use as comparators.

The most common issues are speed (as we have already mentioned), the effects of input structures (protection diodes, phase inversion in FET amplifiers, and many others), output structures which are not intended to drive logic, hysteresis and stability, and common-mode effects.

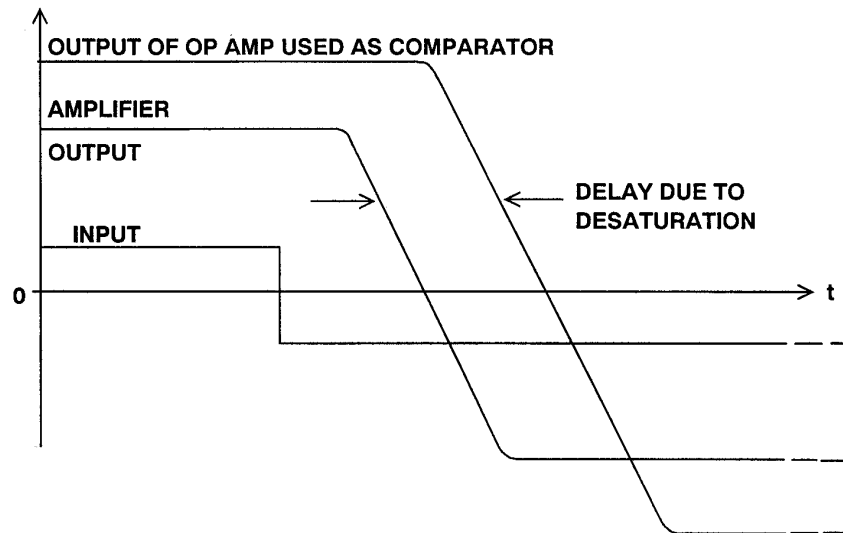
### **SPEED CONSIDERATIONS**

Most comparators are quite fast, but so are many op amps. Why must we expect low speed when using an op amp as a comparator?

A comparator is designed to be used with large differential input voltages, whereas op amps normally operate with their differential input voltage minimized by negative feedback. When an op amp is over-driven, sometimes by only a few millivolts, some of its stages may saturate. If this occurs the device will take a comparatively long time to come out of saturation and will therefore be much slower than if it always remained unsaturated (see Figure 1).

The time to come out of saturation of an overdriven op amp is likely to be considerably longer than the normal group delay of the amplifier, and will often depend on the amount of overdrive. Since few op amps have this saturation recovery time specified for various amounts of overdrive it will generally be necessary to determine, by experiment, the behavior of the amplifier under the conditions of overdrive to be expected in a particular application.

The results of such experiments should be regarded with suspicion and the values of propagation delay through the op amp comparator which is chosen for worst-case design calculations should be at least twice the worst value seen in any experiment.



**Figure 1: Effects of Saturation on Amplifier Speed when Used as a Comparator**

## OUTPUT CONSIDERATIONS

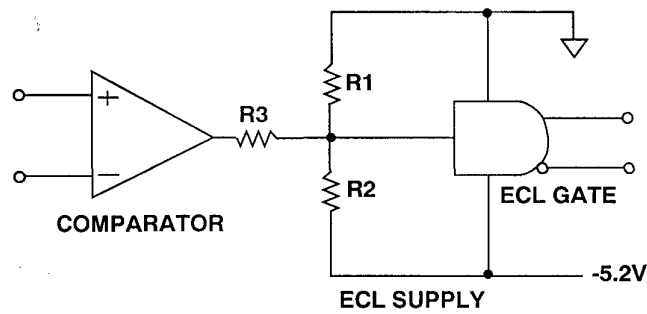
The output of a comparator will be designed to drive a particular logic family or families, while the output of an op amp is designed to swing from supply rail to supply rail.

Frequently the logic being driven by the op amp comparator will not share the op amp's supplies and the op amp rail to rail swing may go outside the logic supply rails—this will probably destroy the logic circuitry, and the resulting short circuit may destroy the op amp as well.

There are three types of logic which we must consider: ECL, TTL and CMOS.

ECL is a very fast current steering logic family. It is unlikely that an op amp would be used as a comparator in applications where ECL's highest speed is involved, for reasons given above, so we shall usually be concerned only to drive ECL logic levels from an op amp's signal swing and some additional loss of speed due to stray capacities will be unimportant. To do this we need only three resistors, as shown in Figure 2.

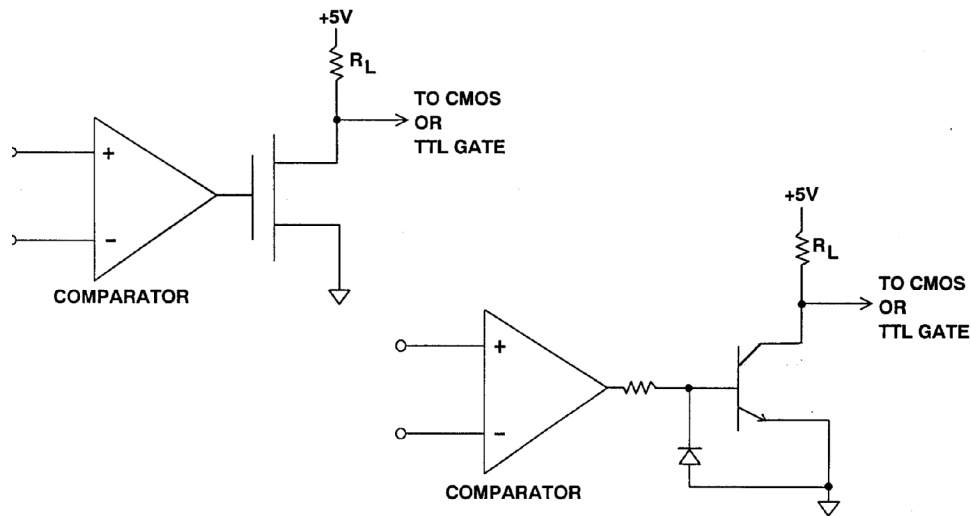
R1, R2 and R3 are chosen so that when the op amp output is positive the level at the gate is  $-0.8$  V, and when it is low it is  $-1.6$  V. ECL is occasionally used with positive, rather than negative, supplies (i.e. the other rail is connected to ground), the same basic interface circuit may be used but the values must be recalculated.



■ LOW RESISTOR VALUES WILL MINIMIZE THE EFFECT OF STRAY CAPACITANCE BUT INCREASE POWER CONSUMPTION

**Figure 2: Op Amp Comparator Driving ECL Logic**

Although CMOS and TTL input structures, logic levels, and current flows are quite different (although some CMOS is specified to work with TTL input levels) the same interface circuitry will work perfectly well with both types of logic, since they both work for logic 0 near to 0 V and logic 1 near to 5 V.



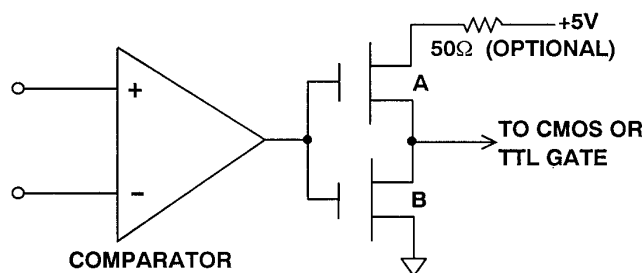
• Low resistor values will minimize the effects of stray capacitance but increase power consumption

**Figure 3: Op Amp Comparator Driving TTL or CMOS Logic**

The simplest interface uses a single N-channel MOS transistor and a pull-up resistor,  $R_L$ , as shown in Figure 3. A similar circuit may be made with an NPN transistor,  $R_L$ , and an additional transistor and diode. These circuits are simple, inexpensive and reliable, and may be connected with several transistors in parallel and a single  $R_L$  to give a "wired-or" function, but the speed of

the 0-1 transition depends on the value of  $R_L$  and the stray capacity of the output node. The lower the value of  $R_L$  the faster, but the higher the power consumption. By using two MOS devices, one P-channel and one N-channel, it is possible to make a CMOS/TTL interface using only two components which has no quiescent power consumption in either state (see Figure 4).

Furthermore, it may be made inverting or non-inverting by simple positioning of components. It does, however, have a large current surge during switching, when both devices are on at once, and unless MOS devices with high channel resistance are used a current limiting resistor may be necessary to reduce this effect. It is also important, in this application and the one in Figure 3, to use MOS devices with gate-source breakdown voltages,  $V_{BGS}$ , greater than the output voltages of the comparator in either direction. A value of  $V_{BGS} > \pm 25$  V is common in MOS devices and is usually adequate, but many MOS devices contain gate protection diodes which reduce the value—these should not be used.



- Can be inverting or non-inverting, depending on placing of VMOS devices.

Inverting: A = P-channel/B = N-channel

Non-inverting: A = N-channel/B = P-channel

( $V_{bgs} > \pm 25$  V for both devices)

**Figure 4: Op Amp Comparator with CMOS Driver**

## INPUT CONSIDERATIONS

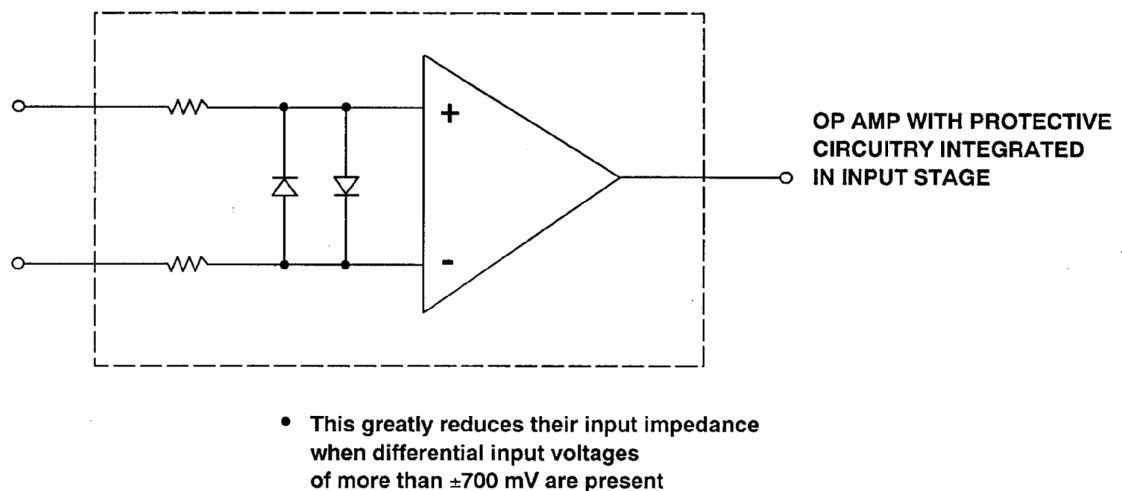
There are a number of effects which must be considered regarding the inputs of op amps used as comparators. The first-level assumption engineers make about all op amps and comparators is that they have infinite input impedance and can be regarded as open circuits (except for current feedback (transimpedance) op amps, which have a high impedance on their non-inverting input but a low impedance of a few tens of ohms on their inverting input)

But many op amps (especially bias-compensated ones such as the OP-07 and its many descendants) contain protective circuitry to prevent large voltages damaging input devices.

Others contain more complex input circuitry, which only has high impedance when the differential voltage applied to it is less than a few tens of mV, or which may actually be damaged by differential voltages of more than a few volts. It is therefore necessary, when using an op amp

as a comparator, to study the data sheet to determine how the input circuitry behaves when large differential voltages are applied to it. (It is always necessary to study the data sheet when using an integrated circuit to ensure that its non-ideal behavior (and every integrated circuit ever made has some non-ideal behavior) is compatible with the proposed application—it is just more important than usual in the present case.) Figure 5 shows an op amp with input diodes for protection against large differential voltages.

Of course some comparator applications never involve large differential voltages—or if they do the comparator input impedance when large differential voltages are present is comparatively unimportant. In such cases it may be appropriate to use as a comparator an op amp whose input circuitry behaves non-linearly—but the issues involved must be considered, not just ignored.



**Figure 5: Op Amp Input Structure with Protection**

As mentioned elsewhere in this seminar, nearly all BIFET op amps exhibit anomalous behavior when their inputs are close to one of their supplies (usually the negative supply). Their inverting and non-inverting inputs may become interchanged. If this should occur when the op amp is being used as a comparator the phase of the system involved will be inverted, which could well be inconvenient. The solution is, again, careful reading of the data sheet to determine just what common-mode range is acceptable.

Also, absence of negative feedback means that, unlike that of op amp circuits, the input impedance is not multiplied by the loop gain. As a result, the input current varies as the comparator switches. Therefore the driving impedance, along with parasitic feedbacks, can play a key role in affecting circuit stability. While negative feedback tends to keep amplifiers within their linear region, positive feedback forces them into saturation.

**SUMMARY**

Operational amplifiers are not designed to be used as comparators, so this tutorial has been, intentionally, a little discouraging. Nevertheless there are some applications where the use of an op amp as a comparator is a correct engineering decision—what is important is to make it a considered decision, and ensure that the op amp chosen will perform as expected. To do this it is necessary to read the data sheet carefully, to consider the effects of non-ideal op amp performance, and to calculate the effects of op amp parameters on the application. Since the op amp is being used in a non-standard manner some experiment may also be necessary—since the amplifier used for the experiment will not necessarily be typical the results of experiments should always be interpreted somewhat pessimistically.

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