
DAC Interface Fundamentals

by Walt Kester

INTRODUCTION

This tutorial outlines some important issues regarding DAC interface circuitry including the voltage reference, analog output, data input, and clock driver. Because ADCs require references and clocks also, most of the concepts presented in this tutorial regarding these subjects apply equally to ADCs.

DAC REFERENCE VOLTAGE

There is a tendency to regard DACs simply as devices with digital inputs and an analog output. But the analog output depends on the presence of that analog input known as the reference, and the accuracy of the reference is almost always the limiting factor on the absolute accuracy of a DAC. Design tools such as the [Voltage Reference Wizard](#) are useful in matching references to data converters. These tools and others are available on the [Design Center](#) portion of the Analog Devices' website.

Some ADCs and DACs have internal references, while others do not. Some ADCs use the power supply as a reference. Unfortunately, there is little standardization with respect to ADC/DAC voltage references. In some cases, the dc accuracy of a converter with an internal reference can often be improved by overriding or replacing the internal reference with a more accurate and stable external one. In other cases, the use of an external low-noise reference will also increase the noise-free code resolution of a high-resolution ADC.

Various ADCs and DACs provide the capability to use external references in lieu of internal ones in various ways. Figure 1 shows some of the popular configurations (but certainly not all). Figure 1A shows a converter which requires an external reference. It is generally recommended that a suitable decoupling capacitor be added close to the ADC/DAC REF IN pin. The appropriate value is usually specified in the voltage reference data sheet. It is also important that the reference be stable with the required capacitive load (more on this to come).

Figure 1B shows a converter that has an internal reference, where the reference is also brought out to a pin on the device. This allows it to be used other places in the circuit, provided the loading does not exceed the rated value. Again, it is important to place the capacitor close to the converter pin. If the internal reference is pinned out for external use, its accuracy, stability, and temperature coefficient is usually specified on the ADC or DAC data sheet.

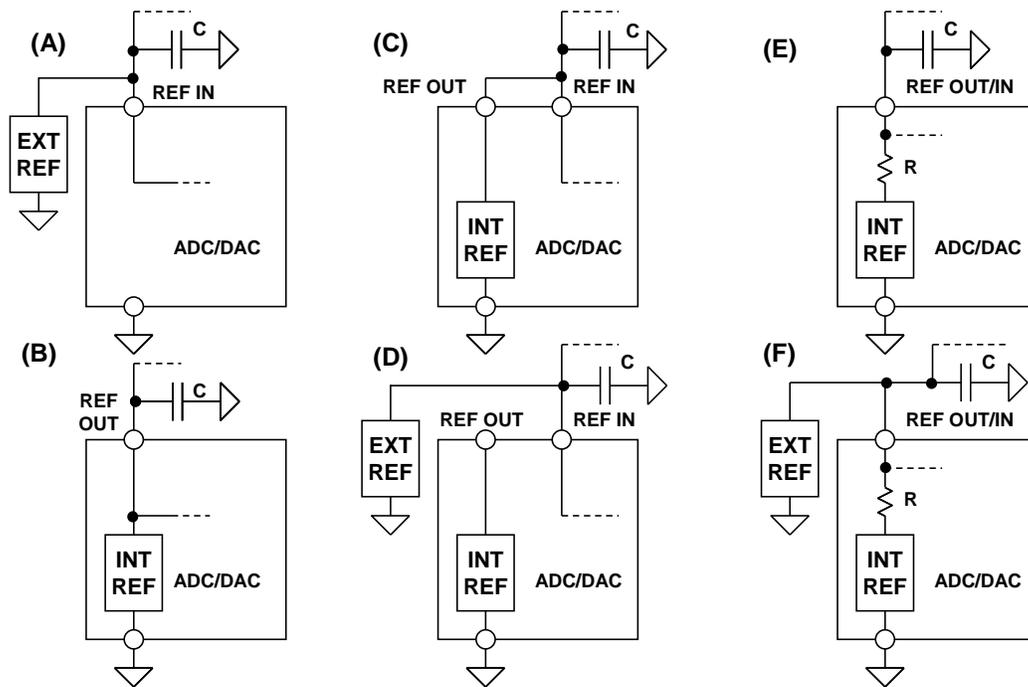


Figure 1: Some Popular ADC/DAC Reference Options

If the reference output is to be used other places in the circuit, the data sheet specifications regarding fanout and loading must be strictly observed. In addition, care must be taken in routing the reference output to minimize noise pickup. In many cases, a suitable op amp buffer should be used directly at the REF OUT pin before fanning out to various other parts of the circuit.

Figure 1C shows a converter which can use either the internal reference or an external one, but an extra package pin is required. If the internal reference is used, as in Figure 1C, REF OUT is simply externally connected to REF IN, and decoupled if required. If an external reference is used as shown in Figure 1D, REF OUT is left floating, and the external reference decoupled and applied to the REF IN pin. This arrangement is quite flexible for driving similar ADCs or DACs with the same reference in order to obtain good tracking between the devices.

Figure 1E shows an arrangement whereby an external reference can override the internal reference using a single package pin. The value of the resistor, R , is typically a few $k\Omega$, thereby allowing the low impedance external reference to override the internal one when connected to the REF OUT/IN pin. Figure 1F shows how the external reference is connected to override the internal reference.

The arrangements shown in Figure 1 are by no means the only possible configurations for ADC and DAC references, and the individual data sheets should be consulted in all cases for details regarding options, fanout, decoupling, etc.

Although the reference element itself can be either a bandgap, buried zener, or XFET™, practically all references have some type of output buffer op amp. The op amp isolates the reference element from the output and also provides drive capability. However, this op amp must obey the general laws relating to op amp stability, and that is what makes the topic of reference decoupling relevant to the discussion.

Note that a reference input to an ADC or DAC is similar to the analog input of an ADC, in that the internal conversion process can inject transient currents at that pin. This requires adequate decoupling to stabilize the reference voltage. Adding such decoupling might introduce instability in some reference types, depending on the output op amp design. Of course, a reference data sheet may not show any details of the output op amp, which leaves the designer in somewhat of a dilemma concerning whether or not it will be stable and free from transient errors. In many cases, the ADC or DAC data sheet will recommend appropriate external references and the recommended decoupling network.

A well-designed voltage reference is stable with heavy capacitive decoupling. Unfortunately, some are not, and larger capacitors actually increases the amount of transient ringing. Such references are practically useless in data converter applications, because some amount of local decoupling is almost always required at the converter.

A suitable op amp buffer might be added between the reference and the data converter. However, there are many good references available which are stable with an output capacitor. This type of reference should be chosen for a data converter application, rather than incurring the further complication and expense of an op amp.

DAC ANALOG OUTPUT CONSIDERATIONS

The analog output of a DAC may be a voltage or a current. In either case it may be important to know the output impedance. If the voltage output is buffered, the output impedance will be low. Both current outputs and unbuffered voltage outputs will be high(er) impedance and may well have a reactive component specified as well as a purely resistive one. Some DAC architectures have output structures where the output impedance is a function of the digital code on the DAC—this should be clearly noted on the data sheet.

In theory, current outputs should be connected to zero ohms at ground potential. In real life they will work with non-zero impedances and voltages. Just how much deviation they will tolerate is defined under the heading "compliance" and this specification should be heeded when terminating current-output DACs.

Most high-speed DACs suitable for video, RF, or IF, have current outputs which are designed to drive source and load-terminated cables directly. For instance, a 20-mA current output DAC can develop 0.5 V across a 25- Ω load (the equivalent dc resistance of a 50- Ω source and load terminated cable). In most cases, single-supply high-speed CMOS DACs have a positive output compliance of at least +1 V and a negative output compliance of a few hundred millivolts.

In many cases, such as the TxDAC® family, both true and complementary current outputs are available. The differential outputs can drive the primary winding of a transformer directly, and a single-ended signal can be developed at the secondary winding by grounding one side of the output winding. This method will often give better distortion performance at high frequencies than simply taking the output signal directly from one of the DAC current outputs and grounding the other.

Modern current output DACs usually have differential outputs, to achieve high common-mode rejection and reduce the even-order distortion products. Fullscale output currents in the range of 2 mA to 30 mA are common.

In many applications, it is desirable to convert the differential output of the DAC into a single-ended signal, suitable for driving a coax line. This can be readily achieved with an RF transformer, provided low frequency response is not required. Figure 2 shows a typical example of this approach. The high impedance current output of the DAC is terminated differentially with 50 Ω , which defines the source impedance to the transformer as 50 Ω .

The resulting differential voltage drives the primary of a 1:1 RF transformer, to develop a single-ended voltage at the output of the secondary winding. The output of the 50- Ω LC filter is matched with the 50- Ω load resistor R_L , and a final output voltage of 1-V_{p-p} is developed.

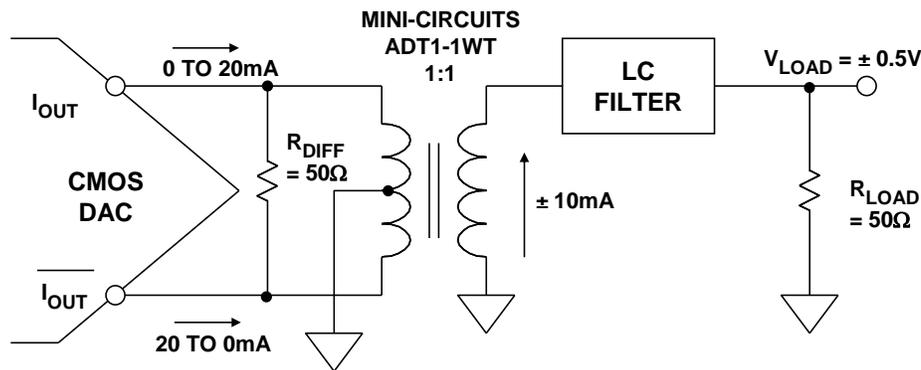


Figure 2: Differential Transformer Coupling

The transformer not only serves to convert the differential output into a single-ended signal, but it also isolates the output of the DAC from the reactive load presented by the LC filter, thereby improving overall distortion performance.

An op amp connected as a differential to single-ended converter can be used to obtain a single-ended output when frequency response to dc is required. In Figure 3 the [AD8055](#) op amp is used to achieve high bandwidth and low distortion. The current output DAC drives balanced 25- Ω resistive loads, thereby developing an out-of-phase voltage of 0 to +0.5 V at each output. This technique is used in lieu of a direct I/V conversion to prevent fast slewing DAC currents from overloading the amplifier and introducing distortion. Care must be taken so that the DAC output voltage is within its compliance rating.

The AD8055 is configured for a gain of 2, to develop a final single-ended ground-referenced output voltage of 2-V p-p. Note that because the output signal swings above and below ground, a dual-supply op amp is required.

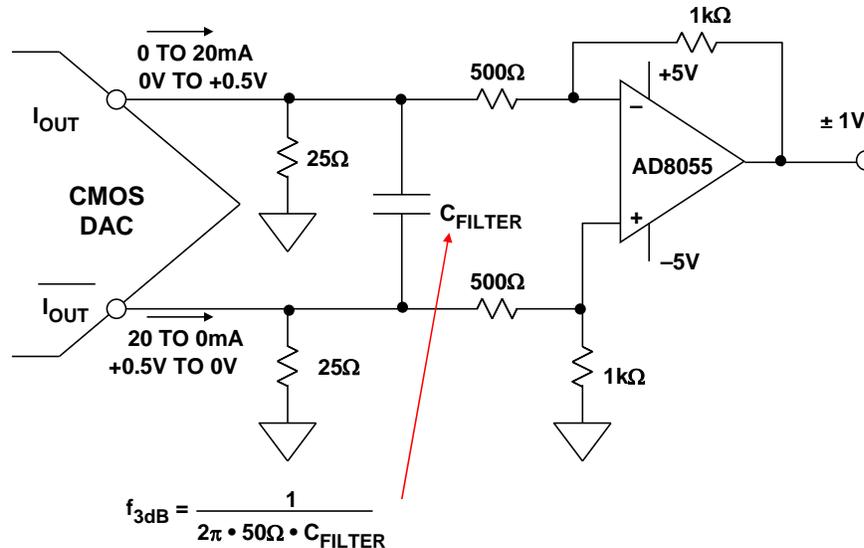


Figure 3: Differential DC Coupled Output Using a Dual Supply Op Amp

The C_{FILTER} capacitor forms a differential filter with the equivalent 50- Ω differential output impedance. This filter reduces any slew-induced distortion of the op amp, and the optimum cutoff frequency of the filter is determined empirically to give the best overall distortion performance.

A modified form of the Figure 3 circuit can be operated on a single supply, provided the common-mode voltage of the op amp is set to mid-supply (+2.5 V). This is shown in Figure 4, where the [AD8061](#) op amp is used. The output voltage is 2-Vp-p centered around a common-mode voltage of +2.5 V. This common-mode voltage can be either developed from the +5 V supply using a resistor divider, or directly from a +2.5 V voltage reference. If the +5 V supply is used as the common-mode voltage, it must be heavily decoupled to prevent supply noise from being amplified.

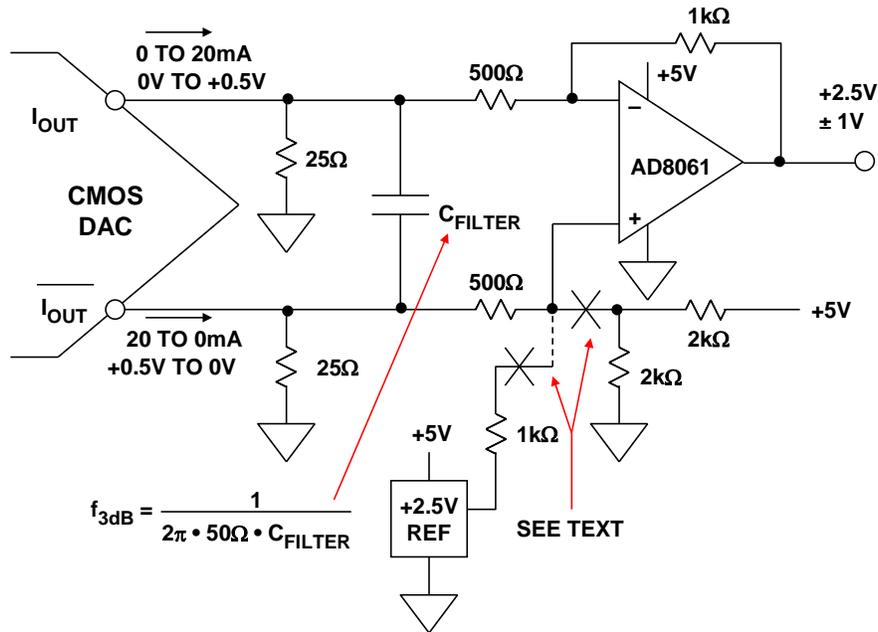


Figure 4: Differential DC Coupled Output Using a Single-Supply Op Amp

SINGLE-ENDED CURRENT-TO-VOLTAGE CONVERSION

Single-ended current-to-voltage conversion is easily performed using a single op amp as an I/V converter, as shown in Figure 5. The 10-mA full scale DAC current from the [AD768](#) develops a 0 to +2 V output voltage across the 200-Ω R_F resistor.

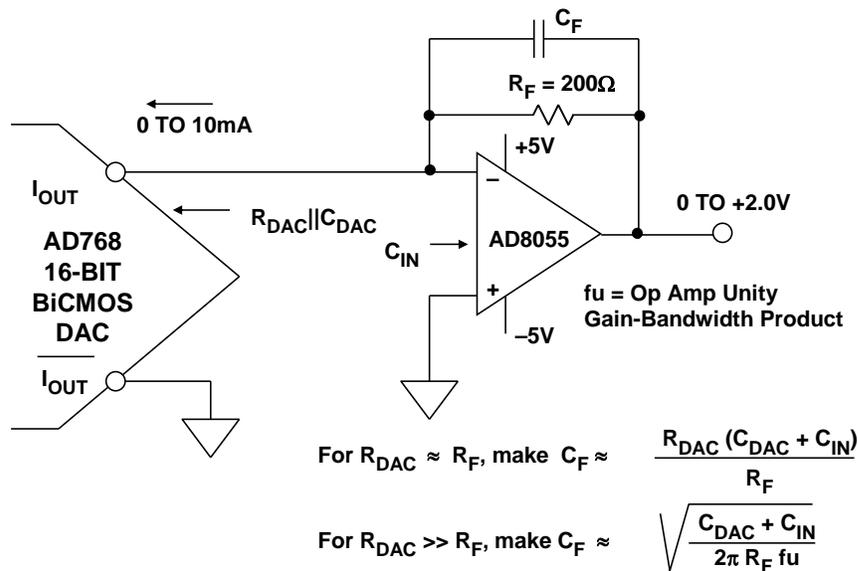


Figure 5: Single-Ended I/V Op Amp Interface for Precision 16-Bit [AD768](#) DAC

Driving the virtual ground of the [AD8055](#) op amp minimizes any distortion due to nonlinearity in the DAC output impedance. In fact, most high resolution DACs of this type are factory trimmed using an I/V converter.

It should be recalled, however, that using the single-ended output of the DAC in this manner will cause degradation in the common-mode rejection and increased second-order distortion products, compared to a differential operating mode.

The C_F feedback capacitor should be optimized for best pulse response in the circuit. The equations given in the diagram should only be used as guidelines.

An R-2R based current-output DAC has a code-dependent output impedance—therefore, its output must drive the virtual ground of an op amp in order to maintain linearity. The [AD5545/AD5555](#) 16-/14-bit DAC is an excellent example of this architecture. A suitable interface circuit is shown in Figure 6 where the [ADR03](#) is used as a 2.5-V voltage reference, and the [AD8628](#) chopper-stabilized op amp is used as an output I/V converter.

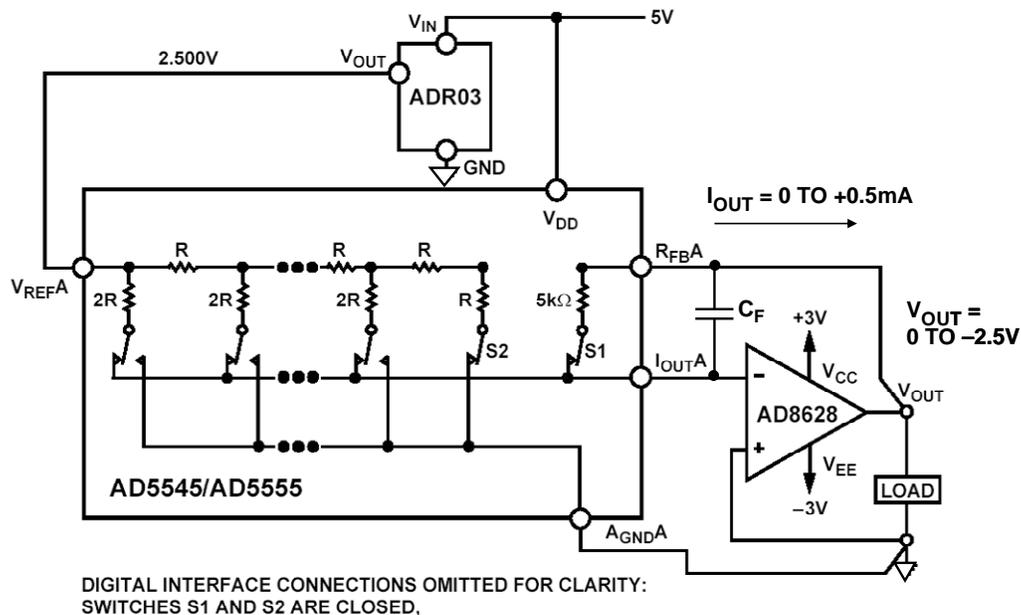


Figure 6: [AD5545/AD5555](#) Dual 16-/14-Bit R-2R Current Output DAC Interface

The external 2.5-V references determines the fullscale output current, 0.5 mA. Note that a 5-kΩ feedback resistor is included in the DAC, and using it will enhance temperature stability as opposed to using an external resistor. The fullscale output voltage from the op amp is therefore – 2.5 V. The C_F feedback capacitor compensates for the DAC output capacitance and should be selected to optimize the pulse response, with 20 pF a typical starting point.

DIFFERENTIAL CURRENT-TO-DIFFERENTIAL VOLTAGE CONVERSION

If a buffered differential voltage output is required from a current output DAC, the AD813x-series of differential amplifiers can be used as shown in Figure 7.

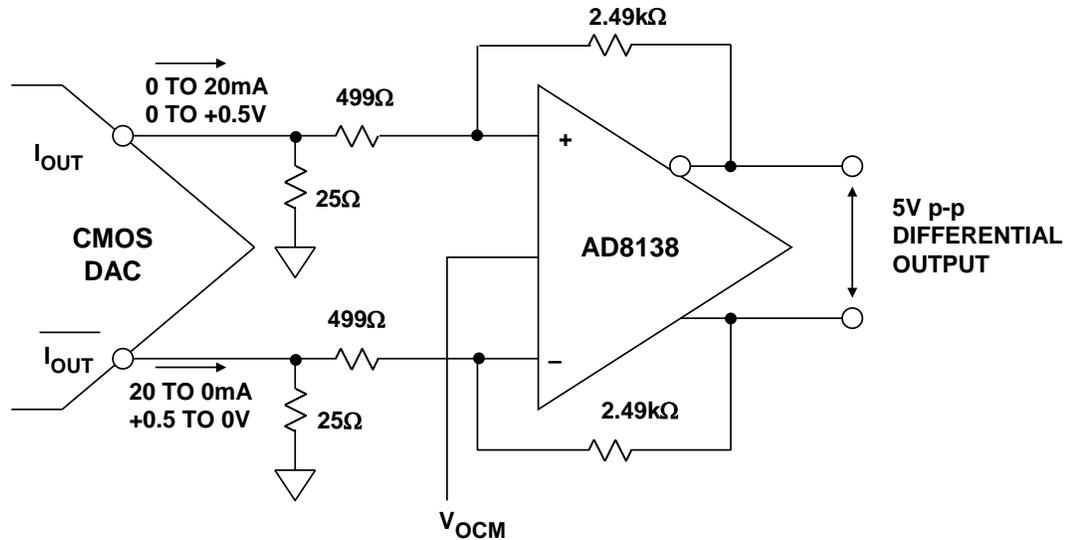


Figure 7: Buffering High Speed DACs Using the [AD8138](#) Differential Amplifier

The DAC output current is first converted into a voltage that is developed across the 25- Ω resistors. The voltage is amplified by a factor of 5 using the [AD8138](#). This technique is used in lieu of a direct I/V conversion to prevent fast slewing DAC currents from overloading the amplifier and introducing distortion. Care must be taken so that the DAC output voltage is within its compliance rating.

The V_{OCM} input on the AD8138 can be used to set a final output common-mode voltage within the range of the AD8138. Adding a pair of 75- Ω series output resistors will allow transmission lines to be driven.

DAC DATA INPUT CONSIDERATIONS

The earliest monolithic DACs contained little, if any, logic circuitry, and parallel data had to be maintained on the digital input to maintain the digital output. Today almost all DACs are latched, and data need only be written to them, not maintained. Some even have nonvolatile latches and remember settings while turned off.

There are innumerable variations of DAC input structure, which will not be discussed here, but nearly all are described as "double-buffered." A double-buffered DAC has two sets of latches. Data is initially latched in the first rank and subsequently transferred to the second as shown in Figure 8. There are several reasons why this arrangement is useful.

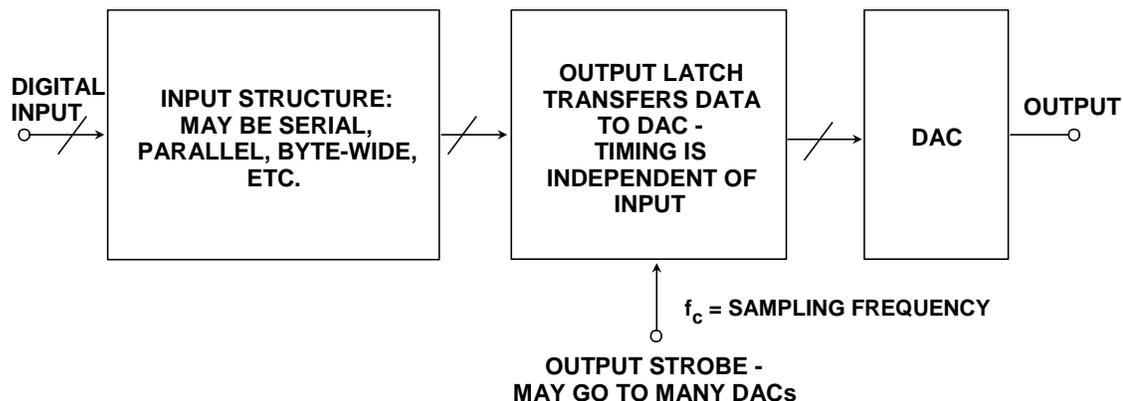


Figure 8: Double-Buffered DAC Permits Complex Input Structures and Simultaneous Update

The first is that it allows data to enter the DAC in many different ways. A DAC without a latch, or with a single latch, must be loaded in parallel with all bits at once, since otherwise its output during loading may be totally different from what it was, or what it is to become. A double-buffered DAC, on the other hand, may be loaded with parallel data, or with serial data, with 4-bit or 8-bit words, or whatever, and the output will be unaffected until the new data is completely loaded and the DAC receives its update instruction.

A second advantage of a double-buffered DAC is that the time skew between the individual switches is minimized by driving all the switches in parallel with a single latch which is updated at the DAC output data rate. This minimizes the glitch impulse and improves distortion performance.

The third convenience of the double-buffered structure is that many DACs may be updated simultaneously. Data is loaded into the first rank of each DAC in turn, and when all is ready, the output buffers of all the DACs are updated at once. There are many DAC applications where the output of a number of DACs must change simultaneously, and the double-buffered structure allows this to be done very easily.

Most early monolithic high resolution DACs had parallel or byte-wide data ports and tended to be connected to parallel data buses and address decoders and addressed by microprocessors as if they were very small write-only memories. (Some parallel DACs are not write-only, but can have their contents read as well—this is convenient for some applications, but is not very common.) A DAC connected to a data bus is vulnerable to capacitive coupling of logic noise from the bus to the analog output, and therefore many DACs today have serial data structures. These are less vulnerable to such noise (since fewer noisy pins are involved), use fewer pins and therefore take less board space, and are frequently more convenient for use with modern microprocessors, most of which have serial data ports. Some, but not all, of such serial DACs have both data outputs and data inputs so that several DACs may be connected in series, with

data clocked to all of them from a single serial port. This arrangement is often referred to as "daisy-chaining."

Serial DACs can be used at voiceband and audio frequency update rates. For instance, 24-bit digital audio updated at 192 kSPS requires a serial port transfer rate of at least $24 \times 192 \text{ kSPS} = 46.08 \text{ MSPS}$, which is easily handled by CMOS logic. However where high update rates are involved, parallel DACs must be used since the required transfer rate of the serial data would be too high.

For parallel data rates greater than approximately 100 MSPS, low-level current-mode differential logic (PECL, reduced-level PECL, LVDS, etc.) is often used because it is much less likely to generate transient glitches than CMOS logic levels (see Figure 9). This helps minimize distortion generated by code-dependent glitches. For instance, the [AD9734/AD9735/AD9736](#) DAC family operates at 1.2 GSPS and accepts LVDS input logic levels. Special circuitry is included on-chip to ensure the proper timing of the input data with respect to the DAC clock.

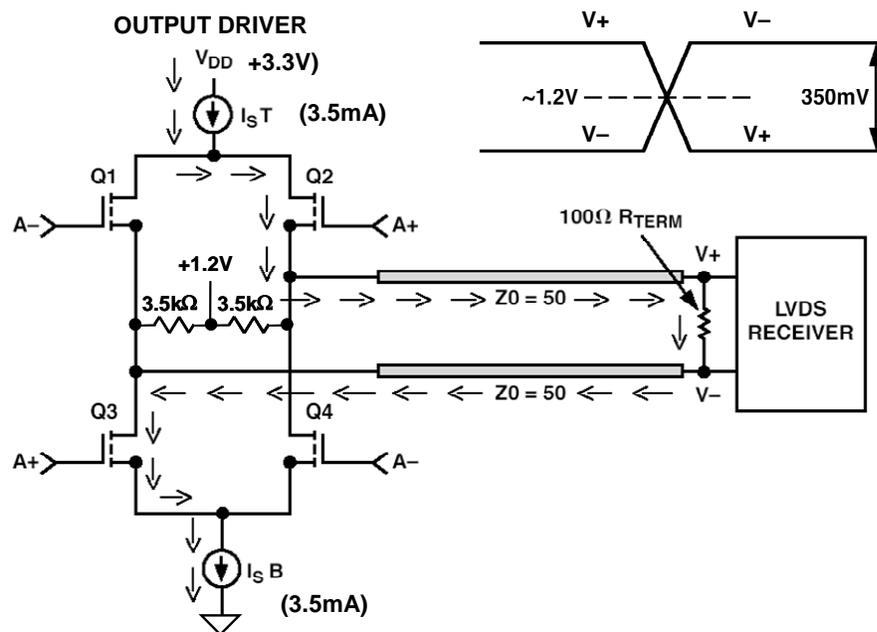


Figure 9: LVDS Driver

DAC CLOCK CONSIDERATIONS

It was shown in Tutorial MT-007 that the relationship between ADC broadband aperture jitter, t_j , converter SNR, and fullscale sinewave analog input frequency, f , is given by

$$\text{SNR} = 20 \log_{10} \left[\frac{1}{2\pi f t_j} \right]. \quad \text{Eq. 1}$$

The same relationship is applicable to reconstruction DACs. The equation assumes an ideal ADC/DAC, where the only error source is clock jitter. The bandwidth for the SNR measurement is the Nyquist bandwidth, dc to $f_c/2$, where f_c is the DAC update rate. Note that Eq. 1 also assumes a fullscale sinewave output. The error due to jitter is proportional to the slew rate of the output signal—lower amplitude sinewaves with proportionally lower slew rate yield higher values of SNR (with respect to fullscale).

It should be noted that t_j in Eq. 1 is the combined jitter of the sampling clock, t_{jc} , and the ADC internal aperture jitter, t_{ja} —these terms are not correlated and therefore combine on an root-sum-square (rss) basis:

$$t_j = \sqrt{t_{jc}^2 + t_{ja}^2} \tag{Eq. 2}$$

High-speed reconstruction DACs, on the other hand, do not have specifications for internal aperture jitter because they have no internal sample-and-hold amplifier. Although there is an internal clock jitter component in a DAC, it is generally not measured or specified, because the jitter of the external clock is the dominant jitter source.

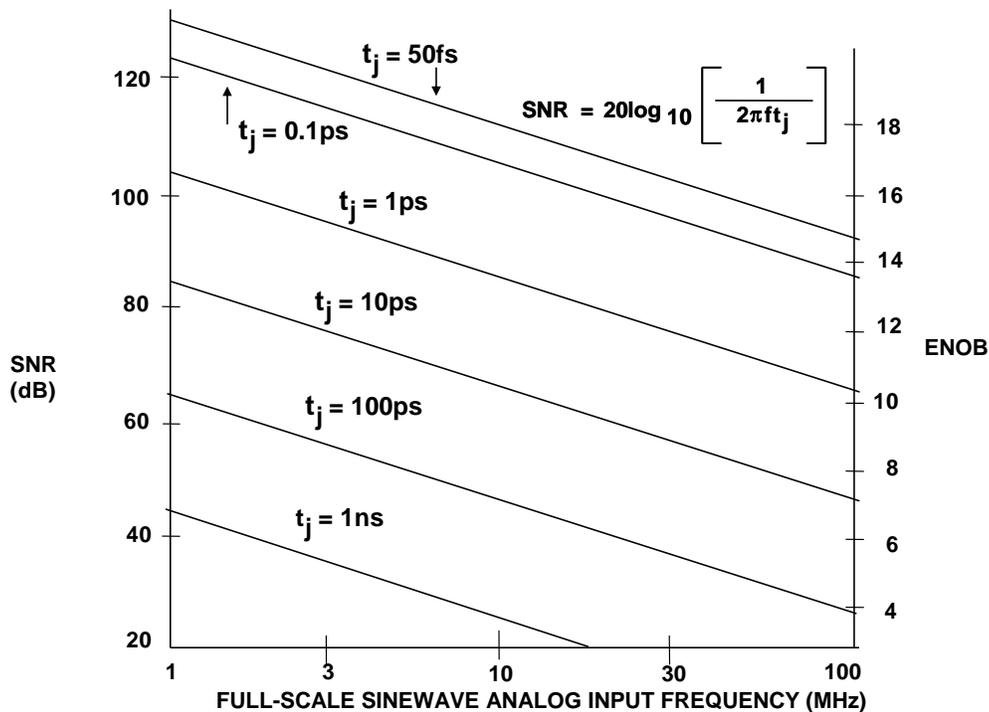


Figure 10: Theoretical SNR and ENOB Due to Jitter vs. Fullscale Sinewave Analog Output Frequency

Figure 10 plots Eq. 1 and graphically illustrates how SNR is degraded by jitter for various fullscale analog output frequencies (note that we assume t_j includes all jitter sources, including the internal DAC jitter). For instance, maintaining 12-bit SNR (74 dB) for a 70 MHz IF output frequency requires the clock jitter to be less than 0.45 ps (using Eq. 1).

From Tutorial [MT-001](#), it was shown that there is a very useful relationship between effective number of bits (ENOB) and the signal-to-noise-plus-distortion ratio (SINAD) given by:

$$\text{ENOB} = \frac{\text{SINAD} - 1.76 \text{ dB}}{6.02 \text{ dB}} \quad \text{Eq. 3}$$

For the purposes of this discussion, assume that the DAC has no distortion, and therefore SINAD = SNR, so Eq. 3 becomes:

$$\text{ENOB} = \frac{\text{SNR} - 1.76 \text{ dB}}{6.02 \text{ dB}} \quad \text{Eq. 4}$$

The SNR values on the left-hand vertical axis of Figure 10 have been converted into ENOB values on the right-hand vertical axis using Eq. 4.

In order to illustrate the significance of these jitter numbers, consider the typical rms jitter associated with a selection of logic gates shown in Figure 11. The values for the 74LS00, 74HCT00, and 74ACT00 were measured with a high performance ADC (aperture jitter less than 0.2-ps rms) using the method described in Chapter 5 of Reference 1, where the jitter was calculated from FFT-based SNR degradation due to several identical gates connected in series. The jitter due to a single gate was then calculated by dividing by the square root of the total number of series-connected gates. The jitter for the MC100EL16 and NBSG16 was specified by the manufacturer.

◆ 74LS00	4.94 ps *
◆ 74HCT00	2.20 ps *
◆ 74ACT00	0.99 ps *
◆ MC100EL16 PECL	0.7 ps **
◆ NBSG16, Reduced Swing ECL (0.4V)	0.2 ps **

- * Calculated values based on degradation in ADC SNR
- ** Manufacturers' specification

Figure 11: RMS Jitter of Typical Logic Gates

Figure 12 shows the same data as Figure 10 but plots maximum allowable jitter as a function of analog output frequency for various resolution requirements. This graph should serve as an approximate guideline for selecting the type of sampling clock generator based upon the maximum output frequency and the required resolution in ENOB. The PLL approach with a standard VCO is an excellent one for generating sampling clocks where the rms jitter requirement is approximately 1 ps or greater. However, sub-picosecond jitter requires either a

VCXO-based PLL or a dedicated low noise crystal oscillator. Tutorial MT-008 explains how to convert oscillator phase noise into jitter.

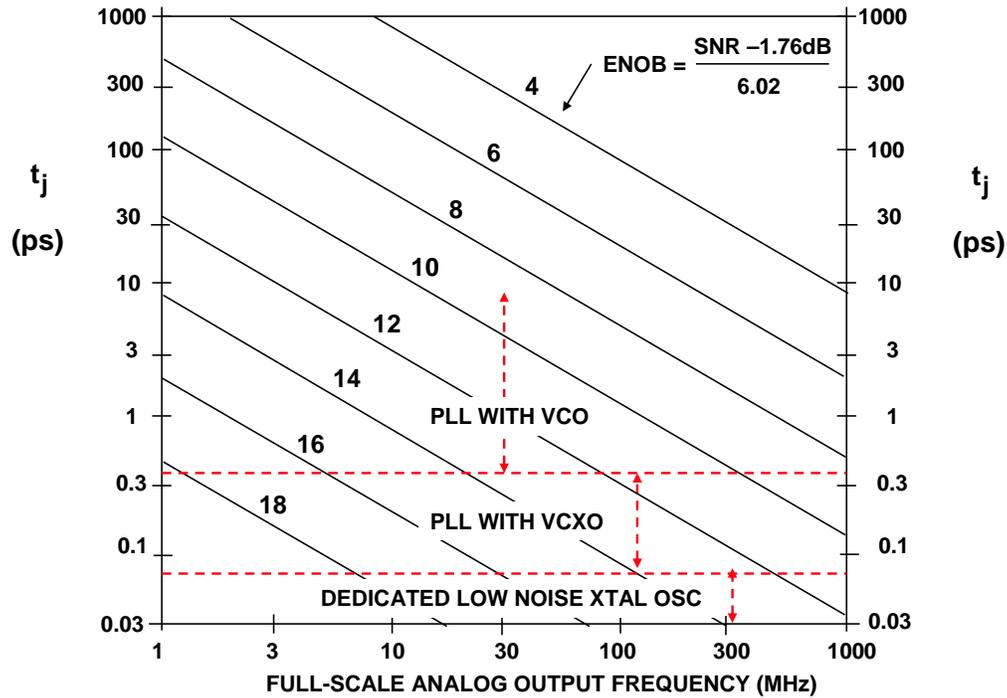


Figure 12: Oscillator Requirements vs. Resolution and Analog Output Frequency

This section has described the effects of jitter on SNR, assuming that the jitter is solely a combination of the internal DAC jitter and the external clock jitter. However, improper layout, grounding, and decoupling techniques can create additional clock jitter which can drastically degrade dynamic performance, regardless of the specifications of the DAC or sampling clock oscillator.

Routing the sampling clock signal in parallel with noisy digital signals is sure to degrade performance due to stray coupling. In fact, coupling high speed data from parallel output ADCs into the sampling clock not only increases noise, but is likely to create additional harmonic distortion, because the energy contained in the digital output transient currents is signal dependent. For further discussion of these and other critical hardware design techniques, the reader is referred to Chapter 9 of Reference 1.

REFERENCE

1. Walt Kester, [*Analog-Digital Conversion*](#), Analog Devices, 2004, ISBN 0-916550-27-3. Also available as [*The Data Conversion Handbook*](#), Elsevier/Newnes, 2005, ISBN 0-7506-7841-0.

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