ADC Noise Figure—An Often Misunderstood and Misinterpreted Specification

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INTRODUCTION

Noise figure (NF) is a popular specification among RF system designers. It is used to characterize the noise of RF amplifiers, mixers, etc., and widely used as a tool in radio receiver design. Many excellent textbooks on communications and receiver design treat noise figure extensively (see Reference 1, for example)—it is the purpose of this discussion to focus on how the specification applies to data converters.

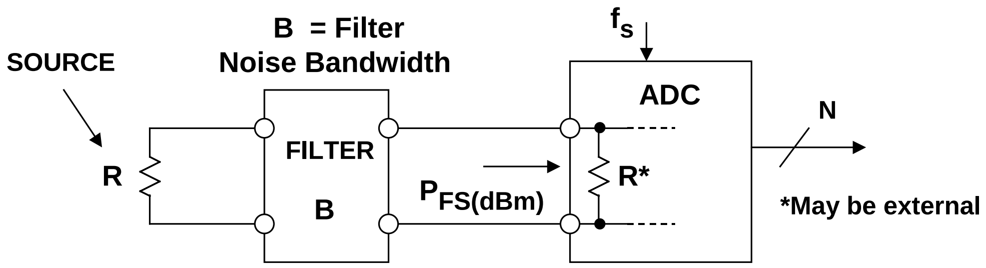
Since many wideband operational amplifiers and ADCs are now being used in RF applications, the day has come where the noise figure of these devices becomes important. Reference 2 discusses the proper methods for determining the noise figure of an op amp. One must not only know the op amp voltage and current noise, but the exact circuit conditions—closed-loop gain, gain-setting resistor values, source resistance, bandwidth, etc. Calculating the noise figure for an ADC is even more of a challenge, as will be seen shortly.

When an RF engineer first calculates the noise figure of even the best low-noise high-speed ADC, the result may appear relatively high compared to the noise figure of typical RF gain blocks, low-noise amplifiers, etc. An understanding of where the ADC is positioned in the signal chain is needed to properly interpret the results. A certain amount of caution is therefore needed when dealing with ADC noise figures.

ADC NOISE FIGURE DEFINITION

Figure 1 shows the basic model for defining the noise figure of an ADC. The *noise factor*, F, is simply defined as *the ratio of the total effective input noise power of the ADC to the amount of that noise power caused by the source resistance alone*.

Because the impedance is matched, the square of the voltage noise can be used instead of noise power. The *noise figure*, NF, is simply the noise factor expressed in dB, $NF = 10\log_{10}F$.



$$\text{NOISE FACTOR (F)} = \frac{\text{(TOTAL EFFECTIVE INPUT NOISE)}^2}{\text{(TOTAL INPUT NOISE DUE TO SOURCE R)}^2}$$

$$\text{NOISE FIGURE (NF)} = 10\log_{10}\left[\frac{\text{(TOTAL EFFECTIVE INPUT NOISE)}^2}{\text{(TOTAL INPUT NOISE DUE TO SOURCE R)}^2}\right]$$

Note: Noise Must be Measured Over the Filter Noise Bandwidth, B

Figure 1: Noise Figure for ADCs: Use with Caution!

This model assumes the input to the ADC comes from a source having a resistance, R, and that the input is band-limited to $f_s/2$ with a filter having a noise bandwidth equal to $f_s/2$. It is also possible to further band-limit the input signal which results in oversampling and process gain—this condition will be discussed shortly.

It is also assumed that the input impedance to the ADC is equal to the source resistance. Many ADCs have a high input impedance, so this termination resistance may be external to the ADC or used in parallel with the internal resistance to produce an equivalent termination resistance equal to R.

ADC NOISE FIGURE DERIVATION

The full-scale input power is the power of a sinewave whose peak-to-peak amplitude exactly fills the ADC input range. The full-scale input sinewave given by the following equation has a peak-to-peak amplitude of $2V_O$, corresponding to the peak-to-peak input range of the ADC:

$$v(t) = V_O \sin 2\pi ft \qquad \text{Eq. 1}$$

The full-scale power in this sinewave is given by:

$$P_{FS} = \frac{(V_O / \sqrt{2})^2}{R} = \frac{{V_O}^2}{2R} \qquad \text{Eq. 2}$$

It is customary to express this power in dBm (referenced to 1 mW) as follows:

$$P_{FS(dBm)} = 10\log_{10}\left[\frac{P_{FS}}{1\,mW}\right]. \qquad \text{Eq. 3}$$

Some more discussion is required regarding the noise bandwidth of filter, B. The *noise bandwidth* of a non-ideal brick wall filter is defined as the bandwidth of an ideal brick wall filter which will pass the same noise power as the non-ideal filter. Therefore, the noise bandwidth of a filter is always greater than the 3-dB bandwidth of the filter by a factor which depends upon the sharpness of the cutoff region of the filter. Figure 2 shows the relationship between the noise bandwidth and the 3-dB bandwidth for Butterworth filters up to 5 poles. Note that for two poles, the noise bandwidth and 3-dB bandwidth are within 11% of each other, and beyond that the two quantities are essentially equal.

NUMBER OF POLES	**NOISE BW : 3dB BW**
1	**1.57**
2	**1.11**
3	**1.05**
4	**1.03**
5	**1.02**

Figure 2: Relationship Between Noise Bandwidth and 3-dB Bandwidth for a Butterworth Filter

The first step in the NF calculation is to calculate the effective input noise of the ADC from its SNR. The SNR of the ADC is shown on the data sheet for a variety of input frequencies, so be sure and use the value corresponding to the IF input frequency of interest. Also, make sure that the harmonics of the fundamental signal are not included in the SNR number—some ADC data sheets may confuse SINAD with SNR. Once the SNR is known, the equivalent input rms voltage noise can be calculated starting from the equation:

$$SNR = 20\log_{10}\left[\frac{V_{FS\ RMS}}{V_{NOISE\ RMS}}\right] \qquad \text{Eq. 4}$$

Solving for $V_{NOISE\ RMS}$:

$$V_{NOISE\ RMS} = V_{FS\ RMS} \cdot 10^{-SNR/20} \qquad \text{Eq. 5}$$

This is the total effective input rms noise voltage measured over the Nyquist bandwidth, dc to $f_s/2$. Note that this noise includes the source resistance noise.

The next step is to actually calculate the noise figure. In Figure 3 notice that the amount of the input voltage noise due to the source resistance is the voltage noise of the source resistance √(4kTBR) divided by two, or √(kTBR), because of the 2:1 attenuator formed by the ADC input termination resistor.

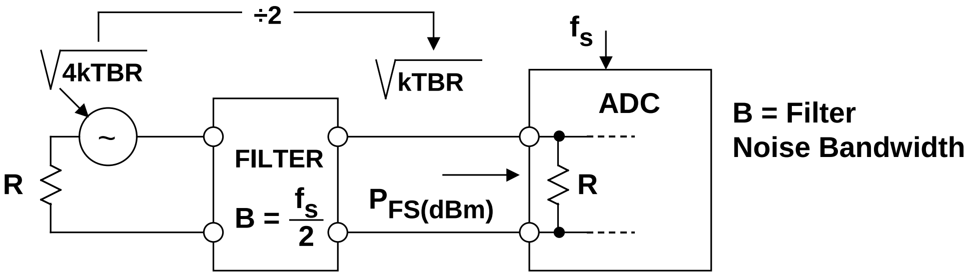
The expression for the noise factor F can be written:

$$F = \frac{V_{\text{NOISE RMS}}^{2}}{kTRB} = \left[\frac{V_{\text{FS RMS}}^{2}}{R}\right]\left[\frac{1}{kT}\right]\left[10^{-SNR/10}\right]\left[\frac{1}{B}\right] \qquad \text{Eq. 6}$$

The noise figure is obtained by converting F into dB and simplifying:

$$NF = 10\log_{10}F = P_{FS(dBm)} + 174\text{ dBm} - SNR - 10\log_{10}B, \qquad \text{Eq. 7}$$

Where SNR is in dB, B in Hz, T = 300 K, $k = 1.38 \times 10^{-23}$ J/K.



$$V_{\text{NOISE-RMS}} = V_{\text{FS-RMS}}\,10^{-SNR/20}$$

$$F = \frac{V_{\text{NOISE-RMS}}^{2}}{kTRB} = \left[\frac{V_{\text{FS-RMS}}^{2}}{R}\right]\left[\frac{1}{kT}\right]\left[10^{-SNR/10}\right]\left[\frac{1}{B}\right]$$

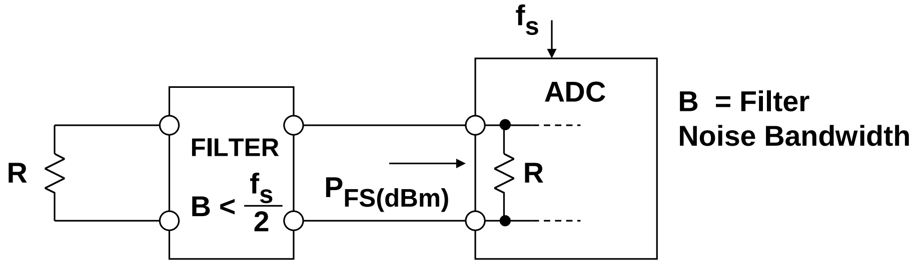
$$\boxed{NF = 10\log_{10}F = P_{FS(dBm)} + 174\text{dBm} - SNR - 10\log_{10}B,}$$

where SNR is in dB, B in Hz, T = 300K, $k = 1.38 \times 10^{-23}$ J/K

Figure 3: ADC Noise Figure in Terms of SNR, Sampling Rate, and Input Power

Oversampling and digital filtering can be used to decrease the noise figure as a result of the process gain as has been previously discussed. In the case of oversampling, the signal bandwidth B is less than $f_s/2$. Figure 4 shows the correction factor which results in the following equation:

$$NF = 10\log_{10}F = P_{FS(dBm)} + 174\text{ dBm} - SNR - 10\log_{10}[f_s/2B] - 10\log_{10}B. \qquad \text{Eq. 8}$$



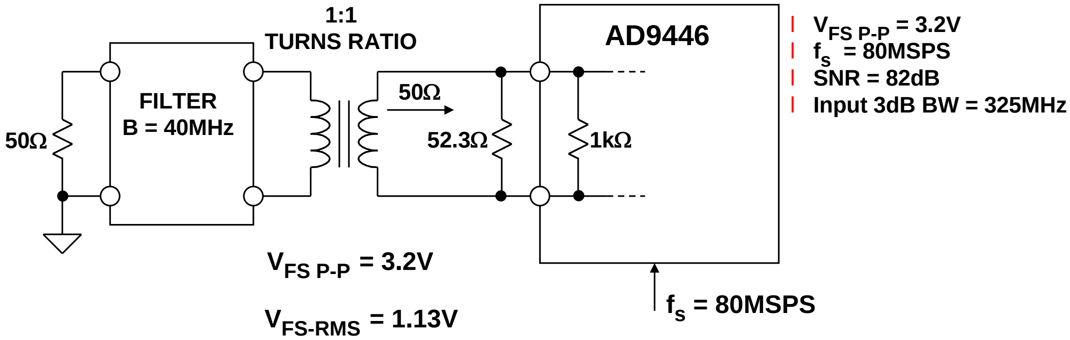
$$NF = P_{FS(dBm)} + 174\text{dBm} \underbrace{-\ SNR}_{\substack{\text{Measured} \\ \text{DC to } f_s/2}} \underbrace{-\ 10\log_{10}\left[\frac{f_s/2}{B}\right]}_{\substack{\text{Process} \\ \text{Gain}}} - 10\log_{10}B$$

where SNR is in dB, B in Hz, T = 300K, k = 1.38 × 10^{-23} J/K

Figure 4: Effect of Oversampling and Process Gain on ADC Noise Figure

EXAMPLE CALCULATION FOR AD9446 16-BIT 80/100-MSPS ADC

Figure 5 shows an example NF calculation for the AD9446 16-bit, 80/105-MSPS ADC. A 52.3-Ω resistor is added in parallel with the AD9446 input impedance of 1 kΩ to make the net input impedance 50 Ω. The ADC is operating under Nyquist conditions, and the SNR of 82 dB is the starting point for the calculations using Eq. 8 above. A noise figure of 30.1 dB is obtained.



- $V_{FS\ P\text{-}P}$ = 3.2V
- f_s = 80MSPS
- SNR = 82dB
- Input 3dB BW = 325MHz

f_s = 80MSPS

$V_{FS\ P\text{-}P} = 3.2V$

$V_{FS\text{-}RMS} = 1.13V$

$$P_{FS} = \frac{(1.13)^2}{50} = 25.5mW$$

$P_{FS(dBm)} = +14.1dBm$

$$\boxed{NF = P_{FS(dBm)} + 174dBm - SNR - 10\log_{10}B}$$

$$= +14.1dBm + 174dBm - 82dB - 10\log_{10}(40 \times 10^6)$$

$$= 30.1dB$$

Figure 5: Example Calculation of Noise Figure
Under Nyquist Conditions for AD9446 16-Bit, 80/100 MSPS ADC

USING RF TRANSFORMERS TO DECREASE ADC NOISE FIGURE

Figure 6 shows how using an RF transformer with voltage gain can improve the noise figure. Figure 6A shows a 1:1 turns ratio, and the noise figure (from Figure 5) is 30.1 dB. Figure 6B shows a transformer with a 1:2 turns ratio. The 249-Ω resistor in parallel with the AD9446 internal resistance results in a net input impedance of 200 Ω. The noise figure is improved by 6 dB because of the "noise-free" voltage gain of the transformer.

Figure 6C shows a transformer with a 1:4 turns ratio. The AD9446 input is paralleled with a 4.02-kΩ resistor to make the net input impedance 800 Ω. The noise figure is improved by another 6 dB. In theory, even higher turns ratios will yield further improvement, but transformers with higher turns ratios are not generally practical because of bandwidth and distortion limitations.

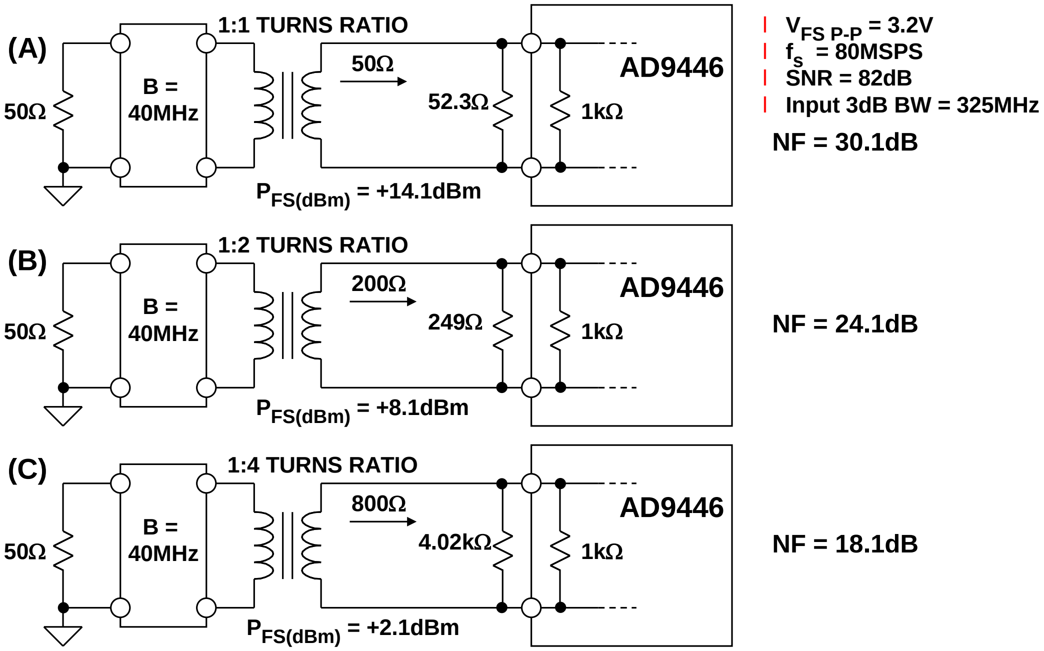
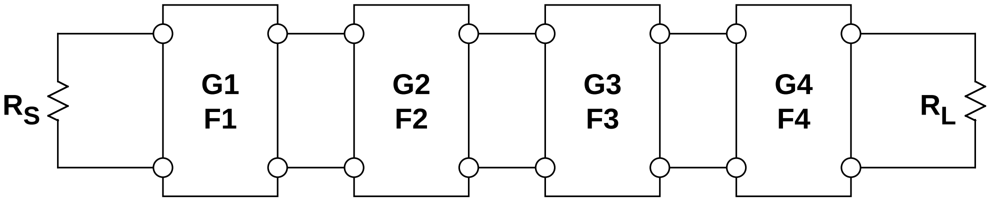


Figure 6: Using RF Transformers to Improve Overall ADC Noise Figure

CASCADED NOISE FIGURE

Even with the 1:4 turns ratio transformer, the overall noise figure for the AD9446 is 18.1 dB, still relatively high by RF standards. It should be noted that the 82-dB SNR of the AD9446 ADC represents excellent noise performance, and the "solution" for system applications is to provide low-noise high-gain stages ahead of the ADC. In a typical receiver there will be at least one low noise amplifier (LNA) and mixing stage ahead of the ADC which provides sufficient signal gain to minimize the degradation in overall system noise figure due to the ADC.

This can be explained in Figure 7 which shows how the Friis equation is used to calculate the noise factor for cascaded gain stages. Notice that high gain in the first stage reduces the contribution of the noise factor of the second stage—the noise factor of the first stage dominates the overall noise factor.



$$F_T = F1 + \frac{F2 - 1}{G1} + \frac{F3 - 1}{G1 \cdot G2} + \frac{F4 - 1}{G1 \cdot G2 \cdot G3} + \ldots$$

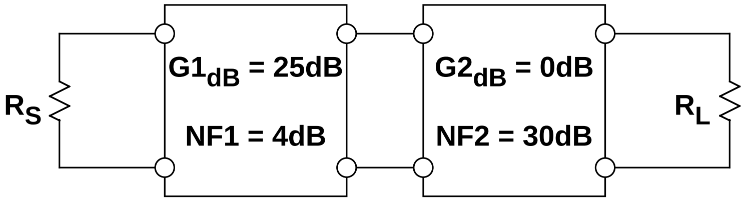
High gain in the first stage reduces the contribution of the NF of the second stage

NF of the first stage dominates the total NF

$$NF_T = 10 \log_{10} F_T$$

Figure 7: Cascaded Noise Figure Using the Friis Equation

Figure 8 shows the effects of a high-gain (25 dB) low-noise (NF = 4 dB) stage placed in front of a relatively high NF stage (30 dB)—the noise figure of the second stage is typical of high performance ADCs. The overall noise figure is 7.53 dB, only 3.53 dB higher than the first stage noise figure of 4 dB.



$$G1 = 10^{25/10} = 10^{2.5} = 316, \quad F1 = 10^{4/10} = 10^{0.4} = 2.51$$

$$G2 = 1, \quad F2 = 10^{30/10} = 10^{3} = 1000$$

$$F_T = F1 + \frac{F2 - 1}{G1} = 2.51 + \frac{1000 - 1}{316} = 2.51 + 3.16 = 5.67$$

$$NF_T = 10 \log_{10} 5.67 = 7.53\text{dB}$$

- **The first stage dominates the overall NF**
- **It should have the highest gain possible with the lowest NF possible**

Figure 8: Example of Two-Stage Cascaded Network

SUMMARY

Applying the noise figure concept to characterize wideband ADCs must be done with extreme caution to prevent misleading results. Simply trying to minimize the noise figure by manipulating the values in the equations can actually increase the total circuit noise.

For instance, NF decreases with increasing source resistance according to the equations, but increased source resistance increases circuit noise. Another example relates to the ADC input bandwidth B. Increasing B reduces NF according to the equations; however, this is contradictory, because increasing the ADC input bandwidth actually increases the effective input noise. In both these examples, the total circuit noise increases, but the NF decreases. The reason NF decreases is because when either the source resistance or bandwidth increases, the source noise simply makes up a larger component of the total noise. However, the total noise remains relatively constant because the noise due to the ADC is much greater than the source noise; therefore according to the equations, NF decreases, but actual circuit noise increases.

For these reasons, NF must be used with some caution when dealing with ADCs. The equations in this article will give valid results, but can be misleading without a full understanding of the noise principles involved.

It is true that on a stand-alone basis even low-noise ADCs have relatively high noise figures compared to other RF parts such as LNAs or mixers. In an actual system application, however, the ADC is always preceded by at least one low-noise gain block which reduces the overall ADC noise contribution to a very small level per the Friis equation (see Figure 8).

REFERENCES:

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