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JESD204B Link Debug

DEL JONES

September 2015





Webinar Agenda

▶ **General Link Debugging Guidelines**

- Process overview
- Detecting where synchronization between the JESD204B transmitter (JTX) and receiver (JRX) failed

▶ **HAD Products**

- Device-specific link startup requirements
- Platform board (FPGA) features and registers
- Debug process
 - Using test modes
 - Using Visual Analog and available FPGA features (product dependent)
- Validating subclass 1 operation
- Common link issues

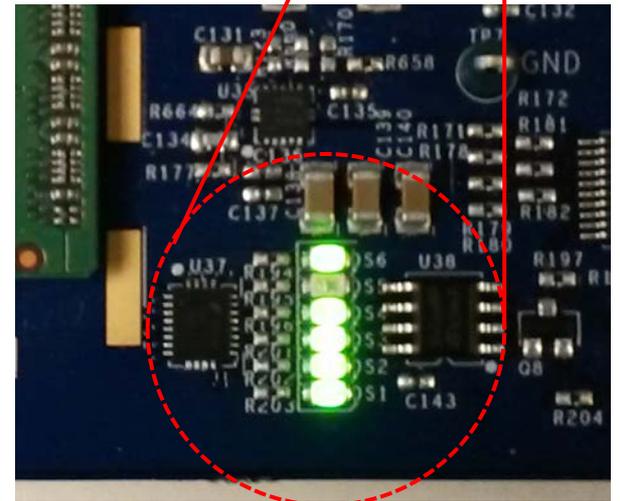
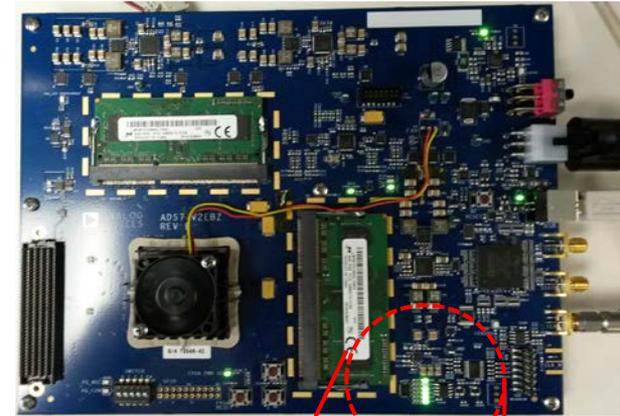
▶ **HDC Products**

- Link startup requirements
- Link status and error monitor registers
- Debug process
 - Using test modes
- Validating subclass 1 operation

General Link Debugging

► Process Overview

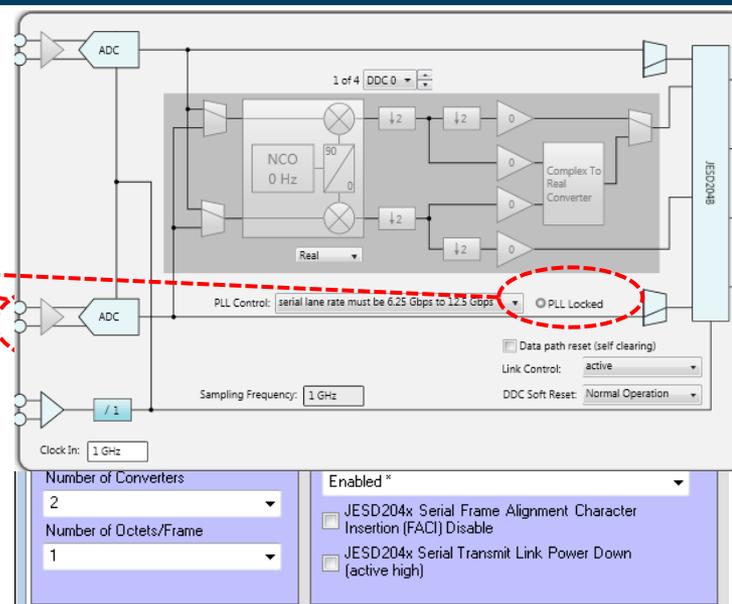
- Is the Link running? – check SYNC~ and link status bits
 - What is the status of the SYNC~ signal?
 - High – usually indicates CGS has completed
 - Low – indicates the JRX is not ready or there is a CGS error
 - Toggling – indicates there is an ILAS error or data bit errors (depending on the JRX error monitoring settings)
 - The ADS7 Evaluation platforms for ADC's include 6 status LED's
 - LED1 indicates GT REFCLK is present.
 - LED2 indicates GT recovered clock is present.
 - LED3 indicates GT reset sequence is complete.
 - LED4 indicates JESD204 CGS detected.
 - LED5 indicates JESD204 ILAS detected.
 - LED6 indicates FIFO is full and ready to be read.
 - ADI DACs include several link status bits
 - CGS passed (0x470)
 - Frame Sync has passed (0x471)
 - ILAS has passed (0x473)
 - Checksums are verified (0x472)
 - ADI transceiver (TRX) devices use API drivers to access framer and deframer status
 - ILAS state and status
 - Checksum valid
 - Frame Sync



General Link Debugging

► Process Overview

- Are the clocks present and PLL's locked?
 - ADS7 LEDs 1 & 2 only indicate clocks are present
 - If LEDs 1, 2, and 3 are on, the PLL is locked
 - ADI ADCs and DACs have a PLL Lock status bit
 - If the reference clock is wrong frequency or has poor signal quality, it is likely to result in CGS error
 - Probe the clock for these issues
 - The 204B lanes can also be probed to confirm it is running at the expected lane rate since CGS is a repetitive pattern
- Do the JTX and JRX configuration parameters match?
 - A configuration mismatch can result in ILAS errors
 - ADI DACs have a configuration mismatch (CMM) flag
 - A mismatch will also result in a 204b configuration checksum error
- If link is up, are there errors?
 - ADS7 platform and DACs provide 8b10b error checking
 - NIT, Disp, and UEKC
 - DACs provide 8b10b error checking
 - Also allows for setting interrupts and error counting thresholds
 - TRX provides API drivers to check for 8b10b errors



Registers	Address (Hex)	Name	Data (Hex)	Data (Binary)
-	0472	GoodChkSumFlg	00	0 0 0 0 0 0 0 0
		GoodChecksum	ageGroup: SERD	0 0 0 0 0 0 0 0
+	0473	InitLaneSyncFlg	00	0 0 0 0 0 0 0 0
+	0477	CTRLREG2	00	0 0 0 0 0 0 0 0
+	0478	Kval	01	0 0 0 0 0 0 0 1
-	047A	IRQVector_mask	00	0 0 0 0 0 0 0 0
-	047A	* IRQVector_flag	00	0 0 0 0 0 0 0 0
-	047B	* SyncAssertionMask	08	0 0 0 0 0 1 0 0
		cmm_enable	ageGroup: SERD	1
		Cmm	ageGroup: SERD	0
		UCC_S	ageGroup: SERD	0
		NIT_S	ageGroup: SERD	0
		baddis_s	ageGroup: SERD	0



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HAD Product 204B Link Startup and Debug

AD9680 Link Startup Procedure (subclass 1)

► Startup conditions with continuous SYREF signal:

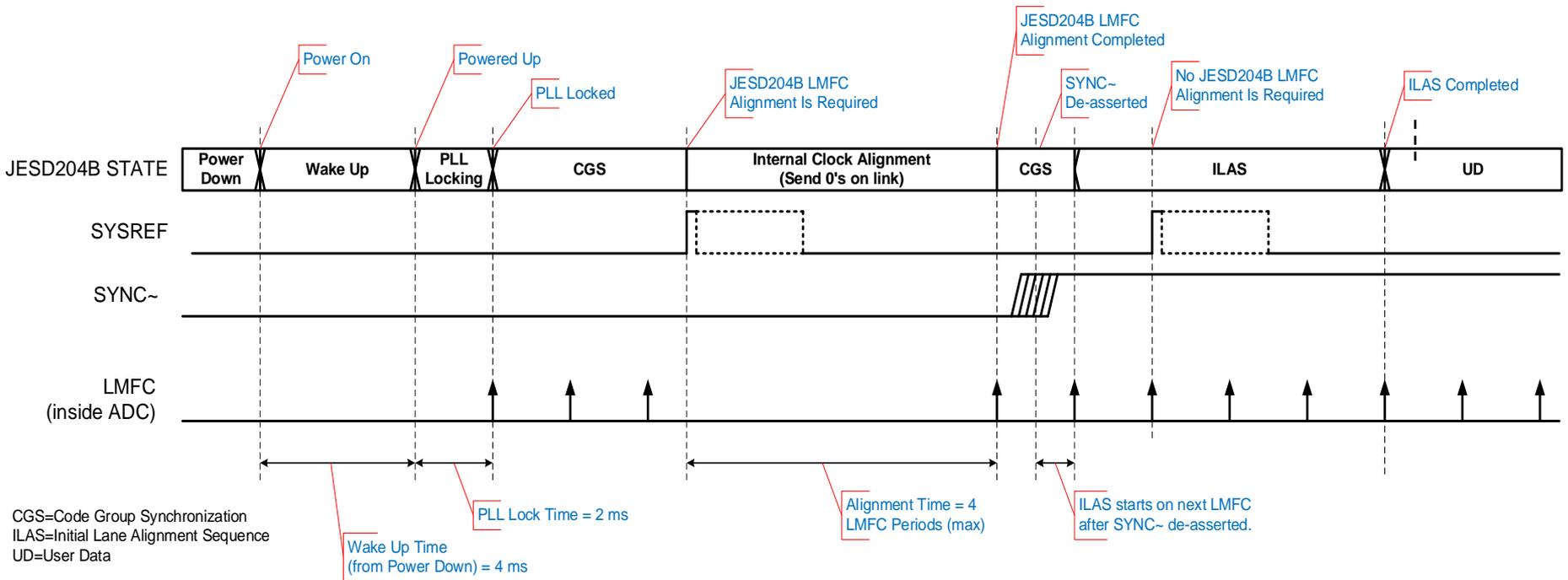
- Power system on
- SYNC~ asserted on power up

► Configuration procedures:

STEP	ADR	DATA	Register name	Note
1	0x000	0x81	Global SPI config	Software Reset
2	wait >=5ms			
3	Set ADC and DSP modes appropriately			Consult AD9680 DS
4	Set clock registers appropriately			Consult AD9680 DS
5	0x571	0x15	204B Link CTRL1	PowerDown_204B_Link
6	0x570	0xnn	204B quick config	Set JESD204B Parameters
7	0x56E	0xn0	204B Configuration	Set lane rate to 0x10 if less than 6.25Gbps
8	See FPGA documentation			Configure JRX paramaters (FPGA)
9	See FPGA documentation			Arm SYSREF in JRX (FPGA)
10	0x121	0xnn	SYSREF CTRL	Set "n" for SYSREF n-shot mode (if necessary)
11	0x120	0xnn	SYSREF CTRL	Set/arm SYSREF mode (n-shot or continuous) if subclass 1
12	wait > =5us			Wait for link power down to settle
13	0x571	0x14	204B Link CTRL1	PowerUp_204B_Link

AD9680 Link Startup Timing

► Startup Timing:



AD9250 Link Startup Procedure (subclass 1)

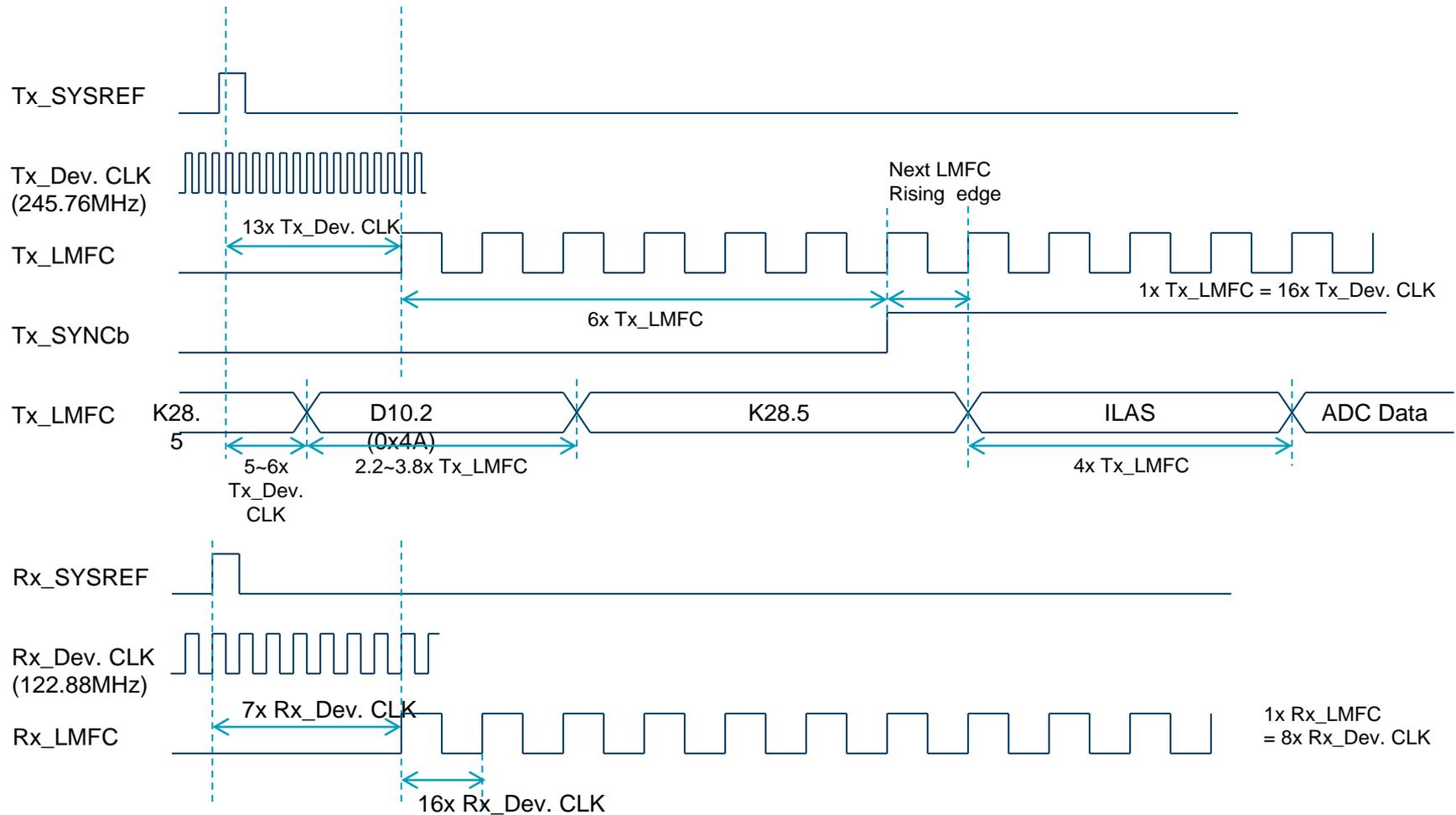
► For Subclass 1 and Nyquist Input clock :

1. Apply power to the AD9250, allow voltages and clocks to stabilize
2. Apply a soft reset by writing 0x3C to Register 0x00
3. Wait at least 500 us
4. Set 0xEE and 0xEF to a value of 0x80 (FIFO clk adjust)
5. Configure the AD9250 as desired including the JESD204B parameters.
6. Establish an LMFC within the AD9250 by providing a SYSREF signal and setting 0x3A appropriately
7. Perform the clock adjustment writes to 0xEE and 0xEF, (see data sheet)
8. Wait at least 6 LMFC's
9. Enable the JESD204B Receiver to initiate link synchronization

► For Subclass 1 and Harmonic Input clock:

1. Apply power to the AD9250, allow voltages and clocks to stabilize
2. Assert power down by either using the PDWN input or by setting register 0x08 to 0x05
3. Configure proper clock divide setting in register 0x0B.
 - Commit clock divide setting by writing 0x01 to register 0xFF.
4. Set 0xEE and 0xEF = 0x80 (FIFO timing adjust enable)
5. Configure the AD9250 as desired including the JESD204B parameters.
6. De-assert power down and wait at least 250 ms
7. Set 0xF3 to 0xFF to reset FIFO clock alignment
8. Wait at least 6 LMFC's
9. Establish an LMFC within the AD9250 by providing a SYSREF signal and setting 0x3A appropriately
10. Perform the clock adjustment writes to 0xEE and 0xEF, (see data sheet)
11. Enable the JESD204B Receiver to initiate the link
12. Wait at least 6 LMFC's
13. Bring the JESD204B receiver out of reset

AD9250 Link Startup Timing



AD9625 Link Startup Procedure (subclass 1)

► Startup conditions with continuous SYREF signal:

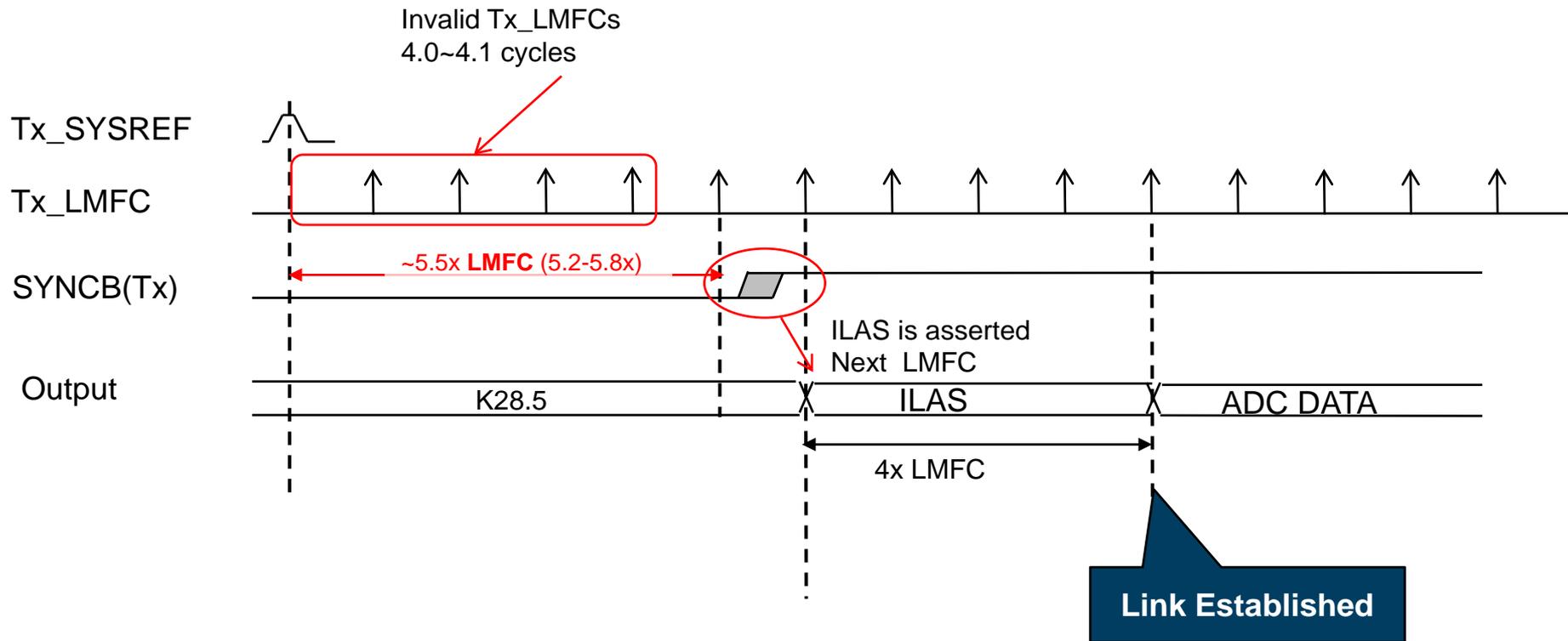
- Power system on
- SYNC~ asserted on power up

► Configuration procedures:

STEP	ADR	DATA	Register name	Note
1	0x00	0x3C	Global SPI config	Software Reset
2	wait >=5ms			
3	Set ADC and DSP modes appropriately			Consult AD9625 data sheet
4	Set clocking registers appropriately			Consult AD9625 data sheet
5	0x5F	0x15	204B Link CTRL1	PowerDown_204B_Link
6	0x5E	0xnn	204B quick config	Configure JESD204B paramaters
7	0x6E	0x0n	204B Configulation	Set number of lanes
8	0x80	0xF0	204B Lane Power Down	Lane4 to 7 Power Down
9	0x3A	0x06	SYSREF CTRL	One shot mode
10	See FPGA documentation			Configure JRX paramaters (FPGA)
11	See FPGA documentation			Arm SYSREF in JRX (FPGA)
12	0x8A	0x20	204B Sysref Control	Sysref Serializer Reset Disable (arm SYSREF)
13	0xFF	0x01	Device update	Transfer data to slave registers
14	wait > =5us			Wait for link power down to settle
15	0xFF	0x01	Device update	Transfer data to slave registers

AD9625 Link Startup Timing (Recommended)

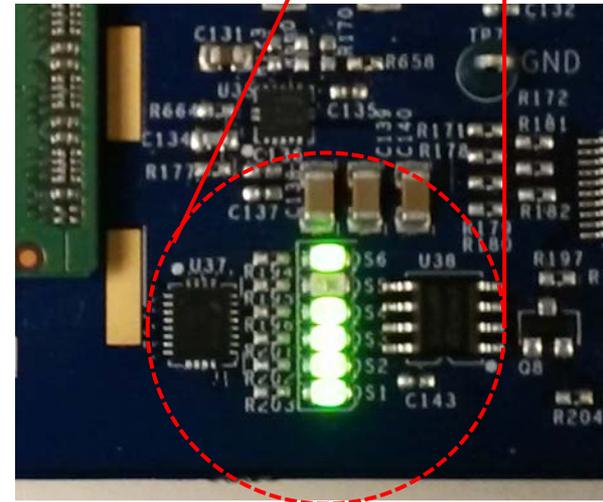
► AD9625 SYSREF to SYNCb Timing (Recommended)



JES204B debugging using the ADS7 platform

► Status LEDs

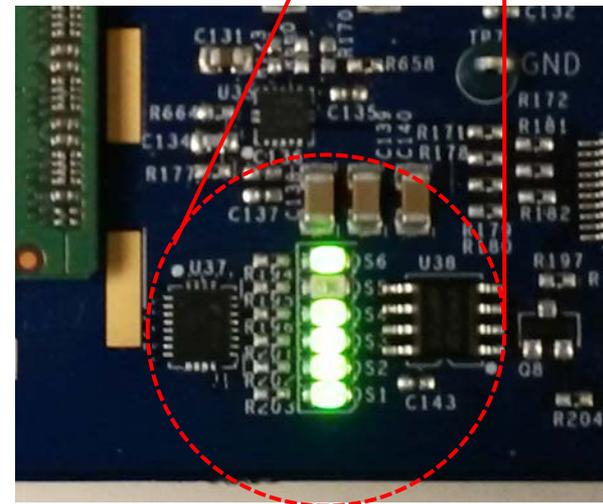
- In general, if one LED is off, then subsequent LEDs can be ignored
- GT REFCLK present (LED1)
 - Activity detection only – frequency and lock status are not detected
 - If not illuminated, check for clock source being present.
- GT recovered clock present (LED2)
 - Activity detection only – frequency and lock status are not detected
 - If not illuminated, check clock frequency, amplitude and signal quality
- GT reset sequence complete (LED3).
 - If LED's 1 & 2 are illuminated, this one should be too, indicating PLL lock
 - If not illuminated, check the frequency and signal quality of the ref clock
- FPGA reference clock (refclk)
 - On ADI ADC evaluation boards, the refclk to FPGA is typically LR/20
 - So, for a 10Gbps lane rate, the refclk should be 500MHz
 - See the device specific ADS7 data capture user guide for guidance on setting refclk



JES204B debugging using the ADS7 platform

► Status LEDs (cont.)

- CGS detected (LED4)
 - K28.5 symbols were detected and CGS is achieved
 - If not illuminated, check the frequency and signal quality of the ref clock
 - L parameter mismatch could also cause a CGS error
- ILAS detected (LED5)
 - K28.0 and K28.3 symbols were detected in the correct sequence
 - Parameters and ramp pattern not checked
 - If not lit, check for CMM between JTX and JRX (affects K28.n placement)
- FIFO full (LED6).
 - Lane FIFO's are full (implies ILAS complete)



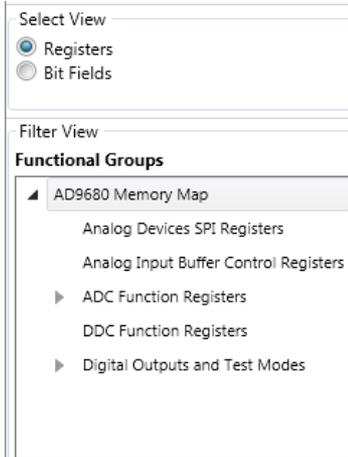
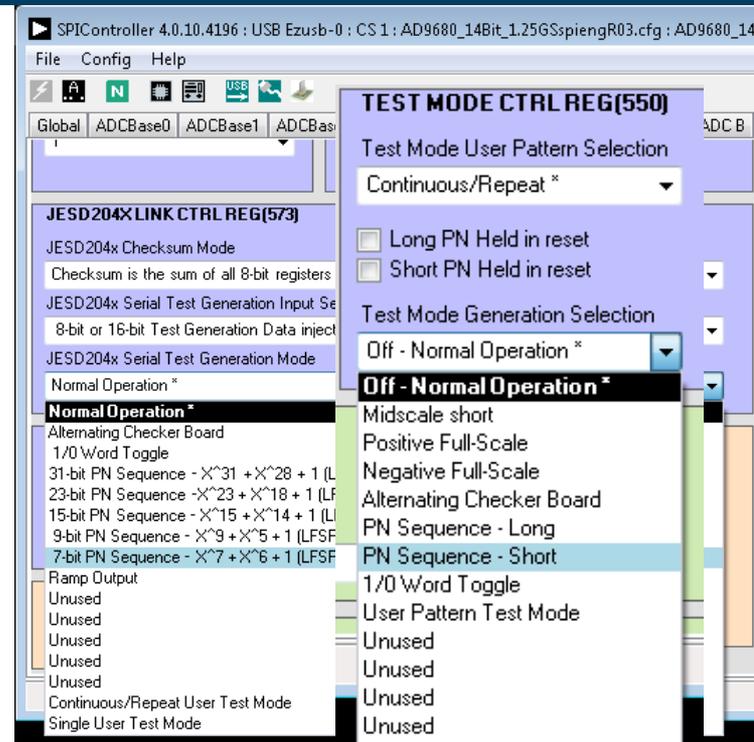
JES204B debugging using the ADS7 platform

- ▶ FPGA registers accessible using direct register access in SPI Controller or ACE
 - Register bits for each of the 1st 5 LEDs are accessible
 - They have the same function as the LEDs
 - Error checking of captured data:
 - Not-in-table error flags, one bit per lane to indicate not-in-table errors have been detected by JESD204 IP during ADC data capture.
 - Disparity error flags, one bit per lane to indicate disparity errors have been detected by JESD204 IP during ADC data capture.
 - Unexpected K error flags, one bit per lane to indicate unexpected K characters have been detected by JESD204 IP during ADC data capture.
 - Continuous GT error checking
 - checking begins at system reset, and continues until the next reset
 - 64-bit total error count register - count is bytes per lane
 - Not-in-table (NIT) error count, 16-bits per lane, bytes are counted, count stops if max is reached
 - Disparity (DISP) error count, 16-bits per lane, bytes are counted, count stops if max is reached
 - See the device specific ADS7 data capture user guide for complete list of FPGA registers and their location

Using ADC Test Modes to Debug the Link

- ▶ There are several test modes available that can be used in conjunction with Visual Analog and/or a high-speed scope to help diagnose link issues
 - PRBS patterns (also called a PN sequence) are typically available at the ADC output or the PHY input
 - For signal integrity testing (8b10b or ILAS errors are occurring) enable the pattern at the PHY input (R0x573)
 - Either the PN7 or PN9 sequences can be used
 - Note that the ADS7 board does not currently have pattern checking capability in the FPGA but VA can validate patterns in software
 - If using VA to validate a PRBS pattern, use ADC test mode register (0x550) to insert the pattern at the ADC output.
 - Settings that can offset signal integrity issues include “pre-emphasis” and “swing voltage” on the ADC and equalizer settings on the FPGA

- Note that the ADS7 platform board does not currently have access to the equalizer registers



Page Selector
ADC channel: Channel A

Registers

	Address (Hex)	Name	Data (Hex)	Data (Binary)
-	05BF	JESD serializer drive adjust	05	0 0 0 0 0 1 0 1
Swing voltage				
+	05C1	De-emphasis select	00	0 0 0 0 0 0 0 0
+	05C2	De-emphasis setting for SERDOUT0±	00	0 0 0 0 0 0 0 0
+	05C3	De-emphasis setting for SERDOUT1±	00	0 0 0 0 0 0 0 0
+	05C4	De-emphasis setting for SERDOUT2±	00	0 0 0 0 0 0 0 0
	05C5	De-emphasis setting for SERDOUT3±	00	0 0 0 0 0 0 0 0

Using ADC Test Modes to Debug the Link

► More test modes

- Ramp and other data patterns are available at the ADC output and can also be used when checking for data errors
 - Visual Analog has the ability to check ADC data patterns
 - Ramp, PN9, and PN23
 - VA does not validate PHY test patterns since they are “per lane”
 - Additionally, for some ADC products, the FPGA program will allow you to trigger a VA capture upon a ramp error
 - Scopes with 10b8b decoding can flag 8b10b errors
- User programmable patterns are also available on some ADC’s
 - Can be useful for duplicating a data-dependent issue
 - Disable scrambling and monitor output with high-speed scope that has 10b8b decode capability

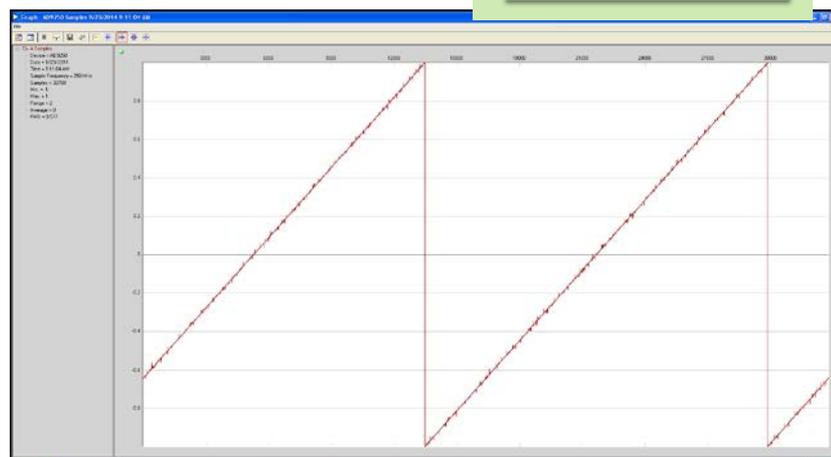
TEST MODE CTRL REG(550)

Test Mode User Pattern Selection
Continuous/Repeat *

Long PN Held in reset
 Short PN Held in reset

Test Mode Generation Selection
Off - Normal Operation *

Off - Normal Operation *
Midscale short
Positive Full-Scale
Negative Full-Scale
Alternating Checker Board
PN Sequence - Long
PN Sequence - Short
1/0 Word Toggle
User Pattern Test Mode
Unused
Unused
Unused
Unused
Unused
Unused
28 Ramp Output



SPIController 4.0.10.4196 : USB Ezusb-0 : CS

File Config Help

Global ADCBase0 ADCBase1 ADCBase2 A

USER TEST PA1(551-552) 0000 Hex OUTPUT Converter I Tie low *

USER TEST PA1(553-554) 0000 Hex OUTPUT Converter I Tie low *

USER TEST PA1(555-556) 0000 Hex OUTPUT Converter I Overrange

USER TEST PA1(557-558) 0000 Hex OUTPUT Ericsson Enabler



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FPGA interface debug

Debugging for users of Xilinx IP in their own system

- ▶ Xilinx Hardware Debug Guide (from Xilinx pg066 user guide):
 - ADI may not currently give users access to these registers on ADS7 platform boards
 - See the device specific [ADS7 data capture user guide](#) for complete list of FPGA registers
 - General Checks
 - Ensure that all the timing constraints for the core were met during implementation
 - Ensure that all clock sources are clean and in particular that the transceiver reference clocks meet the GTX/GTH/GTP transceiver requirements from the appropriate FPGA Data Sheet.
 - Ensure that all GTX/GTH/GTP transceiver PLLs have obtained lock by monitoring the QPLLLOCK_OUT and/or CPLLLOCK_OUT port either using the Vivado lab tools or by routing the signals to a spare pin
 - Ensure that when regenerating a new GTX/GTH/GTP transceiver the reference clock of the new transceiver matches that of the design
 - Obtaining Lane Synchronization
 - Ensure that the AXI4-Lite registers have been programmed with the correct values for the frame size parameters (octets per frame, frames per multiframe) and scrambling enable/disable so the transmitter matches the receiver.
 - In the case of a receiver ensure that SYNC is de-asserted (set to 1) when valid K28.5 (0xBC) characters are received from the GTX/GTH/GTP by monitoring RXDATA and RXCHARISK from the GTX/GTH/GTP using the Vivado lab tools.
 - In the case of a transmitter ensure that core generates valid K28.5 (0xBC) characters to the GTX/GTH/GTP transceiver by monitoring TXDATA and TXCHARISK from the GTX/ GTH/GTP transceiver using the Vivado lab tools until SYNC is de-asserted (set to 1).

Debugging for users of Xilinx IP in their own system

- ▶ Xilinx Hardware Debug Guide (continued):
 - Issues Losing Synchronization Soon After Gaining Synchronization
 - Ensure that the AXI4-Lite registers have been programmed with the correct values for F (Octets per Frame) and K (Frames per Multiframe).
- ▶ Xilinx Interface Debug Guide:
 - Debug AXI4-Lite Interfaces
 - Read from a register that does not have all 0s as a default to verify that the interface is functional. Output `s_axi_arready` asserts when the read address is valid, and output `s_axi_rvalid` asserts when the read data/response is valid. If the interface is unresponsive, ensure that the following conditions are met:
 - The `S_AXI_ACLK` and `ACLK` inputs are connected and toggling.
 - The interface is not being held in reset, and `S_AXI_ARESET` is an active-Low reset.
 - The interface is enabled, and `s_axi_aclken` is active-High (if used).
 - The main core clocks are toggling and that the enables are also asserted.
 - If the simulation has been run, verify in simulation and/or a Vivado lab tools capture that the waveform is correct for accessing the AXI4-Lite interface.

Debugging for users of Altera IP

- ▶ From Altera JESD204B IP Core User Guide (UG-01142):
 - Consult chapter 7 of Altera's IP user guide for a detailed description of the guidelines and tools to use when debugging the JESD204B Link
 - General Checks
 - Clocking
 - Check that the frame and link clock frequency settings are correct in the Altera PLL IP core. For the design example, the frame clock is assigned to outclk0 and link clock is assigned to outclk1.
 - Check the device clock frequency at the FPGA and converter.
 - For Subclass 1, check the SYSREF pulse frequency.
 - Check the clock frequency management. For the design example, using Stratix V and Arria V devices, this frequency is 100 MHz
 - Verify all parameters are matching between the JTX and JRX
 - Troubleshooting tips:
 - Turn off the scrambler and descrambler options as needed.
 - Use single lane configuration and $K = 32$ value to isolate multiple lane alignment issue.
 - Use Subclass 0 mode to isolate SYSREF related issues like setup or hold time and frequency of SYSREF pulse.

Debugging for users of Altera IP

- ▶ From Altera JESD204B IP Core User Guide (UG-01142):
 - General Checks (continued)
 - SPI Programming tip (check for proper sequence)
 - Altera recommends that you first perform a single register bit setting (for the scramble (SCR) or lane (L) parameters, for example) and then verify that each row of the MIF has the same number of bits as the data width of the ROM that stores the MIF.
 - Miscellaneous checks:
 - Ensure that the sampling rate of the converter is within the minimum and maximum requirements
 - Ensure the lane rates are within the operating specs of both the converter and FPGA
 - Verify pin assignments and signal polarities for SYNC and SYSREF are appropriate
 - Debugging the link using Signal Tap
 - Design must contain a Qsys subsystem with the JTAG-to-Avalon-MM Master bridge component
 - Consult UG-01142

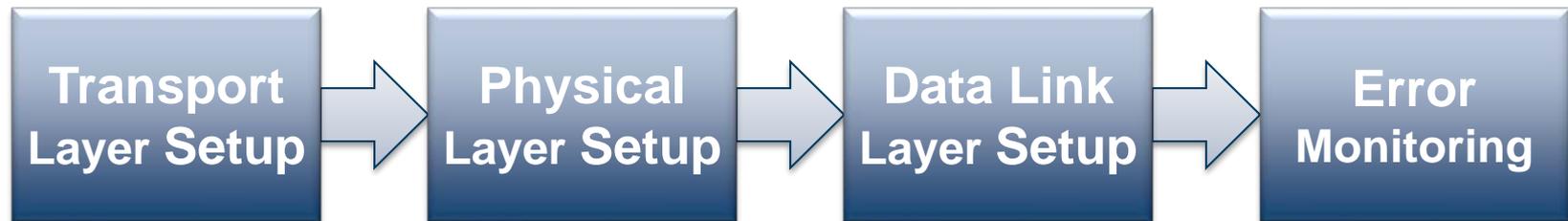


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HDC Product 204B Link Startup and Debug

DAC Startup Overview

Follows Device Setup Guide (in datasheet)



- SERDES Parameters
- Mode Config (L/M/F/S)

- SERDES PLL
- Equalizer

- Deterministic Latency (Subclass 0,1)
- Crossbar

- CGS/FS/CS/ILAS
- Disparity, Not in Table, Unexpected Control Character

DAC Startup : Connect Hardware

- ▶ Before configuring the part, ensure the following items are connected to the board:
 - 5V Power Supply (non-FMC boards)
 - FMC evaluation boards are powered through the FMC connector, no external supply needed
 - Clock source
 - Provide a clean clock source to the evaluation board – distributed on the board to the DAC and FPGA for appropriate clocking needs
 - USB cable to PC
 - Used for SPI communication to the boards
 - Note: FMC boards have option to send SPI over the FMC connector
 - SMA cable to measurement instrument
 - Spectrum analyzer or oscilloscope

- ▶ *Make sure all of these items are connected properly, powered on and stable before moving onto next steps*

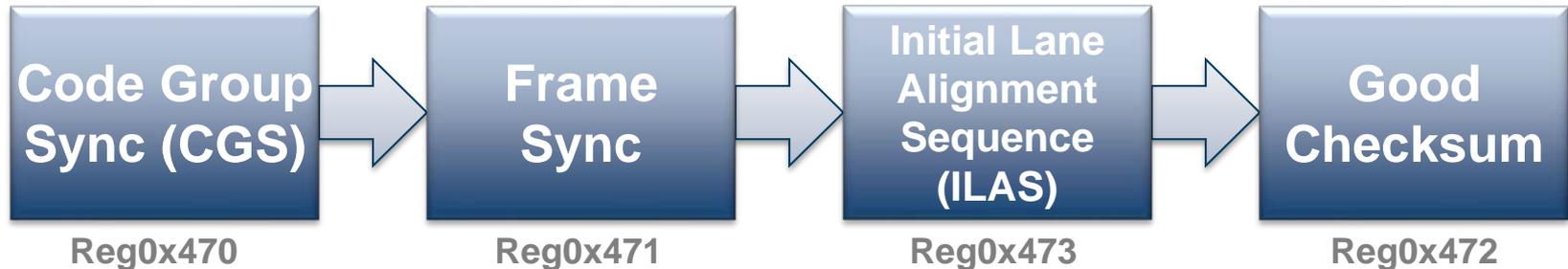
DAC Startup: Using the Device Setup Guide

- ▶ The “Device Setup Guide” is included in the AD9144, AD9136/AD9135, AD9154 and AD9152 datasheets
- ▶ Lists out all register write sequences necessarily to start up the DAC with SERDES interface
- ▶ Worksheet format meant to be self-helping to assist users in calculating their specific condition settings based on the DAC rate, interpolation, and SERDES Mode used
 - Uses variable names where it’s necessary to calculate the appropriate setting for different conditions.
 - Formulas and tables needed for variable/register calculations are included in the summary sections at the end of the Setup Guide. More details for a given section can be found in the remainder context of the datasheet.
 - Gray shaded region denotes the summation of the individual bit variable values for a given register where needed.

Addr.	Bit No.	Value	Variable	Description
0x000		0xBD		Soft reset.
0x000		0x3C		De-assert reset, set 4-wire SPI.
0x011		0x		
	7	0		Power up band gap.
	[6:3]		PdDACs	PdDACs = 0 if all 4 DACs are being used. If not, see the DAC Power-Down Setup section.
	2	0		Power up master DAC.
0x080		0x	PdClocks	PdClocks = 0 if all 4 DACs are being used. If not, see the DAC Power-Down Setup section.
0x081		0x	PdSysref	PdSysref = 0x00 for Subclass 1. PdSysref = 0x10 for Subclass 0. See the Subclass Setup section for details on subclass.

JES204B debugging using ADI DACs

- ▶ Check PLL lock status (0x281[0])
 - If not locked, check CLK input frequency and signal integrity
- ▶ Check the status of each Logical/Link Lane being used
- ▶ Each lane will go through the following steps as it begins to establish the links
 - Flags are paged to read back the status for the QBD selected by CurrentLink
 - For each read back, if Bit $x = 1 \rightarrow$ Link Lane x passed that block



- Link lane has received at least 4 consecutive K28.5 (/K/) characters if it passes this stage
- Link lane has passed initial frame synchronization
- Link lane has passed initial lane alignment sequence
- The checksum sent over the lane matches the sum of the JESD204B parameters sent over the lane during ILAS for that link lane

JES204B debugging using ADI DACs

- ▶ If all the Link Lanes on a link being used for the given condition have passed CGS, Frame Sync and ILAS → that link has been established properly
 - Good Checksum passing is not a requirement to establish the link
 - Configuration Mismatch (CMM) is also not a requirement to establish the link
 - This indicates whether the parameters sent by the transmitter/FPGA (Registers 0x400 to 0x40D) match the parameters that were programmed into the receiver/DAC (Registers 0x450 to 0x45D) – different check than the good checksum flags which only check the transmitter parameters calculated checksum vs checksum value sent over the link by the transmitter
 - Note: Modes 11, 12 and 13 on the AD9135/AD9136 will have this error flag due to the need to program different L and M parameters on the TX vs the RX
- ▶ If all the Link Lanes have not passed these stages, there was an issue establishing the link

JES204B debugging using ADI DACs

► Debug options if the link is NOT established:

- If the SERDES PLL is not locked:

- Check the frequency and signal integrity of the CLK input
- Check the PLLDIV setting in register 0x289[1:0] to ensure it matches the desired lane rate range

LaneRate (Gbps)	Divide by (DivFactor)	SERDES_PLL_DIV_MODE, Register 0x289[1:0]
1.44 to 2.76	1	2
2.88 to 5.52	2	1
5.75 to 10.64	4	0

- If the SERDES PLL locks but the CGS/FrameSync/ILAS flags do not all pass, some areas to check are:
 - If CGS fails → typically an issue with the clock
 - Perhaps the PLL is locked but at the incorrect frequency
 - If ILAS fails → fails if the /R/, /A/ or /Q/ control characters do not fall in the appropriate places during the first 4 ILAS multiframes
 - This can occur if there is a configuration mismatch between the JTX and JRX

JES204B debugging using ADI DACs

- ▶ Debug options if the link is NOT established:
 - FPGAs normally have the ability to run in 'loop back' mode to confirm that the transmitter is not the issue when trying to establish the link
 - Recommended to be done before connecting up the DAC to eliminate the first round of debug questions/issues that may occur
 - PHY PRBS Testing: enables BER testing of each physical lane of the links on the DAC, does NOT require the link to be established
 - PRBS7, PRBS15 and PRBS31 supported

Useful Debug Test Modes on ADI DACs

► The PHY PRBS Test can be used as part of BER testing in order to test the signal integrity of the 204B lanes

- Tests are performed on a “per lane” basis (1 lane at a time)
- Link does not need to be established
- Test procedure
 1. Start PRBS7, PRBS15, or PRBS31 pattern at the JESD204B transmitter.
 2. Select appropriate PRBS pattern in the PHY_PRBS_PAT_SEL register (0x316[3:2])
 3. Enable PHY test for all lanes being tested using the PHY_TEST_EN register (0x315).
 - Each bit PHY_TEST_EN enables the PRBS test for the corresponding lane (bit 0 for lane 0, etc.)
 4. Toggle PHY_TEST_RESET (register 0x316[0]) from 0 to 1 then back to 0.
 5. Set PHY_PRBS_ERROR_THRESHOLD (register 0x319 to register 0x317) as desired.
 6. Write a 0 and then a 1 to PHY_TEST_START (register 0x316[1]) to start the test.
 7. Wait 500 ms.
 8. Stop test - PHY_TEST_START (0x316[1]) = 0.
 9. Read PRBS test results.
 - Each bit of PHY_PRBS_PASS (register 0x31D) corresponds to one SERDES lane: 0 is fail, 1 is pass.
 - The number of PRBS errors seen on each failing lane can be read by writing the lane number (0 to 7) to the PHY_SRC_ERR_CNT register (0x316[6:4]) and reading the PHY_PRBS_ERR_COUNT registers (bits[23:0] at registers 0x31C - 0x31A).
 - Max error count is 2^{23} .

-	0315	PHY_PRBS_TEST_EN	00	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		PHY_test_en		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-	0316	PHY_PRBS_TEST_CTRL	00	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		PHY_test_reset																	0
		PHY_test_start																	0
		PHY_PRBS_pat_sel								0	0								
		PHY_src_err_cnt								0	0	0							
+	0317	PHY_PRBS_TEST_THRESHOLD_LObits	00	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
+	0318	PHY_PRBS_TEST_THRESHOLD_MIDbits	00	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
+	0319	PHY_PRBS_TEST_THRESHOLD_HIbits	00	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
+	031A	PHY_PRBS_TEST_ERRCNT_LObits	00	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
+	031B	PHY_PRBS_TEST_ERRCNT_MIDbits	00	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
+	031C	PHY_PRBS_TEST_ERRCNT_HIbits	00	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
+	031D	PHY_PRBS_TEST_STATUS	FF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Useful Debug Test Modes on ADI DACs

- ▶ The Short Transport Layer (STPL) Test can be used to validate that the JTX design in the logic device is packing the frames of samples appropriately
 - Link must be established and running w/out errors prior to running this test
 - Each sample within a frames worth of data must have a unique value as assigned at both the JTX and the JRX
 - Test procedure
 1. Synchronize the JESD204B link.
 2. Enable the STPL test at the JESD204B Tx. (in the FPGA)
 3. Select Converter 0 Sample 0 for testing.
 - Write SHORT_TPL_DAC_SEL (Register 0x32C[3:2]) = 0 and SHORT_TPL_SP_SEL (Register 0x32C[5:4]) = 0.
 4. Set the expected test sample for Converter 0, Sample 0.
 - Program the expected 16-bit test sample into the SHORT_TPL_REF_SP registers (Register 0x32E and Register 0x32D).
 5. Enable the STPL test.
 - Write SHORT_TPL_TEST_EN (0x32C[0]) = 1
 6. Toggle the STPL reset.
 - SHORT_TPL_TEST_RESET (Register 0x32C[1]) from 0 to 1 then back to 0.
 7. Check for failures.
 - Read SHORT_TPL_FAIL (Register 0x32F[0]): 0 is pass, 1 is fail.
 8. Repeat Step 3 to Step 7 for each sample of each converter, Conv0Sample0 through ConvM – 1SampleS – 1.

Registers				
	Address (Hex)	Name	Data (Hex)	Data (Binary)
-	032C	SHORT_TPL_TEST_0	00	0 0 0 0 0 0 0 0
		short_tpl_test_en		
		short_tpl_test_reset		
		short_tpl_DAC_sel		0 0
		short_tpl_sp_sel		0 0
-	032D	SHORT_TPL_TEST_1	00	0 0 0 0 0 0 0 0
		short_tpl_ref_sp_LSB		0 0 0 0 0 0 0 0
-	032E	SHORT_TPL_TEST_2	00	0 0 0 0 0 0 0 0
		short_tpl_ref_sp_MSB		0 0 0 0 0 0 0 0
-	032F	* SHORT_TPL_TEST_3	00	0 0 0 0 0 0 0 0
		short_tpl_fail		

Device Setup Guide: Error Monitoring

- ▶ Error monitoring options after the link is established properly:
 - Per Section 7.6 of JESD204B specification: the DAC can detect the following errors after the link has been established and can optionally issue a sync request and reinitialize the link when any of these errors occur:
 - Disparity Errors (DIS): this error counter counts ALL characters with invalid disparity, even if they are NOT in the 8b/10b decoding table
 - Minor deviation from the JESD204B spec, only counts errors when they ARE in the 8b/10b table
 - Not In Table Errors (NIT): code group received is not found in the 8b/10b decoding table
 - Unexpected Control Character Errors (UCC): the control character received is not expected at the given character position
 - These errors are counted on a per lane and per error type basis
 - Error count threshold can be set (same threshold used for all 3 error types)
 - Errors can also be monitored via the $\overline{\text{SYNCOUTx}} \pm$ signal
 - If one or more of any of these 3 errors occurs, the $\overline{\text{SYNCOUTx}} \pm$ signal is asserted for some pulse period of time (programmable to be $\frac{1}{2}$, 1, or 2 PClock cycles width)

* Details on the registers and how to program these error monitoring options can be found in the datasheet (JESD204B Error Monitoring)

Summary of Common Link Issues

▶ Link is down

▪ CGS errors

- Symptoms – SYNC~ toggling (wide pulses), CGS error flags/interrupts (of course!)
- Possible causes (in descending order of likelihood)
 - Input clock issue - check frequency and signal integrity of the ref clock on both sides of the link
 - Check for configuration match and for valid configuration (DS contains list of valid “204B modes”)
 - Check for signal integrity issues on 204B lanes

▪ ILAS errors

- Symptoms - SYNC~ toggling (wide or narrow pulses), ILAS error flags/interrupts
- Possible causes:
 - Configuration mismatch between JTX and JRX
 - Check for checksum and configuration mismatch flags, verify setting on both sides of the link
 - If custom FPGA/ASIC code is being used, the format of the ILAS could be corrupt (yes, I’ve seen this!)
 - Validate the ILAS pattern is per JESD204B spec (even the ramp data)

▶ Corrupted/unexpected sample data

▪ Symptoms – incorrect data at the JRX output, 8b10b errors

▪ Possible causes:

- Poor signal integrity on 204B lanes
 - Check eye diagram, try “tuning” emphasis and voltage swing settings at JTX and/or EQ settings at JRX
- Lane swap
 - Verify crossbar mux settings on both ends are appropriate for the pcb routing of the 204b lanes
- Incorrect DSP settings – decimation, interpolation, etc.



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Thanks!