

## Chapter XII

# Use a Wideband, Integer-N, PLL Synthesizer as a Direct 6-GHz Local Oscillator

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### INTRODUCTION

Establishing a new benchmark for speed and RF phase-noise performance, the ADF4106 Phase-Locked-Loop Synthesizer is fully specified to operate at frequencies up to 6.0 GHz. This allows designs for the upper ISM band of 5.4 GHz-to-5.8 GHz to be greatly simplified. Fabricated on an advanced 0.35- $\mu\text{m}$  BiCMOS process, it

displaces the pin- and software-compatible 4-GHz ADF4113 as the fastest available integer-N synthesizer—and can achieve 3-dB lower phase noise to boot! It requires only a 3.3-V supply, yet its  $V_P$  pin is specified at up to 5.5 V, for compatibility with tuning voltage levels often required by modular VCOs used in base stations.

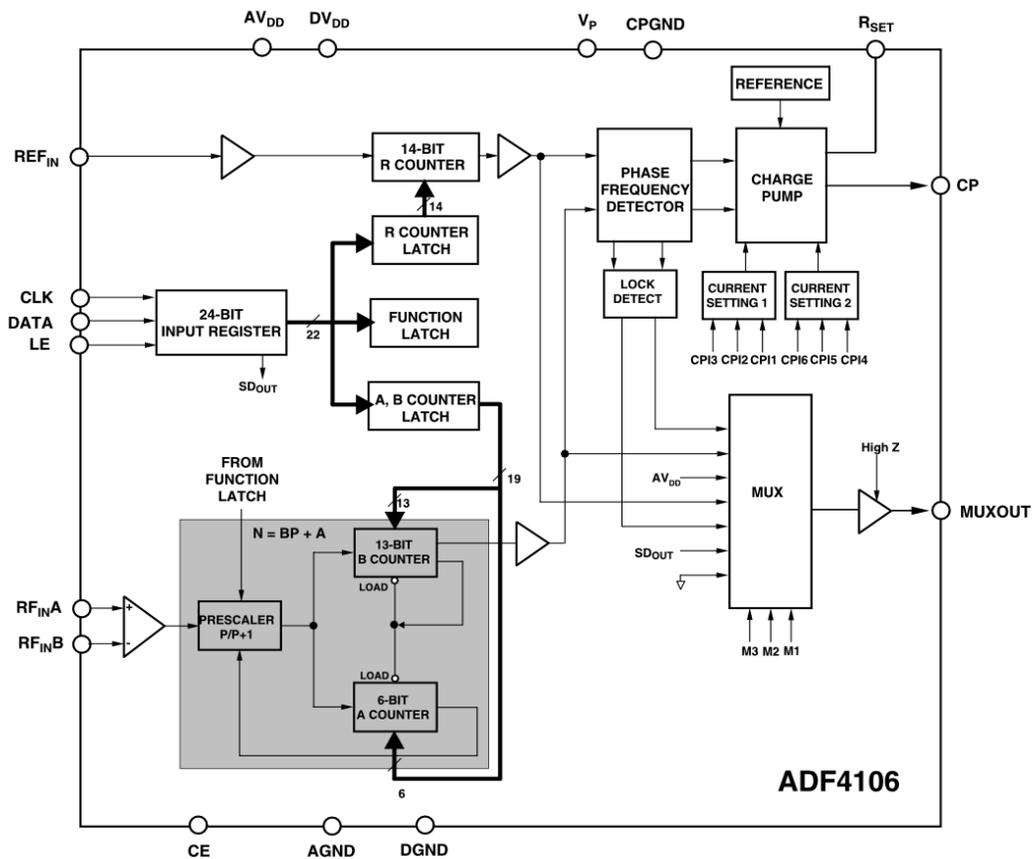


Figure 1. Functional block diagram of the ADF4106

The ADF4106 frequency synthesizer (Figure 1) can be used to implement local oscillators (LOs) in the up- and down-conversion sections of wireless receivers and transmitters. It consists of a low-noise digital phase-frequency detector (PFD), a precision charge pump, a programmable reference divider, programmable A and B counters and a dual-modulus prescaler (P/P+1). The A (6-bit) and B (13-bit) counters, in conjunction with the dual-modulus prescaler (P/P+1), implement an N-divider ( $N = BP+A$ ).

In addition, the 14-bit reference (R) counter, allows selectable REF<sub>IN</sub> frequencies at the PFD input. A complete phase-locked loop (PLL) can be implemented if the synthesizer is used with an external loop filter and voltage-controlled oscillator (VCO). Its very high bandwidth means that frequency doublers can be eliminated in

many high-frequency systems, simplifying system architecture and lowering cost.

The standard PLL system architecture, used by the ADF4106—and its predecessor, the ADF4113—is shown in Figure 2. Since the maximum operating frequency of the ADF4113 is about 4 GHz, higher frequencies require the use of a frequency doubler—which usually calls for an extra RF amplifier to produce an adequate level for the doubler. Use of the ADF4106 eliminates the frequency doubler and its associated circuitry, achieving a much simpler and more power-efficient LO. For example, the design shown in Figure 3 generates RF output frequencies, with 1-MHz channel separation, from 5.4 GHz up to 6.0 GHz. The phase noise measured at the upper end was -83 dBc/Hz.

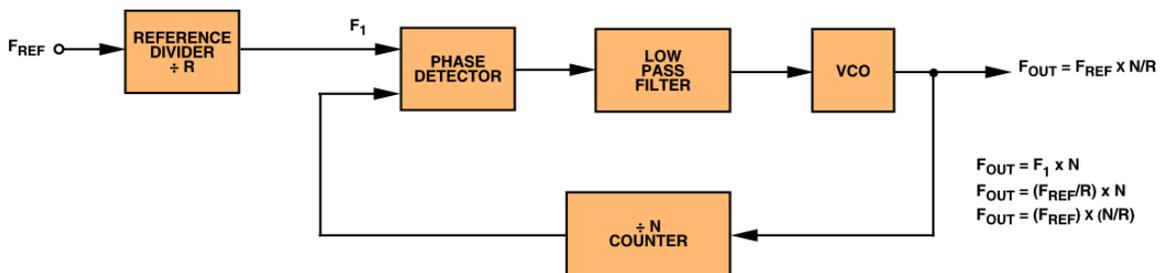


Figure 2. Standard PLL architecture



A typical wireless system might be generating frequencies in 200-kHz increments from 1450 MHz to 1500 MHz. Using an integer-N architecture to do this, a phase/frequency-detector reference frequency of 200 kHz is needed, and the N value would vary from 7250 (1450 MHz) to 7500 (1500 MHz).

Using the ADF4106 for best performance would give a phase noise figure of  $-88$  dBc/Hz. Typical reference spurs in such a system would be  $-88$  dBc at 200 kHz and  $-90$  dBc at 400 kHz. Implementing a loop bandwidth of 20 kHz, typical lock time to 10 degrees of phase error would be 250  $\mu$ s.

However, the wideband operation possible with the ADF4106 allows an alternative architecture to be considered, shown in Figure 4. In this configuration, the core PLL is operated at a multiple of the final desired output frequency. In the example given above, the final desired frequency range is 1450 MHz to 1500 MHz. A multiple within the device's frequency range is to 5800 MHz to 6000 MHz (4 times the desired output band). In the proposed scheme, shown in Figure 4,  $F_{PFD}$  operates at 800 kHz, the  $F_{VCO}$  band is 5800 MHz to 6000 MHz, and the final system LO output is obtained by dividing  $F_{VCO}$  by 4.

$$F_{OUT} = (F_{PFD} \times N)/X \quad (3)$$

Some consequences of using this architecture are outlined below.

### Phase-noise reduction

The synthesizer phase noise has a  $10 \log F_{PFD}$  relationship. This means that for every doubling of the PFD frequency, there will be 3-dB degradation in the synthesizer phase noise. However, the output from the VCO will be divided down, and its phase noise obeys a  $20 \log X$  rule. So, for every doubling of X, there will be a gain of 6 dB in phase-noise performance. If the PFD frequency is quadrupled, as above,  $F_{VCO}$  is divided by four, to end up with the correct  $F_{OUT}$ . Thus 6 dB will be lost due to the quadrupling of  $F_{PFD}$  and 12 dB is gained due to the division by four, resulting in an overall gain of 6 dB in phase-noise performance, using Figure 4, compared to the use of the standard architecture. In the above example, the resulting phase noise would be  $-94$  dBc/Hz.

### Reference-spur reduction

In an integer-N PLL, output reference spurs occur at the PFD frequency. In Figure 4, if you consider  $F_{VCO}$ , the reference spurs will be at  $F_{PFD}$ ,  $2F_{PFD}$ ,  $3F_{PFD}$ , etc. However, this gets divided down by X. In the specific example where  $X = 4$ ,

$$F_{OUT} = F_{VCO}/4$$

In this case, the spurs would remain at  $F_{PFD}$ ,  $2F_{PFD}$ ,  $3F_{PFD}$ , etc., but would decrease by 12 dB due to the  $20 \log X$  relationship.

However, the output channel spacing in Figure 4 is  $F_{PFD}/X$ , or  $F_{PFD}/4$ , in this example. So, using the architecture of Figure 4 with  $X = 4$ , and generating an output frequency of 1450 MHz to 1500 MHz with 200-kHz spacing, the reference spurs would not exist at 200 kHz, 400 kHz and 600 kHz. At 800 kHz, the spur level would be  $-90$  dBc.

### Shorter lock time

Since the PFD in Figure 4 is operating at a higher frequency, phase comparisons are

occurring at a higher rate; this will cause the loop to lock faster. In addition, because of the higher PFD frequency, a wider loop bandwidth is possible, and this too helps in improving the lock time. In this example, the lock time is about  $70 \mu\text{s}$  to within  $10^\circ$  of phase error for a PLL loop-bandwidth of 80 kHz.

The actual implementation of Figure 4 is shown in Figure 5.

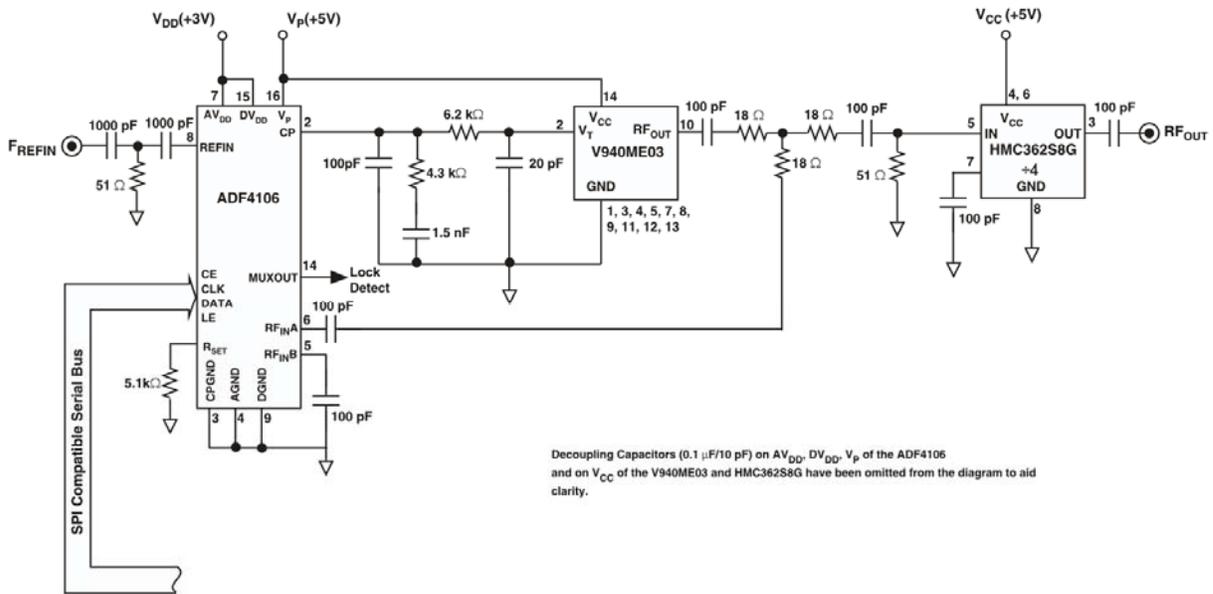


Figure 5. Using the ADF4106 with an output divider to generate a 1.5-GHz local oscillator.

To summarize, the circuit of Figure 5 will provide the following performance:

*Phase Noise*

-94 dBc/Hz @ 1-kHz offset

*Reference Spurs*

<-100 dBc (system noise floor) @

200-kHz, 400-kHz, 600-kHz offsets

-90 dBc @ 800-kHz offset

*Lock Time* 70  $\mu$ s to within 10° phase error

The price of this improved performance is the extra cost of the output divider and the extra power consumption of the system as a whole (the HMC typically adds 68 mA to the ADF4106's 13-mA current requirement). So improved performance must be a critical requirement for going with this architecture. The extra board space needed for implementation is minimal, since the HMC comes in an 8-lead SOIC package.

**BANDWIDTH**

The 0.35- $\mu$ m BiCMOS fabrication process and careful application of RF design techniques permit the prescaler section of the ADF4106 to operate at up to 6.0 GHz with an input level of -10 dBm (referred to 50 ohms), guaranteed over the industrial temperature range (-40 to +85°C). Figure 6 below shows a typical sensitivity plot for the ADF4106 in a TSSOP package at -40°C, +25°C and +85°C. It can clearly be seen that performance to 6 GHz is well within the

limits of the device with signals below -15 dBm.

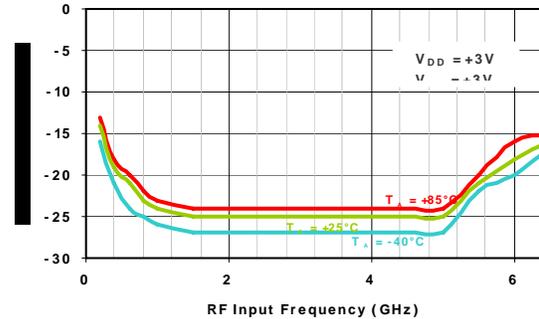


Figure 6. ADF4106 sensitivity vs. frequency.

**PHASE NOISE**

Phase noise, a measure of the purity of the local oscillator signal, is the single most critical specification in the local oscillator section of radios—with a direct bearing on receiver sensitivity. It is the ratio, to output carrier power, of the noise power in a 1-Hz bandwidth at a given offset from the carrier. Expressed as a log ratio, the units of phase noise are dBc/Hz. Phase noise is typically measured with a spectrum analyzer.

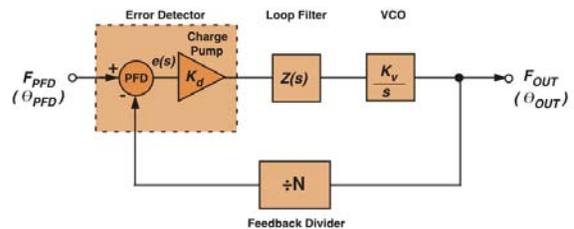


Figure 7. Basic phase-locked-loop model.

The circuit of Figure 7 establishes the circuit model for the following discussion of phase noise,

Total phase noise in a phase-locked loop (dB) can be expressed as follows:

$$PN_{TOTAL} = PN_{SYNTH} + 20\log N + 10\log F_{PFD} \quad (1)$$

where  $PN_{TOTAL}$  is the total phase noise of the PLL

$PN_{SYNTH}$  is the phase noise due to the PLL synthesizer circuit itself

$20 \log N$  is the increase of phase noise due to the frequency magnification associated with the feedback ratio,  $1/N$ .  $10 \log F_{PFD}$  is the increase of noise associated with the incoming PFD frequency. The graph in Figure 8 shows the ADF4106's phase noise characteristics as a function of PFD frequency,  $F_{PFD}$ .

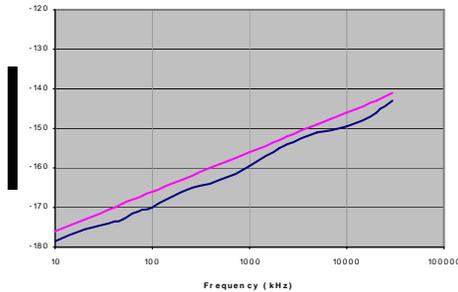


Figure 8. ADF4106 Phase Noise vs. PFD Frequency.

With a given measured total noise, synthesizer noise can be inferred as:

$$PN_{SYNTH} = PN_{TOTAL} - 20\log N - 10\log F_{PFD} \quad (2)$$

This provides a figure of merit for the PLL Synthesizer circuit itself, irrespective of the noise contributed by PLL N value and PFD frequency, since these would be the same for any similar circuit being compared. For the ADF4106, this figure comes out to  $-219$  dBc/Hz—a 3 dB improvement on the ADF4113, which had been the best available integer-N synthesizer in terms of phase noise.

With this phase noise figure of merit, an engineer can work out the total PLL phase noise for any given PFD frequency and RF output frequency. For example, consider generation of a local oscillator signal with frequencies from 1700 MHz to 1800 MHz, and channel spacing of 200 kHz. Using equation (1), the close-in phase noise using the ADF4106 as the PLL synthesizer is

$$\begin{aligned} PN_{TOTAL} &= -219 + 20\log(9000) + 10\log(200 \times 10^3) \\ &= (-219 + 79 + 53) \text{ dBc/Hz} \\ &= -87 \text{ dBc/Hz} \end{aligned}$$

Figure 8 shows that the ADF4106 obeys the  $10 \log F_{PFD}$  “rule” (PFD phase noise substantially linear with log frequency) fairly consistently all the way to 30 MHz. Some integer-N devices begin to degrade rapidly once the PFD frequency goes above 1 MHz.

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