Chapter III
RF/IF Components and Specifications for Transmitters
RF/IF Components and Specifications for Transmitters

- Transmit DACs
- IQ Modulators
- Amplifiers
- Synthesizers
- RF Power Detectors
- Gain/Phase Detectors
- Vector Modulators
Transmit DACs

- Baseband DACS (usually sold in duals) generate baseband modulated drive signals for IQ Modulators
  - Higher order modulation schemes $\rightarrow$ higher resolution DACs
  - Higher symbol rates $\rightarrow$ higher DAC sampling rates
- IF Synthesizing DACS digitally up convert the baseband signal and produce a low Intermediate Frequency either in real form (single DAC) or in complex form (dual DAC)
  - IF Synthesizing DACs $\rightarrow$ higher performance than Baseband DACs
  - Eliminate the need for one PLL and one mixer
  - Produce better modulation quality (lower EVM)
IQ Modulators
RF Components – IQ Modulators

- An un-Modulated Sinewave drives LO input (from PLL). LO is split into “Quadrature” components of equal amplitude but 90 degrees out of phase.
- I and Q drive signals are multiplied by LO Quadrature Components and then combined to make IF or RF output.
- The phase and amplitude of the output carrier can be adjusted continuously if the amplitude of the I and Q signals is varied (vector modulation).
- For QPSK Modulation, input to I and Q can be a (filtered) Digital Bit Streams of +1 and -1 (not 1 and 0).
- For QAM Modulation, I and Q will be multi-level (driven from DAC).
RF Components – IQ Modulators

- Critical IQ Mod Specifications
  - Baseband Bandwidth – higher bandwidth allows higher data rate
  - Output Compression Point and Noise Floor – set SNR
  - Quadrature balance of LO Splitter – affects EVM
  - Amplitude balance of LO Splitter – affects EVM
  - LO to RF Out Leakage – adds unwanted component to modulated signal and degrades EVM (is caused by offset voltages on I and Q inputs)
  - Amplitude Balance of I and Q Channels – affects EVM
  - IP2 and IP3 – determine distortion Products that appear in adjacent channels.
  - Amplitude and phase imbalance of any signals affects image suppression in image-reject upconverter
Quadrature Modulation Refresher

RF(t) = A(t)cos(\omega_ct + \theta(t)) = I(t)cos\omega_ct + Q(t)sin\omega_ct

Polar representation

Cartesian representation
Example - Digital Modulation - QPSK

In Practice bit stream is low pass filtered before modulation to limit the bandwidth of the modulated spectrum.
Higher Order Modulation Schemes → Higher Data Rate.

But Symbols are closer together → Requires higher Signal-to-Noise Ratio for demodulation

Increasing “Symbol Rate” increases data rate but widens Spectrum
Symbolic Representation of Quadrature Modulator

\[ V_{\text{out}} = \cos(\omega_1 t) \cos(\omega_2 t) + \sin(\omega_2 t) \sin(\omega_1 t) \]

\[ = \cos((\omega_1 - \omega_2) t) \]

- Local Oscillator signal is split into quadrature components
- Mix with quadrature baseband components and you get a single tone at the difference frequency \((w_1 - w_2)\)
Symbolic Representation of Quadrature Modulator with Errors and Baseband Offset Errors

Vout = (Cos(\(\omega_2\)t)+Vos)Cos(\(\omega_1\)t+\(\phi\)) + (Sin(\(\omega_2\)t)-Vos)Sin(\(\omega_1\)t-\(\phi\)) = 

\[= \frac{\cos((\omega_2-\omega_1)t - \phi) + \cos((\omega_2-\omega_1)t + \phi)}{2} + \cos((\omega_2+\omega_1)t + \phi) - \cos((\omega_2+\omega_1)t - \phi)\]

\[= \text{Lower Sideband}\]

\[= \text{Unwanted Upper Sideband}\]

• Baseband amplitude, offset and phase errors along with LO quadrature errors will produce unwanted components at the LO and image frequencies
• Baseband Offset Compensation can be used to remove LO Leakage
• To remove upper sideband, baseband amplitude and phase compensation is required.
• 2\textsuperscript{nd} and 3\textsuperscript{rd} order harmonics cannot be easily removed
• While Single Sideband Modulation is not used in end-applications, an SSB spectrum gives valuable information about the quality of the WCDMA, CDMA, GMSK, etc spectrum
• Excessive LO leakage, Sideband Leakage and harmonics will increase Error Vector Magnitude (EVM)
• Noise of a modulator is typically specified in dBm/Hz (output referred)
• Noise (dBm) = Noise floor + 10 log(RBW)
• e.g. Noise Floor of –150 dBm/Hz becomes –90 dBm when measured in a 1 MHz Resolution Bandwidth
• In-Band Noise cannot be filtered in a Direct Conversion Architecture (Zero IF or Low IF)
• Direct Conversion Modulators must be designed for high output power, low distortion and low noise floor
• GSM spec calls for a noise floor of –36 dBm (peak-hold, in 100 KHz BW) at the antenna.
• Toughest WCDMA spec calls for –30 dBm (in 1MHz BW) noise floor at the antenna
• CDMA calls for <-13 dBm dBm (in 1 MHz BW) at either 4 MHz (cell band) or 2.25 MHz (PCS band) carrier offset.
• Need to know how much gain (and noise) comes after the modulator to relate modulator noise specs to system requirement
AD8349 Direct I/Q Modulator

KEY SPECIFICATIONS
- Frequency Range: 700 to 2700 MHz
- Modulation Bandwidth DC-160Mhz
- Accuracy:
  - Phase Error: 0.7°
  - Amplitude Error: 0.1dB
- Sideband Suppression -40dBc
- Noise Floor -156dBm/Hz
- P1dB 7.6 dBm (1900MHz)
- Package 16-TSSOP

FEATURES
- Matched 50 ohm output
- TxDAC compatible base band inputs
- Output disable function
Direct Conversion I/Q Modulators

- "FMOD" Family of I/Q Modulators
  - ADL5370  250MHz – 1.3GHz
  - ADL5371  700MHz – 1.3GHz
  - ADL5372  1.6GHz – 2.4GHz
  - ADL5373  2.4GHz – 2.7GHz
  - ADL5374  3.3GHz – 3.8GHz
- OIP3: 24dBm
- Output Noise: -158dBm/Hz
- OP1dB: 11dBm
- Sideband Rejection: >40dBc
- LO leakage: <-40dBm
- LO power: 0dBm
- I/Q Bandwidth: >500MHz
- DC power: 5V, 190mA
## I/Q Modulators

<table>
<thead>
<tr>
<th>Part No.</th>
<th>RF Freq (MHz)</th>
<th>IQ Bandwidth (MHz)</th>
<th>Carrier Suppress (dBm)</th>
<th>Sideband Suppress (dBc)</th>
<th>Noise Floor (dBm/Hz)</th>
<th>P1dB (dBm)</th>
<th>Power Supply (mA)</th>
<th>Package</th>
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<tr>
<td>AD8345</td>
<td>140 to 1000</td>
<td>80</td>
<td>-42</td>
<td>-42</td>
<td>-155</td>
<td>2.5</td>
<td>65</td>
<td>16-lead TSSOP</td>
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<tr>
<td>AD8346</td>
<td>800 to 2500</td>
<td>70</td>
<td>-42</td>
<td>-36</td>
<td>-147</td>
<td>-3</td>
<td>45</td>
<td>16-lead TSSOP</td>
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<td>AD8349</td>
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<td>160</td>
<td>-42</td>
<td>-43</td>
<td>-156</td>
<td>6</td>
<td>135</td>
<td>16-lead TSSOP</td>
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<td>ADL5390</td>
<td>20 to 2400</td>
<td>230</td>
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<td>N/A</td>
<td>-150</td>
<td>+13</td>
<td>130</td>
<td>24-Lead LFCSP</td>
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<td>ADL5385*</td>
<td>50 to 1000</td>
<td>700</td>
<td>-41</td>
<td>-40</td>
<td>-158</td>
<td>+9</td>
<td>250</td>
<td>24-Lead LFCSP</td>
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<tr>
<td>ADL5370-74*</td>
<td>250-3800</td>
<td>500</td>
<td>-40</td>
<td>-40</td>
<td>-158</td>
<td>+11</td>
<td>190</td>
<td>24-Lead LFCSP</td>
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</tbody>
</table>

* Preliminary Data
RF Components – Amplifiers

- RF Amps
  - Input and Output Impedance is 50-1000 Ω
  - Fixed or Variable Gain
  - Specify Noise as Noise Figure (dB)
  - Specify power-handling capability as P1dB
  - Specify Intermodulation Distortion as IP2 and IP3

- Op Amps
  - High Input Impedance
  - Very Low Output Impedance
  - Gain set using Feedback
  - Specify Noise in nV/√Hz
  - Specify Voltage Swing (rail-to-rail, etc.)
  - Specify Harmonic Distortion in dBc
Intermodulation Distortion*

- IMD products are produced by all active components (mixers, amps, ADCs, DACs)
- Third Order IMD Products (close to carrier, \(\text{nF}_1 + \text{-mF}_2, \text{n+m}=3\)) are most troublesome
  - In Transmitters: IMD causes interference in adjacent channels
  - In Receivers: Blocker inter-mod products can fall on the desired signal and desensitize the receiver
- Second Order IMD Products (\(\text{F}_2-\text{F}_1, \text{n=m}=1\)) cause problems in Direct Conversion Receivers
  - Example: Two RF tones 20 kHz apart produce a 20 kHz product at baseband
- Two-Tone test is commonly used to predict behavior
**Noise**

- A background noise power of -174 dBm/Hz is present at every point in a signal chain.
- **NF = Noise Figure (dB) = 10 \log (Noise Factor)**
- **Noise Power: P = kT (Watts)**
  - \( k = 1.38 \times 10^{-23} \text{ J/K} \) (Boltzman’s constant)
  - \( T = \text{Kelvin Temperature 298K (25 degC)} \)
- **Noise Power (dBm) = 10 \log (kT/1mW)**
  - \( = 10 \log kT + 30 = -173.9 \text{ dBm} \approx -174 \text{ dBm} \)
- **Noise in a bandwidth B in Hz**
  - \( = -174 \text{ dBm/Hz} + 10 \log B \)
- **Noise Floor, or minimum discernable signal (MDS)**
  - \( = -174 \text{ dBm} + 10 \log B + \text{NF} \)
- **Receiver Sensitivity for demodulation at a given carrier to noise (C/N) ratio**
  - \( = -174 \text{ dBm} + 10 \log B + \text{NF} + \text{C/N} \)
  - This is the customer’s design specification!
Noise & IP3 combine to yield Spurious Free Dynamic Range (SFDR)

\[ SFDR = \frac{2}{3} [IP3 - Noise Floor] \]

- Bottom end of SFDR is defined by the required signal-to-noise ratio (to demodulate signal)
- Top end of SFDR is defined by point at which IMD products become equal to noise floor
- SFDR is defined differently for ADCs and DACs
ADL5322/5323 1/2W Driver Amplifiers

- GaAs-based PA drivers with internal matching.
- Operating Frequencies 700-1000 MHz, 1700-2400 MHz
- Gain: 20 dB
- Gain Stable vs. Temp (±0.5dB) and Freq (±0.25dB in-band)
- OIP3: +40/42 dBm
- OP1dB: +27 dBm
- Noise Figure: 4.3/5.1 dB
ADL5323 Single Carrier ACPR

- Low and Noise and Low Distortion results in very low Adjacent Channel Power Leakage
- Reducing Output Power will improve Distortion but will degrade SNR
ADL5330 1MHz to 3GHz Variable Gain Amplifier

KEY SPECIFICATIONS

- Frequency Range 1MHz to 3GHz
- OIP3 31 dBm @ 900 MHz
- Output Noise Floor -150 dBm/Hz
- 50Ω Differential or Single-Ended Input
- Gain Control Range: -34 dB to +22 dB @ 900 MHz
- Package 4x4mm 24-LFCSP

FEATURES

- Voltage-Controlled Amplifier/Attenuator
- Optimized for Controlling Output Power
- Fully-Balanced Differential Signal Path
- Linear-in-dB Gain Control Function, 20 mV/dB
ADL5330: 1MHz to 3GHz VGA

Gain vs. Gain Control Voltage

Gain - dB

Vgain - Volts

-40 -30 -20 -10 0 10 20 30 40

0 0.2 0.4 0.6 0.8 1 1.2 1.4 1.6

100 MHz
900 MHz
1900 MHz
2200 MHz
ADL5330: 1MHz to 3GHz VGA
OIP3, P1dB and Noise Floor vs. Gain @ 900 MHz
# RF/IF Transmit Amplifiers

<table>
<thead>
<tr>
<th>Part#</th>
<th>Freq Range (MHz)</th>
<th>Gain (dB)</th>
<th>Output IP3 (dBm)</th>
<th>Output P1dB (dBm)</th>
<th>Noise Figure (dB)</th>
<th>Comments</th>
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<td>AD8353</td>
<td>1 to 2700</td>
<td>20</td>
<td>23.6</td>
<td>9.1 (900 MHz)</td>
<td>5.3</td>
<td>Rx or Tx</td>
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<td>AD8354</td>
<td>1 to 2700</td>
<td>20</td>
<td>19</td>
<td>4.8 (900 MHz)</td>
<td>4.2</td>
<td>Rx or Tx</td>
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<td>ADL5322</td>
<td>700-1000</td>
<td>20</td>
<td>42</td>
<td>27</td>
<td>5.1</td>
<td>Matched Driver Amp</td>
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<td>ADL5323</td>
<td>1700-2400</td>
<td>20</td>
<td>40</td>
<td>27</td>
<td>4.3</td>
<td>Matched Driver Amp</td>
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<tr>
<td>ADL5330</td>
<td>1-3000</td>
<td>-34 to +22</td>
<td>31</td>
<td>22</td>
<td>8</td>
<td>Tx VGA</td>
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</tbody>
</table>
Oscillators and PLLs
Phase Locked Loops convert a reference frequency $f_{\text{REF}}$ to a higher frequency $f_0$, which is highly stable.

- Integer-N PLLs produce an output frequency that is an integer multiple of the reference frequency.
- Fractional-N PLLs can produce an output which is not an integer multiple of the reference frequency (N can now have a fractional component).

Phase noise and lock time are a PLL’s most critical specifications.

Output frequency is generated by a Voltage Controlled Oscillator (VCO) which may be integrated with the PLL (ADF4360) at the cost of degraded phase noise.
Why is PLL phase noise so important?

Reciprocal mixing occurs when the phase noise (side-skirts) of the LO mixes with an unwanted signal and produces an unwanted interference on top of the desired signal.
Phase noise vs. Thermal noise

Strong blocker is modulated by phase noise of LO and interferes with desired signal.

- Phase noise “spreads” the desired carrier and is usually specified in dBc/Hz at a particular offset from the LO (usually 1 or 10 KHz).
- Background or Thermal noise which is present at all points in the signal chain will be amplified if there is gain in the signal chain.
- Amplifier/Mixer Noise Figure will add additional noise to the output of the signal chain (see slide 26). This resulting noise is usually specified in dBm/Hz.
RF Power Detectors
Why measure RF/IF power?

- Thermal Dimensioning (mostly HPA)
- Signal Leveling in receivers (high precision generally not required, usually done at IF)
- Set mobile’s power level (RSSI measurement in BTS receiver)
- Prevent interference with other systems and other users in same cell (mobile handset).
- Improve mobile talk time (operate at low end of permissible range, reduce SAR).
- Improve network robustness (operate at high end of permissible range).
Transmit Power Measurement/Control Options

(a) Transmit Power Measurement/Control Options

(b) Transmit Power Measurement/Control Options

(c) Transmit Power Measurement/Control Options

(d) Transmit Power Measurement/Control Options

ADP

RSSI

OUTPUT

BASEBAND

OUTPUT

RECEIVER

REPL

DAC

ADP

RSSI

OUTPUT

BASEBAND

OUTPUT

RECEIVER

REPL

DAC
Receiver Power Measurement/Control Options

- **Received Power Measurement**
  - LO2
  - AD8361/62
  - AD8318/14
  - ADC

- **Received Power Control**
  - AD8367
  - LO2
  - Vgain for RSSI
  - ADC

- **Measure received power to ensure that the received signal is not too big or not too small when it reaches the end of the signal chain**
- **Precision requirements for detectors in receivers are generally not as critical as in transmitters**
RF Detectors – Critical Specifications

- Linearity and Temperature Stability of Output
- Dynamic Range
- Pulse Response
- Variations due to Power Supply and Frequency Changes
- Ease of Use and Calibration
- Change in response vs. signal crest factor
- Size and overall Component Count
Power Measurement Techniques
Diode Detection

Diode Detector with Temperature Compensation

• Excellent temperature stability at high power
• Limited Dynamic Range and poor low end temp. stability
• High Resolution ADC required for low end power measurement
• Lots of patented techniques which probably improve this performance
Thermal Detection

- Technique is mostly confined to Instrumentation Applications
Logarithmic Amplifiers
Log Amp Transfer Function in Time Domain
Log Amp Transfer Function - Slope and Intercept

Slope = \((V_{o2} - V_{o1})/(P_{i2} - P_{i1})\)

Intercept = \(P_{i1} - V_{o1}/\text{Slope}\)

\(V_{out} = \text{Slope}(P_{in} - \text{Intercept})\)

\(P_{in} = \left(\frac{V_{out}}{\text{Slope}}\right) + \text{Intercept}\)
RF Power Detector Calibration

- VOUT\_IDEAL = SLOPE \times (PIN - INTERCEPT)
- SLOPE = \frac{(VOUT\_1 - VOUT\_2)}{(PIN\_1 - PIN\_2)}
- INTERCEPT = PIN\_1 - \frac{(VOUT\_1)}{SLOPE}
- Error (dB) = \frac{(VOUT - VOUT\_IDEAL)}{SLOPE}
±1 dB Dynamic Range

Temperature Drift can reduce Dynamic Range
### Detector Calibration Procedure

- **Factory Calibration:** Using a precise power source, measure output voltage from the detector with two known input powers at top and bottom of desired input range
- Perform calibration measurements only at room temperature
- Calculate SLOPE and INTERCEPT and store in non-volatile memory
- When equipment is in operation measure detector output voltage using ADC
- Calculate power using “Pin = (Vout/Slope) + Intercept”
- No temperature compensation necessary
Adjust Calibration Points for optimal accuracy over a narrow range

- Calibrate for highest accuracy at max RF power and degraded accuracy at lower powers
Temperature drift vs. Output Voltage at 25°C

- Calibration eliminates error due to non-linearity at 25 °C
Temperature drift vs. Output Voltage at 25°C

- Removes error due to non-linearity at 25°C
- Provides larger dynamic range and improved accuracy
- Method however does not account for non-linearity in the transfer function at room temperature
- For practical implementation, calibration measurements must be taken at multiple input powers (multi-point calibration vs. 2-point calibration)
AD8318: Highest Performance Log Amp

**KEY SPECIFICATIONS**
- Bandwidth 1MHz to 8Ghz
- Stability over temperature: ±0.5 dB
- Pulse response time 10 ns
- Package: 4mm×4mm, 16-pin LFCSP

**FEATURES**
- Integrated temperature sensor
- Low noise measurement/controller output VOUT
- Power-down feature: <1.5 mW at 5 V
- Fabricated using high speed SiGe process
AD8318 High Performance Log Amp

< ±0.5 dB accuracy over temperature

HIGH Linearity OVER 55dB

5.8 GHz
Log Amp Pulse Response Time

10ns Response Time (10% - 90%)

VOUT

200mV/VERTICAL DIVISION

PULSED RF INPUT 0.1GHz, -10dBm

GND

20ns PER HORIZONTAL DIVISION
Typical and Maximum Errors vs. Temperature

- Production testing of drift over temperature is generally not economical for IC manufacture (or for end equipment manufacture)
- Guaranteed-not-Tested (GNT) specs rely too much on statistics and are much too conservative
- Solution: Show performance data from multiple devices drawn from multiple factory lots
Typical and Maximum Errors vs. Temperature
Log Amp Detectors vs. Diode Detectors

![Diagram of Log Amplifier and Diode Detector Circuits](image)

- **LOG**
- **RF IN**
- **D1**
- **V out**

- **Input Power (dBm)**
- **Voltage Out**

- Resistors: 68Ω, 100pF, R1

Graph showing the relationship between input power (dBm) and voltage output.
Log Amp Detectors vs. Diode Detectors

- Log Amps have a higher dynamic range (40 dB or greater vs. 20-30 dB for a diode detector)
- Log Amps provide good temperature stability over a wide dynamic range.
- Diode detectors only provide good temperature stability at max input power (typically +15 dBm)
## Log Amp Detectors

<table>
<thead>
<tr>
<th>Part No.</th>
<th>RF Freq (MHz)</th>
<th>Dynamic Range (dB)</th>
<th>Temp Drift (dB)</th>
<th>Response Time (ns)</th>
<th>Package</th>
<th>Comments</th>
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<tr>
<td>AD8309</td>
<td>5 to 500</td>
<td>100</td>
<td>±1</td>
<td>67</td>
<td>16-lead TSSOP</td>
<td>Amplitude and Limiter Outputs</td>
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<td>AD8310</td>
<td>dc to 440</td>
<td>95</td>
<td>±1</td>
<td>15</td>
<td>8-lead MSOP</td>
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<td>AD8318</td>
<td>1 to 8000</td>
<td>60</td>
<td>±0.5</td>
<td>8</td>
<td>16-LEAD 3x3 mm CSP</td>
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<td>AD8317</td>
<td>1 to 10000</td>
<td>50</td>
<td>±0.5</td>
<td>5</td>
<td>8-LEAD 3x2 mm CSP</td>
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<td>AD8319</td>
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<td>AD8302</td>
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<td>60</td>
<td>±1</td>
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<td>14-LEAD TSSOP</td>
<td>Dual Gain and Phase Detection</td>
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<td>1 to 10000</td>
<td>50</td>
<td>±0.5</td>
<td>8</td>
<td>24-LEAD LFCSP</td>
<td>Dual Power and Gain Detection</td>
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</table>
Log Amps - Summary

- Provide power detection over large dynamic range (up to 100 dB)
- Operation from DC to 10 GHz
- With 2-Point Calibration, measurement accuracy of << ±1 dB is achievable.
- Devices are generally configured to provide a broadband 50 Ω match
- Pulse Response times of <10 ns are achievable.
- Power consumption varies from 5 mA to 70 mA
RMS-Responding RF Detectors
Response of a Successive Detection Log Amp to Varying Signals with Various Crest Factors
Using a Successive Detection Log Amp to Measure Signals with Varying Crest Factors

- Successive Detection Log Amps produce varying output voltages with varying crest factors
- Intercept varies but slope is unaffected
- Not an issue in systems with constant crest factor
- If the system knows which signal types are being transmitted, a correction factor (from a look-up table) can be applied.
- If the crest factor of the signal is unknown, an RMS-responding detector must be used.
An RMS-Responding RF Detector

![Diagram of an RMS-Responding RF Detector](image_url)
Output Voltage increases exponentially as input increases in dB (i.e. response is linear in V/V, not logarithmic)

Device achieves best temperature stability at max power (desirable for most applications)
ADL5501 RMS / TruPwr Detector

- Linear in Volts
- +/- 0.25dB accuracy and temperature stability
- +/- 0.1dB accuracy and temperature stability at the top end of the input power range where it counts most.
- 100 MHz to 4.0GHz
- SC-70 Package
- Ideal for Measuring Complex Waveforms with varying crest factors (WCDMA, HSDPA, HSUPA, CDMA2000, TD-SCDMA, WiMax).
Log Amps vs. Low Range RMS-to-DC Detector

![Diagram showing the relationship between input power (dBm) and voltage out for a Log Amps vs. Low Range RMS-to-DC Detector system. The diagram includes a graph with input power on the x-axis and voltage out on the y-axis, demonstrating the non-linear response to power levels.](image-url)
Log Amps vs. Low Range RMS-to-DC Detector

- Log Amps have higher dynamic range but rms-to-dc converters have more resolution at the high end. Measurement precision is often most critical at high output power (Emissions Regulations, SAR, etc.)

- Log Amps consume constant supply current independent of input level. RMS-to-DC converters supply current increases with input signal power.
High Dynamic Range
RMS Detection
AD8362  60 dB TruPwr™ RMS Detector

**KEY SPECIFICATIONS**
- Dynamic Range: >60dB
- Temperature Stability: +/-1dB
- Frequency Range: LF to 2.7GHz
- Package: 16 Lead TSSOP

**FEATURES**
- True RMS responding power detector
- Waveform and Modulation Independent
- Linear-in-dB output
Response of AD8362 RMS Detector to CW, QPSK and QAM Signals

@1.9 GHz, Vtgt = 0.625 V
AD8364 Dual Channel TruPwr ™ Detector

**KEY SPECIFICATIONS**
- Dynamic Range: >60dB
- Temperature Stability: +/-0.5dB
- Frequency Range: LF to 2.7GHz
- Package: 5x5mm 32 Lead LFCSP

**FEATURES**
- Dual channel and Difference Output Ports
- Integrated accurately scaled Temperature Sensor
- Linear-in-dB output
AD8364 RMS-DC Accuracy @ 2140 MHz
-40 degC to +85 degC
TruPwr™ RMS Detectors
Modulation Independent RF Measurements

<table>
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<tr>
<th>Part#</th>
<th>RF Freq (MHz)</th>
<th>Dynamic Range (dB)</th>
<th>Temp Stability (dB)</th>
<th>Voltage Supply (V)</th>
<th>Supply Current (mA)</th>
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<td>AD8361</td>
<td>2500</td>
<td>30</td>
<td>±0.25</td>
<td>2.7 to 5.5</td>
<td>1.1</td>
<td>6-Lead SOT-23 8-Lead uSOIC</td>
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<td>ADL5501</td>
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<td>30</td>
<td>±0.25</td>
<td>2.7 to 5.5</td>
<td>1</td>
<td>6-Lead SC-70</td>
</tr>
<tr>
<td>AD8362</td>
<td>2700</td>
<td>60</td>
<td>±1</td>
<td>4.5 to 5.5</td>
<td>20</td>
<td>16-Lead SOP</td>
</tr>
<tr>
<td>AD8364</td>
<td>2700</td>
<td>60</td>
<td>±0.5</td>
<td>4.5 to 5.5</td>
<td>72</td>
<td>32-Lead LFCSP</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>16-Lead SOP (Dual Channel)</td>
</tr>
</tbody>
</table>
Controlling AGC Loops with RF Detectors
A Typical AGC Loop

- Detector measures output power from a variable gain amplifier or power amplifier
- Measured result is compared to a setpoint value
- Error amplifier/Integrator adjusts gain so that output power corresponds to setpoint
- Integrator capacitor/resistor set response time of loop
- Many of ADI’s detectors have an integrated “Controller Mode”
A Practical AGC Loop using a Log Amp

- Setpoint is applied to Detector VSET input
- Vout varies up or down to balance loop
- Use to set output to a fixed value (fixed VSET, variable input power) or to vary output power (variable VSET, fixed or variable input power)
- Set response time of loop by varying Cflt
Controlling Gain with a Dual RMS Detector

- Dual RMS Detector can also operate in Controller Mode
- Detector measures and controls VGA in an analog loop
- Detector tries to balance input power at its two RF inputs
- Gain setpoint is controlled by difference in external attenuators
Gain vs. Input Power for Analog Gain Control Loop

- Gain varies by only +/-0.25 over a 60 dB input range
- Excellent stability over temperature
## RF Detectors for Analog AGC Loops

<table>
<thead>
<tr>
<th>Part No.</th>
<th>RF Freq (MHz)</th>
<th>Dynamic Range (dB)</th>
<th>Setpoint Voltage Range (V)</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>AD8311</td>
<td>100 to 2500</td>
<td>50</td>
<td>0.4 to 1.4</td>
<td>Wafer-Level CSP Package</td>
</tr>
<tr>
<td>AD8315</td>
<td>100 to 2500</td>
<td>50</td>
<td>0.4 to 1.4</td>
<td></td>
</tr>
<tr>
<td>AD8316</td>
<td>100 to 2500</td>
<td>50</td>
<td>0.4 to 1.4</td>
<td></td>
</tr>
<tr>
<td>AD8318</td>
<td>1 to 8000</td>
<td>60</td>
<td>0.5 to 2</td>
<td>Fast Responding</td>
</tr>
<tr>
<td>AD8317</td>
<td>1 to 10000</td>
<td>50</td>
<td>0.3 to 1.6</td>
<td>Fast Responding</td>
</tr>
<tr>
<td>AD8319</td>
<td>1 to 10000</td>
<td>40</td>
<td>0.3 to 1.5</td>
<td>Fast Responding</td>
</tr>
<tr>
<td>AD8362</td>
<td>Low Freq to 2700 MHz</td>
<td>60</td>
<td>0.4 to 3.5</td>
<td>RMS Responding</td>
</tr>
<tr>
<td>AD8364</td>
<td>Low Freq to 2700 MHz</td>
<td>60</td>
<td>0.25 to 3.5</td>
<td>Dual RMS Responding</td>
</tr>
</tbody>
</table>
RF Components in High Power Amplifiers
High Power Amplifiers

- Transmitter is usually segmented into a Radio and a Power Amplifier
- In order to operate as close as possible to the amplifier’s compression point (higher efficiency), many HPAs incorporate circuitry which reduces distortion (Linearization)
- Popular Linearization techniques are Feed Forward, Feedback, Digital Pre Distortion and Analog Pre-Distortion
A Simplified FFLA System – Carrier Cancellation

- Input signal is split onto two paths
- One path goes to input of High Power Amplifier (HPA)
- Output of amplifier comprised of amplified input signal and distortion generated within the HPA
- Distorted output signal for the HPA is sampled and conveyed to one input of a differencing node
- Other input of the differencing node is the undistorted input signal, delayed by an interval equal to the delay of the HPA/sampled output path
- Output of the differencing node is distortion signal only
A Simplified FFLA System – Distortion Cancellation

- Distortion signal is amplified by a very linear error amplifier (EA)
- Output of EA is applied to one input of another differencing node
- Other input to differencing node is the distorted output of the HPA, delayed by an interval equal to the carrier cancellation sampling path and the EA path
- Distortion present in the output of the HPA is cancelled in this differencing node
- Ideal output of differencing node is amplified, undistorted carrier
In the Carrier Cancellation Loop, a voltage variable attenuator (VVA) and a variable phase shifter (VPS) are put in cascade with the input to the HPA.

VVA and VPS are used to optimize carrier cancellation at the input to the EA.

Control voltages to VVA and VPS are often static voltages, set at the factory, but may be adaptively controlled.\(^1\)
In the Distortion Cancellation Loop, a VVA and a VPS are put in cascade with the input to the EA. VVA and VPS are used to optimize distortion cancellation at the output of the FFLA system. Control voltages to VVA and VPS are often static voltages, set at the factory, but may be adaptively controlled.
AD8302 – Gain / Phase Detector

**KEY SPECIFICATIONS**
- Frequency Range: LF to 2.7 GHz
- Gain range: 60 dB, 30mV/dB, 0 to 1.8V
- Phase range: 180 deg, 10 mV/deg, 0 to 1.8V
- Package: 14-TSSOP

**FEATURES**
- Matched Log Amps for Temperature Stability
- Measurement and Control of Gain or VSWR
AD8302 – Gain/Phase Detector
Gain and Phase Transfer Functions
A Complete Feedforward Linearized Amplifier

- AD8302 GPD can be used to control both loops of the FFLA
- AD8302 used to control VVA and VPS in Carrier Cancellation loop to control cancellation of carrier at the input to the EA
- AD8302 used to control VVA and VPS in Distortion Cancellation loop to control cancellation of intermodulation sidebands at FFLA Output
AD8340 and AD8341 Vector Modulator

KEY SPECIFICATIONS
- RF Bandwidth: 0.7 – 1.0GHz / 1.5 – 2.4 GHz
- Gain control range: -32dB to -2dB
- Phase control range: continuous 360°
- Output IP3: 24dBm / 22dBm (max gain)
- Output Noise: -149 dBm/-151Hz
- Package: 4x4mm 24-LFCSP

FEATURES
- Amplitude and Phase Modulator inputs
- Modulation by Cartesian I and Q
- Output power disable function: 40dB, 10ns
AD8340 Vector Modulator – Gain and Phase Control

- 30 dB Gain Control Range
- 360 degree Phase Control Range

880 MHz
ADL5390 RF / IF Vector Multiplier

**KEY SPECIFICATIONS**
- Bandwidth 20MHz to 2.4GHz
- Continuous Amplitude Control +5 to –30dB
- Wide band 230MHz Cartesian Interface
- OIP3 +25dBm
- Output P1dB +13dBm
- Output Noise Floor –150dBm/Hz
- Package 4x4mm LFCSP

**FEATURES**
- Output Switch Disable 40dB, 10ns
Components for PA Feedforward Linearization

### Vector Modulators

<table>
<thead>
<tr>
<th>Part No.</th>
<th>RF Freq (MHz)</th>
<th>IQ Bandwidth (MHz)</th>
<th>Noise Floor (dBm/Hz)</th>
<th>P1dB (dBm)</th>
<th>Power Supply (mA)</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>AD8340</td>
<td>700 to 1000</td>
<td>230</td>
<td>-149</td>
<td>11</td>
<td>130</td>
<td>24-lead CSP</td>
</tr>
<tr>
<td>AD8341</td>
<td>1500 to 2400</td>
<td>230</td>
<td>-151</td>
<td>8.5</td>
<td>130</td>
<td>24-lead CSP</td>
</tr>
<tr>
<td>ADL5390</td>
<td>20 to 2400</td>
<td>230</td>
<td>-150</td>
<td>+13</td>
<td>130</td>
<td>24-Lead LFCSP</td>
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</tbody>
</table>

### Gain/Phase Detector

<table>
<thead>
<tr>
<th>Part No.</th>
<th>RF Freq (MHz)</th>
<th>Dynamic Range (dB)</th>
<th>Accuracy (dB)</th>
<th>Response Time (ns)</th>
<th>Package Type</th>
<th>Comments</th>
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</thead>
<tbody>
<tr>
<td>AD8302</td>
<td>&gt;0 to 2700</td>
<td>60</td>
<td>±0.2</td>
<td>60</td>
<td>14-lead TSSOP</td>
<td>Dual channel gain and phase detector</td>
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