4 Pulse Width Modulation

4.1. Pulse Width Modulation Techniques

An induction motor driven by a six step inverter draws currents at fundamental and harmonic frequencies. Useful output power is produced by the current at fundamental frequency only. The harmonics contribute to additional copper losses in the machine and create torque pulsations. Harmonics also stress the inverter switches by way of large instantaneous current peaks. As has been pointed out, the harmonics in the six-step voltage wave are of order $6m \pm 1$, the most dominant in amplitude being the 5th (20%) and the 7th (14%). The six step inverter requires an additional power converter to vary the **DC** bus voltage and hence the machine voltage.

In six step inverters for high power requirement, reduction of harmonics is achieved by suitable phase shifting and by adding the output voltages of two or more six step inverters. As phase shift is required to reduce the harmonics, the fundamentals add vectorially rather than arithmetically and some reduction in output voltage has to be accepted. Further, control of the fundamental amplitude still requires a variable dc voltage.

With present day power switching devices, switching frequencies of between 500 Hz to 1000 Hz can be comfortably achieved even at high power ratings. The current trend is towards Pulse Width Modulated - **PWM** inverters for driving induction motors.

PWM achieve a favourable harmonic profile as well as control of fundamental amplitude are both accomplished within the inverter itself by suitably designed switching patterns. Various techniques are available for determining switching patterns. The basic principles underlying a few of these are discussed in this manual.

4.2. Motivation for PWM

The basic attempt in all Pulse Width Modulation - **PWM** methods is to produce the required amplitude and frequency of the fundamental, while moving the energy in the harmonics to a higher range in the frequency spectrum. At such high frequencies, the machine leakage inductance will exhibit appreciable reactance, thereby limiting the harmonic currents drawn from the inverter.

Since the torque pulsations created by these high-frequency harmonics are also at high frequencies, the motor should be able to run smoothly. The constraint on the pulse width modulation process is the fact that additional switchings per cycle are required in order to accomplish the modulation. This increases the losses in the inverter.

Moreover, as the switching patterns become more complicated, an individual inverter phase may be required to produce pulses or notches of very small width. The switching times of the devices used in the inverter impose a limitation here.

4.3. Sub Harmonic PWM

This method was first discussed extensively by Schonung and Stemmler and is the oldest of the *carrier* based PWM techniques. The basis of the method can be explained as follows.

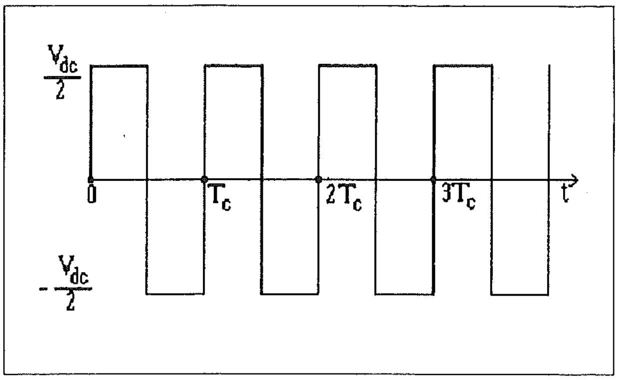

Figure 4.1

Consider a symmetrical square wave of voltage, with a period T_c, as shown in *figure* 4.1. Such a voltage can be produced by one phase of a voltage source inverter switching at a frequency $f_c = 1/T_c$. The positive and negative volt- seconds balance in each cycle and the average value is zero. Subsequently, if the duty cycle of each pulse is increased above 50%, *i.e.*, the positive volt-seconds are more than the negative volt-seconds, the average value will be positive. Similarly, if the duty cycle is reduced below 50%, the average voltage will be negative. If the duty cycle is varied with time in a sinusoidal manner about the 50% level, the average value of the voltage in each cycle will also vary in a sinusoidal manner with respect to time. The frequency at which the duty cycle is varied or *modulated* is referred to as the modulating frequency f_m.

The modulated waveform contains, the component at the modulating frequency and other components in the neighbourhood of the pulse frequency f_c. If f_m is small compared to f_c, the unwanted components will be far removed from the wanted frequency f_m. Such a waveform can therefore be used to feed an induction motor. The modulating frequency f_m is the fundamental and the other components are the unwanted harmonics. Since these harmonics are at frequencies well away from the fundamental, the currents at these harmonics should be small.

The gating pulses for the inverter switches are generated by the following technique. A constant amplitude triangular waveform at the frequency f_c is generated. This is referred to as the carrier waveform. This carrier waveform is then compared with a sinusoidal waveform at the modulating frequency f_m. The amplitude of the sinusoidal waveform is less than that of the triangle. The sine-wave is known as the reference waveform. The carrier, the reference and the output of the comparator are shown in *figure* 4.2.

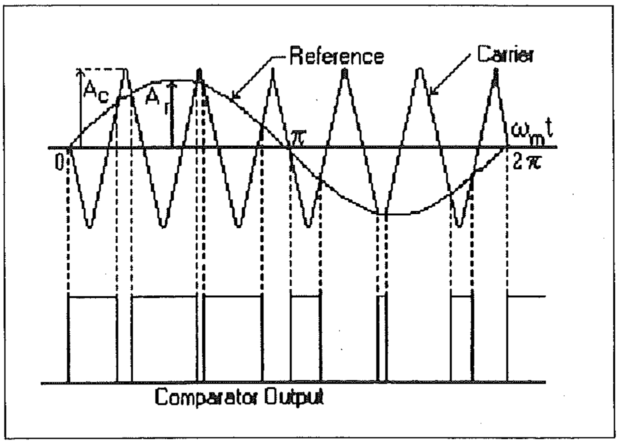

Figure 4.2

The comparator gives an output of 1 whenever the reference wave is greater than the carrier wave and an output of 0 whenever the carrier is greater than the reference.

The output 1's are used as gating pulses for the top switch of the inverter and output 0's for the lower switch. In this manner the phase to centre-tap output voltage of the inverter will be the desired modulated square-wave.

The carrier has an amplitude A_c and the reference wave an amplitude A_r. The ratio of the reference to carrier amplitudes is defined to be the modulation index m:

i.e. $m = A_r/A_c$

By varying A_r while keeping A_c constant, *i.e.* by varying the modulation index, the amplitude of the fundamental component in the output voltage can be varied. Similarly by varying the frequency of the sine waves, the fundamental frequency in the output can be varied.

There are several significant features to be noted in *figure* 4.2. First, one period of the reference waveform is shown to contain an integral number of cycles of the triangle (6 in *figure* 4.2). Synchronization between carrier and reference is achieved by these means. (*i.e.* every cycle of the inverter output waveform will be the same) This feature is essential if the number of triangles per cycle of the reference, *i.e.*, the frequency ratio f_c/f_r is less than 21. Otherwise, adjacent cycles of the inverter output voltage waveform will differ from one another and their differences will repeat periodically at a frequency lower than that of the reference. (*i.e.*, sub-harmonic or beat frequency components will begin to appear in the inverter output)

In three-phase inverters, gating patterns have to be generated for three inverter phases. This is accomplished by employing a common carrier waveform and three sinusoidal reference waveforms having identical amplitude and frequency, with mutual phase displacements of 120°. In order to ensure that the output voltage waveforms produced by each inverter phase is the same, it is ensured that there are an integral number of triangles in 120° of the reference waveforms. Therefore the carrier frequency f_c has to be a multiple of three times the reference frequency f_r. It has been shown that the unwanted harmonic frequency components in the inverter output voltage waveform occur at frequencies $Nf_c \pm Mf_r$, where N and M are integers and N+M is odd. There occur bands of harmonics around each multiple of the carrier frequency f_c as follows:

f_c, $f_c \pm 2f_r$, $f_c \pm 4f_r$ ... first band
$2f_c$, $2f_c \pm f_r$, $2f_c \pm 3f_r$ ... second band
$3f_c$, $3f_c \pm 2f_r$, $3f_c \pm 4f_r$ ... third band

The amplitudes are largest for the first band and decrease progressively as further bands are considered. A typical spectrum of the inverter output voltage is shown in *figure* 4.3. The component at f_c is a triple n harmonic and gets cancelled in the inverter line voltages. By selecting f_c to be an odd multiple of f_r, it is ensured that no even harmonics appear in the output.

The need for keeping the carrier and the reference synchronized implies that the reference frequency is changed, in a variable frequency application like an **AC** drive, the carrier frequency f_c has to change to keep the ratio f_c/f_r constant.

As the amplitude of the sinewave reference is increased, some of the pulses and notches in the inverter gating pulses become very narrow and may be difficult to reproduce accurately in the inverter. The situation where the sine and triangle amplitudes are equal, (*i.e.* modulation index m = 1) represents the maximum value of the fundamental voltage in the output.

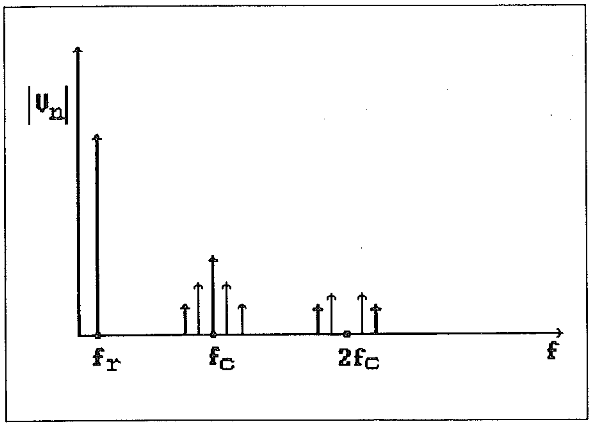

Figure 4.3

The amplitude of the fundamental component of the inverter output voltage, in this case, is given by

$$V_{1peak} = V_{dc}/2$$

Therefore,

$$V_{1rms,m=1} = 1/\sqrt{2}\ V_{dc}/2 = 0.35V_{dc}$$

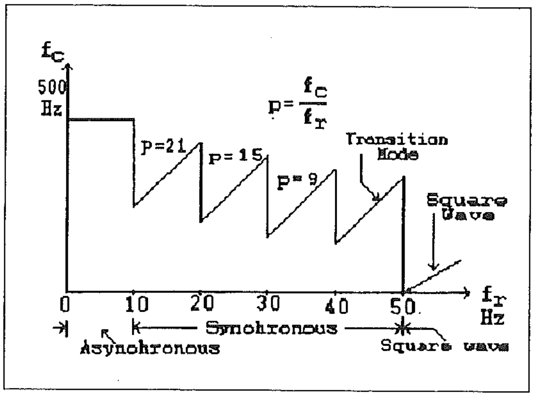

Figure 4.4

This can be compared to the maximum value of $0.45V_{dc}$ for square wave operation

Therefore,

$$V_{1rms,m=1} / .45V_{dc} = 0.78$$

The maximum *rms* value of the fundamental component that can be obtained with sine triangle modulation is only 78% of the value corresponding to square wave operation. If the amplitude of the sine is increased further, the sine will not intersect the triangle during some of the carrier cycles, *i.e.* some of the pulses will start disappearing. This type of operation is referred to as overmodulation. In overmodulation, low frequency components such as the 5th, the 7th, etc. begin to appear in the inverter output voltage.

4.4. Current Regulated PWM

In **AC** drive applications, it is sometimes necessary to control the stator current of the motor rather than the stator voltage. If the inverter uses any of the **PWM** methods described above, it acts as a voltage source only and current control has to be achieved by closing a current loop around the inverter. An alternative technique is the current regulated **PWM** technique. This method, is suitable for inductive loads such as motors. In this method, instantaneous stator current is compared with a reference current waveform, usually sinusoidal.

Suppose, the top switch of the inverter phase is gated on. The phase to centre-tap voltage of that phase will then be $+V_{dc}/2$. This voltage will force the machine current to rise.

When the current exceeds the reference by a margin δ, the gating pulse to the top switch is turned off and the bottom switch is gated on. The current now begins to fall. When the current falls below the reference by δ, the bottom switch is turned off and the top switch is turned on again. Typical load current and inverter phase to centre tap voltage waveforms are shown in *figure* 4.5.

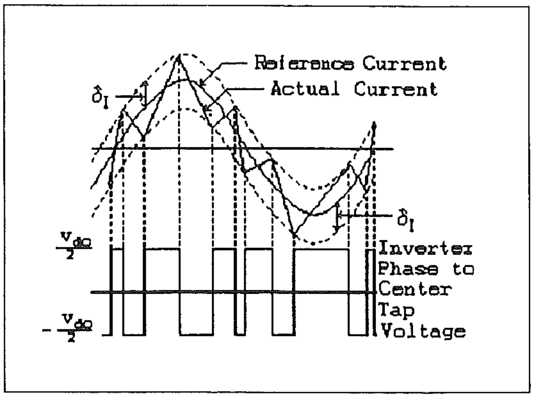

Figure 4.5

The switching instants of the inverter are therefore decided by the current margin δ and the load impedance. The switching frequency of the inverter is therefore not constant in this technique. This characteristic may not be acceptable in some applications.

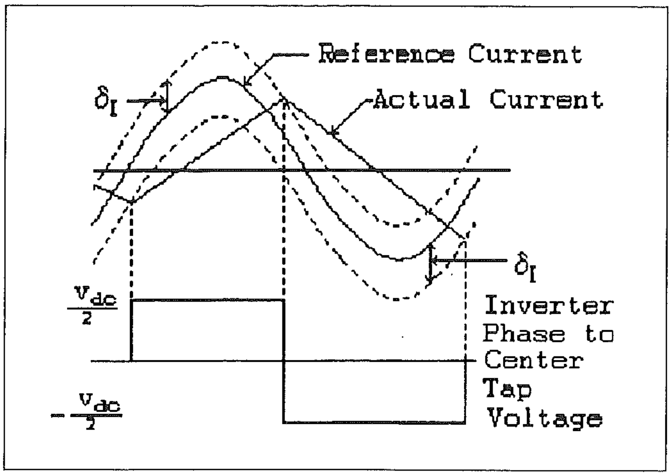

Figure 4.6

Also, a current sensor with good bandwidth is required to accurately reproduce the load current waveform.

In drive applications, the load on the inverter consists of a back *emf* corresponding to the airgap voltage of the motor, in series with the stator resistance and inductance. As the speed of the motor increases, the back *emf* also increases, since the flux is almost constant. At high rotational speeds, the back *emf* may approach the bus voltage and the inverter may not be able to force current into the stator. As a result, the stator current will not follow the reference accurately. *Figure* 4.6 shows possible current and voltage waveforms in such a situation. The inverter is now operating in the square wave mode and the actual current no longer reproduces the reference.

NOTES