### **SECTION 7**

# THE AD1B60: AN INTELLIGENT, DIGITIZING SIGNAL CONDITIONER

- THE ANALOG STATE-OF-THE-ART
- What are Digital Signal Conditioners?
- AN EMBEDDED MICROCONTROLLER GIVES THE AD1B60 "Intelligence"
- Built-In Circuits Makes Acquiring the Sensor Signals Simple
- Communication Ports
- DIGITAL COMMAND AND CONTROL
- Conversion Modes
- CALIBRATING THE AD1B60
- THEAD1B60 IN THERMOCOUPLE APPLICATIONS
- CONFIGURING THE AD1B60 FOR VOLTAGE INPUTS
- CONFIGURING THE AD1B60 FOR RTD APPLICATIONS
- USING THE AD1B60 IN AN INDUSTRIAL ENVIRONMENT
- SUPPLYING POWER TO THE AD1B60
- LAYOUT TECHNIQUES FOR MAXIMUM PERFORMANCE
- THE AD1B60 Evaluation Board
- USING DIGITAL ALGORITHMS IN SIGNAL CONDITIONING CIRCUITRY

System Applications Guide

### **SECTION 7**

# THE AD1B60: AN INTELLIGENT, DIGITIZING SIGNAL CONDITIONER Adolfo Garcia

The design of signal conditioning circuitry for industrial markets places extraordinary demands on the analog circuit designer. Customers frequently require levels of precision and stability that are difficult to obtain at the best of times to be obtained from low level signals contaminated with high levels of noise and interference. Over the years, engineers familiar with the requirements of these applications have developed a number of methodologies and techniques to meet their customers' demands.

Illustrated in Figure 7.1 is a block diagram of a typical measurement/control loop used in industrial processes. These processes vary and can range from setting and controlling temperature (the most frequently conditioned parameter) to robotics. These systems, programmed for autonomous operation, operate in a closed-loop under the control of computers. At the heart of the system is the sensor which

is used to measure a variety of physical quantities: temperature, pressure, flow, humidity, or strain. While some of these sensors are active and generate a voltage or current (for example, thermocouples), most sensors are passive and require external excitation in the form of applied voltages (strain gauges) or currents (RTDs). Nearly all sensors share one feature — their outputs are low-level and vulnerable to interference when operating in high interference environments. In these applications, the sensor output must be conditioned by analog means (filtering, offset, and amplification) before A/D conversion. Galvanic isolation may also be required because of high potential differences between the sensor and the signal conditioning circuitry. Since systems are often controlled by a master computer, provisions for local data processing and communications may also be required. All these issues make the system designer's task challenging.

### BLOCK DIAGRAM OF A MEASUREMENT/CONTROL PROCESS LOOP

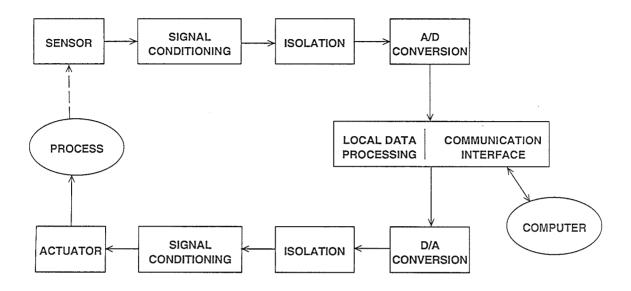


Figure 7.1

#### THE ANALOG STATE-OF-THE-ART

Classic analog signal conditioners are designed to accept signals from sensors such as thermocouples and RTDs, perform all necessary signal conditioning functions, and deliver an accurate representation of the physical input to the sensor as an output. The necessary signal conditioning functions may include: input fault protection, filtering, amplification, zero (or offset) suppression, linearization, cold-junction and/or lead wire compensation, scaling, et cetera.

To keep circuit costs down, the design of these measurement/control loops often

use a single A/D converter to convert the outputs of a number of sensors. As shown in Figure 7.2, analog conditioners may include the following circuits: an analog multiplexer, a programmable gain amplifier (PGA), a precision voltage reference, an analog-to-digital converter, and a microcontroller to control the analog circuits and to facilitate the digital interface between itself and the host computer. The analog signal conditioner requires, at a minimum, half a dozen integrated circuits, passive components, custom software, and PC board. These are expensive.

#### PREVIOUS STATE OF THE ART

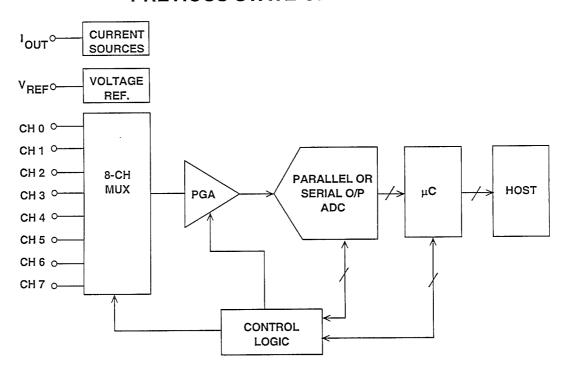


Figure 7.2

The nature of the signal conditioning art is being changed by the introduction of small, inexpensive single-chip microcontrollers. These devices have become inexpensive enough to incorporate into signal conditioning circuitry as an integral element of the component design. Incorporating these microcontrollers adds the advantages of

lower cost, greater flexibility, and higher accuracy when compared to traditional analog signal conditioning approaches. A new class of signal conditioning products, called digital signal conditioners, have appeared in the marketplace as a result of this change of philosophy.

### What are Digital Signal Conditioners?

Digital signal conditioners are identified by their use of a digital output format where an RS-232, RS-485, or even a frequency output replaces the usual analog 4–20mA or 0–10 volt output signal. The use of a digital output format may be an advantage over more traditional analog output formats. Because digital interfaces can be more readily isolated and multiplexed and are far more resistant to the noise and

interference often found in industrial environments. However, the real advantage of digital signal conditioning lies not in the form of the interface, but in the ability of digital circuitry to augment or supplant many of the functions heretofore accomplished exclusively by analog means.

To reflect this change in signal conditioning philosophy, Analog Devices has

designed a first-generation digital signal conditioner in a 44-pin SOIC, the AD1B60. As shown in Figure 7.3, the design of the AD1B60 encompasses signal conditioning and high-resolution A/D conversion with local data process-

ing and a communications interface. The ADC in the AD1B60 is an integrating type. Its output is the *mean* of the input during the conversion process - it does not contain a sample and hold (SHA).

#### HOW DOES THE AD1B60 FIT INTO THIS SCHEME?

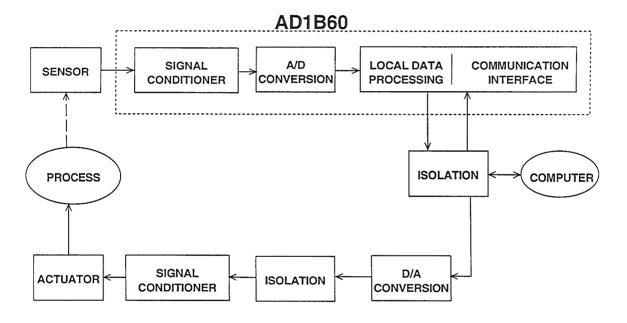


Figure 7.3

As shown in Figure 7.4, the AD1B60 is a single part which contains a mask-programmed microcontroller (with EEPROM memory) and a front-end analog/digital ASIC. The primary application of the AD1B60 is a user-configurable digitizing signal conditioner for RTDs, thermocouples, and low- and high-level voltage signals. The

custom BiCMOS ASIC includes a 9-channel multiplexer, a low-drift voltage reference, a programmable-gain amplifier, a charge-balancing converter, and all the required logic circuitry to permit communication and control via a serial digital interface. Key features of the AD1B60 are summarized in Figure 7.5.

#### AD1B60 SIMPLIFIED BLOCK DIAGRAM SENSOR EXCITATIONS VOLTAGE REF. 16-BIT **SERIAL** CJC ∽ DATA OUTPUT G = 1 TO 128 CH0 o─ 9-CH CHARGE CH1 ° **INTERFACE** $\mu \textbf{C}$ MUX **BALANCING PGA** LOGIC CH2 o-ADC CH3 o-ATTEN <sup>←</sup> **EEPROM GND** SENSE

Figure 7.4

44-PIN PLCC

**CONTROL LOGIC** 

# FEATURES OF THE AD1B60 "INTELLIGENT DIGITIZING SIGNAL CONDITIONER"

- User-configurable inputs (Thermocouples, RTDs, etc.)
- Four modes of CJC for TCs including open TC detection
- Lead compensation for 3 and 4-wire RTDs plus excitation
- Accuracy: 1°C for TCs and 0.2% for RTDs
- Embedded micro-controller and EEPROM
- Digitally controlled configuration and calibration
- Output in Engineering Units (°C, V)

LOCAL

TEMP SENSOR

Asynchronous and synchronous communication ports

Figure 7.5

The AD1B60 requires a small amount of external circuitry to perform its function: an 11.0592MHz crystal clocks the microcontroller and controls the asynchronous communications port; and the internal A/D converter (a chargebalancing type), requires an external 0.0022µF integration capacitor. For

highest performance capacitors with low dielectric absorption, such as NPOs (COGs) or X7Rs, should be used. Integration capacitor stability is not necessary because the AD1B60 is autocalibrated. The device pinout configuration for the AD1B60 is shown in Figure 7.6.

#### AD1B60 PIN-OUT DIAGRAM

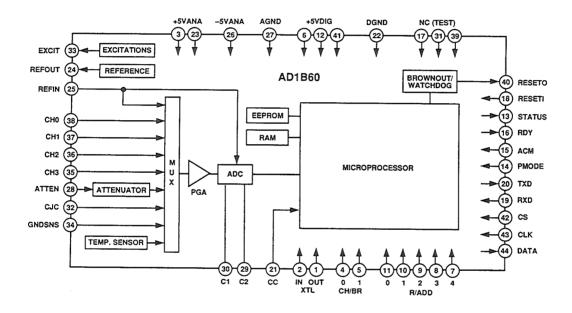


Figure 7.6

### AN EMBEDDED MICROCONTROLLER GIVES THE AD1B60 "INTELLIGENCE"

Circuit drift over time and temperature, circuit effects over the full-scale span, variation of resistors over time and temperature, and many other issues must be addressed if an industrial sensor circuit design is to be a success. In addition, such a design must provide cold-junction compensation in thermocouple applications and lead-wire compensation in remotely-located RTD applications.

The microcontroller internal to the AD1B60 contains custom software for controlling the individual analog functions and scaling and linearizing the sensor data — the chart in Figure 7.7 outlines the built-in routines programmed into the AD1B60. Details of the techniques and algorithms used for the built-in functions can be found in the Appendix.

# THE AD1B60'S INTERNAL MICROCONTROLLER BUILT-IN ROUTINES

- Zero Compensation, Span Compensation
- Lead-Wire Compensation for RTDs
- Cold Junction Compensation for Thermocouples
- Data Scaling (°C, V)
- Data Linearization for RTDs, Thermocouples, etc.
- Addressing and CRC

#### Figure 7.7

The output from this part is a completely conditioned digital representation of the input, and includes linearization and scaling. The output data is represented directly in engineering units (for example, °C, V, etc.) using single-precision IEEE floating point format. A 16-bit integer format result is also available. By combining analog signal conditioning and local intelligence in the form of a microcontroller, the AD1B60 can used in remotelylocated applications. These applications include industrial temperature measurement systems, process control systems, multi-channel thermocouple systems, and analytical instruments where signal conditioning at the sensor is desired.

One function of particular importance is automatic span compensation. The AD1B60 measures both the input signal and the voltage reference with respect to ground at the appropriate gain. The result is a function of the *ratio* of the two measurements. This eliminates ADC drift terms. The voltage reference may be the internal reference or an external precision reference.

The AD1B60 also compensates for temperature drift of the RTD current excitation source. During the AD1B60 manufacturing process the temperature drift of the current source is measured along with an on-board temperature sensor. The correction coefficient is stored in EEPROM, and all RTD readings are adjusted to eliminate thermal drift.

Since the intended use for the AD1B60 is to provide a complete sensor-to-digital interface, the analog front end of the device was designed to work with a

number of passive and active sensors. The AD1B60 accepts a wide range of input signals from devices which include seven types of thermocouples and two types of RTDs. Low-level voltage sources up to  $\pm 2$  V can be applied to input channels CH0 through CH3 while high-level signals up to  $\pm 10$  V can be applied to the device through the AD1B60's internal 5:1 attenuator. The AD1B60's high input impedance of  $\geq 10 \mathrm{M}\Omega$  allows almost any sensor source impedance level.

As previously mentioned, the AD1B60 provides the algorithms required for scaling and linearizing sensors of the types shown in Figure 7.8. Summarized in Figure 7.9 are the ranges, accuracies,

and resolutions for each of the built-in sensor routines.

One clear advantage of the AD1B60 over traditional analog signal conditioners is its flexibility in handling different sensor types. For sensors not included in the built-in routines, a linearization algorithm can be created for any sensor. The sensor's characteristic polynomial coefficients are coded into a custom linearization algorithm which can be downloaded on command into the AD1B60's EEPROM. Thus, for sensors such as Type N thermocouples and subranges, the AD1B60 is the ideal signal conditioning device. The AD1B60 can accommodate two user-defined linearization algorithms.

### THE AD1B60 ACCEPTS A MULTITUDE OF SENSORS AND INPUT RANGES

- Thermocouples: Type J, K, T, E, R, S, B
- Platinum 100Ω RTD:  $\alpha = 3.85 \times 10^{-3}$ ,  $\alpha = 3.92 \times 10^{-3}$
- Low-Level Vin: ±10mV, ±20mV, ±50mV, ±100mV, ±200mV, ±500mV, ±1V, ±2V
- High-Level V<sub>in</sub>: ±5V, ±10V
- Downloadable Ranges: Two User-Defined Ranges

### THE AD1B60'S BUILT-IN ALGORITHMS LINEARIZE THERMOCOUPLE AND RTD OUTPUTS

Thermocouple Type	Temperature Range	Accuracy/Resolution (Typ)
J	0°C ≤ T ≤ 760°C	± 0.25°C / ± 0.15°C
K	0°C ≤ T ≤ 1000°C	± 0.55°C / ± 0.2°C
Т	-100°C ≤ T ≤ 400°C	± 0.25°C / ± 0.15°C
Е	0°C ≤ T ≤ 1000°C	± 0.2°C / ± 0.1°C
R	500°C ≤ T ≤ 1750°C	± 1.00°C / ± 0.55°C
S	500°C ≤ T ≤ 1750°C	± 1.15°C / ± 0.6°C
В	500°C ≤ T ≤ 1800°C	± 1.15°C / ± 0.7°C

100Ω RTD Type	Temperature Range	Accuracy/Resolution (Typ)
$\alpha$ = 3.85 m $\Omega/\Omega/^{\circ}$ C	-200°C ≤ T ≤ 800°C	± 0.2°C/± 0.15°C
$\alpha$ = 3.92 m $\Omega/\Omega/^{\circ}$ C	-200°C ≤ T ≤ 800°C	± 0.2°C/± 0.15°C

Figure 7.9

### BUILT-IN CIRCUITS MAKES ACQUIRING THE SENSOR SIGNALS SIMPLE

Besides its multiplexer, PGA, and A/D converter, an analog signal conditioner must also provide ancillary circuits. Outlined in Figure 7.11, the ancillary analog circuits include digitally-controlled current sources for RTD and thermistor excitation, open thermocouple detection, and an internal 5:1 attenuator for high-level input signals. The AD1B60 digital functionality is enhanced by the addition of a brownout detector and a watchdog timer.

To add current sources to an analog signal conditioner requires precision

resistors and operational amplifiers. The AD1B60 simplifies the process by incorporating digitally controlled current sources. Accuracy is guaranteed for all sensors due to the sequential calibration process.

High-level signals are applied to the AD1B60 through a 5:1 attenuator whose nominal resistance is  $50k\Omega$ . To avoid source loading errors, the source impedance in this case should be low: it may be advisable to buffer the source with a precision operational amplifier to ensure low source impedance.

## ADDITIONAL FUNCTIONALITY USING THE AD1B60'S BUILT-IN CIRCUITS

- RTD Current Source Excitation
- CJC Thermistor Exitation
- Open Thermocouple Detection
- 5:1 Attenuator for High Level Signals
- Brownout Detector / Watchdog Timer

Figure 7.10

### BUILT-IN CIRCUITS REDUCE OVERALL COMPONENTS COUNT

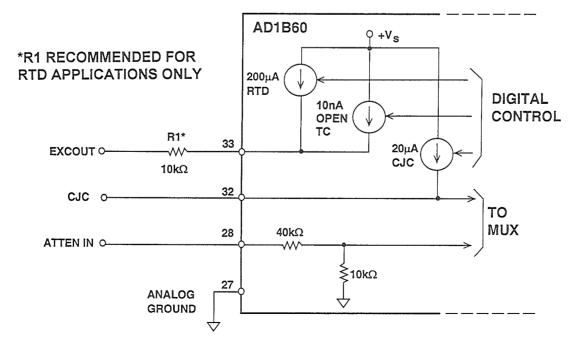


Figure 7.11

To enhance the digital functionality of the AD1B60, a brownout detector and a watchdog timer were added to the internal control circuitry. These functions force the device to a power-up default configuration and are very useful in the event of a power failure or other abnormal operating condition. The brownout detector is designed to reset the AD1B60's microcontroller if the supply voltages to the device drop below the following trip points:

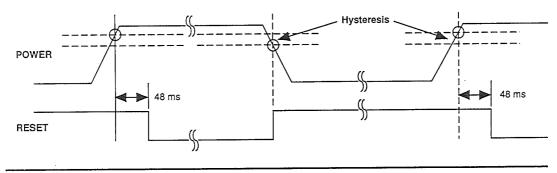
+5 V Digital ≈ +3.5V +5 V Analog ≈ +3.9V -5 V Analog ≈ -3.9V

The operation of the brownout detector is illustrated in Figure 7.12. The trip

points are intentionally set well below the customary -5% range to avoid nuisance trips due to noise. Digital output data is valid after resets when the Data Valid flag in the AD1B60's ADSTAT byte is set to logic "1". However, the amount of time before data becomes valid depends on the input sensor range and integration time.

The watchdog timer automatically resets the AD1B60 in the event of a microcontroller failure. During normal operation, the microcontroller is programmed to strobe the watchdog timer every 20ms. In the event that the microprocessor stops for any reason (for example, a power glitch), the watchdog timer initiates a reset sequence.

### **BROWNOUT DETECTOR TIMING DIAGRAM**



Watchdog Timer Diagram

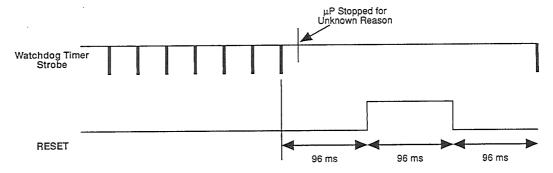
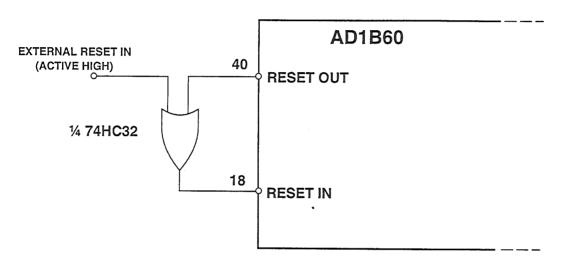


Figure 7.12

Normally, the AD1B60's RESET OUT (pin 40) is connected to its RESET IN (pin 18); however, there are some applications where an asynchronous

reset may be required. In those applications, an OR-gate can be inserted between these two pins to provide asynchronous, system-level reset.

#### ADDING AN OR GATE PROVIDES A RESET INPUT



THE AD1B60 IS INITIALIZED WHEN RESET OUT OR EXTERNAL RESET IN = "HI"

Figure 7.13

#### COMMUNICATION PORTS

By offering both a serial communication port and a high-speed data port, the AD1B60 provides easy access to the sophisticated programmable functions and features which make the device easy to use. The following subsections describe the ports in more detail.

#### **Asynchronous Communications Port**

The asynchronous communication port is a two-wire input/output port through which all the functions of the AD1B60 can be accessed. The port can be connected to a host using its industry-

standard serial interface or using level translation to RS-232 or RS-485 communication standards. A summary of the asynchronous port features is given in Figure 7.14.

### FEATURES OF THE AD1B60 ASYNCHRONOUS COMMUNICATION PORT

- Fast, 2-wire, Input/Output -- Up to 19.2 kBaud
- Direct connection to embedded microcontrollers
- Communication to PCs via RS-232 and RS-422/485
- User Selectable Baud Rates
- Supports up to 32 AD1B60s with CRC
- 16-bit Integer and 32 Bit Floating Point Data Formats
- Simple Binary Protocol
- Command Set

#### Figure 7.14

The asynchronous port operates at 2400, 4800, 9600, or 19200 baud using the following convention: eight bits, no parity, one stop bit. The baud rate is user-selectable, and break detection is supported as an absolute means of resetting the communications routines.

The asynchronous port supports addressability and cyclic redundancy error checking (CRC) which allows up to 32 AD1B60s to share a "party line" and to exist in remote locations from the host system. Addressing and error checking can be enabled by setting the state of the Advanced Communication Mode (ACM) on pin 15 to logic "1." If

the state of the ACM pin is logic "0," address and CRC values are ignored.

The host computer system initiates all communication with the AD1B60: messages are sent over the asynchronous port using a simple binary protocol. Reading converted data, changing configuration parameters in memory, or calibrating the device can be done using the AD1B60 Command Set which is based on this binary protocol. Commands can be sent to the device through the RxD pin (pin 19). Data and device status can be retrieved from the TxD pin (pin 20).

#### SYSTEM APPLICATIONS GUIDE

#### High-Speed Data Port

The high-speed data port is a fast, 3-wire, output-only synchronous port. It is double-buffered and completely independent of the asynchronous port. This

allows access to both ports simultaneously, if required. Features of the high-speed data port are summarized in Figure 7.15.

#### FEATURES OF THE AD1B60 HIGH-SPEED DATA PORT

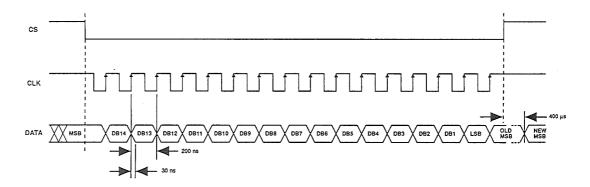
- Fast, 3-wire Output-Only Port
- Double buffered
- Independent of Asynchronous Port
- 16-bit data at 200ns/bit
- Output Buffer Updated at Start of Every Conversion

#### Figure 7.15

The data port consists of two CMOS inputs (CS and CLK, pins 42 and 43, respectively) and one CMOS output (DATA, pin 44). The data port becomes active when CS is set to logic "0". Data can retrieved from this port in 16-bit integer format as fast as 200ns/bit. The timing diagram of the data port is illustrated in Figure 7.16. The AD1B60 updates the buffer at the start of every conversion, thus data can be read at any time. To read data from the highspeed port, both CS and CLK must be

initially set to logic "1." At this time, the state of the DATA output is the MSB of the output word. This is useful for checking the sign bit without reading the entire sixteen-bit word. To read each bit, CS is set to logic "0," and then CLK is cycled. A new bit shifts out on each rising edge of CLK. After the 16-bit data has been read, CLK is set to logic "1" and then the port is disabled by setting CS to logic "1." Whenever CS changes state, CLK must be at logic "1" to avoid metastability problems.

#### AD1B60 HIGH-SPEED DATA PORT TIMING DIAGRAM



- · CS and CLK are CMOS Inputs
- DATA is a CMOS Output
- · State of DATA when CS = HI is the MSB
- Data is Recirculated @ 16th Clock Edge
- Update Has Up to 400 μs Latency

Figure 7.16

For bipolar analog inputs, converted data from the port is represented in 16-bit, twos complement format. For

thermocouple and RTD applications, the converted data is represented in 16bit, offset binary format.

#### DIGITAL COMMAND AND CONTROL

The AD1B60 can be configured through the asynchronous port using its command set or in hardware by setting the appropriate inputs. The AD1B60's power-up default settings are shown in Figure 7.17. For more detailed information regarding the operation of the AD1B60 under hardware configuration, consult the AD1B60 Data Sheet.

The most flexible way to configure and control the AD1B60 is to use the com-

mand set, in this way input ranges can be calibrated and converted data/device status can be read. Figure 7.18 lists the AD1B60 Command Set. Where applicable, the numerical format for communicating with the AD1B60 is based on the 4-byte IEEE floating point standard. For more detailed information regarding the command set and examples of the floating point format, consult the AD1B60 User's Guide.

# CONFIGURATION OF AD1B60 CAN BE HARD-WIRED OR SOFTWARE DRIVEN

- Device Address (0 to 31, 0 default)
- Baud Rate (9600 Baud, default)
- Channel Selection (Channel 0, default)
- Input Range (Type J Thermocouple, default)
- Integration Time (100ms, default)
- CJC Mode (Thermistor, default)
- **■** RTD Configuration Mode (3-wire)

Figure 7.17

### THE AD1B60s COMMAND SET ALLOWS CONFIGURATION AND CONTROL VIA SOFTWARE

Command	Function	
WR_EPM_PARS	Alters Default Values in EEPROM	
WR_RAM_PARS	Alters the Current Value of the Configuration Parameters	
RD_RAM_PARS	Reads Back the Current Values of the Configuration Parameters	
LOAD_RNG	Loads Input Range into EEPROM (Requires 8 bytes)	
GET_RNG	Reads Back Input Range from EEPROM (Requires 8 bytes)	
WR_CJC	Downloads External CJC into RAM	
RD_CJC	Reads Back Current Value of the CJC from RAM	
SEL_CH	Selects an Input Channel	
CAL	Initiates Calibration Cycle	
RD_INTDATA	Reads Converted Data in 16-bit Integer Format and Conversion Status	
RD_FPDATA	Reads Converted Data in Floating Point Format and Conversion Status	

Floating Point Format Used Is 4-Byte IEEE Standard

#### Conversion Modes

The AD1B60 allows the designer control over the conversion process. Two modes of operation are available: a continuous conversion mode and a triggered conversion mode. There are three signals involved in the conversion process: the convert command input (CC, pin 21), integration status output (RDY, pin 16), and conversion status output (STATUS, pin 13). For continuous conversions, the CC input is set to

logic "1." In this mode, the AD1B60 converts continuously with an updated result available every 2 integration times. Conversions continue until CC is cleared to logic "0." When CC is cleared, the AD1B60 completes the current signal and background conversions at which time it waits (in "idle" mode) for CC to go high before starting another conversion.

#### AD1B60 CONTINUOUS CONVERSION MODE

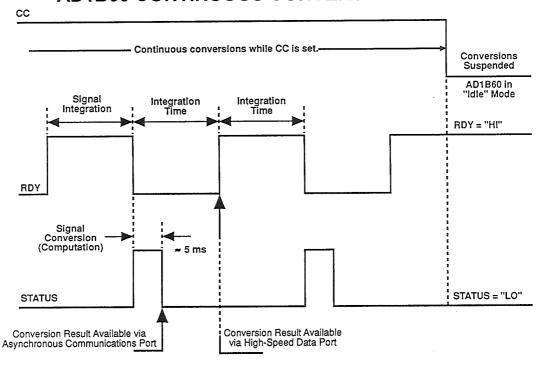


Figure 7.19

In the triggered conversion mode, the AD1B60 is in its "idle" state. In this state, the integration status output, RDY, is at logic "1" and the conversion status output, STATUS, is at logic "0." When CC goes to logic "1," the AD1B60 integrates and converts the input data. The device continuously converts its

input signals until CC is cleared. This conversion mode is particularly useful in applications where synchronous data conversion is required. The ADC in the AD1B60 is an integrating type. Its output is the *mean* of the input during the conversion process - it does not contain a sample and hold (SHA).

#### CC Trigger Conversions Conversions Suspended Suspended AD1B60 in "Idle" Mode Signal Integration RDY RDY = "HI" Signal Conversion (Computation) STATUS = "LO" **STATUS** Conversion Result Available via Conversion Result Available Asynchronous Communications Port via High-Speed Data Port

#### AD1B60 TRIGGERED CONVERSION MODE

Figure 7.20

During conversion, there are two methods by which the state of the AD1B60 can be determined. The first requires polling the states of RDY and STATUS. During conversion, RDY is set if the AD1B60 is integrating the input signal. At the end of signal integration, RDY is cleared and signal conversion commences. At this time, STATUS is set to indicate this condition. The STATUS output remains set until the conversion process is over. When both RDY and STATUS outputs are at logic "0," the result of the conversion is available at the asynchronous communication port of the AD1B60. When RDY goes high again, the output data is then available at the high-speed data port.

The second method to determine the status of the conversion process is by polling the status of the ADSTAT byte

returned by the RD\_INTDATA or RD\_FPDATA commands via the asynchronous communications port. Although delays due to this communications protocol are normal, they are small compared to the programmed integration time. If this is a concern, directly polling RDY and STATUS outputs provides real-time conversion information.

The rate at which the conversions take place depends upon the input range and the integration times programmed into the AD1B60. Figure 7.21 illustrates the relationship between conversion rate and integration time for various sensor configurations. For integration times of 33ms or longer, the conversion rate is constant regardless of input sensor configuration.

#### CONVERSION RATE IS USER-SELECTABLE

INTEGRATION	CONVERSIONS/SEC	CONVERSIONS/SEC	CONVERSIONS/SEC
TIME	CJC = THERMISTOR	WITHOUT CJC	K TYPE+THERMISTOR
2ms	90	100	48
5ms	78	87.5	44
33ms	14.8	14.8	14.8
40ms	12.3	12.3	12.3
50ms	9.9	9.9	9.9
60ms	8.3	8.3	8.3
100ms*	5*	5*	5*
200ms	2.5	2.5	2.5

<sup>\*</sup> Factory default setting

Figure 7.21

#### Calibrating the AD1B60

Although the AD1B60 is calibrated at the factory prior to shipment, the user may choose to calibrate the device for the desired application. The calibration procedure, outlined in Figure 7.22, is sequence-dependent and requires a precision voltage source and two precision resistors, a  $250\Omega$  resistor for RTDs and a  $100k\Omega$  resistor for thermocouples. The accuracy of the AD1B60's calibra-

tion depends upon the accuracy of the reference excitation or resistance. Although calibration accuracy of the AD1B60 does not depend on integration time, using a 200ms integration time for the calibration procedure is recommended to ensure the best resolution and noise rejection. This is the preferred method even though the application may use a shorter integration time.

### CALIBRATION OF AD1B60 IS PERFORMED OVER THE ASYNCHRONOUS PORT

Step	Input Range	Reference Excitation	Circuit Configuration
1	± 2 V	+ 2.00000 V	CH0 to Analog GND
2	± 1 V	+ 1.00000 V	CH0 to Analog GND
3	± 500 mV	+ 0.50000 V	CH0 to Analog GND
4	± 200 mV	+ 0.20000 V	CH0 to Analog GND
5	± 100 mV	+ 0.10000 V	CH0 to Analog GND
6	± 50 mV	+ 50.000 mV	CH0 to Analog GND
7	± 20 mV	+ 20.000 mV	CH0 to Analog GND
8	± 10 mV	+ 10.000 mV	CH0 to Analog GND
9	± 10 V	+ 10.00000 V	Attenuator to Analog GND
10	Type J TC	100.000 kΩ	CJC Input to Analog GND
11	100Ω Pt RTD, $\alpha$ = 0.00385 Ω/Ω/°C	250.000 Ω	4-wire RTD Configuration (CH1 to CH3)

- AD1B60 is Factory Calibrated
- Calibration Sequence is Sequence Dependent
- Not All Calibration Steps Are Required

Figure 7.22

Since the calibration procedure is sequence-dependent, calibration for certain input ranges depends on the prior calibration of one or more voltage ranges. For example, if the AD1B60 is intended to be used in thermocouple applications, calibration step #11 can be skipped; however, steps #1 through #10 cannot be skipped. The following steps illustrate the calibration sequence:

- 1. Configure the AD1B60 for each calibration step using the WR\_RAM\_PARS command. For example, to calibrate the AD1B60 for Step #1, set the input range RAM value to ±2V.
- 2. Apply the specified reference excitation for that particular calibration step.

For example, apply a +2.00000V reference to Channel 0.

- 3. Wait until the Data Valid flag in ADSTAT goes high.
- 4. Wait 1 second to allow the AD1B60 to acquire a stable reading.
- 5. Execute the CAL command.
- 6. Wait until the CAL flag in ADSTAT goes low.
- 7. Repeat Steps 1 through 6 for the remaining input ranges, as necessary.

#### THE AD1B60 IN THERMOCOUPLE APPLICATIONS

The commonest temperature sensors in industrial applications are thermocouples. Their rugged construction and low cost explain their popularity. However, the outputs of these sensors are nonlinear and require cold-junction, or ice-point, compensation to produce the correct measurement. The AD1B60 includes cold-junction compensation as one of its internal routines and offers four options for cold-junction compensation (CJC):

- 1. A 10kΩ, NTC Thermistor (Betatherm 10K3A1)
- 2. An external 1 mV/K temperature sensor (AD592 +  $1 \text{k}\Omega$  resistor)
- 3. An analog cold-junction compensator (AC1226)
- 4. A downloaded cold-junction temperature value

Figure 7.23 shows how the thermocouple, and the thermistor used for coldjunction compensation, are connected to the AD1B60 for temperature measurement. The thermocouple is connected between CH0 and GNDSENSE with the thermistor and the thermocouple's cold junction in close thermal proximity. Thus, if the ambient temperature of the cold junction changes, the thermistor registers the change in temperature, allowing the AD1B60 to compensate for

it. In this mode of cold-junction compensation, the AD1B60 provides the excitation current for the thermistor from CJC IN (pin 32). For open thermocouple detection, a 15nA current source is available at EXCOUT (pin 33) where it can be connected to the thermocouple's positive (+) lead. In the event of an open thermocouple, the output of the PGA saturates, and the AD1B60's output data stream will indicate an upscale fault condition. To avoid errors, the thermocouple's negative (-) terminal and the GNDSENSE pin should form a "star" connection with the analog ground. This is because GNDSENSE is actually an input.

In the second example, illustrated in Figure 7.24, the AD592, a monolithic temperature sensor whose output current exhibits a temperature coefficient of 1μA/K, works with a 1kΩ precision resistor to provide the cold-junction compensation. For optimum performance, the TCR of the precision resistor should be no greater than  $\pm$  10 ppm/°C. Like the thermistor, the AD592 must be in close thermal proximity to the thermocouple's cold junction to avoid measurement error. Again, a "star" connection to the analog ground should be formed with the thermocouple's negative terminal, the return end of the  $1k\Omega$  precision resistor, and the AD1B60's GNDSENSE pin.

### USING A THERMISTOR FOR COLD-JUNCTION COMPENSATION

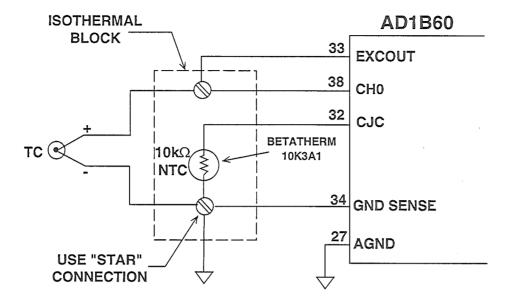
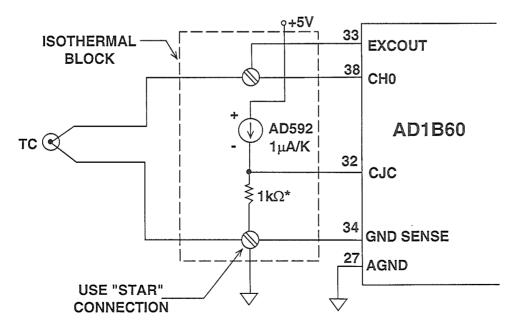


Figure 7.23

# USING THE AD592 TEMPERATURE SENSOR FOR COLD-JUNCTION COMPENSATION



\*PRECISION RESISTOR: 0.01% OR BETTER. TCR  $\leq$  10ppm/°C

Figure 7.24

#### THE AD1B60: AN INTELLIGENT, DIGITIZING SIGNAL CONDITIONER

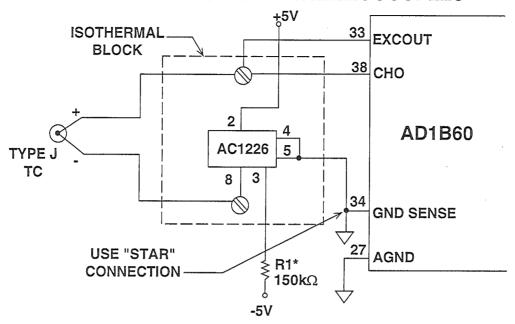
When either the thermistor CJC mode or the mV/K mode is selected, the AD1B60 reads the cold-junction sensor voltage during one of its background conversion cycles and from that reading obtains temperature of the cold junction. It then calculates the required correction voltage for the currently-active thermocouple range. This correction is digitally combined with the actual thermocouple sensor voltage to produce a cold-junction compensated value.

The third method for cold-junction compensation is illustrated in Figure 7.25. In this configuration, an AC1226, a micropower analog cold-junction compensator, produces an analog output voltage proportional to the temperature of the cold junction. This voltage is then subtracted from the thermocouple's terminating junction voltage at the input of the AD1B60. Since the subtraction occurs at the input to the AD1B60, no algorithmic correction is required, and the internal CJ compensation is disabled in this mode. To ensure accurate compensation, the negative (-) terminal of the thermocouple is directly connected to the corresponding pin on the AC1226 at the cold junction. The AC1226 compensator is specifically designed for use with type E, J, K, R, S, and T thermocouples, and is packaged in an 8-pin

DIP. The compensator contains special curvature circuitry and resistive dividers to provide the requisite Seebeck coefficient for each thermocouple type. The special "bow" correction circuitry allows the AC1226 to maintain accuracy over a wider temperature range than other temperature sensors. In fact, over an ambient temperature range of  $30^{\circ}\text{C} \text{ (+20°C} \leq \text{T}_{\text{A}} \leq +50^{\circ}\text{C)}$ , the error is less than 0.5°C. Connections between various thermocouples and the AC1226 are outlined in Figure 7.26. In applications where the ambient temperature of the AC1226 might be below 0°C, an external pull-down resistor (R1) is required for proper operation. A 150k $\Omega$ resistor connected to -5V ensures proper operation of the AC1226 when the ambient temperature is below 0°C.

The fourth method of providing cold-junction compensation is to download a value into the AD1B60's RAM through the asynchronous port using the WR\_CJC command from the command set. This mode is useful in applications where a single cold-junction compensator is used for multiplexing a number of sensors or where a higher accuracy device is used for CJC sensing. In this mode, acceptable values for user-defined CJC range from −25°C ≤ TCJC ≤+85°C, and the CJ variable is initialized to 0°C upon power-up/reset.

### USING THE AC1226 COLD-JUNCTION COMPENSATOR WITH THERMOCOUPLES



\*R1 NOT REQUIRED IF AC1226 TEMPERATURE ≥ 0°C

Figure 7.25

# CIRCUIT CONNECTION BETWEEN THE AC1226 AND VARIOUS THERMOCOUPLES

Thermocouple Type	Connect TC (-) to AC1226 Pin #
E	1
J	8
K	7
R	6
S	6
Т	7

Figure 7.26

When the AD1B60 is used in thermocouple applications, the issues in Figure 7.27 must always be remembered. In applications where more than one thermocouple may be used the AD1B60 may be configured for different thermocouple input ranges. For example, CH0 could be configured for a Type T thermocouple while CH1 is configured for a Type K thermocouple. Up to 12 integra-

tion times are needed for valid data in these applications. Data may be verified by checking the status of the DATA VALID bit in the ADSTAT byte. If the application requires multiplexing between like thermocouples (therefore equal input ranges), then up to 3 integration times are needed for valid data. The channel bits in the ADSTAT byte may be used to check for valid data.

### ISSUES TO CONSIDER WHEN MEASURING THERMOCOUPLES

- Up to 4 thermocouples can be multiplexed
- One CJC can be used for 4 thermocouples
- Open thermocouple detection using internal 15nA current source
- CJC readings updated every 5 signal conversions (10 absolute conversions)
- Open thermocouple detection on 1 thermocouple only

#### Figure 7.27

In applications where a number of thermocouples are used, open thermocouple detection can be applied to only one channel. To provide open circuit detection for all thermocouples, the circuit illustrated in Figure 7.28 can be used.

#### THREE RESISTORS MAKE A SIMPLE OPEN TO DETECTOR

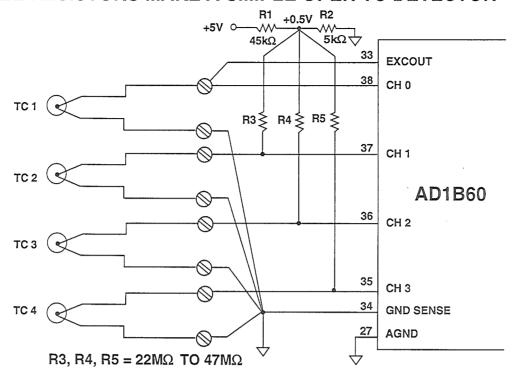


Figure 7.28

In this circuit, R1 and R2 form a voltage divider whose output is set to +0.5V. For each thermocouple, a resistor between  $22M\Omega$  to  $47M\Omega$  is used to inject a very small current into the positive terminal. In the event of an

open thermocouple, that input channel goes towards +5V — a potential sufficiently high to saturate the output of the PGA. This sets the overflow flag in the AD1B60's ADSTAT byte.

#### CONFIGURING THE AD1B60 FOR VOLTAGE INPUTS

The AD1B60 can be configured with low- or high-level input signals. Figure 7.29 shows how to configure the device for low-level voltage inputs. Low-level signals are signals in the range of  $\pm 10 \text{mV} \leq \text{V}_{\text{IN}} \leq \pm 2 \text{V}$ . To minimize errors, a "star" connection is used to connect all the signal returns together

at one point to the analog ground. When the AD1B60 is configured in this mode, the CJC IN channel remains active, therefore it can operate as a "phantom" 5th temperature channel when a thermistor or a mV/K source is connected to it.

# CONNECTING LOW LEVEL (< ±2V) INPUT SIGNALS TO THE AD1B60

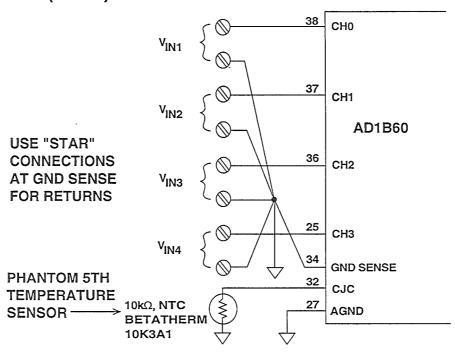


Figure 7.29

Configuring the AD1B60 for operation with a high-level input is also straightforward and is illustrated in Figure 7.30. A high-level input is any signal in the range of  $\pm 5V \le V_{IN} \le \pm 10V$ . The

signal is applied to the internal 5:1 attenuator at the Attenuator Input pin (pin 28) of the AD1B60; hence, only one high-level voltage input source is allowed to the AD1B60.

# CONNECTING HIGH LEVEL (< ±10V) INPUT SIGNALS TO THE AD1B60

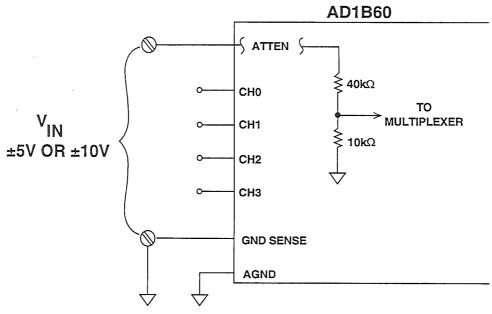


Figure 7.30

When configured for a high level input, all other channels of the AD1B60 are disabled including EXCOUT and CJC IN. The AD1B60, in other words, be-

comes dedicated to this single input. Figure 7.31 outlines the issues to consider when the AD1B60 is configured for voltage inputs.

#### ISSUES TO CONSIDER WHEN USING VOLTAGE INPUTS

- Low-level inputs
  - ♦ All 4 sources must share 1 AGND
  - ♦ If multiplexing, all input ranges must be the same
  - ♦ CJC output active: Phantom 5th temperature channel
- High-level inputs
  - Multiplexing low-level inputs: Not Allowed
  - Multiplexing RTDs: Not Allowed
  - ♦ 50kΩ Input Impedance
  - Dedicated

Figure 7.31

#### CONFIGURING THE AD1B60 FOR RTD APPLICATIONS

The AD1B60 can accommodate both 3and 4-wire RTD applications, as shown in Figure 7.32. For three-wire RTD applications, the internal current source excitation is connected directly to the RTD's FORCE (+) lead wire through a  $10k\Omega$  resistor. This external resistor need not be a precision type — it serves only to reduce current source selfheating. Without this resistor, a gain error of approximately 0.2°C would be introduced. The RTD's FORCE (+) lead is directly connected to the AD1B60's CH0 input. Only in 3-wire applications is a "star" connection required to minimize any additional errors generated by ground loops, it is formed with the RTD's FORCE (-) lead wire and the AD1B60's GNDSENSE input connected to the analog ground.

### CONFIGURING THE AD1B60 FOR RTDs IS EASY

### 3-WIRE RTD CONFIGURATION

#### 4-WIRE RTD CONFIGURATION

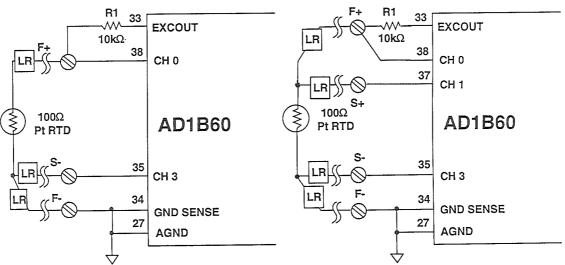


Figure 7.32

In four-wire applications the RTD FORCE(+) lead goes to the  $10k\Omega$  resistor, its SENSE(+) to CH1, and its SENSE(-) to CH3. There is no star connection, and FORCE(-) goes to GNDSENSE and AGND.

When the AD1B60 is configured for RTD applications, issues to consider during the design are outlined in Figure 7.33. Although the AD1B60 provides compensation for lead resistances up to

 $40\Omega$ , total, the lead-wire resistances in 3-wire RTD applications must match; in fact, every  $38.5 m\Omega$  mismatch in lead resistance will introduce an error of  $0.1^{\circ}\text{C}$  in the reading. No such lead-wire resistance matching is required in four-wire applications. To calibrate the AD1B60 for RTD applications, the 4-wire configuration is used with a precision  $250\Omega$  resistor substituted for the RTD.

#### ISSUES TO CONSIDER WHEN USING RTDs

- RTD is biased by an internal 200μA current source
- R1 is recommended to protect against self-heating
- 3-wire RTD applications: Lead lengths (R<sub>S</sub>) must match
- 4-wire RTD applications: Lead lengths (R<sub>S</sub>) can differ
- **■** Calibration procedure requires 4-wire configuration
- Lead wire compensation is updated every 5 signal conversions

#### Figure 7.33

#### Using the AD1B60 in an Industrial Environment

The circuit illustrated in Figure 7.34 shows how the AD1B60 might be used in an industrial environment where remote operation is required. The application requires that the AD1B60 be close to the thermocouple cold junction to minimize ground sense errors. In this circuit, an isolated power supply is used to provide power for the AD1B60 and the optocouplers. The low supply currents of the AD1B60 make the design of the isolated power supply undemanding. To communicate with the host system, optocouplers provide a high-speed, galvanically isolated digital interface.

In general, industrial environments place difficult requirements on inte-

grated circuits. It is well known that these environments, where large voltage transients generated by heavy machinery or power failures are commonplace, wreak havoc on integrated circuits. It is also well known that devices constructed on CMOS-based processes are generally more susceptible to damage from these large transients than integrated circuits built with bipolar devices. Even though the ASIC in the AD1B60 is a custom CMOS device, it was designed to be "protectable"; that is, the design of the AD1B60's analog input circuitry allows for the addition of input protection circuitry without sacrifice of accuracy.

## AN ISOLATED THERMOCOUPLE SIGNAL CONDITIONING APPLICATION CIRCUIT

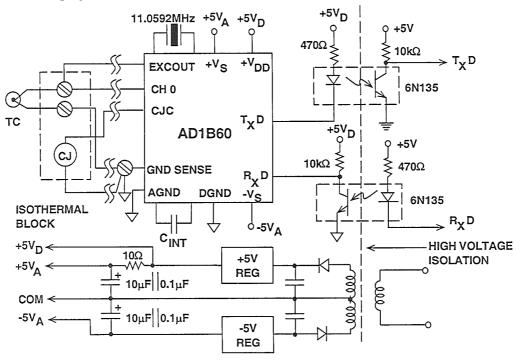


Figure 7.34

#### OPERATING THE AD1B60 IN HOSTILE ENVIRONMENTS

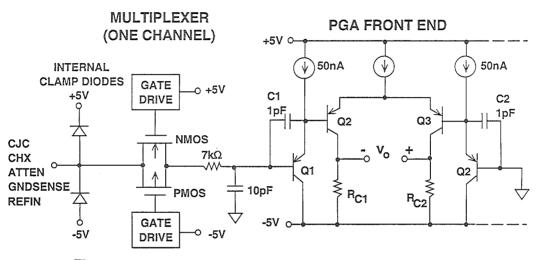
- Industrial environments wreak havoc with ICs
- CMOS is more susceptible than bipolar
- The AD1B60 is designed to be protected easily

Figure 7.35

Illustrated in Figure 7.36 is the equivalent circuit of one AD1B60 input channel. Each multiplexer input is a CMOS transmission gate (T-gate) which is constructed with an N-channel and a P-channel MOSFET. The purpose of the gate drivers is to apply either +5 V or -5V to each gate to ensure an "ON" or an "OFF" condition. When the T-gate is

turned on, the parallel combination of the N-channel and P-channel's drain-source resistance is  $3k\Omega$ . This resistance and the  $7k\Omega$  resistor form a 1.6MHz low pass filter with the 10pF capacitor. This minimizes the need for an external noise filter — another advantage of the AD1B60.

#### EQUIVALENT CIRCUIT OF THE ANALOG FRONT END



- Multiplexer switch: NMOS/PMOS T-gate, Ron ≈ 3kΩ
- Ron + Low-Pass Filter: f<sub>3dB</sub> = 1.6MHz
- PGA input bias current < 3na</p>
- C1, C2 added to reduce RF rectification

Figure 7.36

The input signal is then applied to the PGA whose input circuitry consists of a resistively-loaded PNP differential pair. To minimize input bias currents (and, thus, increase the input impedance), the differential pair is buffered by PNP emitter followers biased at 50nA. As a result of buffering the input differential pair, the AD1B60's input bias currents are typically 0.5nA (3nA, maximum). These low input bias currents permit

the use of external fixed resistors for filtering or current limiting, if required. Capacitors C1 and C2 bypass the base-emitter transistor junctions of Q1 and Q2 at high frequencies. This high frequency bypass technique prevents the input emitter followers from rectifying high frequency noise. As discussed earlier in the seminar, RF rectification in bipolar transistors depends upon the ambient temperature and quiescent

#### THE AD1B60: AN INTELLIGENT, DIGITIZING SIGNAL CONDITIONER

current levels. Shunting the high frequency away from the junction proved to be an effective measure against high frequency interference. The values for C1 and C2 were determined empirically to limit high frequency interference without causing circuit instability. This technique worked well to filter noise up to 20MHz. Above that frequency the low pass filter formed by the T-gate's ON resistance, the  $7k\Omega$  resistor, and the 10pF capacitor rejects any high frequency interference. Last, clamp diodes connected to the analog supplies protect the input multiplexer channels against small transient overvoltages. However, in hostile environments where large transients could be applied

to the AD1B60's inputs, additional external protection circuitry must be used.

The circuit illustrated in Figure 7.37 is an example of an inexpensive circuit for protecting the AD1B60's analog inputs against transient overvoltages. External diodes, D1 and D2, clamp the inputs safely to the supply voltages. To prevent parasitic transistor action, D1 and D2 should be low-leakage schottky diodes or low-leakage FETs. Low-leakage devices are required here because leakage currents double for every 10°C rise in ambient temperature and leakage currents generate offset errors.

### PROTECTING THE AD1B60 ANALOG INPUTS FROM OVERVOLTAGE CONDITIONS

- D1, D2: Low leakage Schottky diode, Type 5082-2835, or Low-Leakage JFETs, Type J201
- Limit diode current < 10mA</p>
- Choose Rs  $\cong V_{ov}$  /10mA;  $P_D = V_{ov}^2/Rs$
- For filtering, limit Cs +  $C_{D1}$  +  $C_{D2}$  < 47pF

Figure 7.37

To limit diode current to 10mA, a resistor, Rg, can be used in series with the AD1B60 input. The value and power rating of the resistor depend upon the level of overvoltage protection required. If a series resistance is used in any of the AD1B60's inputs, an equal-valued resistance must be added to the GNDSENSE input to avoid errors due

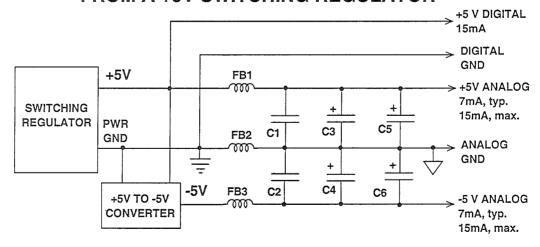
to resistive imbalance. For additional high-frequency filtering, an external capacitor, CS, can be used. When an external capacitor is added to any AD1B60 input the sum of the diode capacitances plus the external capacitor should be less than 47pF, otherwise measurement errors may result from to multiplexer charge pumping.

#### Supplying Power to the AD1B60

There are no special requirements for power supplies for the AD1B60 since it only dissipates about 120mW. However, the AD1B60 does contain both analog and digital circuitry in the same package, and it is important to prevent any digital interference from coupling into the analog supply lines. Also, the digital +5V supply must not be allowed to exceed the analog +5V by more than 200mV. Otherwise, parasitic transistor action will occur.

The circuit shown in Figure 7.38 illustrates the techniques used to generate an analog-quality power supply from a +5V switching regulator. Switchers have a well-earned reputation for generating a great deal of noise over a wide range of frequencies. Ideally they ought not be used; however, their small size, high efficiency, and low cost have made them very popular and it is hard to avoid them.

### SUPPLY POWER TO THE AD1B60 FROM A +5V SWITCHING REGULATOR



- FB1, FB2, FB3: 2 Turns, Fair-Rite #2677006301 Ferrite Beads
- C1, C2: 0.1μF CeramicC3, C4: 10 22μF Tantalum
- C4, C6: 100µF Low ESR Electrolytic

Figure 7.38

The -5V supply is generated from a DC/DC converter, and the filter topology is a differential L-C type with separate power supply feeds for +5V, -5V, and common. With the values shown, the

filter can easily handle 100mA of load current without saturating the ferrite cores. For lowest noise, all electrolytic capacitors should be low a ESR-(Equivalent Series Resistance) type.

## LAYOUT TECHNIQUES FOR MAXIMUM PERFORMANCE

Oftentimes overlooked, the physical layout of a circuit plays almost as important a role as properly filtering the supply feeds. The performance of an AD1B60 can be compromised if the

layout is not well thought out. Summarized in Figure 7.39 are the techniques to follow to achieve maximum performance from an AD1B60 or from any other high performance analog circuit.

# USE PROPER LAYOUT TECHNIQUES TO MAXIMIZE PERFORMANCE

- Keep Analog Input Lead Lengths Short
- Bypass +Vs and -Vs with 10µF/0.1µF to AGND
- Bypass +Vd with 10µF/0.1µF to DGND
- Use Separate AGND and DGND Planes
- Tie AGND to DGND at One Point Only
- 2-Layer PC Board Works Best
- AD1B60 Evaluation Board Available

Figure 7.39

## THE AD1B60 EVALUATION BOARD

A device such as the AD1B60 requires great care to achieve the highest level of performance. Analog Devices offers an evaluation kit for the AD1B60. The evaluation package includes an evaluation board, a menu driven program, and an extensive users guide. The self-contained, ready-to-use evaluation board includes an AD1B60 IC and an RS-232 serial communications port for

direct connection to an IBM PC<sup>TM</sup>, PC/XT<sup>TM</sup>, PC/AT<sup>TM</sup>, or compatible host computer system running PC-DOS<sup>TM</sup> operating system. Figure 7.41 is a simplified schematic diagram of the AD1B60 evaluation board used in a thermocouple application. Details for operating the evaluation board can be found in the AD1B60 Users Guide.

## **EVALUATION BOARD MAKES THE AD1B60 EASY TO USE**

- RS-232 Serial Port Connector Provided For Easy PC Hookup
- Menu Driven Program Included
- Extensive AD1B60 Users Guide Available
- Downloadable Range Library Included

Figure 7.40

#### AD1B60 THERMOCOUPLE APPLICATION 0.1μF 0.1μF 0.1µF O ANALOG DIGITAL GROUND EXCITATIONS AD1B60 BROWNOUT/ WATCHDOG REFOUT TYPE J THERMOCOUPLE REFERENCE RESETI EEPROM CH1 HAM CJC THERMISTOR TI E.G., BETATHERM 10K3A1 PMODE MICROPROCESSOR ADC ATTENUATOR ADM CJC 232L GNDSNS 11.0592 MHz E.G., SARONIX NYMPH NMP111 ADDRESS 00

Figure 7.41

## APPENDIX

# Using Digital Algorithms in Signal Conditioning Circuitry

The marketplace for signal conditioners for thermocouples and RTDs for use in industrial environments requires that they have high accuracy, stability, and resolution. Since thermocouples and RTD sensors have output spans of well

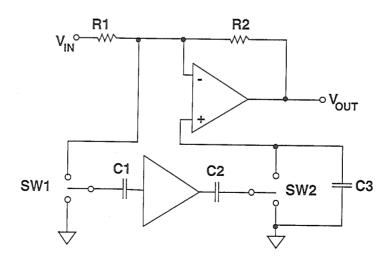
under 100 millivolts full scale, a good signal conditioner must have carefully designed input structures in order to achieve the kind of low offset and gain drift necessary for high performance.

### **Analog Offset Compensation**

Although a number of good quality, low-drift amplifiers can be found on the market today, it is still desirable to have a "chopper" style front end; i.e., an input with some form of servo control for offset, as illustrated in Figure 7.42. Conventional linear amplifiers with sub-microvolt offset drifts can be expen-

sive and may require trimming for initial offset error. Their long-term stability may be suspect, but monolithic "chopper" op amps are comparatively expensive, relatively narrow band, and may exhibit other undesirable characteristics.

## ANALOG OFFSET COMPENSATION



**CHOPPER STABILIZED AMPLIFIER** 

Figure 7.42

In a digital signal conditioner where A/D conversion is provided, the stability of a "chopper" op amp can easily be achieved by the addition of a simple multiplexer at the input. Instead of

continuously chopping the input signal, a digitizing conditioner can alternately convert the input signal and a sample of true ground, as shown in Figure 7.43.

## DIGITAL OFFSET COMPENSATION

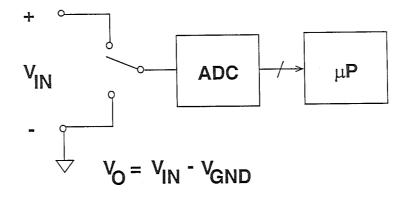


Figure 7.43

As long as the source impedances are reasonably well-matched, the microcontroller can simply subtract the value of the reading obtained at the ground sense input from the reading obtained at the signal input. Thus:  $V_{OUT} = V_{IN} - V_{GND}$ .

Since the offset is continuously sampled, the amplifier need not exhibit particularly good offset performance. Furthermore, the relatively slow offset sampling rate in this kind of system is not important, because whatever op amp is used it will drift quite slowly.

The same concept can be extended to include a servo control of the span. In most A/D converters, there are at least two separate components of span drift: the first is the drift of the voltage reference used by the converter, and the second is the drift of gain elements (i.e., resistors) within the converter itself.

As shown in Figure 7.44, an additional multiplexer input by which the reference voltage can be sampled allows all span error terms other than that of the reference to be canceled.

## SPAN AND OFFSET COMPENSATION

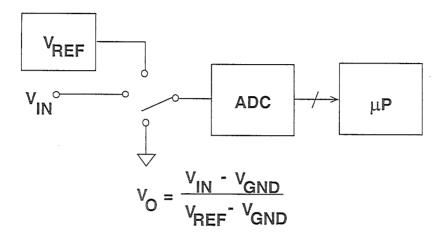


Figure 7.44

When this technique is employed, A/D conversion architectures which exhibit good linearity but poor offset and span stability can be considered. ADC archi-

tectures of the "charge-balancing" type are natural candidates for this approach.

### **Digital Calibration**

Since most industrial measurements require absolute, rather than relative accuracy, all signal conditioners must contain some provision for calibration. In the simplest case, some means of adjusting the gain will be required, either at the factory or in the application.

Conventional analog signal conditioners can be calibrated in a number of different ways. Signal conditioners sold with a specified accuracy limit, and without any user-accessible trims, may be calibrated at the factory with fixed resistors, potentiometers, or even with laser-trimmed resistors networks. Some types of analog signal conditioners have user-accessible trim potentiometers,

usually beneath a cover or other type of access panel.

However, trim controls can be a problem in the actual application. In particular, potentiometers can lose their precise setting under vibration and may also be susceptible to contamination by the environment.

Digital signal conditioners avoid the use of explicit calibration hardware via the use of digital calibration. The equation in Figure 7.44 can be modified to incorporate a span calibration factor, KSPAN, which allows for the correction of full-scale error when multiplied with the output as shown in Figure 7.45.

## DIGITAL SPAN CALIBRATION

$$V_{OUT} = K_{SPAN} \left( \frac{V_{IN} - V_{GND}}{V_{REF} - V_{GND}} \right)$$

$$K_{SPAN} = \frac{V_{REF(NOMINAL)}}{V_{REF(ACTUAL)}}$$

## Figure 7.45

Once this algorithm has been implemented in the design, the voltage reference need not be precise since the nominal error can be compensated. However, to prevent measurement errors, the reference voltage must be stable.

The actual value of KSPAN can be derived automatically. By forcing KSPAN to unity and by performing a

single conversion on a full-scale reference standard, the resulting output will simply be the reciprocal of the required calibration value.

The value for KSPAN is stored in EEPROM (Electrically Erasable Programmable Read Only Memory). The use of EEPROM allows for KSPAN to be changed to compensate for any long term drift of the reference.

## Gain Correction for Gains Greater Than Unity

Although the algorithms described above were applied to unity-gain applications, the same techniques can be extended to applications requiring higher gains (such as thermocouple and RTD applications).

It is possible to use the circuit of Figure 7.44 with a fixed high gain amplifier preceding the A/D converter. However, scaling the voltage reference is necessary to match the effective full-scale input voltage. As a result, two drift error terms appear:

- 1) The drift of the reference attenuator, and
- 2) The drift of the gain-setting resistors in the amplifier.

An improved approach is to use a programmable gain amplifier in place of the fixed-gain amplifier, as shown in Figure 7.46. The lower limit of the PGA's gain range is set to unity. In this arrangement, two measurements are taken of the ground potential: one at unity and one at desired signal gain.

By applying both of these measurements, the algorithm now relates the measurements at the desired signal gain to the ratio of the span at the signal gain to the span at unity. Only one uncompensated drift term remains: the relative temperature coefficient of resistance of the thin-film network used in the PGA.

## **MULTIPLE GAIN COMPENSATION**

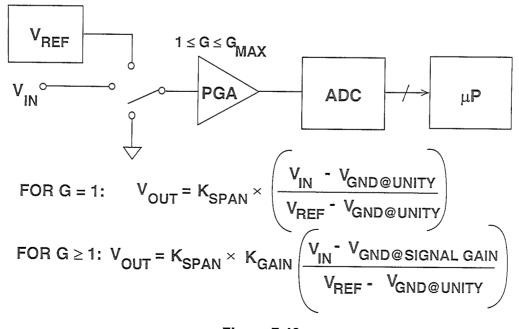


Figure 7.46

## THE AD1B60: AN INTELLIGENT, DIGITIZING SIGNAL CONDITIONER

This equation requires the introduction of a second calibration factor, KGAIN, which accounts for the absolute gain error of the PGA at the signal gain. In practice, KSPAN and KGAIN can be combined into a single calibration factor to conserve both EEPROM space and execution time.

This concept can now be extended to any number of separate gain settings, with K-factors for each and forms the basis for "configurable" signal conditioners which can be programmed to handle a wide range of sensor inputs.

## **Analog Linearization**

Thermocouples and RTD sensors require linearization if the desired output is scaled into engineering units. Although there are a small number of applications where the desired operating span of the sensor is narrow enough to be assumed linear, many applications include some form of linearization.

Analog signal conditioners accomplish linearization using hardware techniques. There are many ways to per-

form this task, each with varying degrees of complexity and conformance to the standard equations governing the sensor.

RTD sensors are easier than thermocouples to linearize. The nonlinearity of an RTD is a relatively gentle parabolic effect which can be canceled with fair accuracy by a circuit shown in Figure 7.47.

#### ANALOG RTD LINEARIZATION

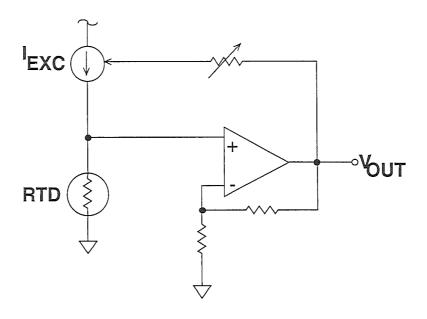


Figure 7.47

In this circuit, a portion of the amplified transducer output is fed back to the excitation circuit. This feedback, if properly scaled, warps the signal with a "bow" that is opposite in shape to that of the sensor output, yielding a linear result.

Thermocouples are more difficult to linearize since their nonlinearity is not a simple second-order function. The most common analog method of thermocouple linearization is the segment approximation method. This technique approximates the thermocouple transfer function as a connected series of straight line segments. With careful placement of the "breakpoints" (the junctions of the segments), a reasonably good fit to the thermocouple characteristic can be obtained.

The circuit in Figure 7.48 is a very simplified example of a passive

breakpoint linearizer. At input voltages near zero, the circuit has unity gain and presents an impedance equal to Rs to the load. As the input voltage rises to V<sub>BP1</sub>, diode D1 begins to conduct, and the circuit gain is reduced due to the shunting effect of the impedance at V<sub>BP1</sub>. As the input voltage continues to rise to V<sub>BP2</sub>, the second breakpoint activates (via diode D2) which further reduces the gain of the circuit. Each of the shunt elements in the circuit represents an additional breakpoint, whose turn-on point, as well as its effect on gain, can be arbitrarily chosen. The main drawback to this particular circuit is that the breakpoints are unidirectional; i.e., they can only reduce the gain, they cannot increase it. In practical applications, a more complex circuit with op amps is used so that the gain of the system can increase or decrease at each breakpoint.

## ANALOG THERMOCOUPLE LINEARIZATION

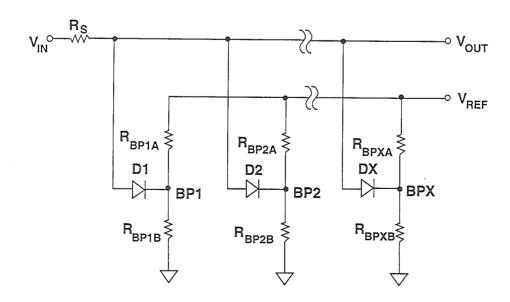


Figure 7.48

#### THE AD1B60: AN INTELLIGENT, DIGITIZING SIGNAL CONDITIONER

The drawback to hardware linearizers is their inflexibility — they must be designed for a specific sensor and operating range; they consume a great deal

of circuit board area; and they usually require precision components because they are extremely difficult to trim.

### **Digital Linearization**

In signal conditioners that incorporate both A/D conversion and "intelligence" (i.e., a microcontroller), linearization by digital means is the best approach. Apart from providing almost unlimited accuracy, digital implementations of linearization algorithms are flexible—accommodating a different sensor type involves no more than changing the coefficients of the linearization algorithm. Thus, the conditioner can be programmed for a variety of sensor transfer functions without altering its circuitry; hence, the term "configurable conditioner" is used.

There are tradeoffs when choosing an algorithm for implementing digital linearization. Microcontrollers can be exceedingly slow when asked to perform complex mathematical operations; thus, one such tradeoff is the complexity and precision of the required computation. Another tradeoff is memory which can be in short supply. Fast algorithms that depend upon lookup-tables can use a large amount of memory.

In general, implementing mathematical functions requires some margin of resolution to allow for truncation error. For example, sixteen-bit integer calculations could be employed in systems to

produce a 14-bit result. However, the dynamic range of the mathematics must also be taken into account. For example, if polynomial approximation techniques are used, then the dynamic range of the coefficients may demand 24- or 32-bit computation to prevent saturation. Therefore, the selection of the mathematical approach will depend upon the nature of the linearization algorithm. In most cases, if dynamic range requirements call for 32-bit mathematics, IEEE single-precision floating-point routines are more efficient than integer routines. The memory requirements for each variable and/or constant are identical, but the dynamic range of IEEE floating-point routines is far less limited, and execution times are roughly comparable for most microcontrollers. Linearization techniques can take many forms, but the most common techniques are shown in Figure 7.49.

The simplest form of digital piece-wise linear approximation method is illustrated in Figure 7.50. The sensor output span is broken into a number of equal length segments, and a lookup table containing a set of offset and span correction values for each segment is stored in memory.

## **DIGITAL LINEARIZATION**

- Single Polynomial (Used in AD1B60)
- Piecewise Linear Approximation
  - Equal Length Segment
  - Optimized Segments
- Segmented Polynomial Splines

Figure 7.49

# BREAKPOINT LINEARIZATION WITH EQUAL LENGTH SEGMENTS

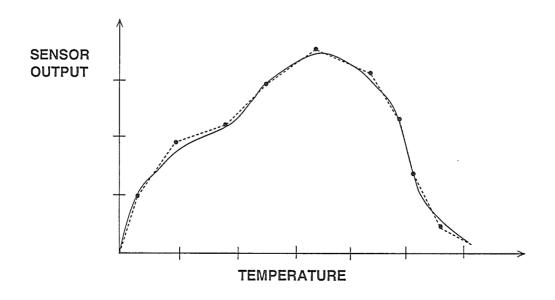


Figure 7.50

#### THE AD1B60: AN INTELLIGENT, DIGITIZING SIGNAL CONDITIONER

The algorithm determines the position of the sensor output relative to the table, retrieves the appropriate coefficients, and performs an "mx + b" operation on the sensor output to produce a linearized result. This approach has the advantage of high speed because only a single multiplication and addition are required to produce the result. However, it requires a large amount of memory to store coefficient table.

The disadvantage of the "equal length segment" method is that the error of approximation is different in each segment. One technique which can be used to minimize the error in each segment is the "optimized segment

length" method. This is an advantageous approach because some portions of the thermocouple's curve are more nonlinear than others. Hence, the algorithm can choose the exact length of the segment to minimize the error, as shown in Figure 7.51. For example, shorter segments can be used to minimize the approximation error on portions of the curve where the sensor's output characteristic is curving sharply. Conversely in regions where the transfer function is linear, the segments can be longer. With this "optimized segment length" method, the coefficient table can have fewer entries for an equivalent worst-case error.

# BREAKPOINT LINEARIZATION WITH OPTIMIZED SEGMENT LENGTHS

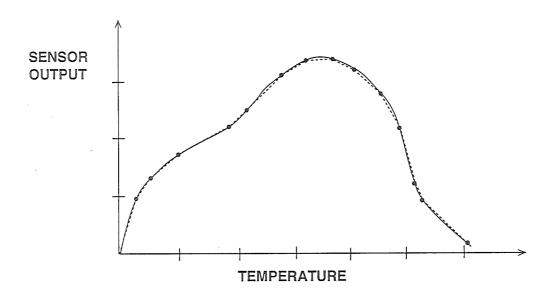


Figure 7.51

This particular method does have one drawback: the separations of the breakpoints vary. The coefficient table must contain the positions of the breakpoints, and the algorithm must search to locate the segment by comparing the sensor output to the breakpoint entries in the table. This segment search can be time consuming, and may negate the speed advantage.

In cases where memory conservation is more important that execution speed, polynomial linearization is a better choice. Only a modest number of coefficients must be stored, and the code for evaluating a polynomial is a simple recursive routine. In some cases, a polynomial approach may actually be

### **Cold-Junction Compensation**

For a signal conditioner to perform linearization on thermocouples, it is necessary to provide for cold-junction, or ice-point, compensation. In analog signal conditioners, cold-junction compensation is usually performed by the use of an analog temperature sensor whose output is scaled to track the thermocouple's Seebeck coefficient at the terminating junction. This is illustrated in Figure 7.52. The signal produced by the temperature sensor is subtracted from the thermocouple signal at the signal conditioner's input, thereby compensating for the cold junction voltage.

This type of analog compensation is limited in both performance and flexibility. One performance limitation is the temperature span over which the compensation circuitry remains accurate. Since thermocouple response at the cold junction is nonlinear, most circuits of this type use a straight-line approximation to the thermocouple curve. Depending upon the particular

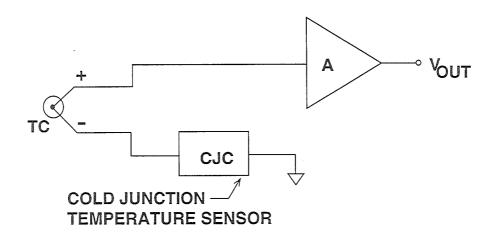
faster than the optimized segment length method because no search for breakpoints is necessary.

The accuracy of the polynomial approximation is limited by the degree of the polynomial used which, in turn, is limited by the resolution and dynamic range of the mathematical capabilities of the microcontroller. If single-precision IEEE mathematics is used, the polynomial is constrained to 9th order or less. Fortunately, reasonable performance can usually be achieved with polynomials ranging from 5th to 7th order. The exception is the more nonlinear thermocouples when they are used over a wide temperature range.

thermocouple chosen, this approximation will have a useful temperature span of only 5°C to 45°C. Outside these limits, the nonlinearity of the thermocouple will result in a inaccurate compensation. This kind of compensation is also notoriously inflexible in that each thermocouple type has a different Seebeck coefficient. Scaling and trimming the CJC circuit for each thermocouple type is essential.

In a digital signal conditioner, both the performance and the flexibility of the CJC can be greatly enhanced. Instead of utilizing physical hardware to add or subtract the cold junction compensation voltage from the input signal, a digital signal conditioner can acquire the coldjunction temperature, perform a "reverse linearization" using polynomial techniques to match the actual thermocouple curve, and combine the result digitally with the input signal after the conversion process. A block diagram for such an operation is shown in Figure 7.53.

## ANALOG COLD JUNCTION COMPENSATION



 $V_{OUT} = A(V_{TC} - V_{CJ})$ 

Figure 7.52

## DIGITAL COLD JUNCTION COMPENSATION

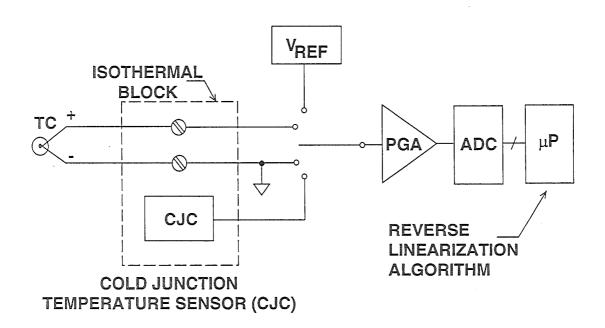


Figure 7.53

#### System Applications Guide

The functional advantages of this scheme are flexibility and simplicity, since no analog circuitry is required to combine the compensation voltage with the input signal. Thus, any thermocouple can be compensated by simple

## substitution of coefficients in the lookup table. This scheme can maintain compensation accuracy over the entire operating range of the signal conditioner.

### **RTD Lead Compensation**

RTD sensors require lead compensation in order to reject the effects of the resistance of the interconnecting leads. In some cases, the sensor is a four-wire device where the leads supplying the excitation are separate from those used to sense the voltage across the element. More commonly, the RTD is supplied with only three leads: two are used to sense the element, and only one excitation lead is attached. One of the sensing leads is used as a return for the excitation current.

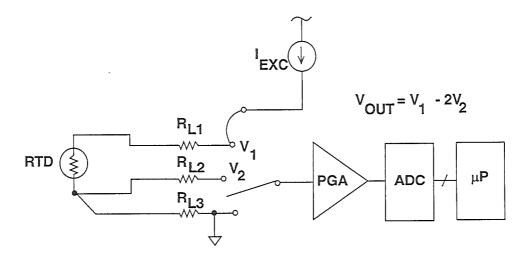
Circuits designed to interface to threewire RTD sensors must contain some provision for reading the excitation drop across one side of the device, and subtracting this voltage drop from the sensor output to compensate for the other, unsensed, side. In analog RTD signal conditioners, there are a number of approaches to solving this problem: some involve the use of multiple current sources and instrumentation amplifiers to affect the subtraction process.

In digital conditioners, this subtractive process can be achieved by an algorithm rather than in hardware. Referring to Figure 7.54, the digital conditioner can be configured to read two separate voltages with respect to the circuit common. V<sub>1</sub> represents the "top" of the RTD and contains the effects of voltage drop on both sides of the RTD. V<sub>2</sub> senses the voltage drop on the lower side of the element.

Assuming that the lead resistances are equal (a requirement for three-wire RTD applications), the effect of leadwire resistance can be eliminated, and the voltage at the RTD calculated. The expression for this operation is given by:  $V_{OUT} = V_1 - (2 \cdot V_2)$ .

Apart from hardware savings, the digital approach to lead-wire compensation also yields a significant performance advantage. The lead-wire resistance rejection capability of an RTD signal conditioner is often quoted as a ratio. In analog RTD conditioners, a typical specification might be  $0.01\Omega/\Omega$ which means that a  $1\Omega$  difference in the lead resistance is perceived as  $0.01\Omega$  in the RTD. The rejection ratio depends upon the matching and tracking of current sources and/or precision analog trims. The digital lead compensation has a much better rejection ratio because it does not depend upon precision analog hardware. The full accuracy and resolution of an A/D system is used to measure and compute the required compensation. In digital RTD signal conditioners, infinite rejection is possible and no significant error is introduced into the measurement by lead resistance until the excitation current source saturates (providing-in the 3 wire case-the lead resistances match).

## DIGITAL LEAD RESISTANCE COMPENSATION



 $R_{L1}$  AND  $R_{L3}$  MUST BE EQUAL

Figure 7.54

#### Conclusion

Although additional enhancements and corrections are theoretically possible, they have not been implemented due to memory and execution speed constraints. As microcontroller functions

become faster and denser, it will be possible to extract significantly better performance from even simpler analog circuits.

## Acknowledgments

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System Applications Guide