SECTION 6

HIGH ACCURACY A/D CONVERSION

- SIGNAL CONDITIONING TRANSDUCER INPUT ADCs
- SINGLE-SUPPLY ADCs
- SERIAL OUTPUT ADCs
- COMPLETE DATA ACQUISITION ON A CHIP
- ULTRA-HIGH RESOLUTION DAS ON A CHIP

SECTION 6

HIGH ACCURACY A/D CONVERSION

Joe Buxton

SIGNAL CONDITIONING TRANSDUCER INPUT ADCs

The AD7710, AD7711, AD7712, and AD7713 are the first members of a family of sigma-delta converters designed for high accuracy, low frequency measurements. They have no missing codes at 24-bits and useful resolution of up to 21.5-bits. They all use the same sigma-delta core, and their main differences are in their analog inputs, which are optimized for different transducers.

The digital filter in the sigma-delta core may be programmed by the user for output update rates between 10Hz and 1kHz. The resolution is inversely proportional to the bandwidth. For example, for 21.5-bits of effective resolution, the output update rate cannot exceed 10Hz. The AD771x family is ideal for such sensor applications as those shown in Figure 6.1.

SIGNAL CONDITIONING, TRANSDUCER INPUT ADCs: THE AD7710, AD7711, AD7712, AD7713

- Ultra-High Resolution Measurement Systems
- Implemented Using ΣΔ Conversion
- Ideal for Applications Such As:
  - Weigh Scales
  - RTDs
  - Thermocouples
  - Strain Gauges
  - Process Control
  - Smart Transmitters
  - Medical

Figure 6.1

The AD771x family has a high level of integration which simplifies the design of data acquisition systems. The AD7710 (Figures 6.2 and 6.3) has two high impedance differential inputs that can be interfaced directly to many different sensors, including resistive bridges. The two inputs are selected by the internal multiplexer, which passes the signal to a programmable gain amplifier. The PGA has a digitally programmable gain range of 1 to 128 to accommodate a wide range of signal inputs. After the PGA, the signal is digitized by the sigma-delta modulator. The digital filter may be adjusted from 10Hz to 1kHz which allows various input bandwidths. To achieve this high accuracy, the AD771x family has four different internal calibration modes, including system and background calibration. All of these functions are controlled via a microcontroller compatible serial interface. A benefit of this serial interface is that the AD771x fits into a 24-pin package, giving it a small footprint for its high level of integration. All of the parts except the AD7713 can operate on a single +5V or dual ±5V supplies. The AD7713 is designed for single supply (+5V) low power applications only. The AD771x family has <0.0015% non-linearity.

All four devices in the AD771x family have identical structures of PGA, sigma-delta modulator, and serial interface. Their main differences are in their input configurations. The AD7710 has two low level differential inputs, the AD7711 two low level differential inputs with excitation current sources which make it ideal for RTD applications, the AD7712 has one low level differential input and a single ended high level input that can accommodate signals of up to four times the reference voltage, and the AD7713 is designed for loop-powered applications where power dissipation is important, the AD7713 consuming only 3.5mW of power from a single +5V supply.

THE AD771X-SERIES PROVIDES A HIGH LEVEL OF INTEGRATION IN A 24-PIN PACKAGE

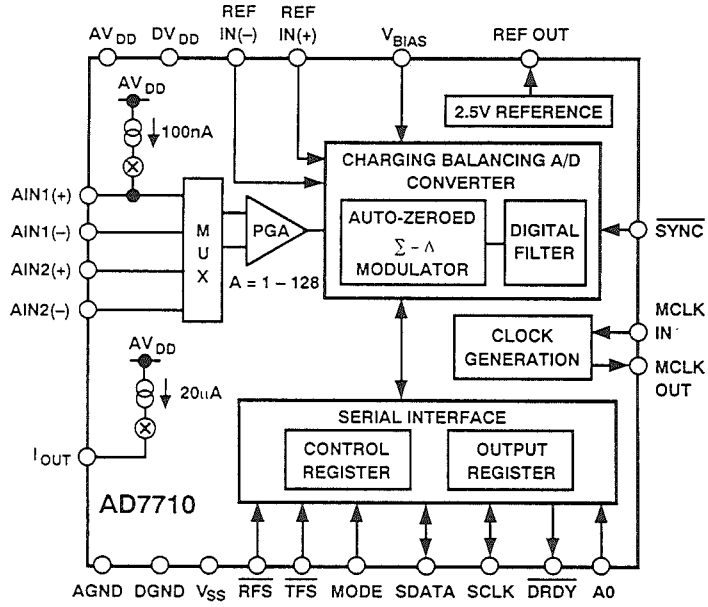


Figure 6.2

KEY FEATURES OF THE AD7710

- ±0.0015% Nonlinearity
- Two Channels with Differential Inputs
- Programmable Gain Amplifier (G = 1 to 128)
- Programmable Low Pass Filter
- System or Self-Calibration Option
- Single or Dual 5V Supply Operation
- Microcontroller Serial Interface

Figure 6.3

SUMMARY TABLE OF AD771X DIFFERENCES

- AD7710:
  - 2-Channel Low-Level Differential Inputs
- AD7711:
  - 1-Channel Low-Level Differential Input
  - 1-Channel Low-Level Single-Ended Input
  - Excitation Current Sources for 3 or 4-Wire RTDs
- AD7712:
  - 1-Channel Low-Level Differential Input
  - 1-Channel High-Level Single-Ended Input
- AD7713:
  - 2-Channel Low-Level Differential Inputs
  - 1-Channel High-Level Single-Ended Input
  - Excitation Current Sources for 3 or 4-Wire RTDs
  - Single 5V Operation Only
  - Low Power (3.5mW)
  - No Internal Reference

Figure 6.4

Because of the differences in analog interfaces each device is best suited to a particular sensor application. In other words, the sensor determines which converter should be used. Figure 6.5 lists the converters, and the sensors or applications to which they are best suited.

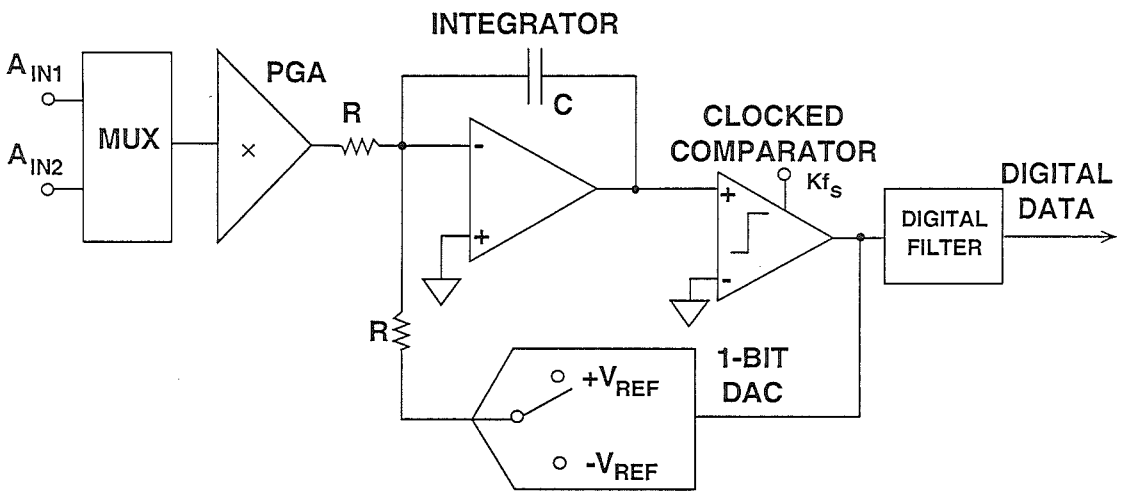
AD771X APPLICATIONS

- AD7710:
  - Weigh Scales
  - Thermocouples
  - Chromatography
  - Strain Gauge
- AD7711:
  - RTD Temperature Measurement
- AD7712:
  - Smart Transmitters
  - Process Control
- AD7713:
  - Loop-Powered Smart Transmitters
  - RTD Temperature Measurement
  - Process Control
  - Portable Instruments

Figure 6.5

Although the AD7710 is used as an example the following discussion applies to all the converters in the family (Figure 6.6). The modulator balances the signal input current to the integrator (derived from the input voltage applied to a resistor in the diagram, but quite often obtained by switched capacitor techniques in practical monolithic sigma-delta ADCs) with feedback current from the 1-bit DAC (a resistor and a changeover switch between $+V_{REF}$ & $-V_{REF}$) so that the net input current to the integrator, averaged over a long period, is zero. On each clock cycle the clocked comparator at the integrator output determines whether the output is above or below zero, and sets the DAC to bring the output back towards zero - the DAC only changes state on a clock.

THEORY OF OPERATION



Sigma-Delta Modulator Loop

Figure 6.6

The output is therefore a synchronous bit stream. If it is fed to a counter, rather than to a digital filter, and integrated for an accurately timed period, we have a classical charge-balance ADC (which is closely related to the VFC plus frequency counter ADC), but very long integration periods are required for high resolution.

The sigma-delta ADC is also a charge-balance device, but the digital filter in the bit stream looks at rates of change as well as absolute numbers of 0s and 1s and thereby yields a high resolution conversion with a wider signal bandwidth and a higher output data rate. Understanding of the detailed operation of a sigma-delta ADC involves considerations of oversampling, noise shaping, and decimation and the interested reader should refer Section 14 of this book and References 1 & 3.

Up to this point the PGA has been shown as separate from the modulator. In fact it is part of the integrator. The differential signal input charges C2, which is then discharged into the integrator summing node (Figure 6.7). This is done by closing S1 and S2, and then, after opening them, closing S3 and S4. When the PGA has a gain of 1 this happens once per cycle of the basic 19.5kHz clock, but for gains of 2, 4 and 8 respectively it happens 2, 4 or 8 times per cycle. The integrator charge is balanced by switching charge in the same way from the reference into C1 and thence to the integrator summing node. The polarity of reference switched depends on the state of the comparator output.

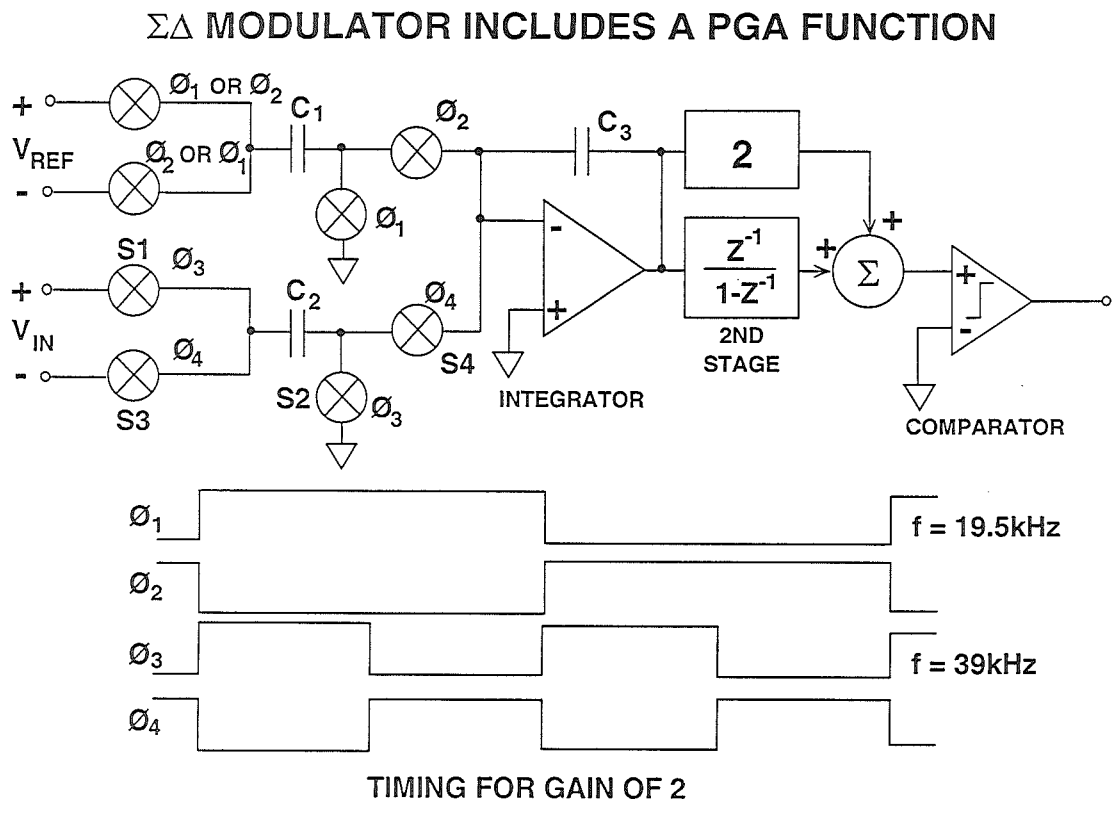


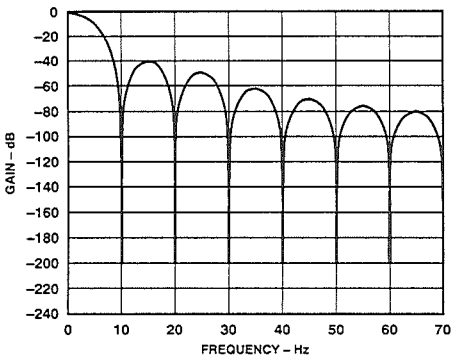
Figure 6.7

At a gain of 8 the sampling rate is 156kHz. Higher switching rates than this would not allow C2 sufficient time to charge, so for PGA gains greater than 8 the value of the reference capacitor, C1, is reduced, rather than the sampling rate being increased. Each time C1 is halved the gain of the system is doubled. The original value of C1 for gains of 1-8 is about 20pF, so for a gain of 16 it is 10pF and for a gain of 128 it is 1.25pF.

The digital filter has the $sinc^3$ response illustrated in Figure 6.8.The first notch in the filter response is programmable according to the formula:

$$f_{notch} = \left(\frac{f_{clkin}}{512}\right)\left(\frac{1}{\text{Decimal Value of Digital Code}}\right)$$

DIGITAL FILTER FREQUENCY RESPONSE



- Response Follows a $\text{sinc}^3 = \left(\frac{\sin x}{x}\right)^3$
- First Notch Frequency is Programmable and given by:

$$f_{notch} = \left(\frac{f_{clkin}}{512}\right)\left(\frac{1}{\text{Decimal Value of Digital Code}}\right)$$

- For f_{clkin} = 10MHz, 9.76Hz ≤ f_{notch} ≤ 1.028kHz

Figure 6.8

The notch frequency is 3.82 times the -3 dB frequency, so the notch frequency must be chosen so that the maximum signal frequency falls within the filter passband.

The lower the notch frequency the lower the noise bandwidth and therefore the higher the resolution of the converter. Moreover, the PGA gain will also set limits on the achievable resolution. With a 5V span 1 LSB in a 24-bit system is only 300nV - with a gain of 128 it is 2.3nV!

As is evident from their pipeline architecture, sigma-delta ADCs have a conversion time which is related to the bandwidth of the digital filter:- the narrower the bandwidth, the longer the conversion. For a 10Hz notch frequency the AD7710 has a 10Hz output data rate.

When the input to a sigma-delta ADC changes by a large step the entire digital filter must fill with the new data before the output becomes valid, which is a slow process. This is why sigma-delta ADCs are sometimes said to be unsuitable for multi-channel multiplexed systems - they are not, but the time taken to change channels can be inconvenient. In the case of the AD771X four conversions must take place after a channel change before the output data is again valid (Figure 6.9). The $\overline{\text{SYNC}}$ input pin resets the digital filter and, if it used, data is valid on the third output afterwards, saving one conversion cycle (when the internal multiplexer is switched the $\overline{\text{SYNC}}$ is automatically operated). The $\overline{\text{SYNC}}$ input also allows two AD771X ADCs to be synchronized.

THE RATE OF CONVERSION AND SETTLING TIME DEPENDS ON THE FILTER SETTING

	FILTER NOTCH FREQUENCY (Hz)								
	10	25	30	50	60	100	250	500	1k
CONVERSION TIME (ms)	100	40	33.3	20	16.7	10	4	2	1
MUX SWITCHING OR FULLSCALE WITH $\overline{\text{SYNC}}$, SETTLING TIME (ms)	300	120	100	60	50	30	12	6	3
ASYNCHRONOUS FULLSCALE SETTLING TIME (ms)	400	160	133.3	80	66.7	40	16	8	4

- Conversion Time = $\frac{1}{\text{Filter Notch Frequency}}$
- Digital Filter Requires Settling Time for Input Step Changes
- Use $\overline{\text{SYNC}}$ Input to Decrease Settling Time

Figure 6.9

Although the AD771X sigma-delta ADCs are 24-bit devices, it is not usually possible to obtain 24 bits of useful resolution, because noise limits the amount of useful data available. We thus confront the concept of "Effective Number of Bits" or ENOB. This is a measure of the useful signal-noise ratio of an ADC.

The full scale signal is the voltage difference between the most negative input the ADC will accept without overloading and the most positive one. The RMS noise is the amount that the output varies from conversion to conversion when a fixed input is applied to the ADC.

Noise may be generated by signal leakage and components (resistors and active devices) in the ADC. There is also intrinsic *quantization noise* which is inescapably linked to the analog-digital conversion process. Sigma-delta ADCs use special techniques to shape their quantization noise and thus reduce their oversampling ratio for a given ENOB, but they cannot eliminate quantization noise entirely. (Section 14 of this book and References 1 & 3)

DETERMINING EFFECTIVE RESOLUTION

- Effective Number of Bits (ENOB) = $\log_2\left(\frac{\text{Full Scale Signal}}{\text{RMS Noise}}\right)$
- Output RMS Noise = Effective Noise in the Digital Output Code
- ENOBs is Greatest at Low Filter Frequency and Low Gain

Figure 6.10

Figure 6.11 shows how RMS noise in an AD7710 varies with gain and notch frequency. Figure 6.12 gives the same results in terms of ENOB. Voltage noise drops with increasing sampling rate (remember that at gains of >8 the sample rate does not increase further) but rises, as we should expect, with increasing filter bandwidth. At higher bandwidths the dominant noise is the quantization noise, which occurs after the PGA and is therefore independent of gain. In general both noise and ENOB drop monotonically with increasing gain and increasing bandwidth (there is a small ENOB anomaly at 1kHz and gains between 2 and 32) but the drops are not linear for the reasons we have discussed: in some regions (e.g., 10Hz / gain = 1-8) ENOB does not vary much with gain, in others (e.g., 10-60 Hz / gain = 128) it does not vary much with bandwidth. In others it does vary with both.

NOISE VARIES AS A FUNCTION OF GAIN AND FILTER CUTOFF FREQUENCY

First Notch of Filter and O/P Data Rate	-3dB Frequency	Typical Output RMS Noise (μV)							
		Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
10 Hz	2.62 Hz	1.7	1.0	0.5	0.36	0.36	0.36	0.36	0.36
25 Hz	6.55 Hz	4.9	2.2	1.2	0.6	0.36	0.36	0.36	0.36
30 Hz	7.86 Hz	6.1	2.4	1.2	0.84	0.5	0.36	0.36	0.36
50 Hz	13.1 Hz	7.5	3.8	2.0	1.0	0.6	0.5	0.5	0.45
60 Hz	15.72 Hz	8.5	4.0	2.0	1.0	0.6	0.5	0.5	0.45
100 Hz	26.2 Hz	13	6.4	3.7	1.8	1.1	0.9	0.65	0.65
250 Hz	65.5 Hz	130	75	25	12	7.5	4	2.7	1.7
500 Hz	131 Hz	600	260	140	70	35	25	15	8
1 kHz	262 Hz	3100	1600	700	290	180	120	70	40

- Quantization noise arises from digitization. After PGA, so it is independent of gain.
- Device noise is determined by kT/C noise. Decreases for gains up to 8.

Figure 6.11

EFFECTIVE RESOLUTION VERSUS GAIN AND FIRST NOTCH FREQUENCY

First Notch of Filter and O/P Data Rate	-3dB Frequency	Effective Resolution (ENOBs)							
		Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
10 Hz	2.62 Hz	21.5	21.5	21.5	20.5	19.5	18.5	17.5	16.5
25 Hz	6.55 Hz	20	20	20	20	19.5	18.5	17.5	16.5
30 Hz	7.86 Hz	19.5	20	20	19.5	19.5	18.5	17.5	16.5
50 Hz	13.1 Hz	19.5	19.5	19.5	19.5	19	18.5	17.5	16.5
60 Hz	15.72 Hz	19	19.5	19.5	19.5	19	18.5	17.5	16.5
100 Hz	26.2 Hz	18.5	18.5	18.5	18.5	18	17.5	17	16
250 Hz	65.5 Hz	15	15	15.5	15.5	15.5	15.5	15	14.5
500 Hz	131 Hz	13	13	13	13	13	12.5	12.5	12.5
1 kHz	262 Hz	10.5	10.5	11	11	11	10.5	10	10

- $\text{ENOBs} = \log_2\left[\frac{2 \times V_{REF}}{\text{GAIN}} \bullet \frac{1}{\text{RMS NOISE}}\right]$
- Highest resolution occurs at low gains and low frequency

Figure 6.12

It is important to distinguish between RMS and peak-to-peak noise. Noise in a sigma-delta ADC has a gaussian (or near gaussian) distribution. This means that if you wait long enough any value of peak noise will eventually occur and it is not possible to write a specification *absolutely* prohibiting a specified value of noise peak. For practical purposes the peak-to-peak noise is defined as 6.6 times the RMS noise, since such peaks occur less than 0.1% of the time. The noise specified in the ENOB table in Figure 6.12 is expressed in RMS terms. If a figure for "noise-free" code is required it will be 3-bits worse: 20-bits ENOB becomes 17-bits noise-free code, etc. Since most applications are concerned with noise *power*, however, the RMS ENOB figure is the more commonly used.

This does not mean that the original 24-bit resolution is pointless, however. Additional filtering, to narrower bandwidths than the internal filter is capable of, can further improve the resolution and ENOB at the expense of very long conversion times.

ESTIMATING NOISE-FREE CODES

- Determined Using Peak-to-Peak Noise
- Output RMS Noise × 6.6 = Peak-to-Peak Noise
- Factor of 6.6 is Approximately Equal to 3 bits
- Subtract 3 bits from Effective Resolution Given in Figure 6.12 to Determine Noise Free Codes
- Further Digital Filtering Will Realize Figure 6.12 Values

Figure 6.13

The results in Figures 6.11 and 6.12 assume that the input and reference signals are noise free. Noisy inputs (and the reference is an input) reduce the effective resolution. For this reason, careful attention must be paid to external noise sources. Figure 6.14 lists aspects of board layout which may affect system noise and hence the ENOB of the AD7710. Many of these issues are discussed in detail in the 1992 Amplifier Applications Guide. If external amplifiers are used, low noise devices such as the OP-213 and AD797 should be chosen.

To determine if external amplifiers will lower the AD7710 system resolution,

the total additional noise (in the bandwidth 0.1 Hz to the cutoff frequency set in the AD7710) should be calculated and compared with the RMS noise figures given in Figure 6.11. (Uncorrelated noise adds by root sum of squares, so if the additional noise is <50% of the AD7710 noise it may be ignored, but if it exceeds this level its effect on system performance must be studied carefully.)

OPTIMIZING NOISE PERFORMANCE

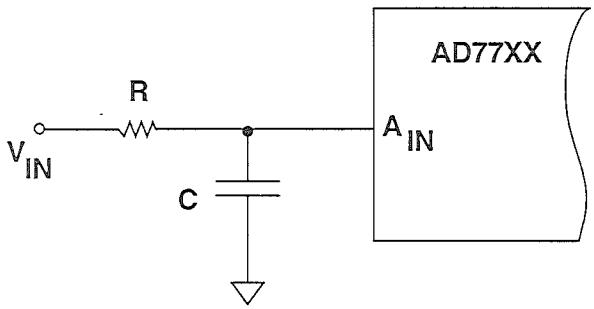
- Pay Attention to Layout!
- Use Ground Planes
- Keep Analog PCB Tracks Short
- Use Low Noise Amplifiers (AD797, OP-213, OP-177, AD707)
- Connect Analog and Digital Grounds of Converters Together at the Device and Connect them to Analog Ground
- Route Digital PCB Tracks Clear of Analog Tracks
- Filter Signal and Reference Inputs
- Minimize Reference Noise
- The Evaluation Board is an Example of Good Layout

Figure 6.14

An anti-aliasing filter on the input of the AD7710 will improve its noise performance because the modulator does not reject noise at integer multiples of the sampling frequency. (Figure 6.15) The internal analog front end does provide some filtering at these frequencies (the attenuation at 19.5kHz is approximately 70dB) but high level wideband noise can degrade system ENOB. A simple RC low-pass filter, ideally with a cut-off well below 19.5kHz, is generally sufficient, but the resistor must not be so large that it affects gain accuracy of the AD7710.

A simplified model of the analog input of the AD7710 is shown in Figure 6.16. It consists of a resistor of approximately 7kΩ connected to the input terminal and to an analog switch which switches an 11.5pF capacitor between the resistor and ground with a mark-space ratio of 50%. The switching frequency depends on f_{clkin} and the gain which is being used: with a gain of unity and the standard clock frequency of 10MHz the switching frequency is 19.5kHz, and at gains of 2, 4 and 8 or more it is 39, 78 and 156kHz respectively.

ANTIALIASING FILTER HELPS REDUCE NOISE



- Digital filter does not reject noise at integer multiples of f_S (n × 19.5kHz, where n = 1, 2, 3, . . .)
- RC Low Pass filter on the inputs prevents aliasing and limits noise
- Select R small enough to prevent gain error

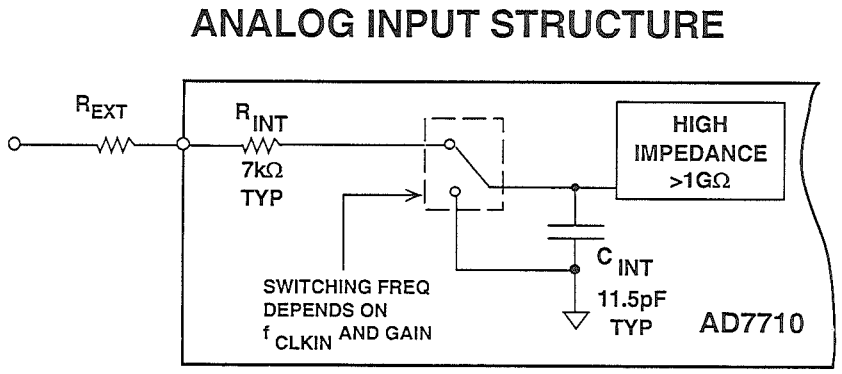
Figure 6.15

If the converter is working with an accuracy of 20-bits the capacitor must charge with an accuracy of 20-bits. The input RC time constant is 80ns. If the charge is to achieve 20-bit accuracy it must charge for at least 14× the time constant, or 1.13µs. Any external resistor in series with the input will increase the time constant, and the chart in Figure 6.16 shows acceptable values of series resistance necessary to maintain 20-bit performance.

To determine the minimum charge time for 20-bit performance with an external resistance R_{ext} we use the equation:

Minimum Charge Time = $14(R_{ext} + 7k\Omega) \times 11.5pF$

The minimum charge time must be less than half the period of the switching signal used (it has a 50% duty cycle). The fastest switching frequency with the standard 10MHz clock is 156kHz, and half of that clock period is 3.2 µs, which allows a maximum R_{ext} of 12.8 kΩ. At lower gains R_{ext} may be larger.



- R_{EXT} increases C_{INT} charge time and may result in gain error
- Charge time dependent on the input sampling rate and therefore gain
- Use following R_{EXT} values to maintain 20 bit accuracy:

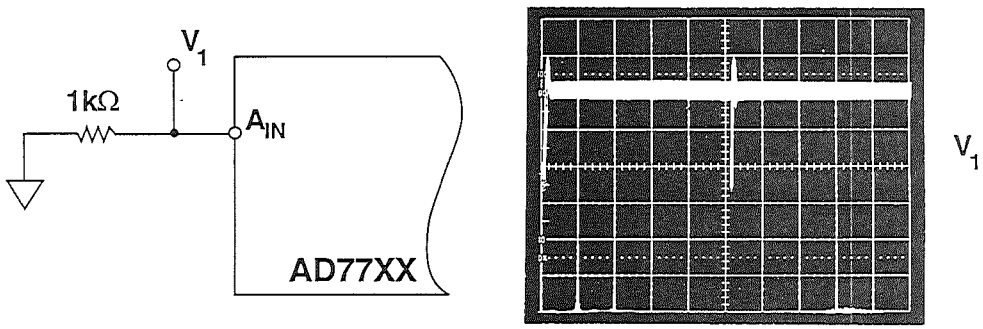
GAIN:	1	2	4	8-128
R_{EXT} :	<145kΩ	<70.5kΩ	<31.8kΩ	<13.4kΩ

Figure 6.16

It is not practical to use R_{ext} in conjunction with a capacitor to ground from the input pin of the AD7710 to make an anti-aliasing filter, unless the capacitor is dramatically larger than the 11.5pF C_{int}. This is because C_{int} is discharged on every sampling clock cycle and will recharge from the filter capacitor. Therefore, either the filter capacitor must be so large that charging C_{int} from it changes its voltage by less than an LSB at 20-bits (i.e. it is larger than 11.5μF), or the time constant $R_{ext}C_{ext}$ must be short enough for C_{ext} to recharge before the next clock cycle - in which case $R_{ext}C_{ext}$ does not make an anti-aliasing filter.

Some successive approximation and sub-ranging ADCs draw transient currents at their analog inputs which load their analog drive circuitry and cause errors. Often special drive amplifiers with low output impedance at the conversion clock frequency are necessary to avoid this problem, but these problems do not occur with the very small transient loads of the AD771X devices. The oscilloscope photograph in Figure 6.17 shows the transient current in an AD7710. It was taken with a 1kΩ resistor in series with the input to measure the change in current. This circuit produces a 15mV spike of less than 1μs duration. The peak pulse current is only 15μA, which permits the use of quite high impedance signal sources with no risk of degrading the ENOB.

INPUT TRANSIENT LOADING DOES NOT CAUSE CONVERSION ERRORS



VERTICAL SCALE: 5mV/div.
HORIZONTAL SCALE: 5μs/div.

- Transient settles quickly and does not affect conversion
- Inputs can accommodate high bridge resistances

Figure 6.17

The AD771x family was designed to simplify transducer interfacing. Many types of transducer can be connected directly to the input of one of the AD771x family without additional circuitry, but some care is necessary to achieve the best possible accuracy:- noise needs to be minimized (a simple capacitor across a resistive sensor may be all the filtering that is needed, but this must be checked - noise is particularly important because noise cannot be removed by the system calibration which eliminates gain and offset errors); transducer source impedance may affect charge times (as mentioned above); and bias currents flowing in high impedance transducers may cause errors, although these can be removed by system calibration. In general system calibration can remove most DC errors in systems using the AD771X family.

TRANSDUCER CONNECTION CONSIDERATIONS

- Filter Noisy Signals
- DC Leakage (bias) Current = 10pA can cause offset with R_{source}
- This causes drift over temperature
- To Maintain Accuracy:
  - Minimize R_{source}
  - Use differential inputs and balance R_{source}
  - Use system calibration

Figure 6.18

As discussed in Section 1, circuitry connected to transducers must generally be protected against over-voltage from ESD or noise pickup. If signals are likely to go outside the positive or negative supplies some form of clamp is necessary to keep them within them. Figure 6.19 shows a suitable circuit for protecting AD771X devices. The AD7710 has internal ESD protection diodes between the input and both supplies which conduct when the input exceeds either supply by more than about 0.6V. Excessive current in these diodes will vaporize metal tracks on the chip and damage the circuit, so an external resistor, R_p, is necessary to limit current to a safe 5mA during over-voltage events. R_p may be determined by a simple calculation:

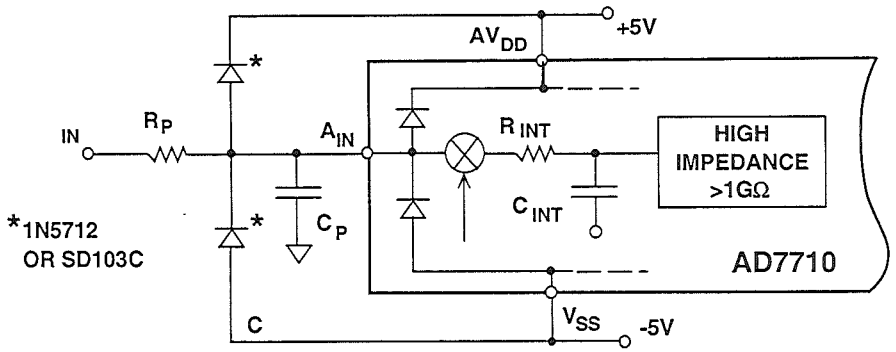
$$R_p = \frac{V_{max} - V_{supply}}{5\,mA}$$

R_p will contribute noise to the system (the basic Johnson noise equation applies:

$$e_n = \sqrt{4kTBR_p}$$

where k is Boltzmann's Constant, T is the absolute temperature and B is the bandwidth). If the noise due to R_p is too high, R_p can be reduced if external schottky diodes are used in addition to the diodes on the chip.

INPUT OVERVOLTAGE PROTECTION



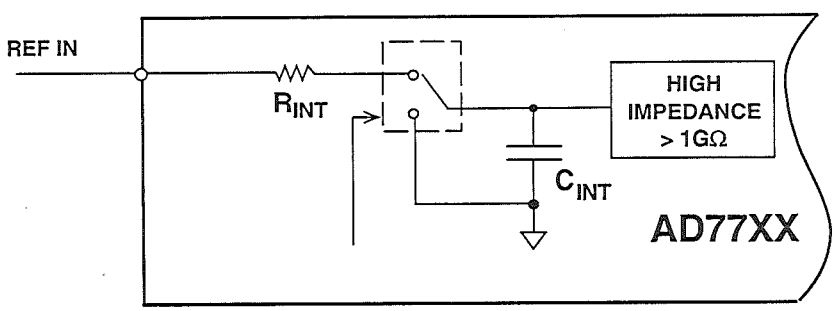
- Internal ESD protection diodes clamp input to within 0.6V of either supply.
- Limit current due to overvoltage to less than 5mA.

$$R_P = \frac{A_{inmax} - AV_{DD}}{5mA}, \text{ or } \frac{|A_{inmin}| - |V_{SS}|}{5mA}, \text{ whichever is greater.}$$

- External Schottkys can be added to reduce the size of R_P.
- Include C_P to filter noise due to R_P.

Figure 6.19

REFERENCE VOLTAGE CONSIDERATIONS



PGA GAIN	1	2	4	8	16	32	64	128
C_{INT} (pF)	20	20	20	20	10	5	2.5	1.25

- Antialiasing filter needed if reference is noisy
- Minimal transient load is similar to analog input

Figure 6.20

There are no special requirements for these schottky diodes, as long as they have low leakage current and can handle the necessary fault current levels while maintaining a low turn-on voltage.

As important as the analog signal input is the reference input. Figure 6.20 shows a simplified model of the reference input, which is very similar to that of the analog input. The series resistor is 5kΩ and the value of the capacitor depends on the gain setting. For gains of 1-8 the capacitor is 20pF. Above 8 the capacitor's value is halved for each doubling of gain.

An important consideration in choosing a reference for the AD7710 is noise. Many references have output noise which exceeds that of the AD7710 and causes reduced accuracy. Filtering will help in such cases but a low noise reference should be selected wherever possible.

The AD7710 has an internal 2.5V reference, which may be connected to its positive reference input. This internal reference is more than adequate for use in applications with filter cut-off frequencies above 60Hz but at the higher resolution of the lower settings, where reference noise becomes critical, its noise of (typically) 50μV pk-pk (8.3μV rms) in the 0.1 to 10Hz bandwidth is too high.

If the noise is 8.3μV (rms) in a 10Hz bandwidth it is 3.4μV in the 2.62Hz bandwidth associated with a 10Hz update rate. Since the AD7710 has an effective noise of 1.7μV rms this reference noise will increase the effective noise to 3.8μV rms and reduce the ENOB from 21.5 to 20.5. A low noise external reference is evidently necessary to improve resolution. (Actual measurements show that the degradation, though real, is a little less than this, but a better reference is still necessary.)

INTERNAL REFERENCE VOLTAGE NOISE CONSIDERATIONS

- Specified Output Noise = 8.3μV rms typical (0.1 to 10Hz)

  = 3.4μV rms (0.1 to 2.62Hz, for 10Hz Output Rate)

- Noise adds to device noise shown in Figure 6.11

  AD7710 Noise = 1.7μV rms (G = +1)

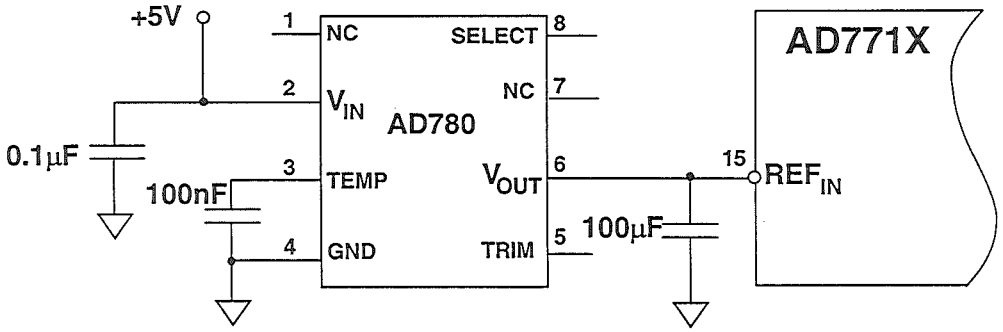
  $$\text{Total Noise} = \sqrt{(1.7\mu V)^2 + (3.4\mu V)^2} = 3.8\mu V \text{ rms, or } 25\mu V\ p-p$$

- This reduces ENOB from 21.5 to 20.5 bits

Figure 6.21

The AD780 2.5V reference has noise of 670nV rms in the range 0.1 to 10Hz. This gives 0.35μV rms noise in the 2.62Hz bandwidth associated with a 10Hz update rate, which is negligible compared to the noise of the AD7710. With output rates of 1kHz or more, and cutoff frequency of 262Hz, the noise of the AD780 may be reduced by 50% if a 100μF capacitor is connected to its output (unlike many IC voltage references the AD780 is stable with all values of capacitive load).

USE A LOW NOISE EXTERNAL REFERENCE FOR OPTIMUM RESOLUTION



- AD780 has 215nV/√Hz noise at 1Hz
- Total noise for AD771X Notch Frequency of 10Hz:

  RMS Noise = (215nV/√Hz) √2.62Hz = 0.35μVrms
- Well below noise of AD771X

Figure 6.22

DC errors also affect conversion accuracy, but AD771X devices can calibrate themselves to correct DC errors. Every member of the family has four different calibration modes. These are summarized in Figure 6.23 and comprise Self Calibration, System Calibration, System-Offset Calibration, and Background Calibration. Each calibration cycle contains two conversions, one each for zero-scale and for full-scale calibration.

AD771X OFFERS 4 CALIBRATION OPTIONS

	SELF-CALIBRATION	SYSTEM CALIBRATION	SYSTEM OFFSET CALIBRATION	BACKGROUND CALIBRATION
1st Cycle	Internally Short Inputs to Ground	Externally Short Inputs to Ground (Zero-Scale)	Externally Short Inputs to Zero-Scale	Internally Short Inputs to Ground
2nd Cycle	Internally Short Input to V_{REF}	Externally Short Input to Fullscale	Calibrate for Span from AV_{IN} to V_{REF}	Internally Short Inputs to V_{REF}
Duration	9 ÷ Output Rate	4 ÷ Output Rate Each Step	9 ÷ Output Rate	6 ÷ Output Rate

Figure 6.23

To initiate a calibration cycle the appropriate code must be sent to the control register. After the code is sent, the AD7710 automatically conducts the entire operation, and clears the control register of the calibration command so that a separate command to stop calibration is not necessary. Since the filter in the sigma-delta converter must purge itself of its previous result for four output update cycles whenever the input sees a full-scale step the total calibration operation takes nine such cycles.

Self Calibration removes errors in an AD771X by connecting the input to ground and performing a conversion, and then connecting the input to Vref and performing another. The results of these conversions are used to calibrate the device.

Background Calibration is a variation of Self Calibration. The only difference is that when an AD771X is placed in Background Calibration mode, it continually calibrates itself at regular intervals without further instructions. This ensures that the AD771X remains calibrated regardless of drift. The Background Calibration cycle alternates calibration conversions with signal conversions: zero calibrate/ convert signal/full-scale calibrate/ convert signal/zero calibrate/etc. This provides continuous calibration but reduces the output data rate by a factor of six.

System Calibration is intended to calibrate all the elements prior to the ADC which may contribute to system errors, as well as the ADC itself. (For example an instrumentation amplifier

introduces errors into a system due to its own offset, drift and gain error. These errors can be removed by System Calibration.) However, System Calibration requires additional analog switches to connect *system* inputs to ground and a reference as well as to the original signal source. The first step in System Calibration requires external grounding of the system input terminal to calibrate out offsets. The second step requires that the input be connected to a reference, which calibrates gain error at full-scale. The System Calibration cycle requires the sending of two separate instructions to the control register as well as control of the analog switches at the system input. It must be repeated regularly to correct for drift with time and temperature.

The final calibration mode is System-Offset Calibration. This calibrates *system* offsets, and *the AD771X* gain. Again, it requires external analog switches at the system input, and separate instructions for zero and gain calibration. For the first cycle, the system input is connected to ground and the AD771X calibrates for system offsets. During the second cycle, the ADC input is connected to the reference for ADC gain calibration.

CALIBRATION ISSUES

- Always calibrate on power-up!
- Background calibration sequence: (Zero-Scale, Convert, Fullscale, Convert, Zero-Scale, Convert, . . .)

  This reduces the data rate by a factor of 6.
- $\overline{\text{DRDY}}$ signals when calibration cycle is complete by going low.
- $\overline{\text{DRDY}}$ may already be low if a conversion is taking place.

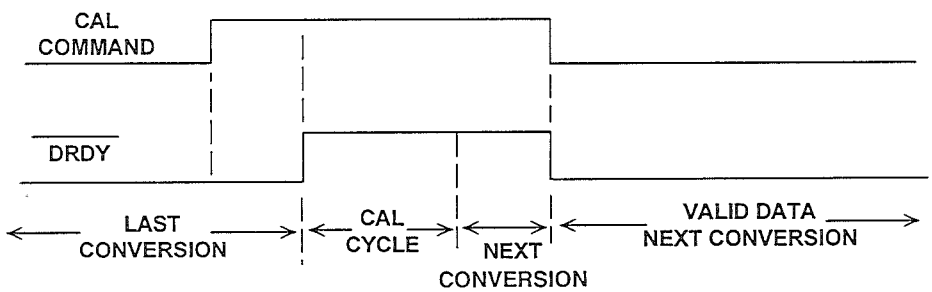


Figure 6.24

When calibration is complete $\overline{\text{DRDY}}$ goes low - but it does not necessarily go high as soon as the calibration command is sent to the ADC, there may be a delay of up to one output data cycle before it does so. Controllers should therefore look for a 0→1 transition, rather than the presence of a 0, on $\overline{\text{DRDY}}$ to signal the completion of a calibration after it has been commanded.

Calibration is crucial to achieving the rated accuracy of AD771X devices and

should be performed immediately after power-up and repeated regularly. A 2.5μV/°C temperature coefficient of input offset and a 2°C temperature change causes an lsb of error in a 20-bit 5V system. Any reference drift adds to the error. Frequent calibration ensures that temperature changes do not degrade the accuracy of conversions.

CALIBRATE OFTEN TO MAINTAIN ACCURACY

- Temperature Drift can cause errors
- Unipolar offset drift of 5μV is

  1 LSB in a 20 bit system (5V fullscale)
- Reference voltage drift adds to this error
- Therefore, to minimize drift errors, calibrate often.

Figure 6.25

When the AD7710 executes a calibration cycle, it saves two coefficients in internal registers. One register stores the full scale calibration coefficient, FSC, and the other stores the zero scale calibration coefficient, ZSC. Adjusting the calibration coefficients manually may be useful in some applications. For example, in a weigh scale application it may be necessary to insert an offset to account for a fixed weight. It is possible to read from and write to the calibration registers of members of the AD771X family, making adjustment of calibration coefficients a trivial task. (Figure 6.26)

MANUALLY ADJUSTING CALIBRATION COEFFICIENTS

- Perform a Self-Calibration Cycle for Desired Gain and Filter Settings
- Read Calibration Coefficients from Register
- Calculate New Coefficients Using Formulas in Figure 6.27
- Use Different Formula for Bipolar Case
- Write New Coefficients Back into Calibration Registers
- Reading and Writing to the Calibration Registers is Controlled by Operating Mode Bits, MD0 - MD2

Figure 6.26

The equations for adjusting calibration coefficients are given in Figure 6.27. The terms used are defined in Figure 6.28. The equations use the old calibration coefficients, the old data, and the desired new data. Before calculating new coefficients, a self calibration cycle should be performed at the gain and filter settings to be used to ensure that the old internal coefficients are current. To calculate the new full scale calibration coefficient, FSC_{NEW} the old full scale calibration coefficient, FSC_{OLD} must first be read from the register. Its value is multiplied by the ratio of the required full scale range to the old full scale range. The FSC is a gain coefficient. The formula to calculate the new zero scale calibration coefficient, ZSC_{NEW} is a little more complex, but the calculation is still straightforward and again based on the old coefficient, ZSC_{OLD} - plus the old data and the desired new data. Using these two simple formulas, the system software can quickly determine new calibration coefficients for a particular application, which may then be written into the calibration registers to replace the old coefficients. Reading and writing data in the calibration registers is controlled by the operating mode bits, MDO-MD2, in the control register.

CALCULATING CALIBRATION COEFFICIENTS

- $$FSC_{NEW} = FSC_{OLD}\left(\frac{FSR_{NEW} - ZSR_{NEW}}{FSR_{OLD} - ZSR_{OLD}}\right)$$
- Unipolar:

$$ZSC_{NEW} = ZSC_{OLD} - \left(\frac{ZSR_{NEW} \cdot FSR_{OLD} - ZSR_{OLD} \cdot FSR_{NEW}}{\frac{FSC_{OLD}}{2^{21}}(FSR_{NEW} - ZSR_{NEW})}\right)$$

- Bipolar:

$$ZSC_{NEW} = ZSC_{OLD} - \left(\frac{ZSR_{NEW} \cdot FSR_{OLD} - ZSR_{OLD} \cdot FSR_{NEW}}{\frac{FSC_{OLD}}{2^{20}}(FSR_{NEW} - ZSR_{NEW})}\right)$$

Figure 6.27

CALIBRATION COEFFICIENT TERMS DEFINED:

- FSC_{NEW} = New Fullscale Calibration Coefficient, Load into Register
- FSC_{OLD} = Old Fullscale Calibration Coefficient, Read from Register
- ZSC_{NEW} = New Zero Scale Calibration Coefficient, Load into Register
- ZSC_{OLD} = Old Zero Scale Calibration Coefficient, Read from Register
- FSR_{NEW} = New, Desired Fullscale Output Reading (Code)
- FSR_{OLD} = Old Fullscale Output Reading (Code)
- ZSR_{NEW} = New, Desired Zero Scale Output Reading (Code)
- ZSR_{OLD} = Old Zero Scale Output Reading (Code)

Figure 6.28

A typical application of the AD7710 is in a weigh scale (Figure 6.29). These generally use a resistive bridge as their sensing element and require resolution of at least 16-bits and often more. The AD7710 dramatically simplifies the design of such a system: the bridge is connected directly to its differential inputs, making an external instrumentation amplifier unnecessary. The excitation for the bridge, and the reference for the AD7710, are provided by an AD780, whose low noise helps to preserve the system ENOB. Because the system bandwidth is limited (both by the conversion rate selected and the filter capacitors on the bridge) the ENOB achievable is quite high (≈ 20-bits) but the conversion (and output data) rate is rather low at 10Hz.

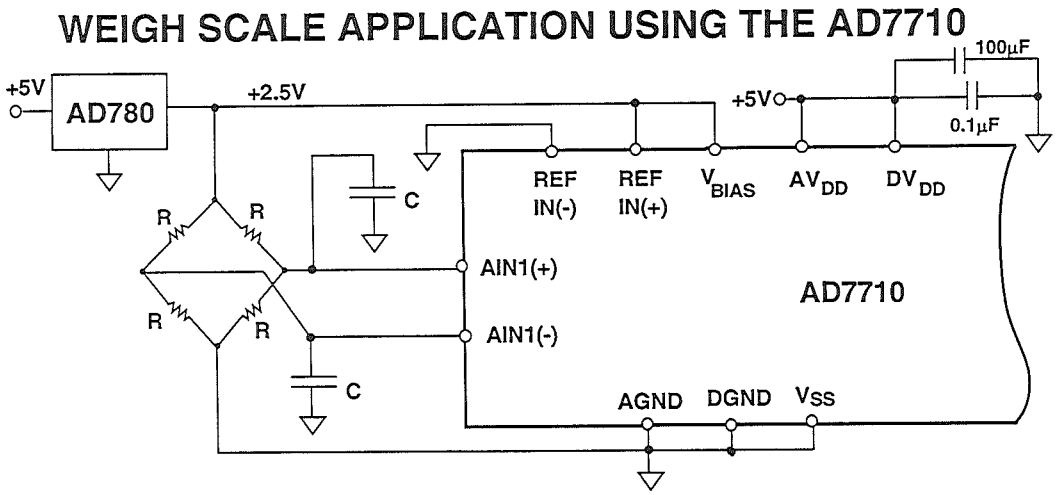


Figure 6.29

The converters in the AD771x family all have the same serial interface, which is described in detail in the data sheet. They have a 24-bit control register that controls all their operations. Changing the PGA gain, starting a calibration, and changing the filter parameters are all accomplished by writing a 24-bit word to this register. On the other hand, data can be read either as a 16-bit or a 24-bit operation - one of the bits in the control register controls the size of the data word. The $\overline{\text{DRDY}}$ output indicates when a conversion is complete and valid data is available in the output register.

The output register is continually updated as new conversion take place, and if the data is not read it is overwritten by new data. However, if a conver-

sion finishes while data is being read from the output register, the new conversion results are lost. The benefit of this feature is that the data can be read slowly without any danger of its being corrupted by new conversion results. In fact, until all bits have been read from the output register, no new conversion results will appear, so a controller can read 8-bits from the register, service an unrelated interrupt, and return to read the remaining word of data without it being corrupted by the results of new conversions.

SERIAL INTERFACE ISSUES

- Configurable for 16 or 24 bit Read mode
- $\overline{\text{DRDY}}$ low indicates valid data in Output Registers
- $\overline{\text{DRDY}}$ stays low until data read is complete
- Continually updates output register if no read occurs
- During slow read, new data is lost
- Must complete read or toggle A0 for output register to be updated
- SCLK can run as slow as desired, remembering above
- Need to write all 24 bits to control register

Figure 6.30

Figure 6.31 shows an isolated 4-wire interface to the AD7713 using common opto-isolators. Over 6kV of isolation is possible. The $\overline{\text{TFS}}$, A0, and $\overline{\text{SYNC}}$ lines are tied together at the converter to minimize the number of control lines. Tying $\overline{\text{TFS}}$ to AO causes a write to the device to load data to the control register, and any read accesses the data register. The only restrictions of this method of control is that the controller cannot write to the calibration registers and cannot read from the control register. In many applications these capabilities are unnecessary. Four opto-isolators carry data and instructions from the controller to the ADC and a fifth, with a 74HC125 on each side of the isolation barrier, carries data to the controller. The AD7713 is ideal for this particular application because its low supply current minimizes the load on the isolated power supply.

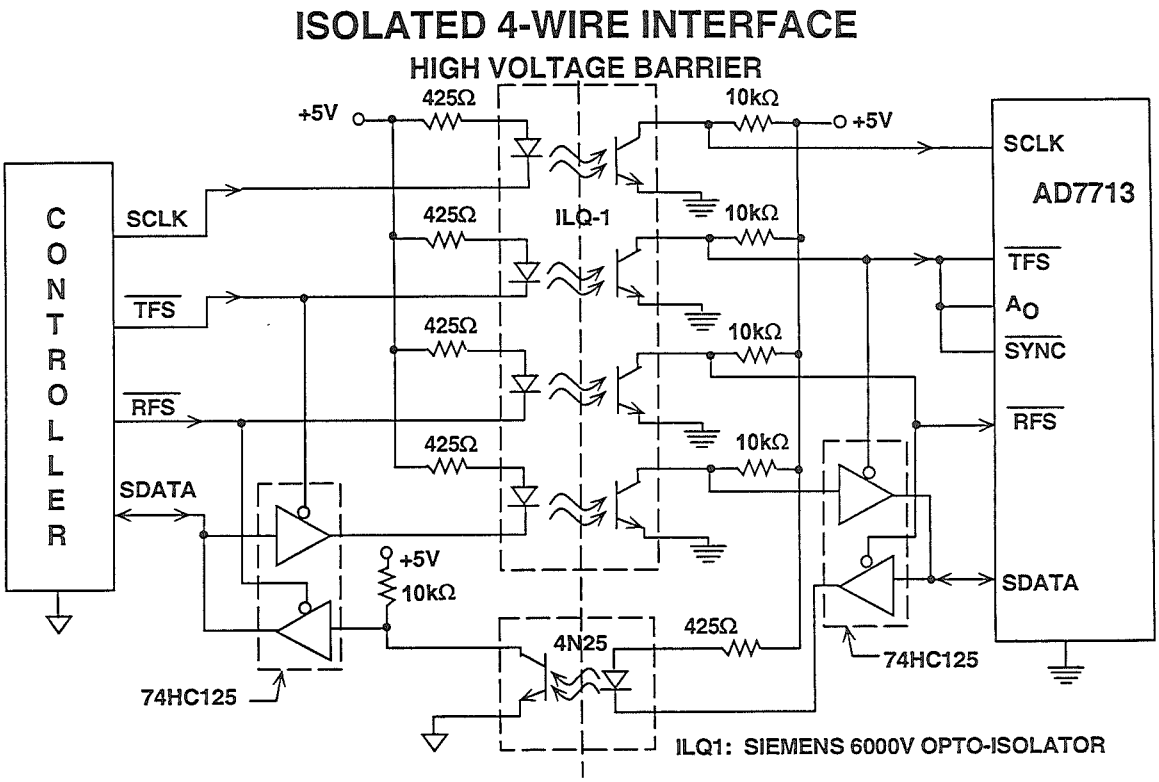


Figure 6.31

The AD771X family generally interfaces with some type of microprocessor. Their data sheet includes circuits and microcode for interfacing to the 8051 microcontroller and the ADSP-2105 DSP processor. Figure 6.32 shows how they may be interfaced to the 68HC11 microcontroller, and the code is included at the end of this section. The SPI serial port of the 68HC11 handles the sending and receiving of data to the AD771X, and pins PCO through PC3 control the different logic inputs. The 68HC11 should be configured in the master mode, as is explained in the assembly code at the end of this section.

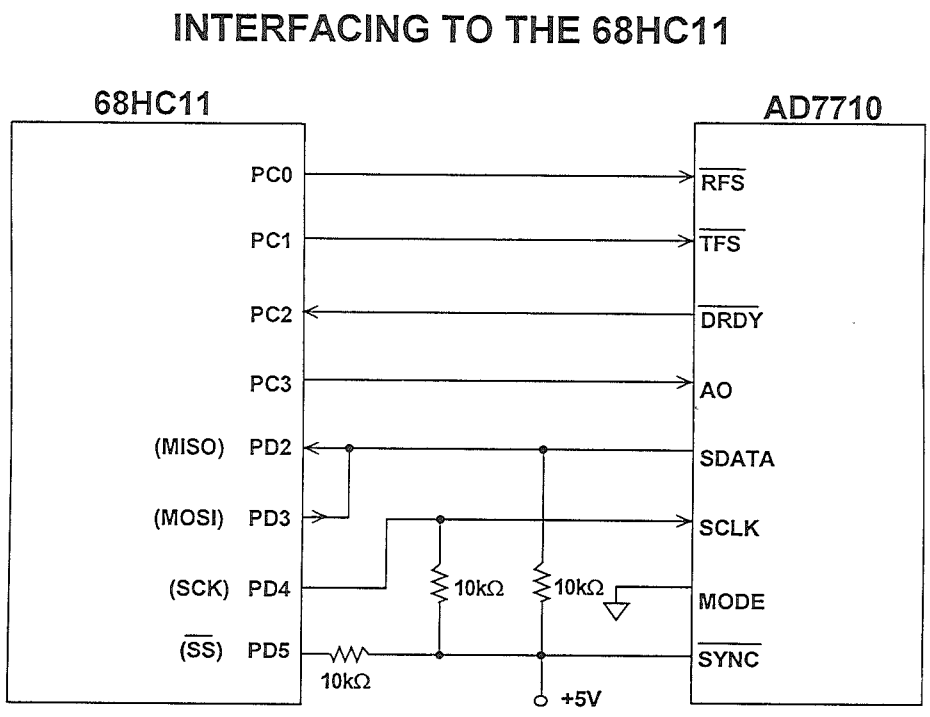


Figure 6.32

The AD771X sigma-delta converters are powerful tools for building high accuracy systems. Every one of them combines high resolution, system calibration, a programmable gain amplifier, and high impedance differential inputs with great ease of design. Their adjustable digital filters provides flexibility in the choice of data rates and resolution and their serial interface minimizes their pin count, so that they fit in a 24-pin skinny DIP package, providing a high degree of functionality in a small space.

MICROCODE FOR READING AND WRITING TO THE AD771X FAMILY FROM THE 68HC11 MICROCONTROLLER

```
* This program contains subroutines to read and write
* to the AD7710 family of ADCs from the 68HC11
* microcontroller.  These subroutines were developed for the
* 68HC11 Evaluation board, which is where the references to BUFFALO
* come from, in conjunction with the AD7710 Evaluation board.
* The following connections need to be made.
*  68HC11      AD7710
*  PC0         RFS
*  PC1         TFS
*  PC2         DRDY
*  PC3         A0
*  PD2,PD3     SDATA      10K pull-up resistor
*                         PD2 and PD3 attached together
*  PD4         SCLK       10K pull-up
*  PD5                    10K pull-up, no connection to AD7710
*
portc  equ   $1003
portd  equ   $1008
ddrd   equ   $1009
spcr   equ   $1028
spsr   equ   $1029
spdr   equ   $102a
ddrc   equ   $1007
*
```

```
        org   $C000
read    lds   #$CFFF   subroutine to read from the AD771X
*
        ldaa  #$fb     initialize port c ouputs:  11111011
        staa  ddrc     Set up drdy as input (PC2) and
*                      A0, RFS, TFS (PC3,PC0,PC1) as outputs
        ldaa  #$30     00110000
        staa  ddrd     MOSI is low for input,
*                      MISO is high, SCK as output
*
        ldaa  #$37     00110111
        staa  spcr     SPI system off, resets itself
*
        ldaa  #$77     01110111
        staa  spcr     Interrupts disabled, SPI system on,
*                      DWOM mode, 68hc11 is master,
*                      CPOL 0, CPHA 1, SCK=ECK/32
*
        ldy   #$1000
        bset  portc,y  $03   TFS and RFS set high
*
        bset  portc,y  $08   A0 high to read data
*                            set A0 low to read control reg.
*
        ldaa  spsr     Initial dummy read to clear port
        ldaa  spdr     and SPIF
*
        ldab  #$03     b counts to 0 when read finished
        ldx   #$00     x points to memory location where
*                      the data is stored. (24 bits wide)
*
pause   ldaa  #$04
        anda  portc
        bne   pause    Wait until DRDY is low
*
        bclr  portc,y  $01  Clear RFS for read
*
go1     staa  spdr     Start SCK
wait1   ldaa  spsr
        bpl   wait1    wait until SPIF flag is clear
        ldaa  spdr     and then read.
        staa  0,x      And then put in memory
*
        decb
        beq   fin1     if b=0 then finished reading
        inx            increment memory location for next byte
        jmp   go1
*
fin1    bset  portc,y  $09  set RFS and A0
*
        jmp   $e000    Return to BUFFALO
```

```
write   lds   #$cfff   subroutine to write to AD771X
        ldaa  #$fb
        staa  ddrc     Set up drdy as input (PC2) and
*                      A0, RFS, TFS (PC3,PC0,PC1) as outputs
        ldaa  #$37
        staa  spcr     SPI system off, resets itself
*
        ldaa  #$73
        staa  spcr     Interrupts disabled, SPI system on,
*                      DWOM mode, 68hc11 is master,
*                      CPOL=0, CPHA=0, SCK=ECK/32
        ldaa  #$38
        staa  ddrd     MOSI is high for output,
*                      MISO is low, SCK is high

        ldy   #$1000
        bset  portc,y  $03   Set TFS and RFS
*
        bclr  portc,y  $08   Set A0 low to write
*                            to control register
*
        ldab  #$03     b is 0 when write finished
        ldx   #$00     x points to memory location of
*                      start of 24 bit to be written
*
        bclr  portc,y  $02  clear TFS
*
go2     ldaa  0,x
        staa  spdr     write byte to serial port
*
wait2   ldaa  spsr
        bpl   wait2    wait until SPIF flag is clear
*
        decb
        beq   fin2     if b=0 then finished
        inx            points to memory location of next byte
        jmp   go2
*
fin2    bset  portc,y  $0a    set TFS and A0
*
        jmp   $e000    Return to BUFFALO
```

SINGLE SUPPLY ADCs

Single supply ADCs are an important type of Analog to Digital Converter. There are many systems where only one power supply is available, and it is convenient if the converters in the system can be run from that supply, rather than necessitating special, additional, power supplies. Single supply circuits are most commonly found in portable, battery powered devices, but do have many other applications. In the past, analog integrated circuits for complete single supply data acquisition systems were not available and designers were forced either to provide a second supply or work with artificial center rails or other ground substitutes. Today, however, ADI has a complete range of suitable analog integrated circuits, including ADCs, DACs, op amps and instrumentation amplifiers, that operate from a single supply. Single supply ADCs are generally either Sigma-Delta or Successive Approximation types.

SINGLE SUPPLY ADCs

- Often Required in Portable/Battery Powered Applications
- Simplify Power Supply Requirements
- Single Supply ADCs are Usually Either ΣΔ or SAR Type
- Have Reduced Input Signal Range
- What About 3V Operation?

Figure 6.33

Whenever single supply circuitry is used, the input signal range is reduced, and frequently halved. If a negative supply is unavailable signals within the circuit cannot drop below ground potential (inputs, under some circumstances, can do so). The dynamic range is thereby reduced and careful circuit design is necessary to ensure that accuracy is not lost.

Battery technology often dictates the supply possibilities in portable systems. The designer must choose the battery type and the number of cells, but his choices are limited. Despite this there are sufficient possibilities that single supply ICs may have to work over a wide range of supply voltages. In the past single supply systems have generally operated in the +5V to +12V range but today there is a growing demand for +3V operation. Analog ICs operating at +3V are still quite scarce, but ADI does offer ADCs, DACs and amplifiers that are fully characterized for +3V operation.

A comprehensive range of single supply ADCs is available from ADI, with a wide variety of accuracies and speeds. (Figure 6.34) The AD771X family, which we have just discussed, employs sigma-delta techniques in a high accuracy, single supply converter. Other devices, such as the AD1878/79 and AD1848/49 were designed for computer audio applications. In a computer there is almost always a single +5V supply, and frequently +12V or ±12V supplies are available as well. However, all of these supplies are extremely noisy, due to the digital environment. For any analog circuitry in the computer the noisy +12V supply is often reduced to +5V and heavily filtered to provide a noise-free analog supply. So the AD1878/9 and the AD1848/9 operate from a single +5V supply to provide high performance, high resolution audio A-D and D-A conversions. The AD7880 and AD789X converters are 12-bit high speed converters which operate from a single +5V supply, and the AD7883 is a 12-bit converter designed to operate from a +3V supply. There are also numerous 8 and 10-bit converters.

ADI OFFERS A WIDE SELECTION OF SINGLE SUPPLY ADCs

PART #	RESOLUTION (BITS)	SUPPLY RANGE (V)	THROUGHPUT (SAMPLES/SEC)	DIGITAL INTERFACE	COMMENTS
AD7710	21	+5 to +10	10 - 1,000	Serial	ΣΔ
AD7711	21	+5 to +10	10 - 1,000	Serial	ΣΔ
AD7712	21	+5 to +10	10 - 1,000	Serial	ΣΔ
AD7713	21	+5 to +10	2 - 200	Serial	ΣΔ
AD1879	18	+5	48,000	Serial	Stereo Audio ΣΔ
AD1878	16	+5	48,000	Serial	Stereo Audio ΣΔ
AD1848	16	+5	5,500 - 48,000	Parallel	Stereo ΣΔ Audio Codec
AD1849	16	+5	5,500 - 48,000	Serial	Stereo ΣΔ Audio Codec
AD776	16	+5	100,000	Serial	ΣΔ
AD7880	12	+5	66,000	Parallel	
AD7890	12	+5	100,000	Serial	8 - Channel
AD7891	12	+5	100,000	Parallel	8 - Channel
AD7892	12	+5	100,000	Parallel	
AD7893	12	+5	100,000	Serial	8-Pin Package
AD7883	12	+3 to +3.6	50,000	Parallel	Lowest Supply Voltage

Figure 6.34

An important consideration in the design of a single supply data acquisition system is the input range of the converter. Ideally, the input range should be as wide as possible to maximize the dynamic range of the system. ADCs operating from dual supplies frequently have a bipolar input signal range:- the input is symmetrical about ground. However, in single supply circuits the input range is often limited to positive signals. To achieve the same resolution the magnitude of an lsb must be halved. For example a dual supply 16-bit converter with ±5 V inputs an LSB is $2^{-16} \times 10V$ or 153μV, while a single supply converter with an input range of 0-5V has an lsb of 76μV and

any errors such as DC offset, non-linearity, or noise must be halved to maintain resolution. High performance single supply amplifiers are necessary to do this:-the OP-213 offers extremely low drift and low noise; in addition to excellent DC accuracy, the OP-295 has a rail-to-rail output swing, which increases the dynamic range; the AD820 combines a rail-to-rail output with an FET input, making it an excellent amplifier for high impedance signal sources; and the OP-90/290/490 family are DC precision amplifiers that operate with only 10μA of supply current per amplifier.

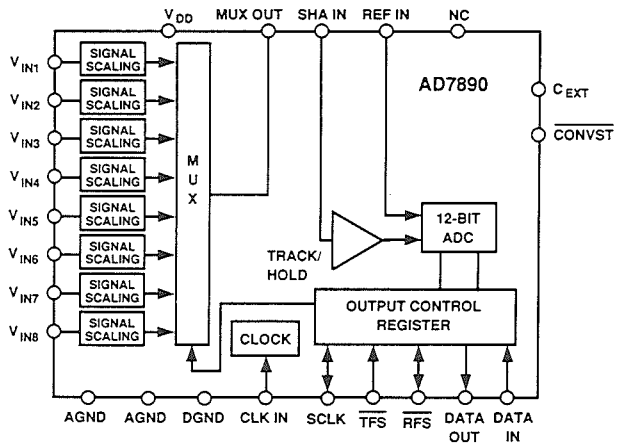
SINGLE SUPPLY ADC INPUT RANGE MAY BE LIMITED BY THE SUPPLY VOLTAGE

- Input Range Often Limited to the Supply Voltage
- For a +5V Supply, Input Range = 5V
- Smaller Input Ranges Reduce the Size of the LSB
- More Attention Needs to be Given to Input Errors
- If an Input Amplifier is Needed, Use a Single-Supply Op Amp Such as the OP-213, OP-295, AD820, or OP-90

Figure 6.35

The AD789x family of ADCs (Figure 6.36) achieves a signal span outside its supply by using thin film resistors in the input stages to attenuate the input signal by a factor of 8. These converters accept inputs of ±10V despite operating from a single +5V supply. The actual input range for the internal sample and hold amplifier and ADC is 0-2.5 V at the "SHA IN" pin and the internal ADC is no different from many other 5V ADCs, but the attenuator (signal scaling) network allows much higher input signals. External resistors can be employed with any ADC to reduce the signal range to the range of the converter; but by including accurate, thin film resistors on chip, the AD789x family ensures 12-bit accuracy and simplifies external circuit design. Not only does the input scaling attenuate the signal, it also attenuates any external errors by the same ratio, maintaining a constant signal to noise ratio.

AD789X-FAMILY UTILIZES INPUT SCALING FOR WIDE INPUT RANGE



- Thin Film Resistors on Input Allow ±10V Inputs
- Internal Signal to ADC is 0 to +2.5V
- Input Scaling Also Attenuates Such Input Errors as Noise and Offset

Figure 6.36

The most common reference for single supply ADCs is +2.5V, but +3V is also used. To be compatible with the ADC the reference must also operate from a single +5V supply (most 2.5V references meet this requirement, including the AD780 which can supply +2.5V or +3V). The reference chosen must meet the current and transient specifications of the ADC reference input. Of the single supply ADCs listed in this section of the seminar, the sigma-delta converters have the simplest reference requirements. The main considerations are the noise and accuracy, not the drive capabilities.

REFERENCES FOR SINGLE SUPPLY ADCs

- Most Single Supply ADCs Require a +2.5V Reference
- The Reference Must Operate With a Single +5V Supply
- As With All ADCs, Consider the Reference Voltage Drive Requirements
- 2.5V References from ADI:

  AD580, AD680, AD780, REF-03, REF-43

Figure 6.37

Digital ICs that operate from +3V are increasingly common. This creates a demand for analog circuits which will operate from the same supplies. ADCs which operate from +3V are still scarce, but are becoming more common. The AD7883 is a +3V 50kSPS successive approximation ADC with an integral track and hold amplifier (Figure 6.38 and 6.39). Its input range is V_{REF} or $\pm V_{REF}$ and it will operate with +2.5 or +3V references, but as it draws less than 3mA from its supply it is often operated with a common +3V supply to V_{DD} and reference inputs. It has also a *power saving* mode where it consumes less than 1mW. A suitable op-amp to use with the AD7883 is the OP-295 with its rail-to-rail output swing and guaranteed specifications at 3V.

THE AD7883 12-BIT, 50kSPS ADC GUARANTEES 3V OPERATION

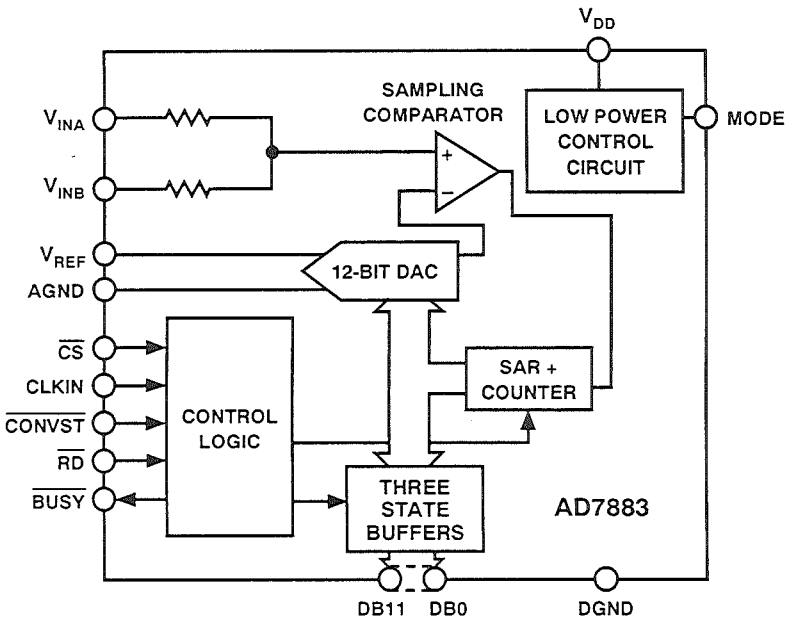


Figure 6.38

AD7883 12-BIT, 50kSPS, 3V ADC KEY FEATURES

- Guaranteed Specifications for 3V to 3.6V Supply Voltage
- 12-Bit SAR Converter
- 50kSPS Throughput Rate
- On-Chip SHA
- DC and AC Specifications
- Low Power: 8mW Typical, 1mW in Power Save Mode
- 24-Pin SOIC Package
- Bipolar or Unipolar Inputs

Figure 6.39

The block diagram of a +3V four channel data acquisition system (DAS) is shown in Figure 6.40. The ADG511 and ADG512 quad CMOS analog switches are fully specified for +3V operation. They are ideal for use in battery-powered instruments as their power requirement is only 3μW and their signal range includes their supply rails. Their leakage currents are typically 50pA, and Ron <200Ω.

FOUR-CHANNEL, SINGLE-SUPPLY (+3V) DATA ACQUISITION SYSTEM

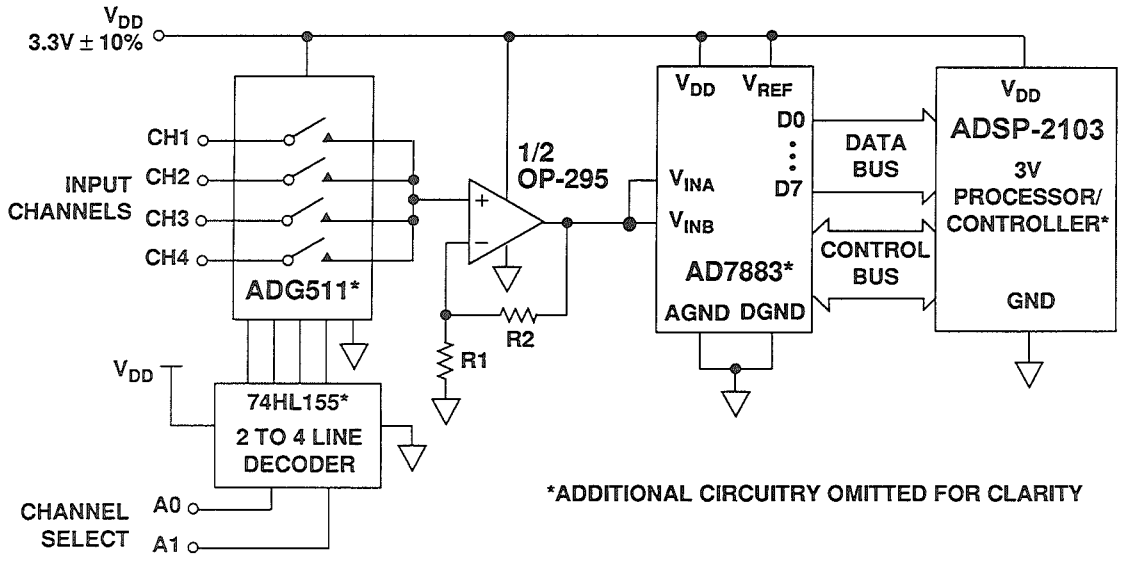


Figure 6.40

The input multiplexer comprises an ADG511 quad analog switch and a 74HL155 two-to-four line decoder. The digital inputs A0 and A1 select the input channel. The signal on the input channel is amplified by an OP-295, used in the non-inverting mode with a gain of [1 + R2/R1], and the amplifier output drives the AD7883, which performs the 12-bit A-D conversion. Figure 6.40 shows the same +3V used for both the supply and the reference, but a 2.5V reference could equally well be used if it is available. (A 2.5V reference could be provided from a 3V supply by using two AD589 two-terminal 1.235V references in series with 250Ω or by using one AD589 in series with 1kΩ and a buffer amplifier with a gain of 2 made from half of an OP-295 and two 10kΩ resistors.)

The gain resistors, R1 and R2, should be chosen to amplify the input signal sufficiently to use the entire dynamic range of the ADC - but without clipping.

The overall bandwidth of the system is limited by the op amp:- the multiplexer and the ADC have much higher bandwidths. Many low-power amplifiers have limited bandwidths and slew rates

and the OP-295 is typical. When powered with +3V its slew rate is only 0.03V/μs, its full-power bandwidth is about 3.8kHz, and its small-signal gain-bandwidth product is only 75kHz. As many transducers have very limited bandwidths the 3.8kHz full-power bandwidth is rarely an important limitation.

For wider bandwidth applications, the single-supply AD820 op-amp may be suitable. It has an FET input stage and a slew rate of 3V/μs, a full power bandwidth of about 380kHz and a gain bandwidth-product of 1.5MHz.

Figure 6.41 shows the results of an evaluation of the circuit. An FFT shows that with an input of 1.11kHz and an amplitude of 2.2V pk-pk, and a sampling rate of 61.44kSPS, the signal/(noise plus distortion) ratio was 67dB over the 30.7kHz Nyquist bandwidth and the THD was -72dBc.

SINGLE-SUPPLY DATA ACQUISITION SYSTEM
FFT OUTPUT FOR 1.11kHZ INPUT SAMPLED
AT 61.44kSPS YIELDS SNR OF 67dB

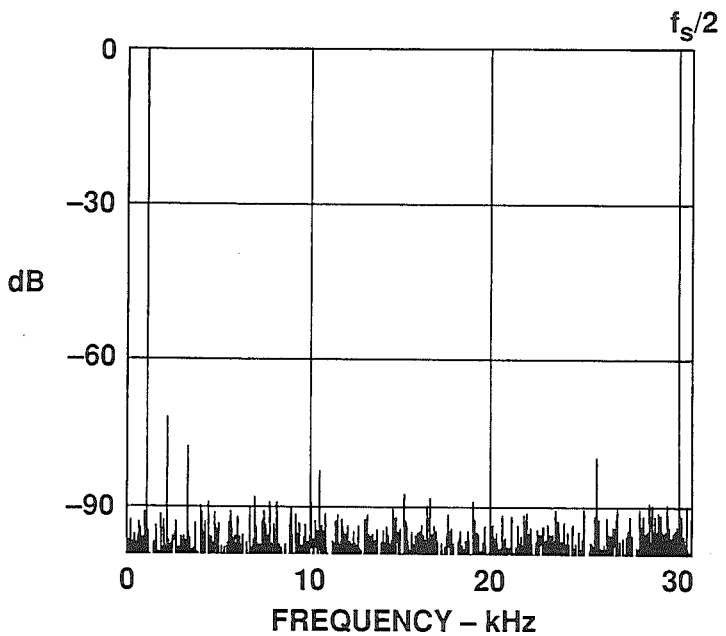


Figure 6.41

SERIAL OUTPUT ADCs

ADCs with a serial, rather than a parallel, interface are valuable when board space is limited, because their packages have fewer pins, and are therefore smaller, and because fewer PC tracks and fewer components are required to interface with them. Both sigma-delta and successive approximation ADCs produce serial data during the conversion process, and may be said to be inherently serial. The AD771X family of 24-bit sigma-delta ADCs provides a clear example of the benefits of serial interfaces:- despite their high resolution and complex functionality they are supplied in small 24 pin packages.

Of course intrinsically serial conversions are not always convenient, since the output data rate may be set by the conversion process and not by system requirements. It is often necessary to have complex logic in an inherently serial ADC with a serial output in order to alter the output data rate, to prevent update during readout, or to perform other necessary housekeeping functions.

Despite their advantages of size and convenience, there is no doubt that serial interfaces are slower than parallel ones, and in the fastest ADCs (which are usually flash or subranging types, which have a more parallel type of architecture) only a parallel interface will be fast enough. The system designer must make the final choice between simplicity and small size, and speed.

SERIAL OUTPUT ADCs SAVE BOARD SPACE

- Reduce Pin Count to Save Board Space
- Reduces the Amount of PC Tracks to Save More Space
- Cause Less Digital Noise
- ΣΔ and SAR Architectures are Inherently Serial
- Reading From Serial ADCs Requires Multiple Clock Cycles so is Slower

Figure 6.42

Figure 6.43 shows the wide selection of serial ADCs available from ADI. They range from 12-bits of effective resolution to 21 or more. They are all smaller than the corresponding parallel parts (if they exist). The ADC-170 and the AD7893 are conspicuously smaller, being 12-bit ADCs in 8 pin packages.

ADI OFFERS NUMEROUS SERIAL ADCs

PART #	RESOLUTION (BITS)	THROUGHPUT (SAMPLES/SEC)	NUMBER OF PINS	SUPPLY VOLTAGE (V)	COMMENTS
AD7710	21	10 - 1,000	24	+5	ΣΔ
AD7711	21	10 - 1,000	24	+5	ΣΔ
AD7712	21	10 - 1,000	24	+5	ΣΔ
AD7713	21	10 - 1,000	24	+5	ΣΔ
AD7703	20	4,000	20	±5	ΣΔ
AD7701	16	4,000	20	±5	ΣΔ
AD1879	18	48,000	28	+5	Stereo ΣΔ Audio
AD1878	16	48,000	28	+5	Stereo ΣΔ Audio
AD1849	16	5,500 - 48,000	44	+5	Stereo ΣΔ Audio Codec
AD1876	16	100,000	16	±12	Sampling ADC
AD677	16	100,000	16	±12	Switched Capacitor
AD776	16	100,000	20	+5	ΣΔ
AD7872	14	83,000	16	±5	Complete SAR
AD7890	12	100,000	24	+5	8 - Channel
AD7893	12	100,000	8	+5	Small Package
ADC-170	12	175,000	8	+5, -12	Small Package

Figure 6.43

COMPLETE DATA ACQUISITION SYSTEMS ON A CHIP

VLSI mixed-signal processing allows the integration of large and complex data acquisition circuits on a single chip. Most signal conditioning circuits including multiplexers, filters, PGAs and SHAs, may now be manufactured on the same chip as the ADC. This high level of integration permits data acquisition systems to be specified and tested as a single complex function.

ADVANTAGES OF AN INTEGRATED SOLUTION TO DATA ACQUISITION

- Built-In Signal Conditioning and ADC
- Multiple Input Channels with Multiplexer
- All System Errors are Characterized
- System Calibration is Easily Performed Internally or Externally
- Reduced Component Count

Figure 6.44

INTEGRATED DATA ACQUISITION SYSTEMS ARE USUALLY PROGRAMMABLE

- Gain Adjustment
- Filter Characteristic Adjustment
- Input Channel Selection

Figure 6.45

Such functionality relieves the designer of most of the burden of testing and calculating error budgets. The DC and AC characteristics of a complete data acquisition system are specified as a complete function, which removes the necessity of calculating performance from a collection of individual worst case device specifications. A complete monolithic system should achieve a higher performance at much lower cost than would be possible with a system built up from discrete functions. Furthermore, system calibration is easier and in fact many monolithic DASs are self calibrating.

With these high levels of integration, it is both easy and inexpensive to make many of the parameters of the device programmable. Parameters which can be programmed include gain, filter cutoff frequency, and even ADC resolution and conversion time, as well as the obvious digital/MUX functions of input channel selection, output data format, and unipolar/bipolar range.

The AD7890 is an example of a highly integrated monolithic data acquisition system. It has 8 multiplexed input channels with scaling, a SHA amplifier, an internal voltage reference, and a fast 12-bit ADC. Its block diagram is shown in Figure 6.46 and key specifications are summarized in Figure 6.47. Both AC and DC parameters are fully specified, simplifying the preparation of an error budget, and three types are available with three different standard input ranges:-

AD7890-10	±10 V
AD7890-5	0 to 5V
AD7890-2	0 to +2.5V

THE AD7890 12-BIT, 8-CHANNEL SAMPLING ADC WITH SERIAL OUTPUTS

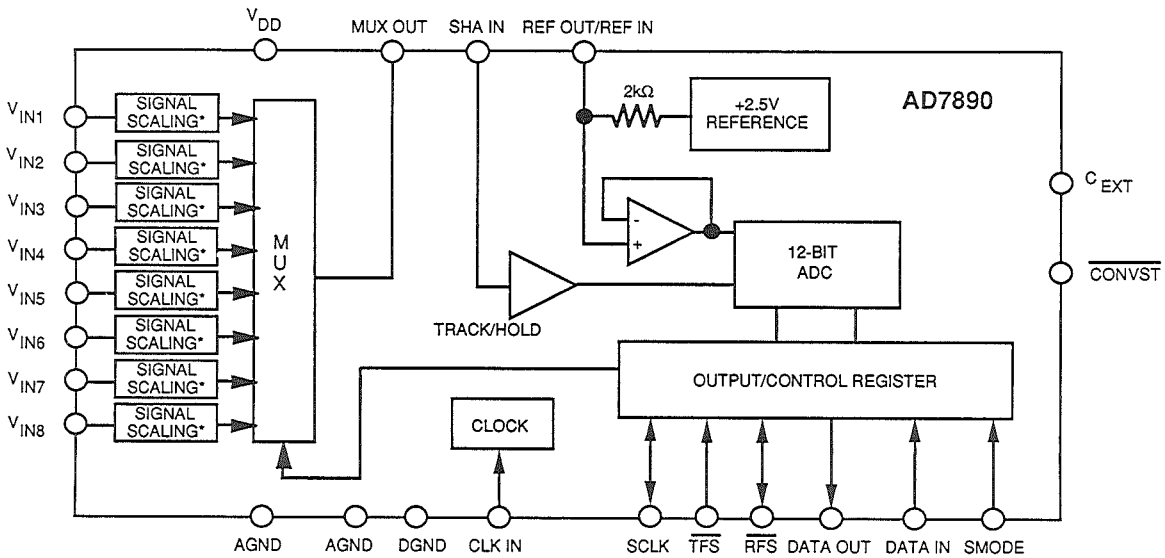


Figure 6.46

AD7890 SPECIFICATIONS

- ADC Conversion Time: 5µs
- SHA Acquisition Time: 2µs
- 100kSPS Throughput Rate
- AC and DC Specifications
- Single +5V Operation
- Low Power Drain:
  - Operational: 30mW
  - Power Down Mode: 1mW
- Standard Input Ranges:
  - AD7890 - 10: ± 10V
  - AD7890 - 5: 0 to +5V
  - AD7890 - 2: 0 to +2.5V

Figure 6.47

The input channel selection is via a serial input port. A total of 5 bits of data control the AD7890 via a serial port:- 3 address bits select the input channel, a CONV bit starts the A-D conversion, and 1 in the STBY register places the device in a power-down mode where its power consumption is under 1mW. All timing takes place on the chip and a single external capacitor controls the acquisition time of the internal track-and-hold. A-D conversion may also be initiated externally using the $\overline{\text{CONVST}}$ pin.

The AD7890 acquires a signal in under 2µs, and completes its 12-bit conversion in under 5µs. This allows a 100kSPS conversion. The AD7890 draws 30mW from a +5V supply.

A single channel version of the AD7890 data-acquisition system having similar performance, and available in an 8-pin DIP (dual-in-line) package is known as the AD7893. Its functional block diagram is shown in Figure 6.48 and its similar performance characteristics are listed in Figure 6.49.

AD7893, A SINGLE-CHANNEL VERSION OF THE AD7890 IN AN 8-PIN PACKAGE

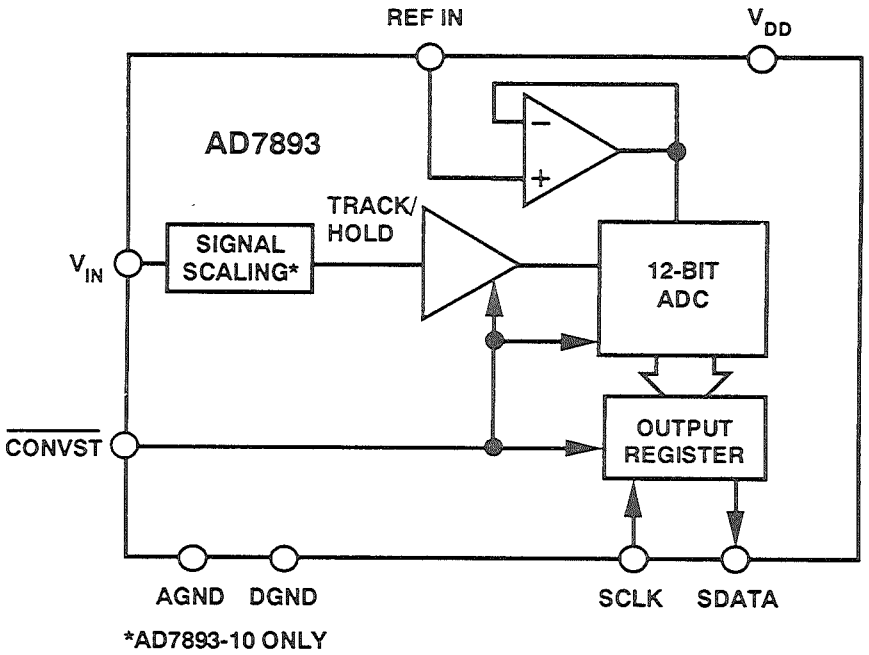


Figure 6.48

KEY FEATURES OF THE AD7893

- Conversion Time: 6µs
- SHA Acquisition Time: 1.5µs
- 117kSPS Throughput Rate
- Complete AC and DC Specifications
- Single +5V Supply Operation
- Low Power Drain: 30mW
- Small 8-Pin Minidip or SOIC Package

Figure 6.49

Another useful circuit which may be made with monolithic mixed signal VLSI technology is an analog I/0 (Input/ Output) port, which contains A-D and D-A converters on a single chip. The AD7869 is a good example. It comprises a 14-bit sampling ADC (i.e. with a SHA) and a 14-bit DAC together with an integral reference. Both ADC and DAC have update rates of up to 83kSPS. The AD7869 has a 12-bit version, the AD7868.

THE AD7869 14-BIT ANALOG I/O PORT

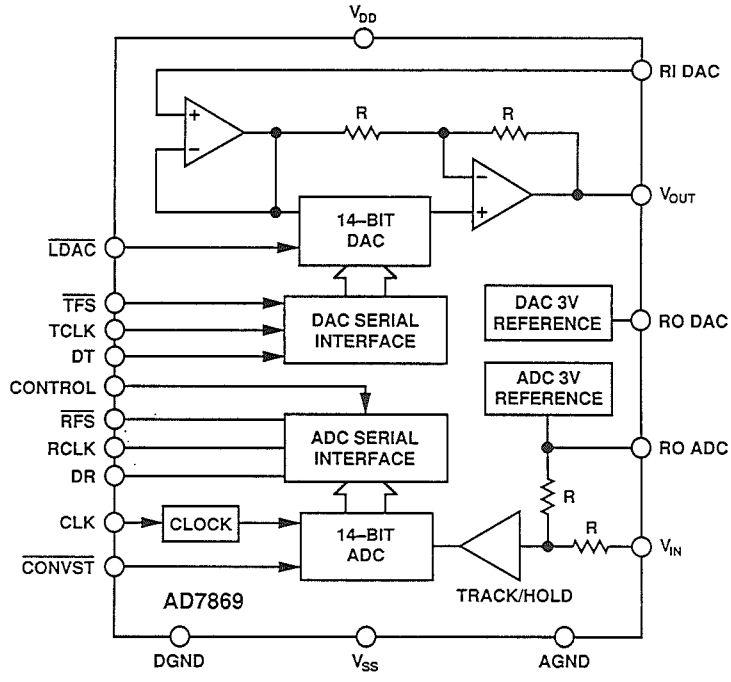


Figure 6.50

AD7869 I/O PORT KEY FEATURES

- 14-Bit ADC with SHA, 83kSPS Throughput Rate
- 14-Bit DAC with On-Chip Output Amplifier, 3.5µs Settling Time
- ± 5V Supply Operation
- Fully Specified for SNR and THD

Figure 6.51

The highest resolution monolithic DAS circuits available today have resolutions of well over 20-bits. The AD7716 is a quad sigma-delta ADC with 22-bit resolution and an over-sampling rate of 570kSPS. A functional diagram of the AD7716 is shown in Figure 6.52 and some of its key features in Figure 6.53. The device does not have a "start conversion" control input but samples continuously. The cutoff frequency of the digital filters (which may be changed during operation, but only at the cost of a loss of valid data for a short time while the filters clear) is programmed by data written to the DAS. The output register is updated at a rate which depends on the cutoff frequency chosen. The AD7716 contains an auto-zeroing system to minimize input offset drift.

AD7716 22-BIT QUAD SIGMA-DELTA ADC

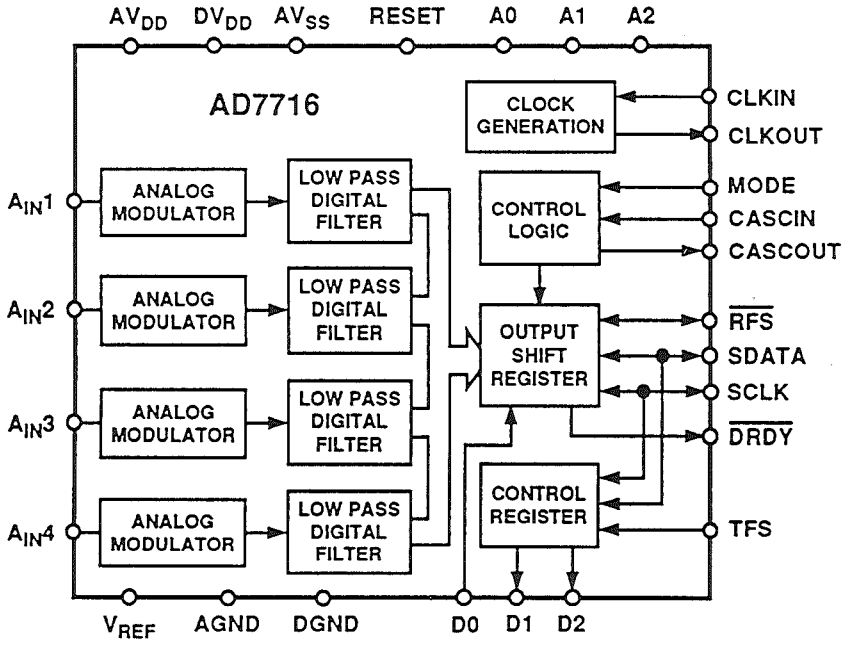


Figure 6.52

AD7716 QUAD SIGMA-DELTA ADC KEY FEATURES

- 22-Bit Resolution, 4 Input Channels
- ΣΔ Architecture, 570kSPS Oversampling Rate
- On-Chip Lowpass Filter, Programmable from 36.5Hz to 584Hz
- Serial Input / Output Interface
- ±5V Power Supply Operation
- Low Power: 50mW

Figure 6.53

REFERENCES

1. **Mixed Signal Design Seminar**, Analog Devices, 1991, Section 6.

2. **1992 Amplifier Applications Guide**, Analog Devices, 1992, Section 11

3. "A Non-Mathematical Introduction to SIGMA-DELTA ADCs" by James Bryant. Analog Devices Ltd., Walton-on-Thames, England. 1993