SECTION 4

HIGH ACCURACY SAMPLE AND HOLD CIRCUITRY

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James Wong

The "sample and hold" amplifier or SHA is a critical part of many data acquisition systems. It captures an analog signal and holds it during some operation (most commonly analog-digital conversion). The circuitry involved is demanding, and unexpected properties of commonplace components such as capacitors and printed circuit boards may degrade SHA performance.

In the past the commonest application of a SHA was to maintain the input to an ADC at a constant value during conversion (with many, but not all, types of ADC the input may not change by more than 1 LSB during conversion lest the process be corrupted - this either sets very low input frequency limits on such ADCs, or requires that they be used with a SHA to hold the input during each conversion). Today, high density IC processes allow the manufacture of ADCs containing an integral SHA. Wherever possible such ADCs with integral SHA (often known as *sampling* ADCs) should be used in preference to separate ADCs and SHAs. The advantage of such a sampling ADC, apart from the obvious ones of smaller size, lower cost and fewer external components, is that the overall performance is specified and the designer need not spend time ensuring that there are no specification, interface or timing issues involved in combining a discrete ADC and a discrete SHA.

While both AC and DC specifications are important in determining the accuracy of a SHA, the AC specifications are generally the most difficult to achieve. The dynamic behavior, and typical dynamic imperfections, of a SHA are shown in Figure 4.2.

SAMPLE-AND-HOLDS ARE DEMANDING CIRCUITS

- Where Possible use ADCs with Built-In SHAs (Sampling ADCs)
- Understand SHA Parameters
- Select the Hold Capacitor Carefully
- Take Great Care with Board Layout

Figure 4.1

KEY SHA DYNAMIC PERFORMANCE CHARACTERISTICS

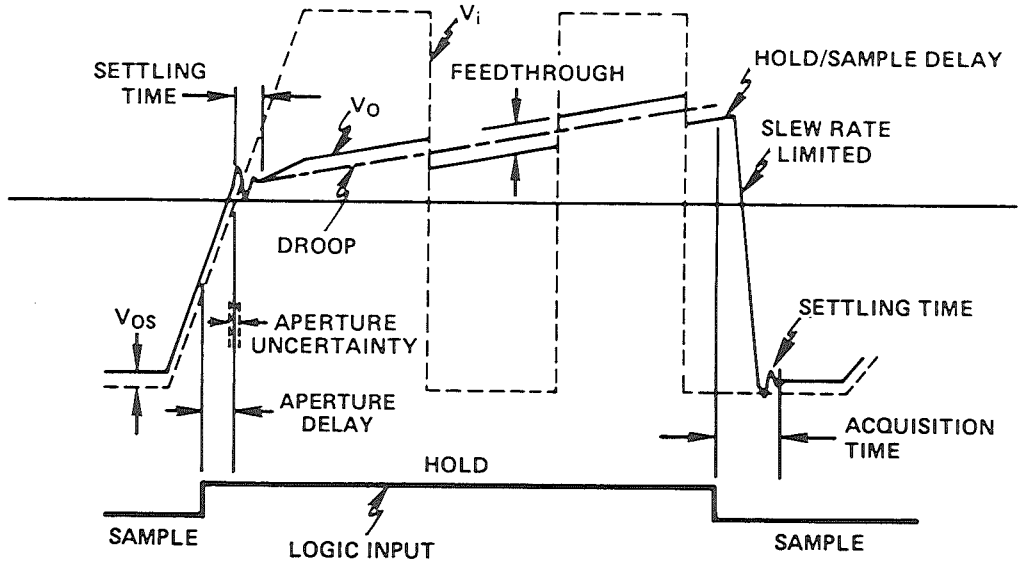


Figure 4.2

The input signal is illustrated as a dotted line and the SHA output as a solid line. When the sample/hold control is in sample mode the output follows the input with only a small voltage offset. (There do exist SHAs where the output during "sample" does not follow the input accurately and the output is only accurate during the "hold" period - these are uncommon and will not be considered here. Strictly speaking a sample and hold with good tracking performance should be referred to as a "track and hold" circuit, but in practice the terms are used interchangeably.)

Ideally, when the "hold" signal is asserted the SHA output is locked at its value at the instant of assertion. In practice there is a delay, known as the aperture time, before the hold command takes effect, and there is an uncertainty, which varies from sample to sample, in the exact value of the aperture time - this is known as the aperture jitter. In a sampled data system it may be demonstrated that phase noise, or jitter, on the sampling clock is a major cause of loss of system resolution (Reference I). In early sampled data systems the major cause of sampling clock jitter was the aperture jitter of the SHA in the system - today SHA performance has improved and other sources of jitter (noisy clocks, digital interference, etc.) are at least equally important.

Switching to hold disturbs the system. There will be a short interval, known as the settling time, while it settles down to its proper value again. Settling time is defined as the delay between the hold edge and the SHA returning within *and remaining within* some error band. Different SHAs have widely different settling times, but for a given SHA the settling time will be longer if a tight error band is chosen.

Ideally the output of a SHA immediately before and immediately after the hold transition should be identical. In practice the transients generated by the sample-hold transition inject a small amount of charge into the capacitor which stores the signal and produce an offset between the sample and hold states. This offset is called the *pedestal.* In some SHAs the pedestal amplitude varies with signal and is a source of non-linearity.

Almost all SHAs use a capacitor to store the voltage which is being "remembered". If a leakage current flows in or out of this capacitor it will slowly charge or discharge, and its voltage will change. This effect is known as "droop" in the SHA output. Droop can be caused by leakage across a dirty PCB if an external capacitor is used, or by a leaky capacitor, but is most usually due to leakage current in semiconductor switches and the bias current of amplifiers connected to the capacitor. Droop is expressed in V/μS. An acceptable value of droop is where the output of a SHA does not change by more than ½ LSB during the conversion time of the ADC it is driving. Where droop is due to leakage current in reverse biased junctions (switches or FET amplifier gates) it will double for every 10°C increase in chip temperature - which means that it will increase a thousand fold between 25°C and +125°C. Droop and pedestal can be reduced by increasing the value of the hold capacitor, but this will also increase acquisition time and reduce bandwidth in sample mode.

Stray capacity in a SHA may allow a small amount of the AC input to be coupled to the output during hold. This effect is known as *feedthrough.*

SHAs which are built into sampling ADCs do not require very good droop

specifications, since the ADC conversion takes place quite quickly and once the conversion is complete the SHA need not store accurately any longer. Such SHAs generally use a small hold capacitor built on the chip itself. Where long hold times and low droop are required a separate discrete hold capacitor will be required.

Hold capacitors for SHAs must have low leakage, but there is another characteristic which is equally important: low *dielectric absorption*. If a capacitor is charged, then discharged, and then left open circuit it will recover some of its charge. The phenomenon is known as *dielectric absorption*, and it can seriously degrade the performance of a SHA, since it causes the remains of a previous sample to contaminate a new one, and may introduce random errors of tens or even hundreds of mV.

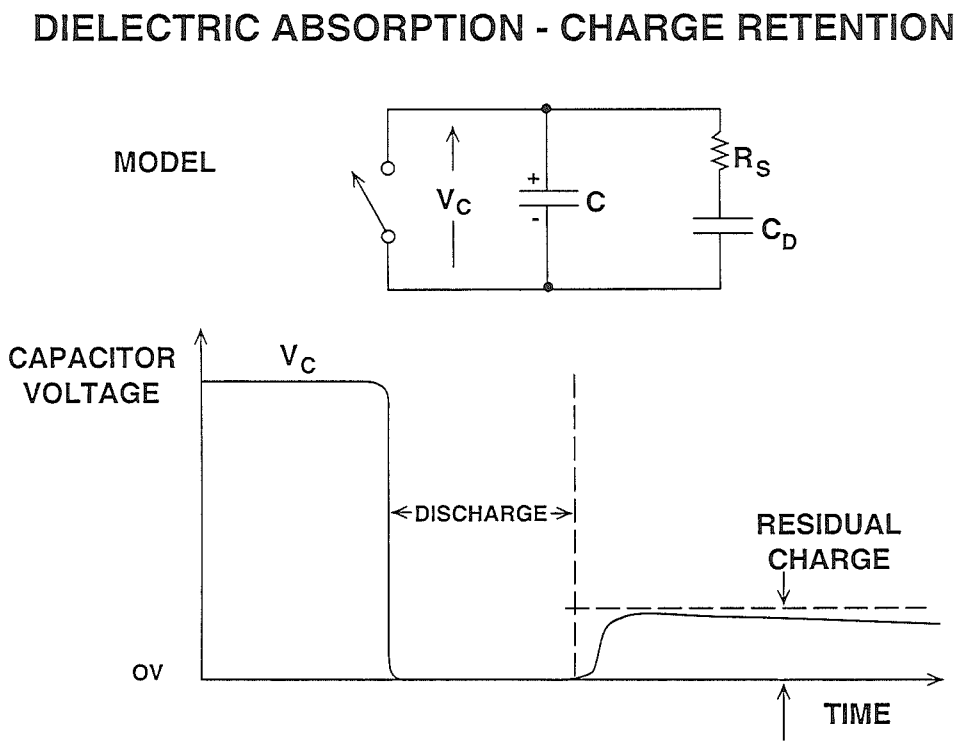


Figure 4.3

Different capacitor materials have differing amounts of dielectric absorption:- electrolytic capacitors are dreadful (their leakage is also high) and some high-K ceramic types are bad, while mica, polystyrene and polypropylene are generally good. Unfortunately dielectric absorption varies from batch to batch and even occasional batches of polystyrene and polypropylene capacitors may be affected. It is therefore wise to pay 30-50% extra when buying capacitors for SHA applications and buy devices which are guaranteed by their manufacturers to have low dielectric absorption, rather than types which might generally be expected to have it.

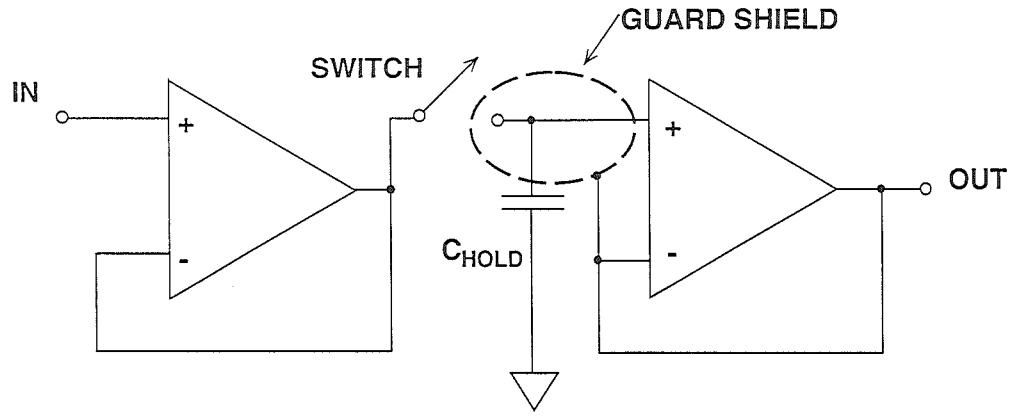
THE CHOICE OF HOLD CAPACITOR AFFECTS ACCURACY

- Must Have: Low Leakage and Low Dielectric Absorption
- Best:
  - Polystyrene
  - Polypropylene
  - Teflon
  - Polycarbonate
- Worst:
  - Mylar
  - Glass
  - Electrolytic

Figure 4.4

Even quite small leakage currents can cause troublesome droop when SHAs use small hold capacitors. Leakage currents in PCBs may be minimized by the intelligent use of guard rings. A guard ring is a ring of conductor which surrounds a sensitive node and is at the same potential. Since there is no voltage between them there can be no leakage current flow. In a non-inverting application, such as is shown in Figure 4.5, the guard ring must be driven to the correct potential, whereas the guard ring on a virtual ground can be at actual ground potential. The surface resistance of PCB material is much lower than its bulk resistance, so guard rings must always be placed on both sides of a PCB - and on multi-layer boards guard rings should be present in all layers.

DRIVE THE GUARD SHIELD WITH THE SAME VOLTAGE AS THE HOLD CAPACITOR TO REDUCE BOARD LEAKAGE



Note: Be Sure a Guard Shield is in Each Layer of the PCB

Figure 4.5

We have mentioned that modern ADCs frequently contain integral SHAs. Figure 4.7 shows how a venerable old ADC, the AD574 (the most widely sold 12-bit ADC ever manufactured), has been redesigned as a sampling ADC, the AD1674. The AD1674 is identical to the AD574 in most respects, including pinout and power requirements, although it outperforms it on a number of specifications, but contains a high performance SHA to extend its utility. The AD1674 may be used in any AD574 socket but will also handle much faster input signal changes.

USING A GUARD SHIELD ON A VIRTUAL GROUND SHA DESIGN

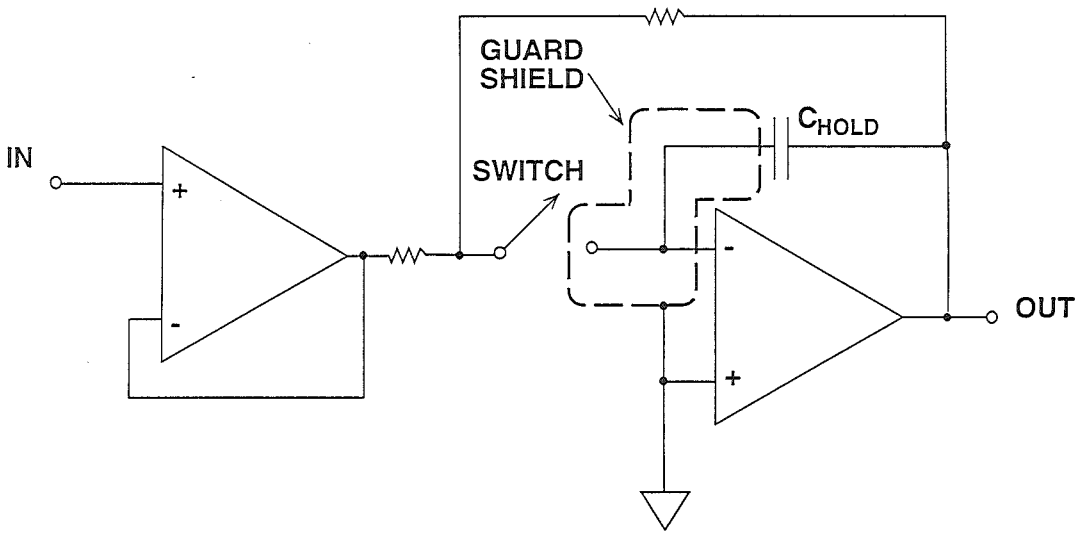


Figure 4.6

MANY LATEST GENERATION ADCs HAVE ON-CHIP SHAs

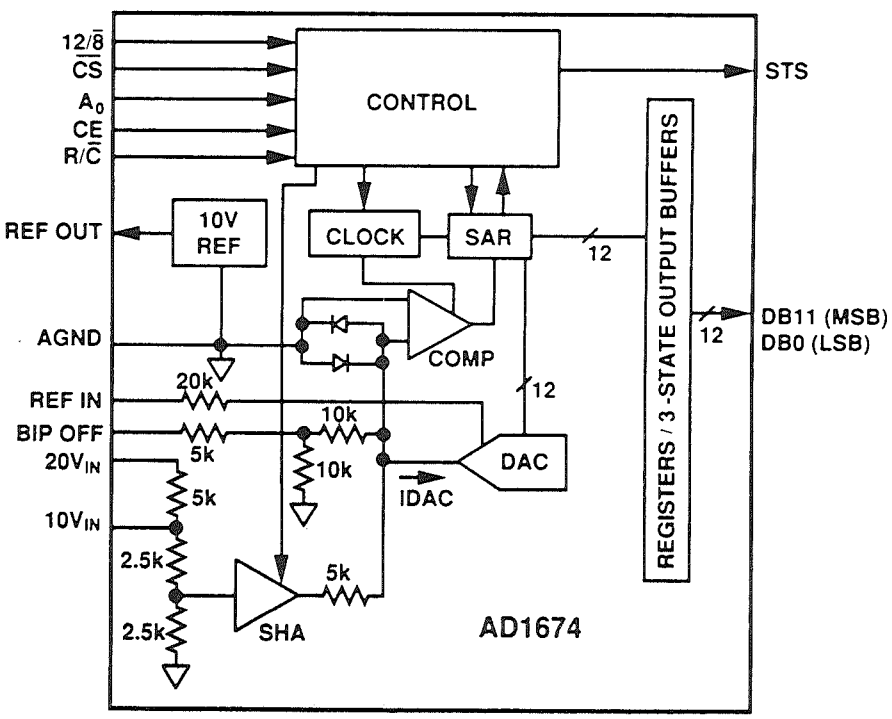


Figure 4.7

REFERENCES

[1] **Mixed Signal Seminar,** Analog Devices, Chapter 1