SECTION 3

PROGRAMMABLE GAIN AMPLIFIERS

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Most systems with wide dynamic range need some method of adjusting the input signal level to the analog to digital converter. The ADC compares the input signal to a fixed voltage reference (+5V or +10V are typical values). To achieve the rated precision of the converter, the input should be fairly near its full scale voltage. However transducers have a wide range of output voltages. High gain is needed for a small sensor voltage, but with a large transducer output a high gain will cause the amplifier or ADC to saturate. So some type of controllable gain device is needed. Such a device has a gain that is controlled by a DC voltage or, more commonly, a digital input. This device is known as a *programmable gain amplifier* or PGA. Programmable gain amplifiers have a variety of applications, and Figure 3.2 lists some of them .

PROGRAMMABLE GAIN AMPLIFIERS (PGAs)

- When Are They Needed?
- How is the Gain Switched
- What Are the Important Design Considerations?
- Tradeoffs Between Integrated and Home-Made Solutions

Figure 3.1

PGA APPLICATIONS

- Instrumentation
- Photodiode Circuits
- Ultrasound Preamplifiers
- Sonar
- Wide Dynamic Range Sensors
- Automatic Gain Control (AGC) Loops

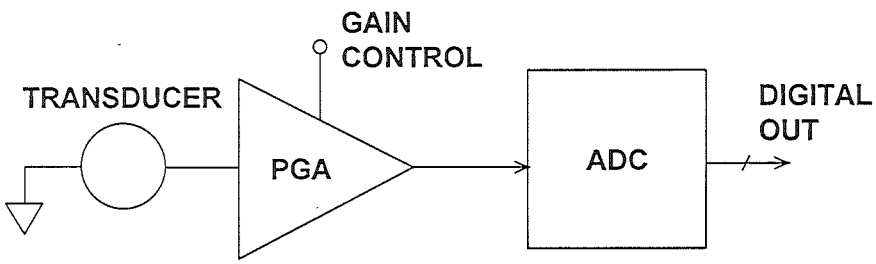
Figure 3.2

A PGA is usually located between a sensor and its ADC. Additional signal conditioning may take place before or after the PGA, depending on the application. For example, a photodiode needs a current to voltage converter between it and the PGA. In other systems, it is better to place the gain first, and condition a larger signal. This reduces errors introduced by the signal conditioning circuitry.

To understand the benefits of variable gain, assume an ideal PGA with two settings, gains of one and two. The dynamic range of the system is increased by 6dB. Increasing the gain to four results in a 12dB increase in dynamic range.

If the LSB of an ADC is equivalent to 10mV of input voltage, the ADC cannot resolve smaller signals but when the gain of the PGA is increased to two, input signals of 5mV may be resolved. Thus, the processor can combine gain information with the digital output of the ADC to increase its resolution by one bit. Essentially this is the same as adding additional resolution to the ADC.

PROGRAMMABLE GAIN AMPLIFIERS (PGAs)



- Used to Increase Dynamic Range of Circuit
- A PGA With a Gain From 1 To 2 Theoretically Increases the Dynamic Range by 6dB, A Gain of 1 To 4 Gives 12dB Increase, etc.

Figure 3.3

In practice PGAs are not ideal, and their error sources must be studied. The most fundamental problem with PGA design is accurate gain programming. Electromechanical relays have minimal R_{ON} but are otherwise unsuitable for gain switching, being slow, large and expensive, while silicon switches, as discussed in the section on switches and multiplexers, have quite large R_{ON}, which is both voltage- and temperature-variable, and stray capacities which may affect the AC parameters of a PGA using them.

PGA DESIGN ISSUES

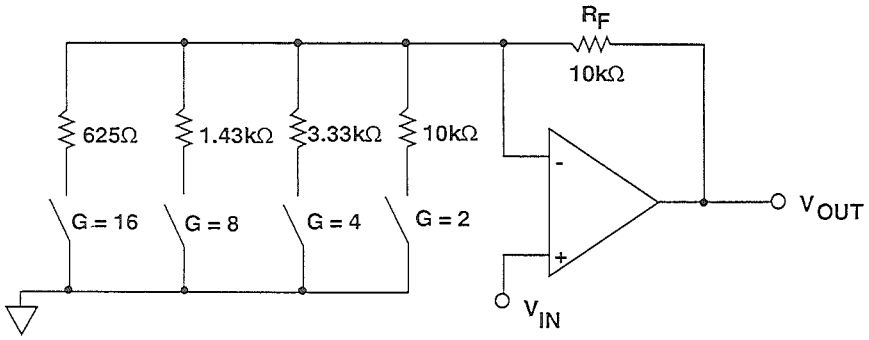
- How to Switch the Gain
- Effects of Switch On-Resistance
- Gain Accuracy
- Gain Linearity
- Bandwidth versus Frequency versus Gain
- Offset
- Temperature Effects on Gain and Offset
- Settling Time After Switching

Figure 3.4

To understand how R_{ON} can affect the performance of a PGA, let us consider a poor PGA design (Figure 3.5). An op amp is configured in the standard non-inverting gain circuit with 4 different gain setting resistors, each grounded by a switch. Most silicon switches have ON resistance in the range of 100Ω-500Ω. Even if the ON resistance were as low as 25Ω, the error for a gain of 16 would be 2.4%, much worse than 8-bits. Furthermore R_{ON} drifts over temperature, and varies from switch to switch. If the value of the feedback and gain setting resistors were increased, noise and offset would become a problem. The only way to achieve accuracy with this circuit is to replace silicon switches with relays which have virtually no ON resistance.

It is better to use a circuit where R_{ON} is unimportant. In Figure 3.6, the switch is placed in series with the inverting input of an op amp. The input impedance of an op amp is very large, the R_{ON} of the switch is irrelevant. The gain is now determined by the resistors. The R_{ON} may add a small offset error if the op amp bias current is large.

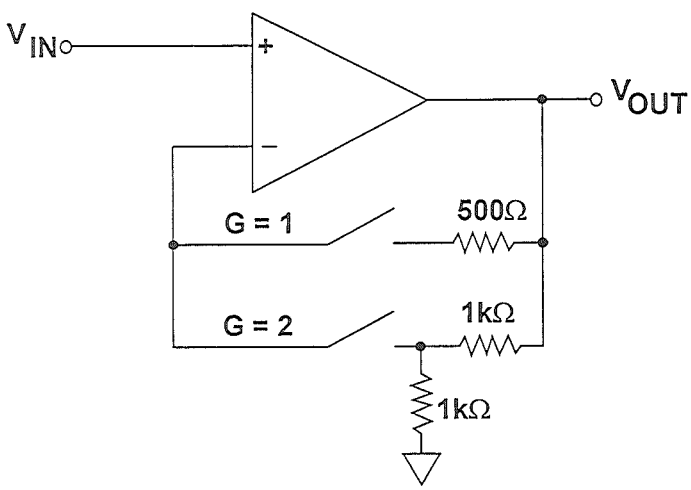
HOW NOT TO BUILD A PGA



- Gain Accuracy Limited by Switch's On Resistance, R_{on} and R_{on} Modulation
- R_{on} Typically 100 - 500Ω for a CMOS Or JFET Switch
- Even With R_{on} = 25Ω, There is a 2.4% Gain Error for A_V = 16
- R_{on} Drift Over Temperature Limits Accuracy
- Only Solution is to Use Very Low R_{on} Switches (Relays)

Figure 3.5

ALTERNATE CONFIGURATION MAKES R_{on} NEGLIGIBLE



- R_{on} is Not in Series With Gain Setting Resistors
- R_{on} is Very Small Compared to Input Impedance
- Only a Slight Offset Error Occurs Due to the Bias Current Flowing Through the Switch

Figure 3.6

The AD526 amplifier uses this method of building a PGA and integrates it onto a single chip. The AD526 has 5 binary gain settings from 1 to 16 and its internal JFET switches are connected to the inverting input of the amplifier. The gain resistors are laser trimmed. The maximum gain error is only 0.02%, far better than the 2.4% error in Figure 3.4. The linearity is also very good at 0.001%. The AD526 is controlled by a latched digital interface.

AD526 MONOLITHIC SOFTWARE PROGRAMMABLE PGA

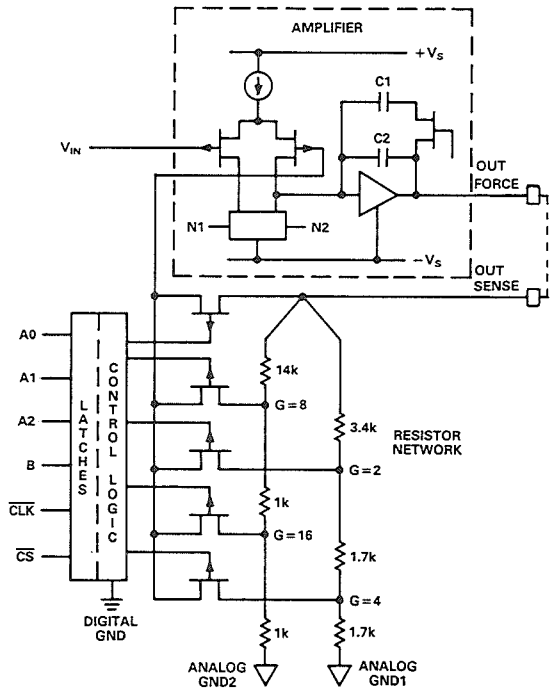


Figure 3.7

AD526 PGA KEY FEATURES

- Software Programmable Binary Gains From 1 to 16
- Low Bias Current JFET Input Stage
- Worst Case Gain Error is 0.02% (12 Bit Performance)
- Gain Nonlinearity is 0.001% Maximum
- Latched TTL Compatible Control Inputs

Figure 3.8

This same design can be used to build the discrete PGA shown in Figure 3.9. It uses a single op amp, a quad switch, and precision resistors. The low noise AD797 replaces the JFET input op amp of the AD526, but almost any voltage feedback op amp could be used in this circuit. The ADG412 was picked for its low ON resistance of 35Ω.

The resistors were chosen to give gains of 1, 10, 100 and 1000, but if other gains are required the resistor values may easily be altered. Ideally, a trimmed resistor network should be used both for initial gain accuracy and for low drift over temperature. The 20pF ensures stability and holds the output voltage when the gain is switched. The control signal to the switches turns one switch off a few nanoseconds before the second switch turns on. During this break the op amp is open-loop. If the capacitor was not used the output would start slewing. Instead, the capacitor holds the output voltage during the switching. Since the time that both switches are open is very short, only 20pF is needed. For slower switches a larger capacitor may be necessary.

A VERY LOW NOISE PGA USING THE AD797 AND THE ADG412

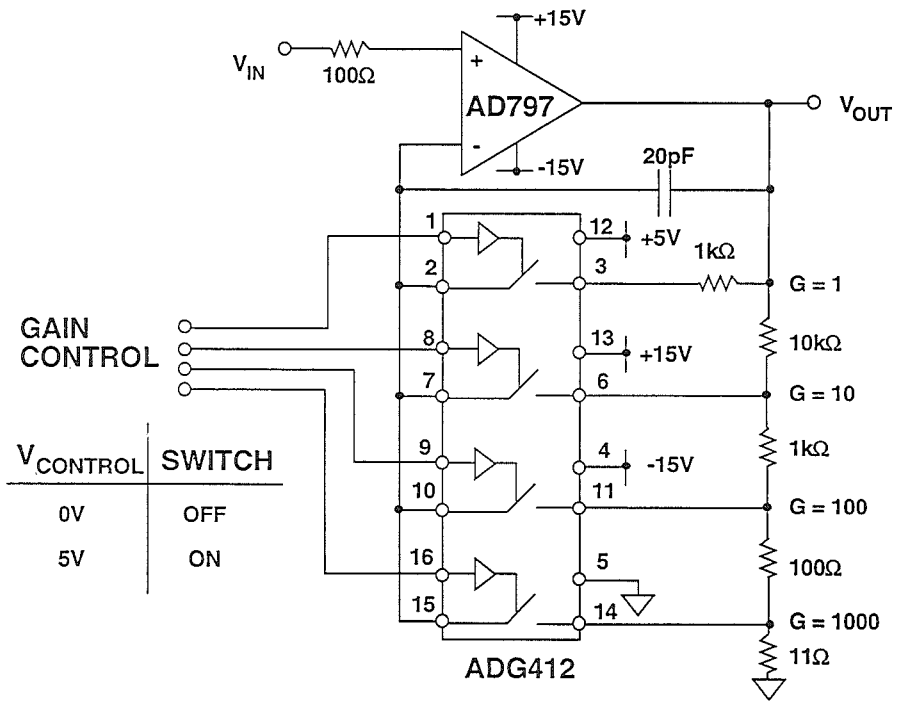


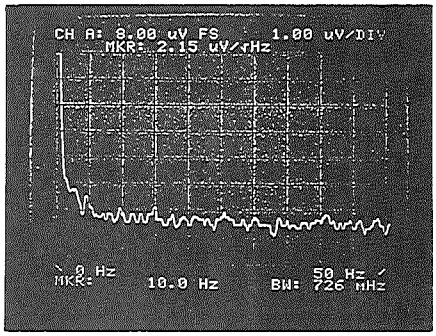
Figure 3.9

Figure 3.10 shows the noise and switching performance of the circuit. The spectral noise density is only 1.65nV/√Hz at 1kHz, only slightly higher than the noise performance of the AD797 alone. The increase is due to the noise of the ADG412 and the current noise of the AD797 flowing through the ON resistance. The noise was measured at a gain of 1000. The second photo shows the output as a function of the gain setting. The top two traces show the switch control changing the gain from 1 to 10 and back to 1. The AD797 has a constant 1 V input during this time, and as the bottom trace shows, the output changes from 1V to 10V. The circuit is well behaved with no unexpected glitches, and minimal overshoot and ringing.

AD797, ADG412 PGA NOISE AND SWITCHING TIME

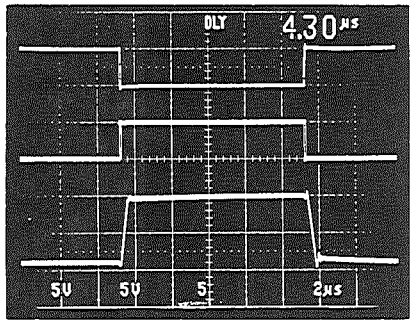
Spectral Noise Density

2.15nV/√Hz @ 10Hz
1.65nV/√Hz @ 1kHz
G = 1000



Vertical: 1μV/√Hz/div.
Horizontal: 5Hz/div., BW = 0.726Hz

Switching Time for 1V Input
From G = 1 to G = 10 to G = 1
Top Trace: G = 1 Switch Control
Middle Trace: G = 10 Switch Control
Bottom Trace: Output



Vertical: 5V/div.
Horizontal: 2μs/div.

Figure 3.10

The accuracy of the PGA is important in determining the overall accuracy of a system. The AD797 has a bias current of 0.9μA, which, flowing in 35Ω R_{ON}, results in an additional offset error of 31.5μV (Figure 3.11). Combined with the AD797 offset, the total Vos becomes 71.5μV (max). Offset temperature drift is affected by the change in bias current and ON resistance. Calculations show that the total temperature coefficient increases from 0.6μV/°C to 1.6μV/°C. These errors are small and may not matter, but it is important to be aware of them. Input characteristics such as common mode range and input bias current are determined solely by the AD797. The circuit could be converted to single supply simply by changing the op amp. The switches do not need to be changed.

AD797 PGA ACCURACY

- R_{on} Adds Additional Input Offset And Drift:

  $\Delta V_{os} = I_b R_{on} = (0.9\mu A)(35\Omega) = 31.5\mu V$ (max)

  Total $V_{os} = 40\mu V + 31.5\mu V = 71.5\mu V$ (max)
  (Note: 40μV is Due To The AD797B)

- Temperature Drift Due To R_{on} :

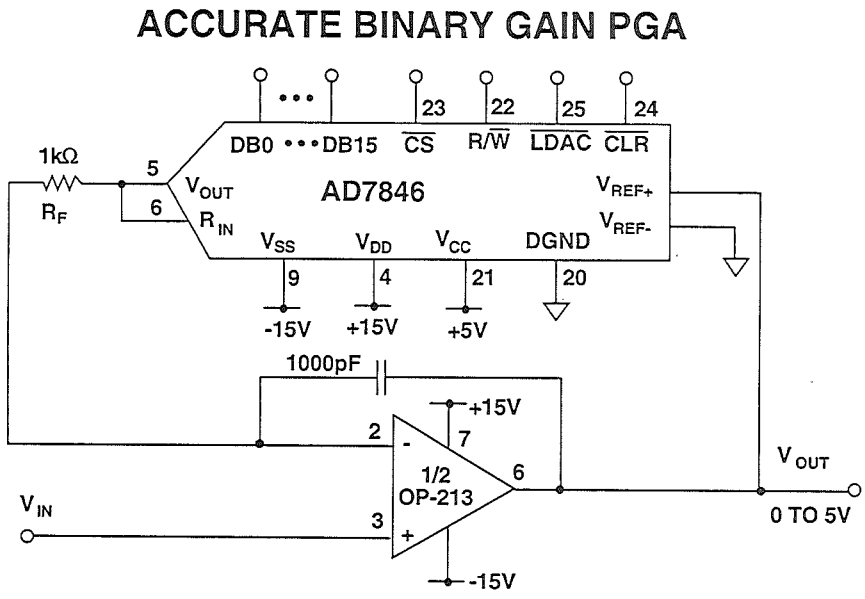
  At +85°C, $\Delta V_{os} = (2\mu A)(45\Omega) = 90\mu V$ (max)

- Temperature Coefficient Total:

  $\Delta V_{os} / \Delta T = 0.6\mu V/°C + 1.0\mu V/°C = 1.6\mu V/°C$ (max)
  (Note: 0.6μV/°C Is Due To The AD797B)

Figure 3.11

Another PGA configuration uses a DAC in the feedback loop of an op amp to adjust the gain under digital control (Figure 3.12). The digital code of the DAC controls its attenuation. Attenuating the feedback signal increases the closed-loop gain. A non-inverting PGA of this type requires a multiplying DAC with a voltage output (a multiplying DAC is a DAC with a wide reference voltage range *which includes zero*). For most applications of the PGA the reference input must be capable of handling bipolar signals. The AD7846 is a 16-bit converter that meets these requirements. In this application it is used in standard 2-quadrant multiplying mode. The OP-213 is a low drift, low noise amplifier, but the choice of amplifier is flexible and depends on the application. The input voltage range depends on the output swing of the AD7846, which is 3V less than the positive supply and 4V above the negative supply. A 1000pF capacitor is used in the feedback loop for stability.



- Multiplying DAC in Feedback Loop Adjusts Gain
- $G = \frac{2^{16}}{\text{Decimal Value of Digital Code}}$

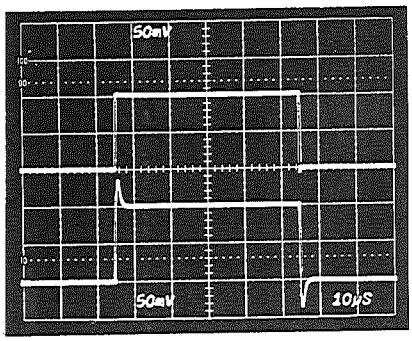
Figure 3.12

The gain of the circuit is set by adjusting the digital inputs of the DAC according to the equation given in Figure 3.12. $D_{0\text{-}15}$ represents the decimal value of the digital code. For example, if all the bits were set high the gain would be 65,536/65,535 = 1.000015. If the 8 least significant bits are set high and the rest low the gain would be 65,536/255 = 257.

Figure 3.13 shows the small signal response at a gain of 1 with a 100mV square wave input. The bandwidth is a fairly high 4MHz. However, this does reduce with gain, and for a gain of 256 the bandwidth is only 600Hz. If the gain bandwidth product were constant, the bandwidth in a gain of 256 should be 15.6kHz; but the internal capacitance of the DAC reduces the bandwidth to 600Hz.

BINARY GAIN PGA PERFORMANCE

SMALL SIGNAL RESPONSE



Top Trace: Input, 50mV/div.
Bottom Trace: Output, 50mV/div.
Horizontal Scale: 10µs/div.

Bandwidth (G=+1) = 4MHz
Bandwidth (G=+256) = 600Hz

Nonlinearity (G=+1) = 0.001%

Offset = 100µV

Noise = 50nV/√Hz

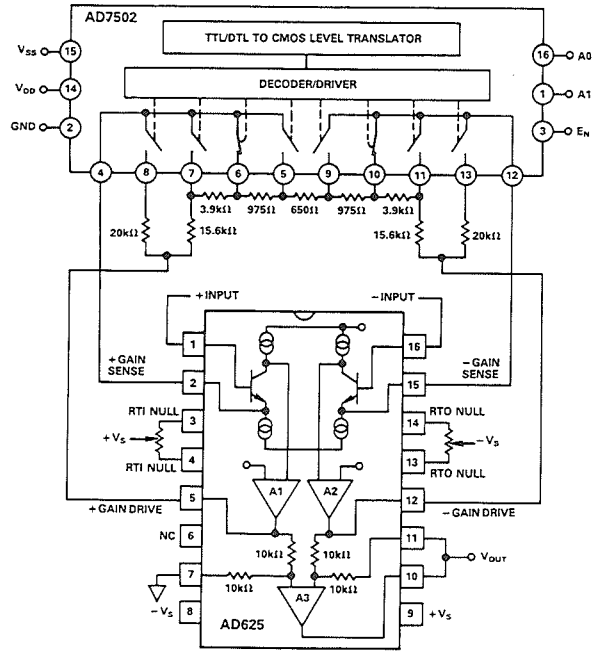
Gain Accuracy (G=+1) = 0.003%
Gain Accuracy (G=+256) = 0.1%

Figure 3.13

The gain accuracy of the circuit is determined by the resolution of the DAC and the gain setting. At a gain of 1 all bits are on, and the accuracy is determined by the DNL specification of the DAC, which is ±1 LSB maximum. Thus, the gain accuracy is equivalent to 1LSB in a 16-bit system, or 0.003%. However, as the gain is increased, fewer of the bits are on. For a gain of 256 only bit 8 is turned on. The gain accuracy is still dependent on the ±1 LSB of DNL, but now that is compared to only the lowest 8 bits. Thus, the gain accuracy is reduced to 1 LSB in a 8-bit system, or 0.4%. If the gain is increased above 256, the gain accuracy is reduced further. The designer must determine an acceptable level of accuracy. In this particular circuit the gain was limited to 256.

There are often applications where a PGA with differential inputs is needed instead of the single ended types discussed so far. The AD625 combines an instrumentation amplifier topology with gain switching capabilities to accomplish 12 bit gain accuracy (Figure 3.14). An external switch is needed to switch between different gain settings. In the example shown, resistors were chosen for gains of 1, 4, 16, and 64. Other features of the AD625 are 0.001% nonlinearity, wide bandwidth, and very low input noise.

A SOFTWARE PROGRAMMABLE GAIN AMPLIFIER



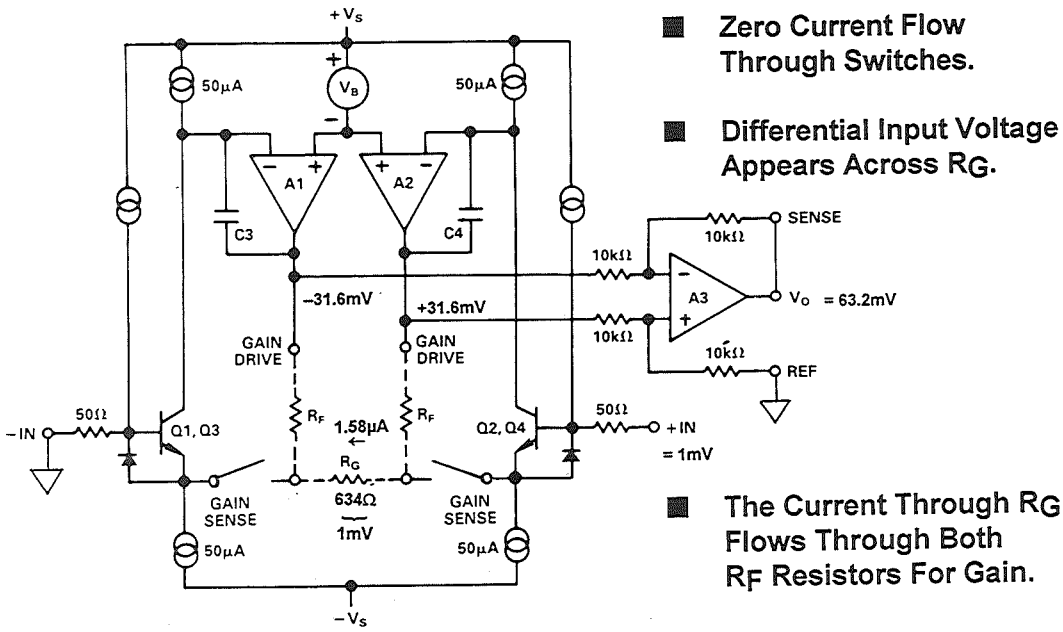
- G = 1, 4, 16, 64
- Differential Input Stage
- 12 Bit Gain Accuracy
- Nonlinearity = ± 0.001% (G = 1 to 256)
- Low Noise: 4nV/√Hz
- 25MHz Gain-Bandwidth Product

Figure 3.14

Consider the circuit in Figure 3.15. The gain is set to 64 with R_G=634Ω and the two resistors R_F=20kΩ. Since transistors Q1 & Q3, and Q2 & Q4 have 50μA current sources in both their emitters and their collectors, negative feedback around A1 and A2 respectively will ensure that no net current flows through either gain sense pin into either emitter. Since no current flows in the gain sense pins no current flows in the gain setting switches and their R_{on} does not affect either gain or offset. In real life there will be minor mismatches but the errors are well under the 12-bit level.

If no current is to flow in the gain sense pins the voltages at the ends of R_G must equal the voltages on the pins, and the voltages are determined by the voltages on the outputs of A1 and A2 and the voltage drops due to current flowing in the two R_F resistors. The differential gain between the amplifier inputs and the outputs of A1 and A2 is therefore set by the ratio (R_F+R_F):R_G. The unity gain subtractor amplifier formed by A3 and four matched resistors removes the common-mode and drives the output.

SIMPLIFIED CIRCUIT FOR AD625



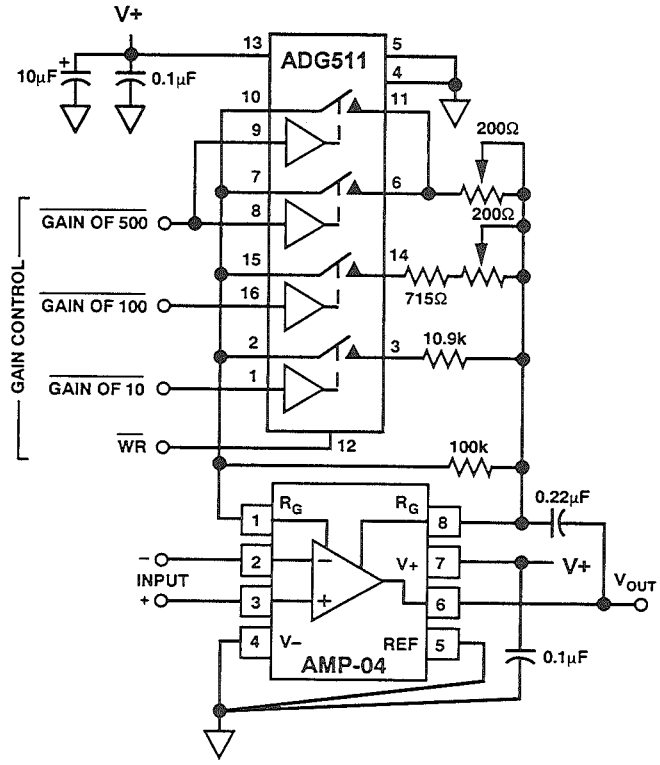
- Zero Current Flow Through Switches.
- Differential Input Voltage Appears Across R_G.
- The Current Through R_G Flows Through Both R_F Resistors For Gain.

Figure 3.15

Noninverting PGA circuits using an op amp are easily adaptable to single supply, but the instrumentation amplifier topology does not lend itself to single supply applications. However, the AMP-04 can be used with an external switch to produce the single supply instrumentation PGA shown in Figure 3.16. This circuit has selectable gains of 1, 10, 100, and 500, which are controlled by an ADG511. The ADG511 was chosen as a single supply switch with a low R_{ON} of 45Ω. The gain of this circuit is dependent on the R_{ON} of the switches. Trimming is required at the higher gains to achieve accuracy. At a gain of 500, two switches are used in parallel, but their resistance causes a 10% gain error in the absence of adjustment.

As will be discussed in Chapter 6 certain ADCs have PGAs built in. Circuit design is much easier because an external PGA and its control logic are not needed. Furthermore, all the errors of the PGA are included in the specifications of the ADC, making error calculations simple. The PGA gain is controlled over the same serial interface as the ADC, and the gain setting is factored into the conversion, saving additional calculations to determine input voltage. This combination of ADC and PGA is very powerful and enables the realization of highly accurate system with a minimum of circuit design.

SINGLE SUPPLY (+5V TO +10V) INSTRUMENTATION PGA



- G = 100kΩ/RG
- RG Is a Combination of Switch Ron and the External Resistor
- Trim Required at High G Due to Uncertainty Of Ron
- Relays Can Be Used to Avoid Trim

Figure 3.16

THE AD7710 ADC HAS A BUILT-IN PGA WITH GAIN CONTROLLED BY A SERIAL INTERFACE

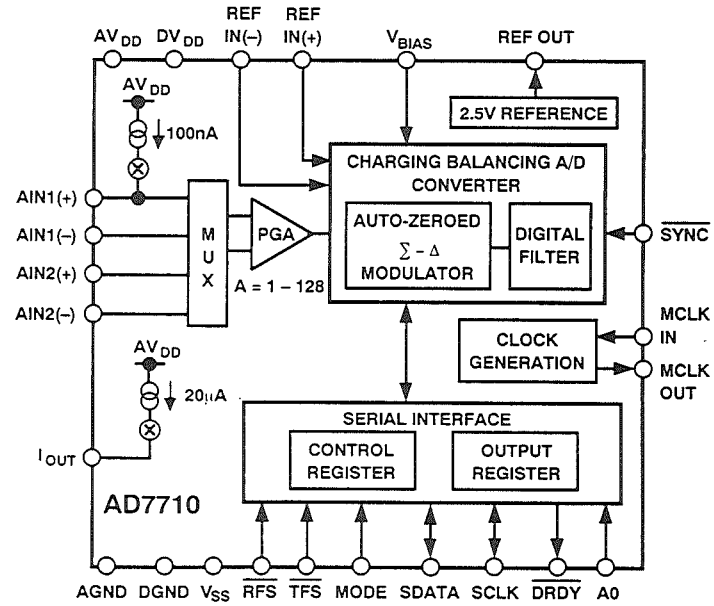


Figure 3.17