SECTION 2

MULTIPLEXING SIGNALS WITH ANALOG SWITCHES

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MULTIPLEXING SIGNALS WITH ANALOG SWITCHES, *James Wong, Jerry Whitmore*

Analog signals can be switched, multiplexed, and easily connected using analog switches. With sufficient care there will be little or no degradation of signal quality. This section is devoted to CMOS technology in analog switch circuitry, their parasitic latchup mechanisms, and effective protection methods. It also discusses AC switch characteristics and how they affect the performance of a system, and some application circuits.

MULTIPLEXING CONCEPTS

- Advantages of CMOS Technology in Analog Switch Circuitry
- Parasitic Transistors/Latchup and Protection Methods
- Switch Equivalent Circuit dc and ac Analysis
- Applying the Analog Switch

Figure 2.1

The ideal analog switch has no ON-resistance, infinite OFF impedance and zero time delay, and can handle large signal and common-mode voltages. Real CMOS analog switches meet none of these criteria, but if we understand the limitations of analog switches, most of these limitations can be overcome.

CMOS switches have an excellent combination of attributes. In its most basic form, the MOSFET transistor is a voltage-controlled resistor. In the ON state, its resistance can be less than 100Ω, while in the OFF-state, the resistance increases to several hundreds of megohms, with nanoamp leakage currents.

CHARACTERISTICS OF THE IDEAL ANALOG SWITCH

- On Resistance: Zero
- Off Impedance: Infinite at All Frequencies
- Switching Time: Zero
- Switch Leakage: Zero
- Power Dissipation: Zero
- MTBF: Infinite

Figure 2.2

CMOS technology is compatible with logic circuitry and can be densely packed in an IC. Its fast switching characteristics are well controlled with minimum circuit parasitics.

MOSFET transistors are bilateral. That is, they can switch positive and negative voltages and conduct positive and negative currents with equal ease.

ADVANTAGES OF MIXED SIGNAL CMOS TECHNOLOGY

- A Great Logic Technology
  - High Density
  - Moderate to High Speed
  - Low Power Dissipation
- An Excellent Switch Technology
  - MOSFETs are Voltage Controlled Resistors
  - MOSFETs Lose No Current to the Control Input (Gate)
  - MOSFETs are Electrically Bilateral -- Can Switch Positive or Negative Voltages or Steer Positive or Negative Current with Equal Ease
  - No Offset Voltage in Series With ON MOSFET (Unlike Bipolar Transistor)

Figure 2.3

A MOSFET transistor has a voltage controlled resistance which varies nonlinearly with signal voltage as shown in Figure 2.4. Figure 2.5 shows a basic CMOS switch using complementary P-channel and N-channel MOS devices connected in parallel. This reduces the ON-resistance and also produces a resistance which varies less with signal voltage.

MOSFET SWITCH ON-RESISTANCE VERSUS SIGNAL VOLTAGE

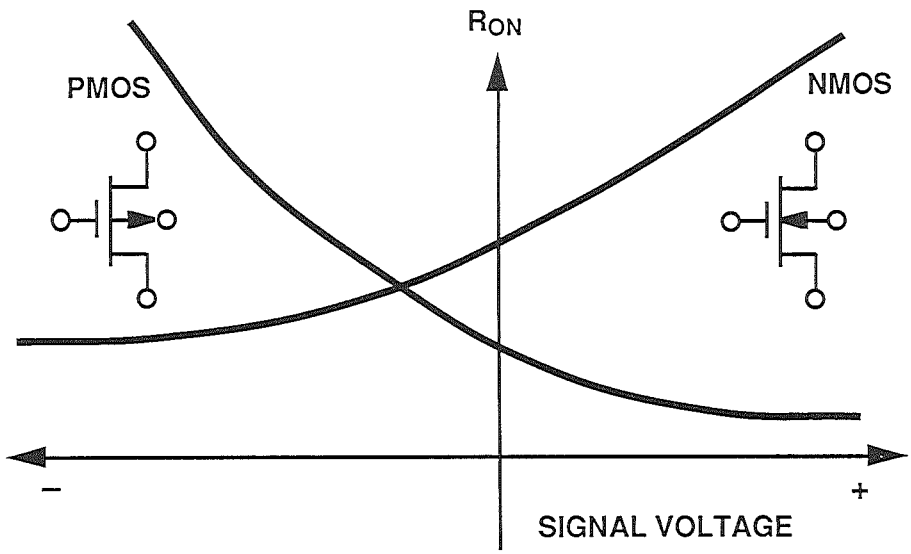


Figure 2.4

BASIC CMOS SWITCH USES COMPLEMENTARY PAIR TO MINIMIZE Ron VARIATION DUE TO INPUT SIGNAL SWING

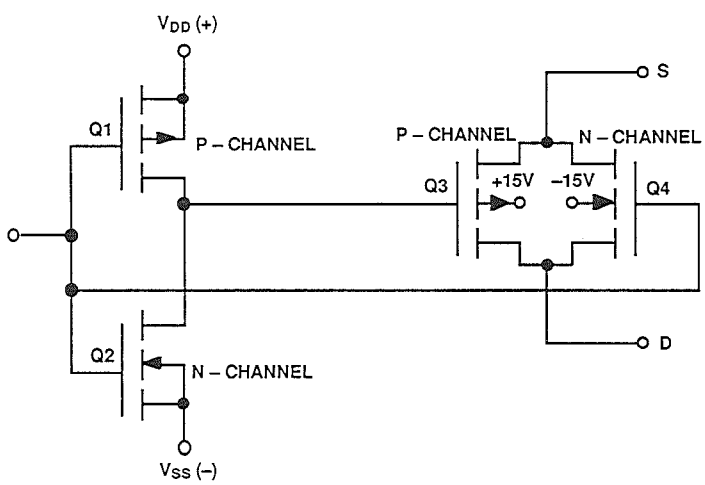


Figure 2.5

Figure 2.6 shows the ON-resistance changing with channel voltage for both N-type and P-type devices. This nonlinear resistance can causes errors in DC accuracy as well as AC distortion. The bilateral CMOS switch solves this problem. ON-resistance is minimized and its linearity is also improved. The bottom curve (Figure 2.6) shows the improved flatness of the ON-resistance characteristic of the switch.

CMOS SWITCH ON-RESISTANCE VERSUS SIGNAL VOLTAGE

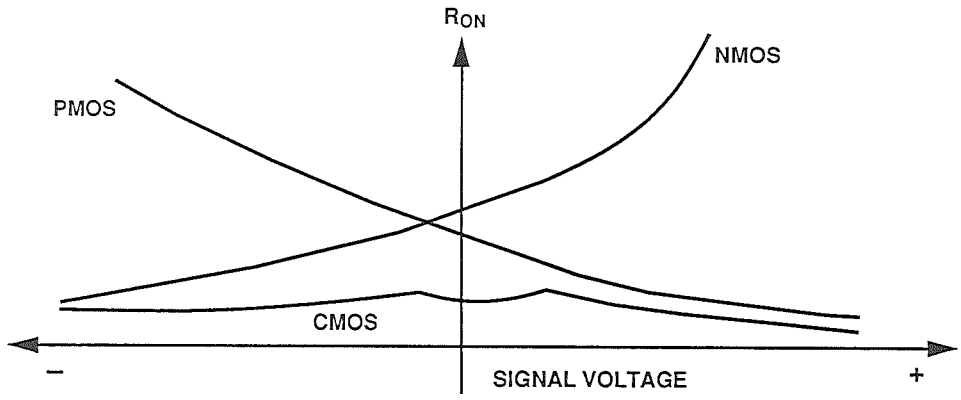


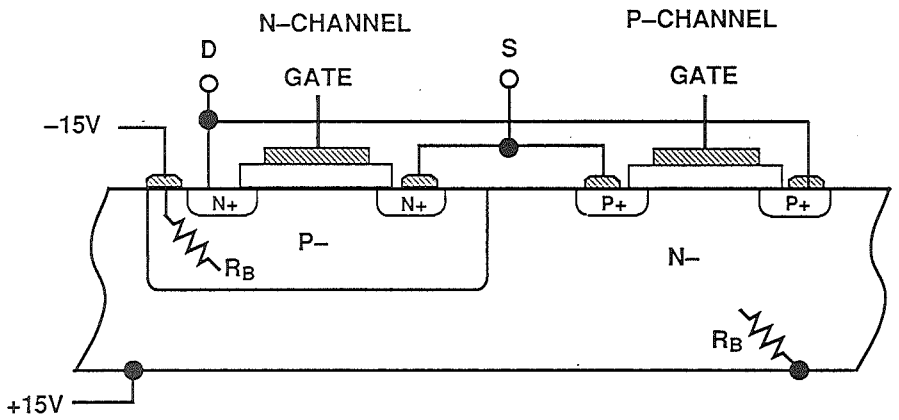
Figure 2.6

PARASITIC LATCHUP

Most CMOS analog switches are built using junction-isolated CMOS processes. A cross-sectional view of a single switch cell is shown in Figure 2.7. Parasitic SCR (silicon controlled rectifier) latchup can occur if the analog switch terminal has voltages more positive than V_{DD} (+15V) or more negative than V_{SS} (-15V). Even a transient situation such as power-on with an input voltage present can trigger a parasitic latchup. If the conduction current is too great (several hundred milliamperes or more), it can damage the switch.

The parasitic SCR mechanism is shown in Figure 2.8. SCR action takes place when either terminal of the switch (source or the drain) is either one diode drop more positive than V_{DD} or one diode drop more negative than V_{SS}. In the former case, the V_{DD} terminal becomes the SCR gate input and provides the current to trigger SCR action. In the case where the voltage is more negative than V_{SS}, the V_{SS} terminal becomes the SCR gate input and provides the gate current. In either case, high current will flow between the supplies. The amount of current depends on the collector resistances of the two transistors, which can be fairly small.

CROSS SECTION OF JUNCTION-ISOLATED CMOS SWITCH



- Problems Occur if Voltages More Positive Than V_{dd} or More Negative than V_{SS} are Applied to an Analog Switch Terminal

Figure 2.7

BIPOLAR TRANSISTOR EQUIVALENT CIRCUIT OF CMOS SWITCH SHOWS PARASITIC ACTION (A CLASSIC SCR LATCH)

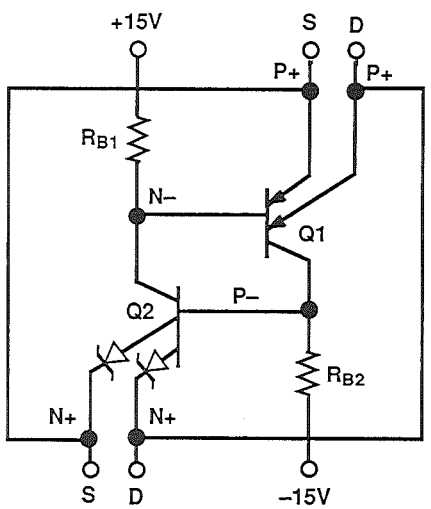
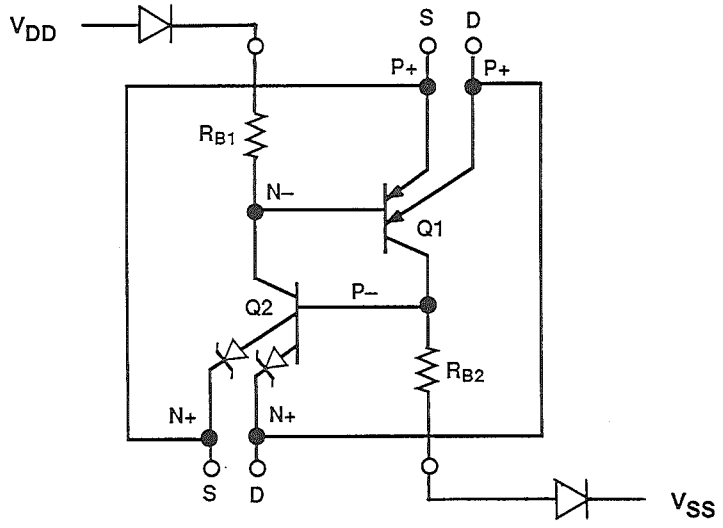


Figure 2.8

In order to prevent this type of SCR latchup, a series diode can be inserted into the V_{DD} and V_{SS} terminals as shown in Figure 2.9. The diodes block the SCR gate current. Normally the parasitic transistors Q1 and Q2 have low beta (usually less than 10) and require a comparatively large gate current to fire the SCR. The diodes limit the reverse gate current so that the SCR is not triggered.

DIODE PROTECTION SCHEME FOR CMOS SWITCH



■ Protection Diodes CR1 and CR2 Block Base Current Drive to Q1 and Q2 in Event of Overvoltage at S or D

Figure 2.9

If diode protection is used, the analog voltage range of the switch will be reduced by one V_{be} at each rail.

Analog switches must also be protected from possible overcurrent by inserting a series resistor to limit the current to a safe level, generally less than 25mA. This method works only if the switch drives a high impedance load (Figure 2.11).

PROTECTING CMOS SWITCH / MUX FROM LATCHUP USING DIODES

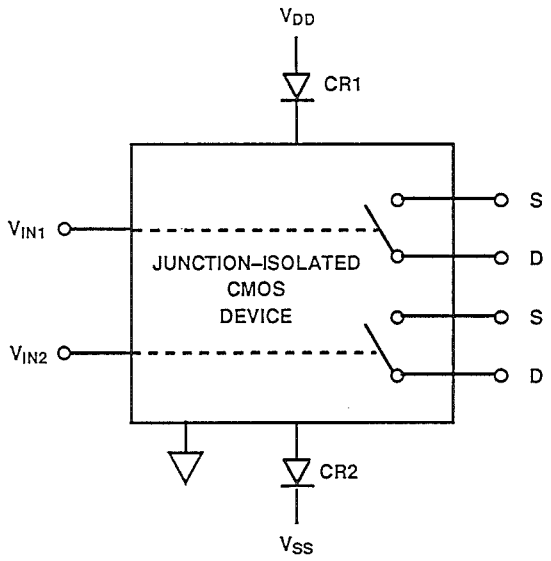
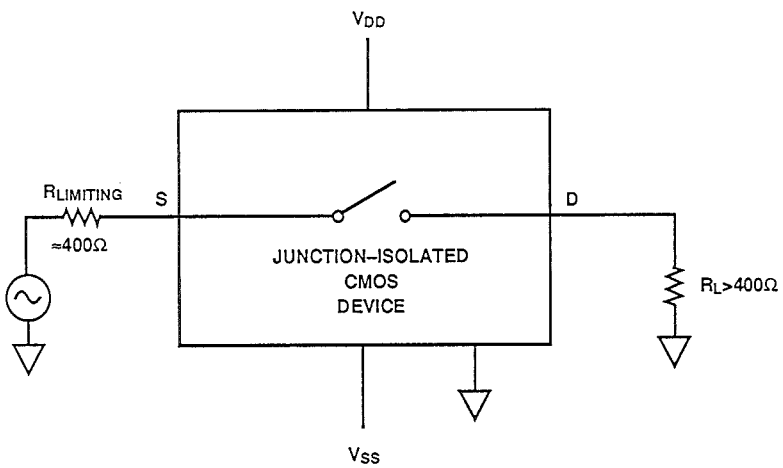


Figure 2.10

PROTECTING CMOS SWITCH / MUX FROM OVERCURRENT



- External Resistor Limits Current to Safe Value

Figure 2.11

Latchup protection and overcurrent protection schemes are mutually exclusive. If both fault conditions can exist in a system, then both protection protective diodes and resistors should be used.

"LATCHPROOF" VERSUS "OVERVOLTAGE PROTECTED"

- *Latchproof* only means the device won't go into an SCR mode.
- It does not guarantee *Overvoltage Protection.*

Figure 2.12

THE ANATOMY OF THE ANALOG SWITCH

It is important to understand the error sources in an analog switch. Many affect AC and DC performance, while others only affect AC. Figure 2.13 shows the equivalent circuit of two adjacent switches. It includes leakage currents and junction capacitances.

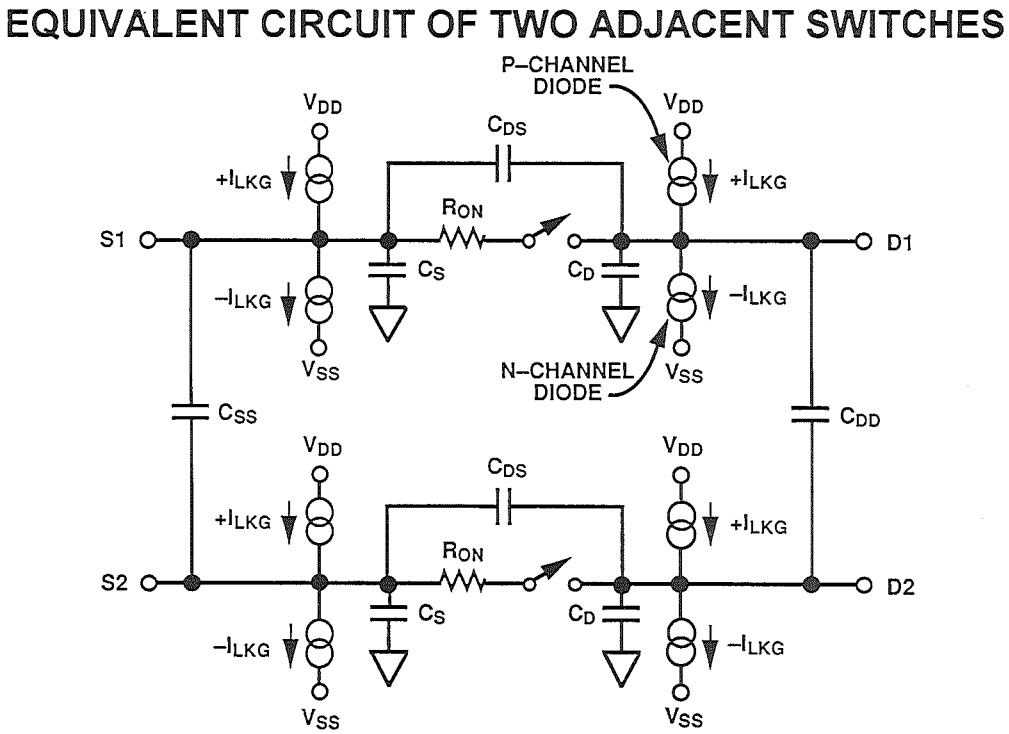
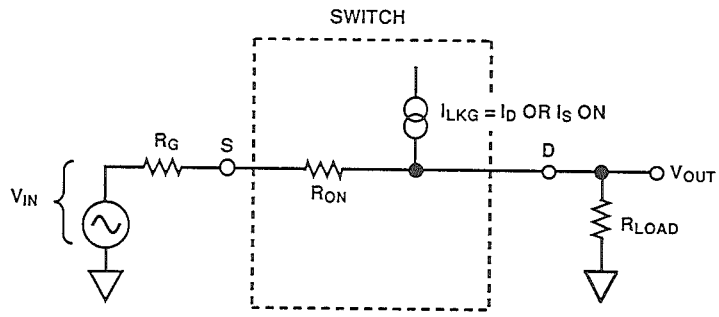


Figure 2.13

DC performance is affected mainly by the switch ON-resistance (R_{ON}) and leakage. Low resistance circuits are more subject to errors due to R_{ON} while high resistance circuits are affected by leakage currents. Figure 2.14 shows how these parameters affect DC performance.

FACTORS AFFECTING DC PERFORMANCE FOR *ON* SWITCH CONDITION: R_{ON}, R_{LOAD}, AND I_{LKG}



$$V_{OUT} = V_{IN}\left[\frac{R_{LOAD}}{R_G + R_{ON} + R_{LOAD}}\right] + I_{LKG}\left[\frac{R_{LOAD}(R_{ON} + R_G)}{R_G + R_{ON} + R_{LOAD}}\right]$$

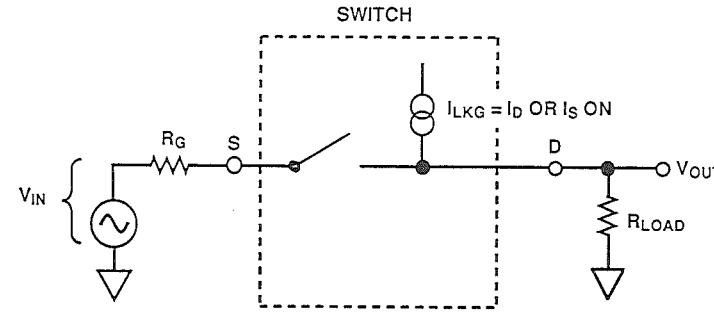
IF $R_G \rightarrow 0$,

$$V_{OUT} = V_{IN}\left[\frac{R_{LOAD}}{R_{ON} + R_{LOAD}}\right] + I_{LKG}\left[\frac{R_{LOAD}R_{ON}}{R_{ON} + R_{LOAD}}\right]$$

Figure 2.14

When the switch is OFF, leakage current can introduce errors. (Figure 2.15)

FACTORS AFFECTING DC PERFORMANCE FOR *OFF* SWITCH CONDITION: I_{LKG}, AND R_{LOAD}



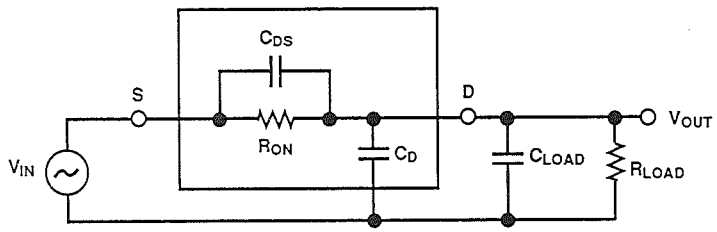
- Leakage Current Creates Error Voltage at V_{OUT} Equal to:

$$V_{OUT} = I_{LKG} \times R_{LOAD}$$

Figure 2.15

Figure 2.16 illustrates the parasitic components that affect the AC performance of CMOS switches. Additional external capacitances will further degrade performance. These capacitances affect feedthrough, crosstalk and system bandwidth.

DYNAMIC PERFORMANCE CONSIDERATIONS: TRANSFER ACCURACY VERSUS FREQUENCY



$$A(s) = \left[\frac{R_{LOAD}}{R_{LOAD}+R_{ON}}\right]\left[\frac{sR_{ON}C_{DS}+1}{s\left(\frac{R_{LOAD}R_{ON}}{R_{LOAD}+R_{ON}}\right)(C_{LOAD}+C_D+C_{DS})+1}\right]$$

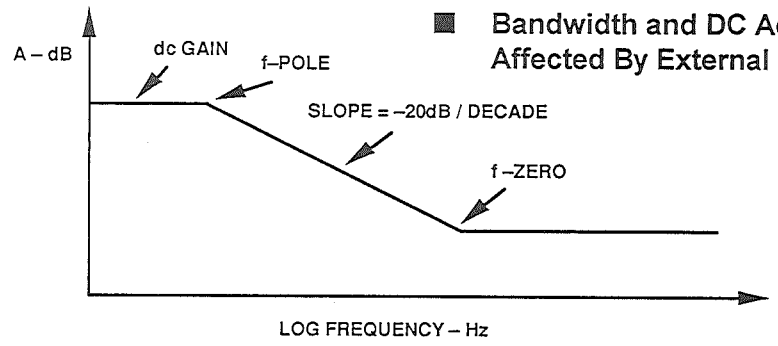
$$A(dB) = 20\log\left[\frac{R_{LOAD}}{R_{LOAD}+R_{ON}}\right]+10\log\left[\omega^2(R_{ON}C_{DS})^2+1\right]-10\log\omega^2\left[\left(\frac{R_{LOAD}R_{ON}}{R_{LOAD}+R_{ON}}\right)^2(C_{LOAD}+C_D+C_{DS})^2+1\right]$$

Figure 2.16

The signal transfer characteristic is dependent on the switch channel capacitance, C_{DS}. This capacitance creates a frequency zero in the numerator of the transfer function A(s). This zero usually occurs at high frequencies because the switch ON resistance is small. The bandwidth is also a function of the switch output capacitance in combination with C_{DS} and the load capacitance. This frequency pole appears in the denominator of the equation.

The composite frequency domain transfer function may be re-written as shown in Figure 2.17. In most cases, the pole breakpoint frequency occurs first because of the dominant effect of the output capacitance C_D. Thus, to maximize bandwidth a switch must have low input and output capacitance and low ON resistance.

DYNAMIC PERFORMANCE CONSIDERATIONS: TRANSFER ACCURACY VERSUS FREQUENCY



■ Bandwidth and DC Accuracy is Affected By External R and C

$$A(s) = \left[\frac{R_{LOAD}}{R_{LOAD}+R_{ON}}\right]\left[sR_{ON}C_{DS}+1\right]\left[\frac{1}{s\left(\frac{R_{LOAD}R_{ON}}{R_{LOAD}+R_{ON}}\right)(C_{LOAD}+C_D+C_{DS})+1}\right]$$

$$\text{DC GAIN} = \frac{R_{LOAD}R_{ON}}{R_{LOAD}+R_{ON}}, \quad f_{ZERO} = \frac{0.159}{R_{ON}C_{DS}}, \quad f_{POLE} = \frac{0.159}{\left(\frac{R_{LOAD}R_{ON}}{R_{LOAD}+R_{ON}}\right)(C_{LOAD}+C_D+C_{DS})}$$

Figure 2.17

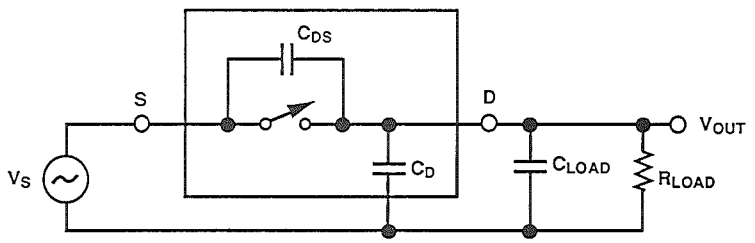
The series-pass capacitance, C_{DS}, not only creates a zero in the response in the ON-state, it degrades the feedthrough performance of the switch during its OFF state. When the switch is off, C_{DS} couples the input signal to the output load. (Figure 2.18)

Large values of C_{DS} will produce large values of feedthrough, proportional to the input frequency. Figure 2.19 illustrates the drop in OFF-isolation as a function of frequency. The simplest way to maximize the OFF-isolation is to choose a switch that has as small a C_{DS} as possible.

Figure 2.20 shows typical CMOS analog switch OFF-isolation as a function of frequency. From DC to several kilohertz, the switch has over 100dB isolation. As the frequency increases, an increasing amount of signal reaches the output. However, even at 1MHz, the switch still has nearly 70dB of isolation.

DYNAMIC PERFORMANCE CONSIDERATIONS: OFF ISOLATION

- OFF Isolation is Affected by External R and C Load



$$A(s) = \frac{s(R_{LOAD})(C_{DS})}{s(R_{LOAD})(C_{LOAD} + C_D + C_{DS}) + 1}$$

Figure 2.18

DYNAMIC PERFORMANCE CONSIDERATIONS: *OFF* ISOLATION VERSUS FREQUENCY

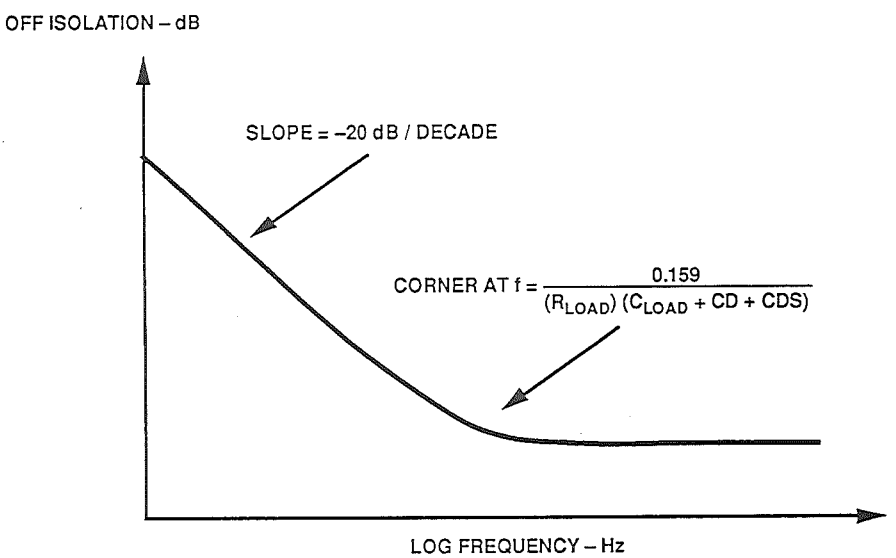


Figure 2.19

TYPICAL CMOS SWITCH *OFF* ISOLATION PERFORMANCE (ADG511/ADG512)

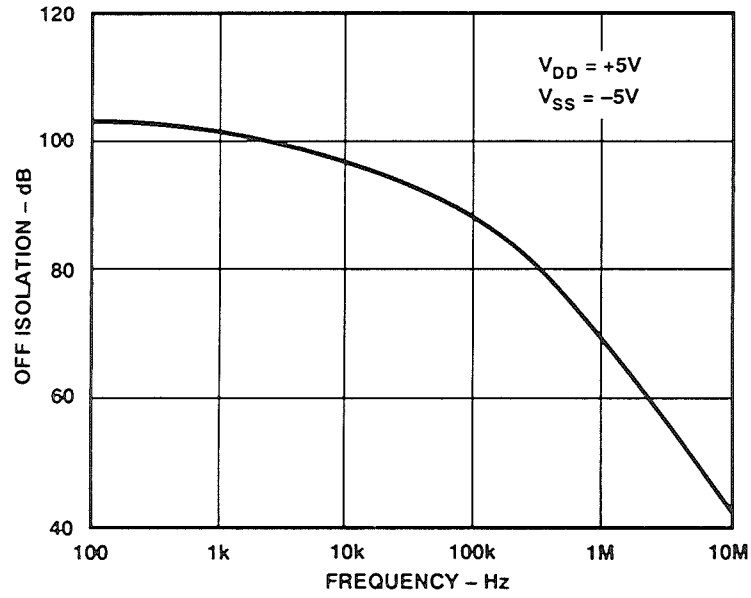


Figure 2.20

DYNAMIC PERFORMANCE CONSIDERATIONS: CHARGE INJECTION MODEL

- Step Waveforms of +/- (V_{dd} - V_{ss}) are Applied to C_Q, the Gate Capacitance of the Output Switches

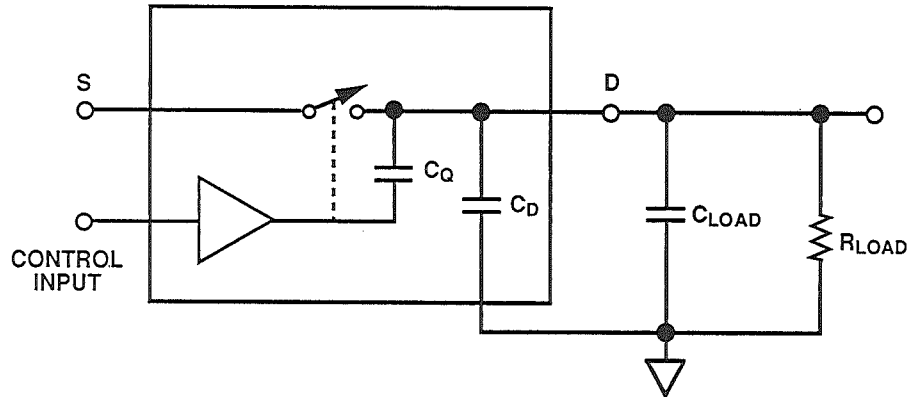


Figure 2.21

Another AC parameter that affects system performance is the charge injection that takes place during switching. Figure 2.21 shows the equivalent circuit of the charge injection mechanism.

When the switch control input is asserted, it causes the control circuit to apply a large voltage change (from V_{DD} to V_{SS}, or vice versa) at the gate of the MOSFET switch. This fast change in voltage injects a charge into the switch output through the gate-drain capacitance C_Q. The amount of charge coupled depends on the gate-drain capacitance.

The charge injection introduces a step change in output voltage when switching (refer to Figure 2.22). The change in voltage is a function of the amount of charge injected, which is in turn a function of the gate-drain capacitance.

Another problem caused by switch capacitance is the retained charge when channel switching which can cause transients in the switch output. Figure 2.23 illustrates the phenomenon.

EFFECTS OF CHARGE INJECTION

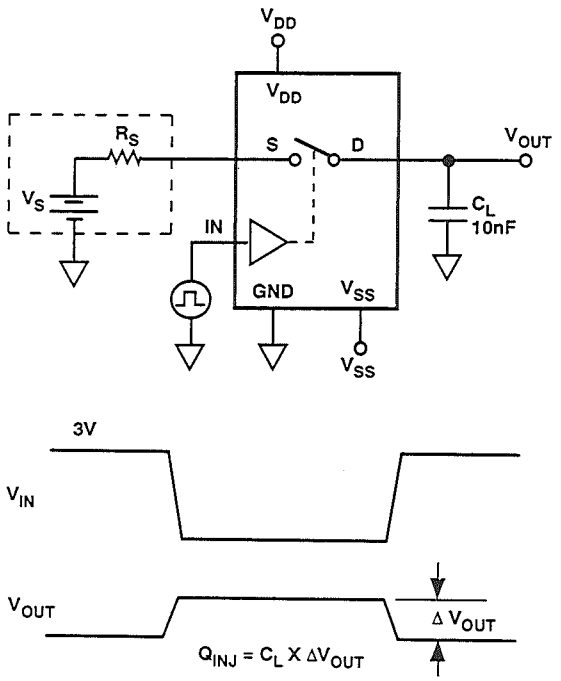


Figure 2.22

CHARGE COUPLING CAUSES DYNAMIC SETTLING NOISE WHEN MULTIPLEXING SIGNALS

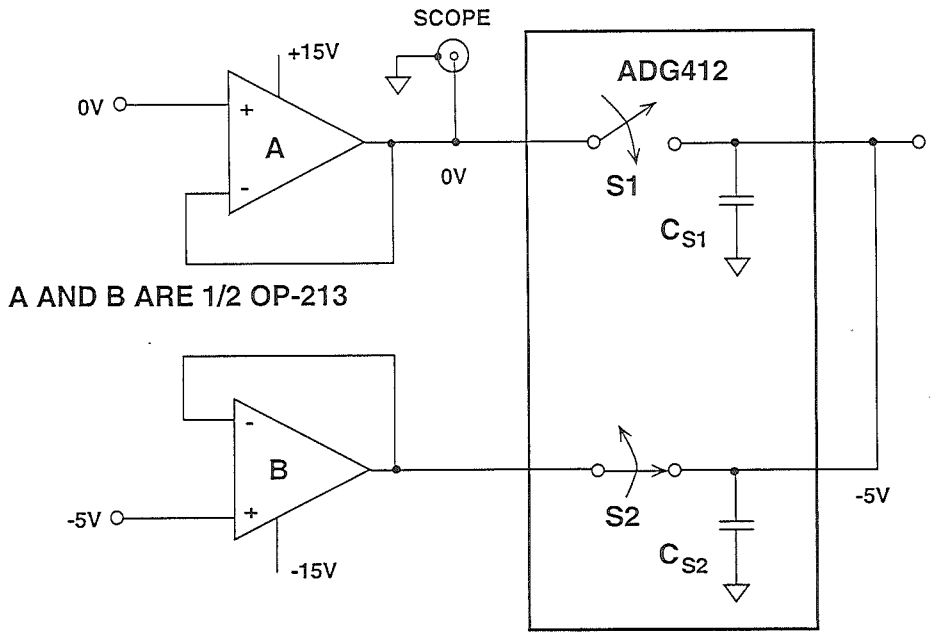


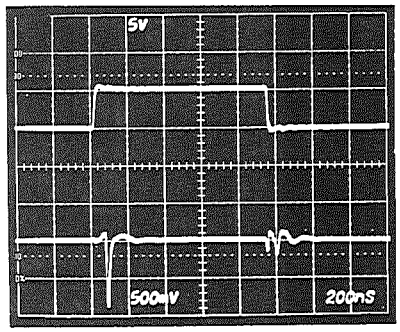
Figure 2.23

Assume that initially S2 is closed and S1 open. C_{S1} and C_{S2} are charged to -5V. As S2 opens, the -5V remains on C_{S1} and C_{S2}, as S1 closes. Thus the output of Amplifier A sees a -5V transient. The output will not stabilize until Amplifier A's output fully discharges C_{S1} and C_{S2} and settles to 0V. The scope photo in Figure 2.24 depicts this transient. The amplifier's transient load settling characteristics will be an important consideration when choosing the right device.

OUTPUT OF OP AMP SHOWS DYNAMIC SETTLING DUE TO CHARGE COUPLING

SWITCH CONTROL
5V/div.

AMPLIFIER A OUTPUT
500mV/div.



HORIZONTAL SCALE: 200ns/div.

Figure 2.24

Crosstalk is related to the capacitances between two switches. This is the C_{SS} shown in Figure 2.25.

CHANNEL-TO-CHANNEL CROSSTALK CONSIDERATION: EQUIVALENT CIRCUIT FOR ADJACENT SWITCHES

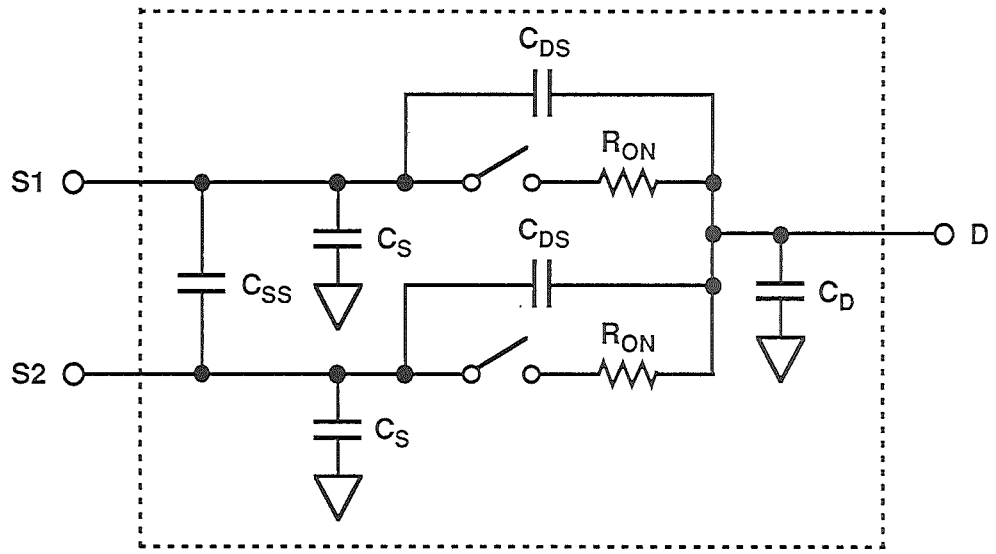


Figure 2.25

Figure 2.26 shows typical crosstalk performance of a CMOS analog switch.

CROSSTALK PERFORMANCE OF ADG511 SWITCH

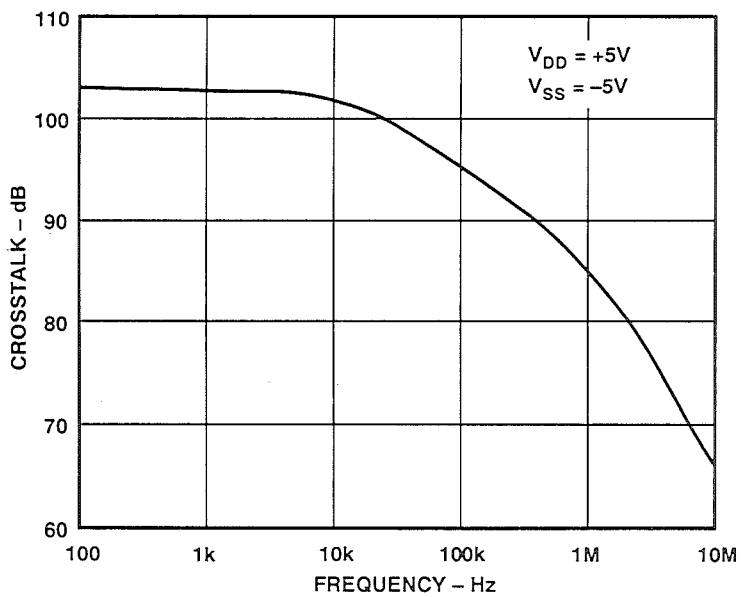
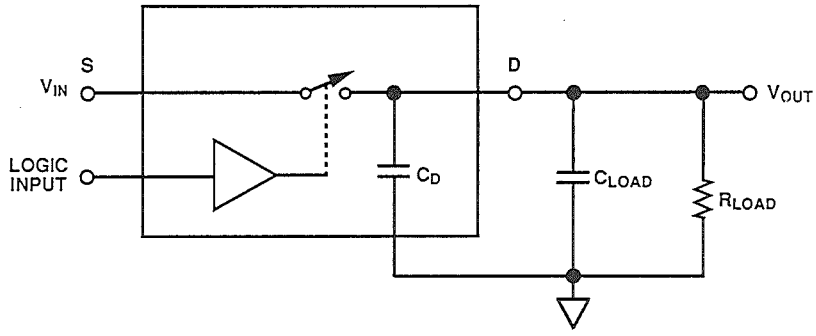


Figure 2.26

Finally, the switch itself has a settling time that must be considered. Figure 2.27 shows the dynamic transfer function.

DYNAMIC PERFORMANCE CONSIDERATIONS: SETTLING TIME

- Settling Time is the Time Required for the Switch Output Voltage to Settle to Within a Given Accuracy Band of the Final Value.



$$\text{OFF-TO-ON:}\quad t_{SETT} = t_{ON} + \left(\frac{R_{ON}R_{LOAD}}{R_{ON}+R_{LOAD}}\right)(C_{LOAD}+C_D)\left(-\ln\frac{\%ERROR}{100}\right)$$

$$\text{ON-TO-OFF:}\quad t_{SETT} = t_{OFF} + (R_{LOAD})(C_{LOAD}+C_D)\left(-\ln\frac{\%ERROR}{100}\right)$$

Figure 2.27

The settling time can be calculated because the response is a function of the switch and circuit resistances and capacitances. One can assume that this is a single-pole system and calculate the number of time constants required to settle to the desired system accuracy (Figure 2.28).

NUMBER OF TIME CONSTANTS REQUIRED TO SETTLE TO GIVEN ACCURACY BAND

RESOLUTION	% REQUIRED FOR 1/2 LSB	# OF TIME CONSTANTS
8 Bits	0.1953	6.24
10 Bits	0.0488	7.63
12 Bits	0.0122	9.01
14 Bits	0.0031	10.38
16 Bits	0.0008	11.74
18 Bits	0.0002	13.12

Figure 2.28

TRENCH-ISOLATED LC²MOS ANALOG SWITCH FAMILY OFFERS MANY BENEFITS

Analog Devices uses trench-isolation technology to produce its LC²MOS analog switches. The process reduces the latchup susceptibility of the device, the junction capacitances, increases switching time and leakage current, and extends the analog voltage range to the supply rails.

ADG411/ADG511 FAMILY OF TRENCH-ISOLATED LC²MOS ANALOG SWITCHES

- Latch-Up Proof
- Analog Signal Range to Supply Rails
- Fast Switching Times
- Break Before Make Switching
- Low ON-Resistance
- Low Leakage

Figure 2.29

Figure 2.30 shows the cross-sectional view of the complementary CMOS structure. The buried oxide layer and the side walls completely isolate the substrate from each transistor junction. Therefore, no reverse-biased PN junction is formed. Consequently the bandwidth-reducing capacitances and the possibility of SCR latchup are greatly reduced.

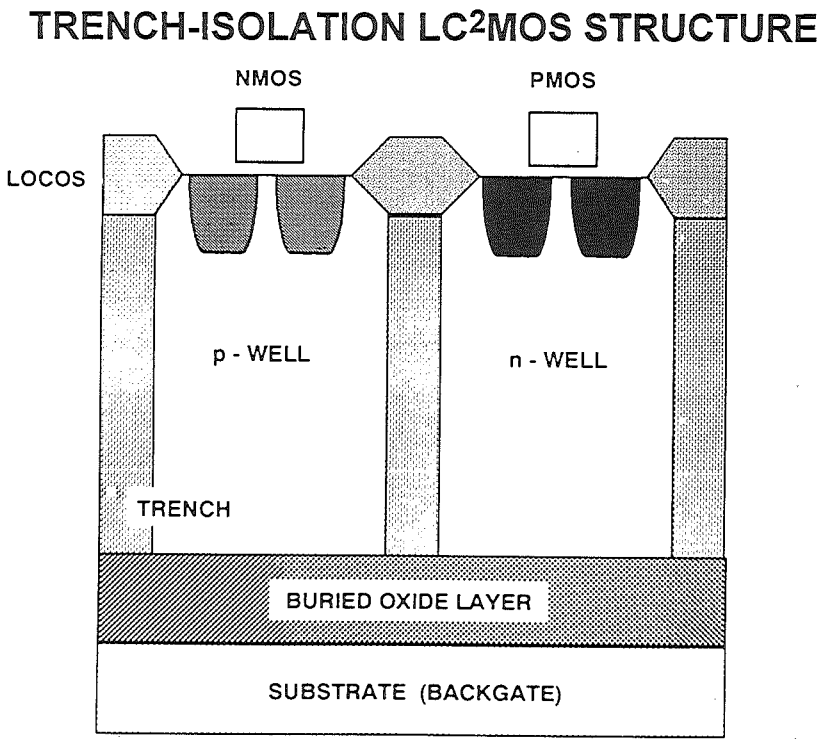


Figure 2.30

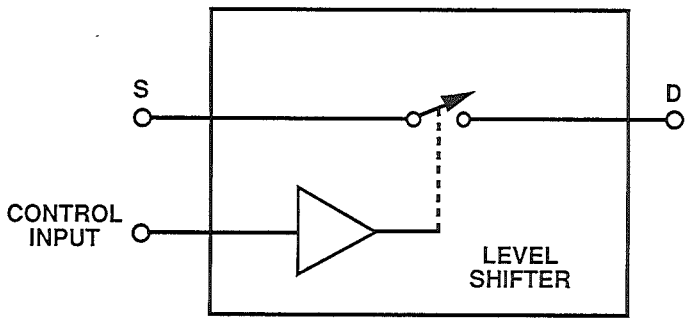
APPLYING THE ANALOG SWITCH

Switching time is an important consideration in applying analog switches, but switching time should not be confused with settling time. ON and OFF times are simply a measure of the propagation delay from the control input to the toggling of the switch and are largely caused by time delays in the drive and level-shift circuits.

When a CMOS multiplexer switches inputs to an inverting summing amplifier, it should be noted that the ON-resistance, as well as its nonlinear change as a function of input voltage, will cause errors (refer to Figure 2.32). If the resistors are large the switch leakage current may introduce error. Small resistors minimize leakage current error but increase the error due to the finite value of R_{ON}.

APPLYING THE ANALOG SWITCH: DYNAMIC PERFORMANCE CONSIDERATIONS

- t_{on} and t_{off} should not be confused with settling time.



- t_{on} and t_{off} are simply a measure of the propagation delay from control input to operation of the analog switch. It is caused by time delays in the drive / level-shifter logic circuitry.

Figure 2.31

APPLYING THE ANALOG SWITCH: UNITY GAIN INVERTER WITH SWITCHED INPUT

- Problem: Effect of ΔR_{ON} versus ΔV_S on Circuit Linearity.
- R_{ON} variation due to ΔV_{IN} degrades linearity of V_{OUT} relative to V_{IN}

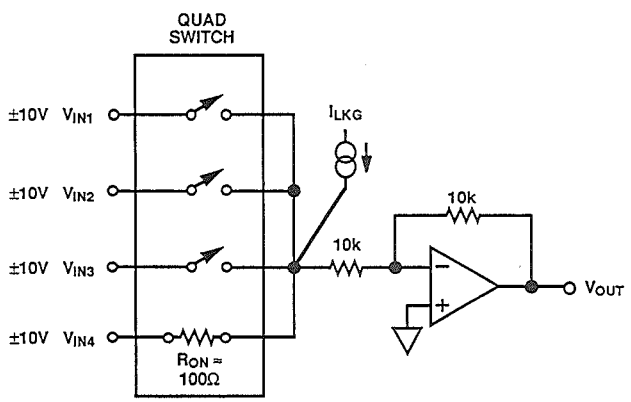
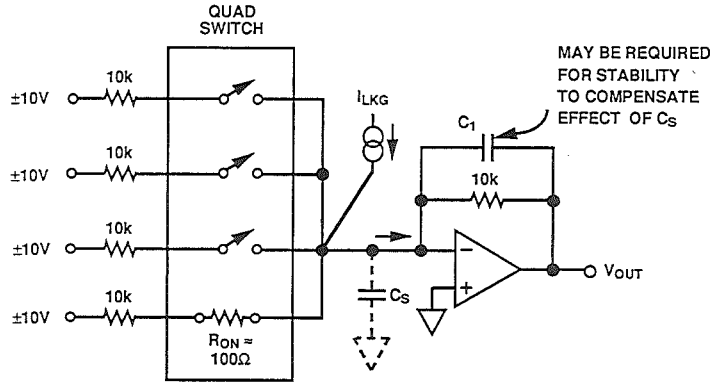


Figure 2.32

To minimize the effect of R_{ON} change due to the change in input voltage, it is advisable to put the multiplexing switches at the op amp summing junction as shown in Figure 2.33. This ensures the switches are only modulated with about ±100mV rather than the full ±10V - but a resistor is required for each input leg.

APPLYING THE ANALOG SWITCH: MINIMIZING THE INFLUENCE OF ΔV_S (AND THUS ΔR_{ON})



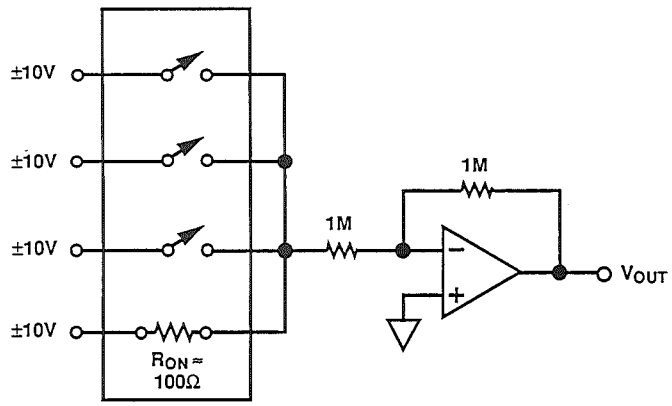
- Connecting the Switch at the Summing Point
- The switch only sees ± 100mV, not ± 10V. R_{ON} variation is minimized, and V_{OUT} accuracy is improved.

Figure 2.33

It is important to know how much parasitic capacitance has been added to the summing junction as a result of adding a multiplexer because any capacitance added to that node introduces phase shift to the amplifier closed loop response. If the capacitance is too large, the amplifier may become unstable and oscillate. A small capacitance, C1, across the feedback resistor may be required to stabilize the circuit.

The finite value of R_{ON} is a significant error source. The gain-set resistors should be at least 1,000 times larger than the switch ON-resistance to guarantee 0.1% gain accuracy. Higher values yield greater accuracy, but the proper selection of C1 is critical to maintain stability.

APPLYING THE ANALOG SWITCH: MINIMIZING THE INFLUENCE OF ΔV_S (AND THUS ΔR_{ON})

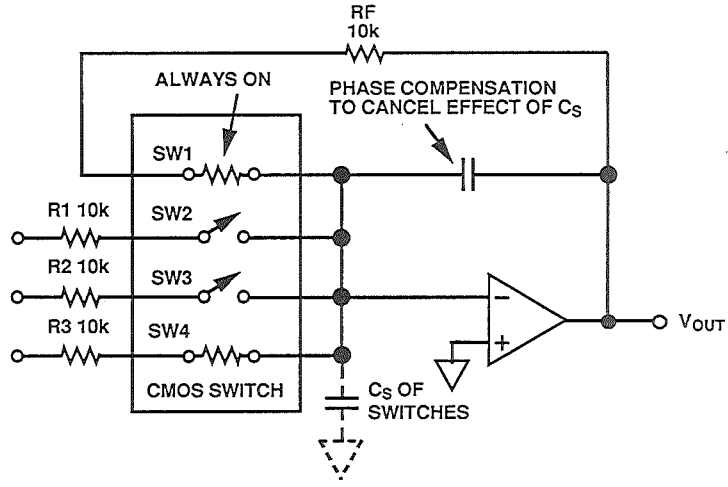


- Using Larger Values of Resistance
- R_{ON} Variation due to Input Signal is Small Compared to the 1MΩ Switch Load. Effect on Transfer Accuracy is Minimized.
- Bias Current and Leakage are now very important

Figure 2.34

A better method of compensating for R_{ON} is to place one of the switches in series with the feedback resistor of the inverting amplifier as shown in Figure 2.35. It is a safe assumption that the multiple switches, fabricated on a single chip, are well-matched in absolute characteristics and tracking over temperature. Therefore the amplifier closed loop gain stable at unity gain, since the total feedforward and feedback resistors are matched.

APPLYING THE ANALOG SWITCH: MINIMIZING THE INFLUENCE OF R_{ON} AND ΔR_{ON} VERSUS TEMPERATURE ON CIRCUIT ACCURACY



■ Switch in Series With Feedback Resistor Compensates for Gain Error.

Figure 2.35

The best multiplexer drives the non-inverting input of the amplifier. The high input impedance of the non-inverting input eliminates the errors due to R_{ON}. (Figure 2.36)

When multiplexing signals into an ADC, particularly the successive-approximation (SAR) type, it is advisable to place a buffer between the switch output and the input of the converter. The transient currents at the ADC input produced by the conversion process (DAC switching) are absorbed by a drive amplifier of sufficiently low output impedance and high bandwidth. Driving the ADC directly with the switches will produce significant conversion errors due to the finite R_{ON} resistance.

APPLYING THE ANALOG SWITCH: MINIMIZING THE INFLUENCE OF ΔV_S (AND THUS ΔR_{ON}) NON-INVERTING SOLUTION

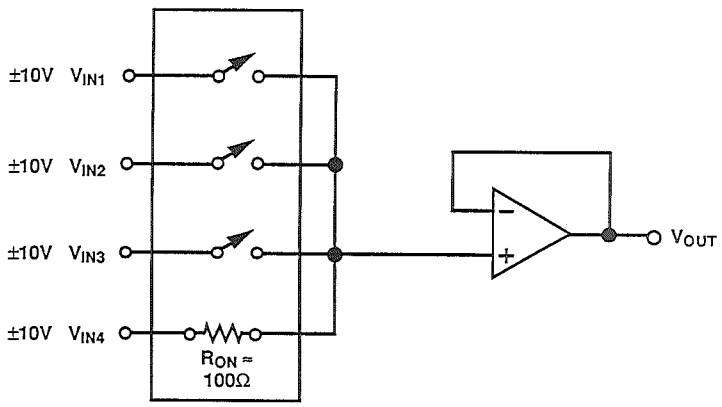


Figure 2.36

APPLYING THE ANALOG SWITCH: BUFFER THE MUX OUTPUT INTO AN ADC TO MINIMIZE GAIN ERROR AND PROVIDE ISOLATION

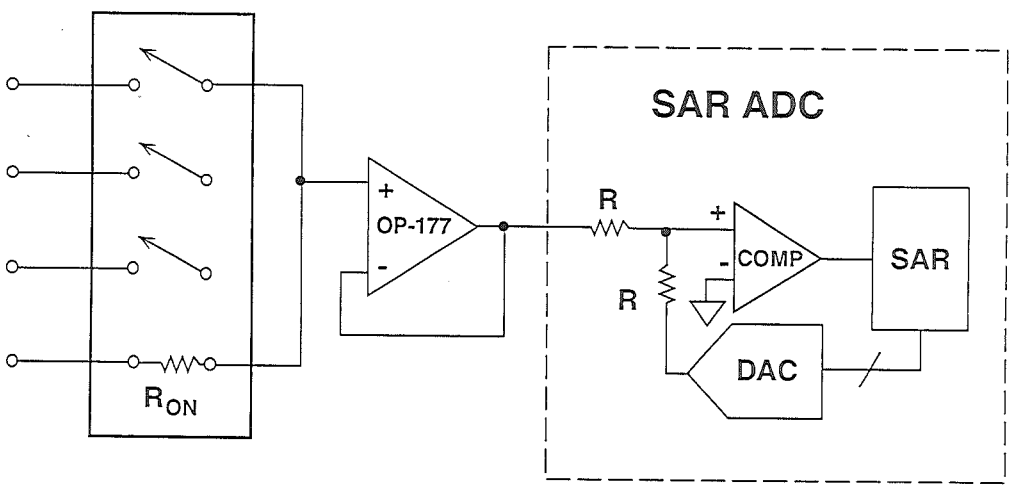


Figure 2.37

SECTION 3

PROGRAMMABLE GAIN AMPLIFIERS