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# SYSTEM APPLICATIONS GUIDE

## SECTION 18

# SIGNAL COMPUTING APPLICATIONS IN COMMUNICATIONS

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## INTRODUCTION TO SIGNAL COMPUTING

*Bill Schweber*

Signal Computing is a technology framework and business model which recognizes that DSP-based signal-processing applications can benefit substantially by combining sets of high-performance processor- and interface chips with powerful, sophisti-

cated algorithms from independent third parties. Employing open designs and architectures, signal computing is characterized by well-defined levels of standardization that carefully define the hardware and software roles and the layers that make them up.

### SIGNAL COMPUTING: A TECHNOLOGY AND BUSINESS MODEL FOR REALTIME SIGNAL PROCESSING SOLUTIONS

- **Hardware Chipsets:**  
Analog I/O (Codecs), DSP Processors, ASIC Interface Chips
- **Software Algorithms:** Independent Algorithm Vendors (IAVs)
- **Manufacturing Design Kits**
- **Typical Applications:**  
Modems, Speech Processing, Music Processing, Digital Mobile Radio, Image Processing, Multimedia

This allows companies—both chip- and software vendors and OEM and system designers—to participate at the level where each brings maximum “value-added” expertise to the application. The chip supplier furnishes standard high-performance, low-cost ICs; the market-oriented algorithm developer provides the standard configurable software that produces the desired electronic performance from the chips; and the OEM designer integrates them into a system specialized to meet the performance needed within his market niche. This environment avoids saddling the designer with the job of recreating all aspects of the overall design. An example of a signal computing product, a telecommunications modem chipset and algorithm toolkit, is discussed later in this section.

Low-cost digital signal processing is an “enabling” function, allowing broad expansion of *real-time* signal processing, through the combination of software and hardware defined as “signal computing.” Signal computing is characterized by the synchronized execution of algorithms on *real-time* data streams. It is quite distinct from the use of DSP, or any processor, in conventional numerical acceleration, where computations and graphics are simply speeded up—but still occur off-line: images are redrawn “more quickly” on the graphics workstation screen, but even though waiting time is reduced, it is still palpable.

In contrast to numerical acceleration, signal computing involves real-time

signal processing with a straightforward criterion: if it isn’t fast enough for the real-time requirements and synchronization of the application, it simply isn’t fast enough. Speeded-up processing alone doesn’t help if the real-time constraint can’t be satisfied.

End users see signal computing functionality in two distinct forms. First, personal computers (whatever actual form they take) can have signal computing circuitry built in to add those real-time functions (involving intensive computation) that the user needs to access, such as audio, video, and telecommunications capabilities. The software to exercise the hardware for the application must be as available as—or more available than—the hardware, and is generally downloaded into RAM as needed from disk. In this way, new functions can execute on the same hardware, or existing functions can be enhanced with new, more efficient algorithms or incorporate newly defined standards.

Second, in a large number of applications, the signal-computing capabilities are *embedded*, in an essentially non-reprogrammable design, for dedicated use. For example, voice recognition in home “appliances” will be implemented by a carefully defined, fixed-function, minimum-cost subsystem that is optimized for the application, with code in ROM.

## APPLICATIONS OF SIGNAL COMPUTING

As low-cost DSP ICs and interface chips, and the software to drive them, are becoming more widely available, signal computing is spurring a mind-boggling expansion of real-time applications that work with real-world information and signals: voice recognition (including voice-programmed operation of mundane products such as VCRs); spoken-word-to-text and spoken-word-to-spoken-word language translation; personal communications systems; fax-to-OCR-to-voice (so that incoming faxes received at your office can be passed to you over the phone); and voice synthesis that is tailored to the application and the listener. CD quality (44-kbps) will be the standard used for audio and music, except in standard voiceband applications, where the higher sampling rates make less sense.

Video has a place among signal computing applications. Under the broad title

of “multimedia”—perhaps better characterized as “mixed media”—it allows for integration of audio and video where appropriate. This means that a video signal, along with its audio channel, can be compressed, stored, transmitted, and recreated with perfect synchronization. Video telephones and conferencing are in the cards—especially for business applications, as a ready substitute for costly and time-consuming travel. Video segments can be stored as easily as typed text is now, and then incorporated into picture-and-sound documents and messages. Video processing allows users to perform editing on images, reducing blurring, improving sharpness, and performing other enhancements with the ease-of-use and power of today’s word processors.

## SIGNAL COMPUTING HARDWARE

The early days of the microprocessor were characterized by a highly fragmented industry without an architectural standard. Each microprocessor-based design was sufficiently different from others that economies of design standardization could not be realized. The wide acceptance and cloning of the PC-platform changed all that; the core hardware design of each PC is virtually the same. Although each PC design today may use different specific ICs or levels of IC integration, the overall functionality is identical, with the same signal interface functions at the block diagram level.

A similar thing is happening around the signal-computing model. “Reference” designs—complete working schematics and block diagrams—are being made available as chips or sets of chips to provide a standard set of circuit functions. Engineers who use DSP, whether embedded in systems or available with PC-like flexibility, can choose the reference design that has the capabilities they need—and seek out those vendors whose components can implement the design most cost-effectively. Scalable architectures allow more-powerful DSPs (faster clock, more

memory) to be used as needed with minimum system-design disruption.

For signal computing, the hardware system consists of three low-cost blocks integrated as a "datapump": the *DSP*, as the controller and central processor, the *analog input/output interface* to the

signal source or sink (Examples include the public switched telephone network (PSTN), an audio source and its corresponding output, or a video source and its output), and the *signal processing algorithm* (usually downloaded and resident in *RAM*).

### GENERALIZED SIGNAL COMPUTING HARDWARE BLOCK DIAGRAM

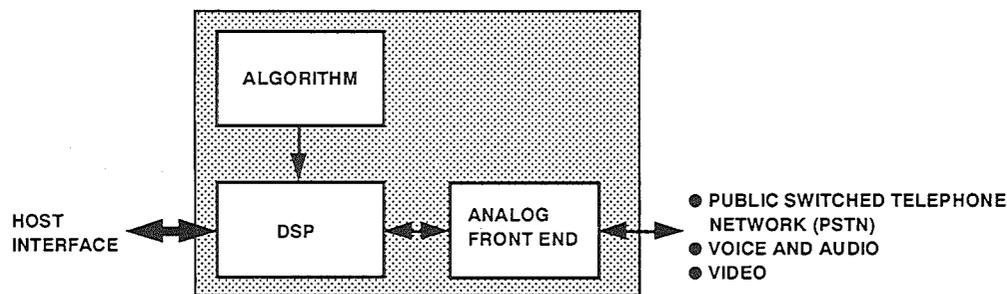


Figure 18.2

This datapump supports a host interface for PC-based applications. The DSP and analog front end are available as chipsets, specifically designed to work with each other and compatible with

available algorithms. For embedded, dedicated applications the host interface is not needed, and the algorithm is in ROM.

SOFTWARE: OPEN ARCHITECTURE THE KEY

At present, much DSP-related software is custom-fit to the application. This includes the application code itself, as well as the operating system (if any), and the “hooks” to the rest of the system. Libraries and library calls to these libraries are available, but they lack the high degree of standardization found in the PC world with well-defined BIOS and operating system, and related interfaces.

Fortunately, many of the software elements needed to encourage the growth of creative algorithms and software are now taking shape. The final structure is roughly analogous to

the 7-layer OSI telecommunications model (Figure 18.3), which has worked very well at providing flexibility to users by assigning implementation responsibility in well defined blocks, while at the same time assuring transparency between layers. As a result, vendors can offer unique, innovative solutions within each layer—solutions that enhance performance or reduce cost of the total system, yet do not adversely affect the total system structure. While this process, when we discuss its details, may sound complicated, it does indeed model a working technology.

SIGNAL COMPUTING LAYERED SOFTWARE STRUCTURE

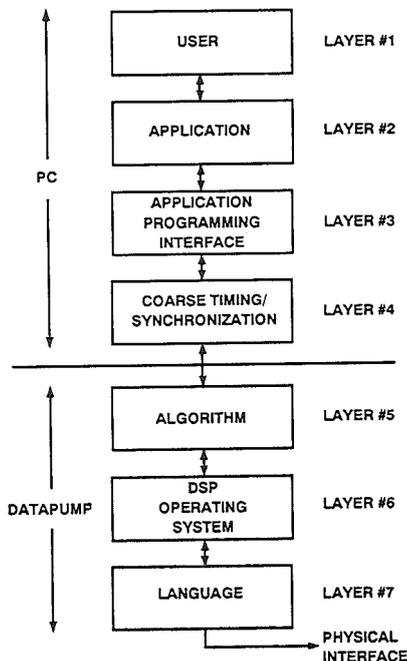


Figure 18.3

The key to this layer structure is its *open architecture*. Each interface between layers is well-defined and distinct. Individual algorithm vendors and complementary software vendors are free to offer their solutions in competition, to meet the challenges of the market and the application. Algorithm vendors provide algorithms to solve specific application needs, such as image compression, audio compression, or telecommunication interface. Software vendors convert these algorithms to code which actually implements these algorithms on specific DSP and chipset platforms.

The “best” hardware and software solution for a particular application is thus determined by the competitive market, since all vendors are free to offer their product on whatever sale or licensing terms they choose. Although DSP IC vendors offer proprietary chip solutions focused on specific market needs—and will continue to do so—the ferment in the open-system marketplace, involving vendors of ICs, software, and algorithms, will encourage a wider range of innovative solutions.

The upper four layers of the model reside in the PC and its microprocessor.

### WHAT IT ALL MEANS

What does all this mean for the industry? It means that new categories of DSP and signal-computing vendors emerge (Figure 18.4): the independent algorithm vendor, the software vendor, and the DSP O/S supplier. Each provides solutions designed for specific

At the top layer is the user interface, for example screen and keyboard. Immediately below is the application, which defines the broad needs of the user. The application program interface (API), layer #3, is where the broadly defined needs are translated into more-specific instructions and service requests. Layer #4 is the PC's operating system, which provides coarse timing, prioritization, synchronization, and scheduling among the various applications requesting service.

The lower three layers, #5 through 7, are implemented by the signal-computing DSP chipset and algorithm. For embedded, dedicated applications, are the only layers needed. The *algorithm* layer defines how the specific application needs will be implemented in real time. The lowest layer, *language*, provides the set of instructions for the DSP and analog front end as executable code to actually implement the requirements of the application. The execution of these instructions, with fine resolution timing and detailed resource management, is controlled by the *real-time operating system*.

applications, using well-specified open interfaces and architectures at each boundary. The vendors do not have to offer complete solutions at all layers: they need only compete to provide a solution to a part of the problem—for a specific layer.

## SIGNAL COMPUTING BUSINESS MODEL

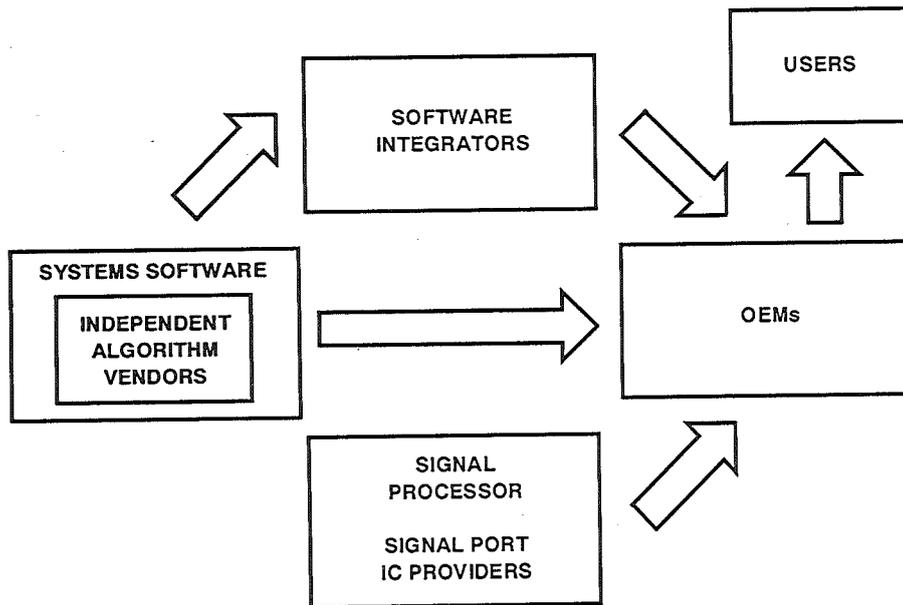


Figure 18.4

Since these independent vendors provide support for all the major DSP families used in signal computing, design engineers are not tied exclusively to one IC vendor. Small, innovative companies also have clear opportunities in the market, since they can leverage their efforts via the path provided by the well-defined layers and open architecture.

What does this mean for the design engineer who must assemble a complete system? In the future, he or she will choose among the various vendors to find a suitable chipset, along with appropriate operating system and algorithms. The project engineer's principal focus will be on system integration. For the many applications with industry-wide standards (for example, JPEG and MPEG image compression and telecommunications), algorithm vendors will offer a variety of solutions. For more-specialized, less-standard

niche applications, where there may be only a handful of vendors (of not-totally suitable solutions for the specific problem), the design engineer may find it more cost-effective to develop the algorithm and code as part of the project.

Once the algorithm has been selected, the design engineer can choose between buying the code to implement it, or writing the code as part of the project. Again, the choice depends on the application and the number of vendors. For some applications—such as telecom or voice and image compression—“validated” (tested and verified) code will be available and preferable.

Here's an example: suppose a company that designs answering machines, with expertise in telephone-system line format and protocol, wants to develop a DSP-based, no-moving-part answering machine. The designer can buy suitable algorithms for voice compression, add to

these the unique features needed in an answering machine (dial-tone recognition, for example), and so produce a product leveraging the areas of greatest competence while not "re-inventing the wheel" of voice compression software.

Signal computing is bringing DSP, a specialty technology, into the mainstream of computing applications. The PC platform brought processor power to both PCs and embedded applications, and created new approaches and busi-

ness/technology models for system hardware/software design and integration. Similarly, the advent of open architectures and structured layers offers the same opportunity to the processing of real-time signals with DSP as the engine.

In the following section, the technical details of high performance modems will be discussed as well as another important application of signal computing in Digital Mobile Radio.

## HIGH PERFORMANCE MODEMS FOR DATA TRANSMISSION

*Walt Kester*

Modems (*Modulator/Demodulator*) are widely used to transmit and receive digital data over analog channels, especially, but not exclusively over the Public Switched Telephone Network (PSTN). Although the data to be transmitted is digital, the telephone channel is designed to carry voice signals having a bandwidth of approximately 300 to 3300Hz. The telephone transmission channel suffers from delay distortion, noise, crosstalk, near-end and far-end echoes, and other imperfections listed in Figure 18.5. While certain levels of these signal degradations are perfectly acceptable for voice communication, they can cause high error rates in digital data transmission. The fundamental purpose of the transmitter portion of the modem is to prepare the digital data for transmission over the analog voice line. The purpose of the receiver portion of the modem is to receive the signal which contains the analog representation of the data, and reconstruct the original digital data

with an acceptable error rate. High performance modems make use of digital computing techniques to perform such functions as modulation, demodulation, error detection and correction, equalization, and echo cancellation.

A block diagram of a telephone channel is shown in Figure 18.6. Most voiceband telephone connections involve several connections through the telephone network. The 2-wire subscriber line available at most sites is generally converted to a 4-wire signal at the telephone central office. The signal is converted back to a 2-wire signal at the far-end subscriber line. The 2- to 4-wire interface is implemented with a circuit called a *hybrid*. The hybrid intentionally inserts impedance mismatches to prevent oscillations on the 4-wire trunk line. The mismatch forces a portion of the transmitted signal to be reflected or echoed back to the transmitter. This echo can corrupt data the transmitter receives from the far-end modem.

## IMPERFECTIONS IN THE TELEPHONE CHANNEL

- Attenuation
- Bandwidth Flatness
- Harmonic Distortion
- Echoes (Near-End and Far-End)
- Phase Jitter
- Phase Distortion, Group Delay Variation
- Noise
- Impedance Mismatches
- Frequency Offset
- Phase and Gain Hits

Figure 18.5

## TELEPHONE CHANNEL BLOCK DIAGRAM

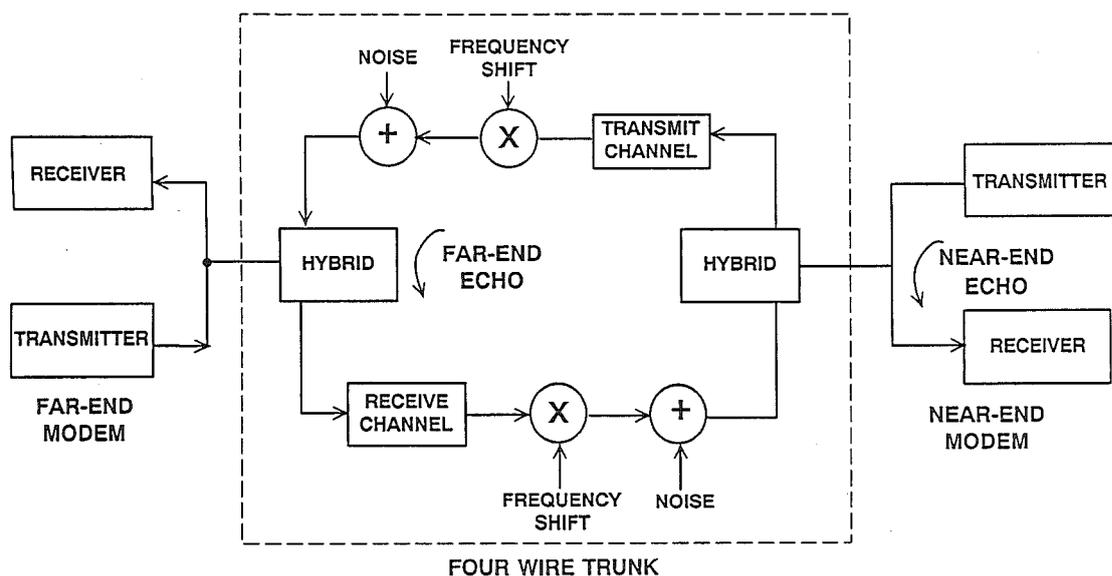


Figure 18.6

*Half-duplex* modems are capable of passing signals in either direction on a 2-wire line, but not simultaneously. *Full-duplex* modems operate on a 2-wire line and can transmit and receive data simultaneously. Full-duplex operation requires the ability to separate a receive signal from the reflection (echo) of the transmitted signal. This is accomplished by assigning the signals in the two directions different frequency bands separated by filtering, or by echo canceling in which a locally synthesized replica of the reflected transmitted signal is subtracted from the composite receive signal.

There are two types of echo in a typical voiceband telephone connection. The first echo is the reflection from the near-end hybrid, and the second echo is from the far-end hybrid. In long distance telephone transmissions, the transmitted signal is heterodyned to and from a carrier frequency. Since local oscillators in the network are not exactly matched, the carrier frequency of the far-end echo may be offset from the frequency of the transmitted carrier signal. In modern applications this shift can affect the degree to which the echo signal can be canceled. It is therefore desirable for the echo canceller to compensate for this frequency offset.

For transmission over the telephone voice network, the digital signal is modulated onto an audio sinewave carrier, producing a modulated tone signal. The frequency of the carrier is chosen to be well within the telephone band. The transmitting modem modulates the audio carrier with the transmit data signal, and the receiving modem demodulates the tone to recover the receive data signal.

The baseband data signal may be used to modulate the amplitude, the frequency, or the phase of the audio carrier, depending on the data rate required. These three types of modulation are known as amplitude shift keying (ASK), frequency shift keying (FSK), and phase shift keying (PSK). In its simplest form the modulated carrier takes on one of two states - that is, one of two amplitudes, one of two frequencies, or one of two phases. The two states represent a logic 0 or a logic 1.

Low- to medium-speed data links usually use FSK up to 1200 bits/s. Multiphase PSK are used for 2400 bits/s and 4800 bits/s links. PSK utilizes bandwidth more efficiently than FSK but is more costly to implement. ASK is least efficient and is used only for very low speed links (less than 100 bits/s). For 9600 bits/s, a combination of PSK and ASK is used, known as Quadrature Amplitude Modulation (QAM). Better performance at 9600 bits/s can be achieved using Trellis Code Modulation (TCM). For 14400 bits/s, Trellis Code Modulation (TCM) is essential.

Assuming 7-bit ASCII and 4 bits/character overhead (start, parity, and two stop bits), a data transmission rate of 300 bits/s translates to approximately 27 characters/s. This is faster than a person can type but is too slow for transferring large files or for many applications requiring graphics.

The International Telegraph and Telephone Consultative Committee (generally known as the CCITT) has established standards and recommendations for fax machines and modems which are given in Figure 18.8.

## MODULATION METHODS FOR MODEMS

- Amplitude Shift Keying (ASK): Up to 100 bits/s
- Frequency Shift Keying (FSK): Up to 1200 bits/s
- Phase Shift Keying (PSK) and Differential Phase Shift Keying (DPSK): Up to 4800 bits/s
- Quadrature Amplitude Modulation (QAM): Up to 9600 bits/s
- Trellis Code Modulation (TCM): Up to 14400 bits/s

Figure 18.7

## CCITT MODEM AND FAX STANDARDS

CCITT Standard	Speed (bits/s)	Half Duplex/ Full Duplex/ Echo Cancellation	Modulation Method
V.17 (FAX)	14400	Half Duplex	TCM
V.21	300	Full Duplex	FSK
V.22	1200	Full Duplex	DPSK
V.22bis	2400	Full Duplex	QAM
V.23	1200/75rev	Half Duplex	FSK
V.24	RS-232 Serial Connection		
V.27ter (FAX)	4800	Half Duplex	DPSK
V.29 (FAX)	9600	Half Duplex	QAM
V.32	9600	Full Duplex (EC)	QAM
V.32bis	14400	Full Duplex (EC)	TCM

Figure 18.8

### **V.32 Modem Overview**

The goal in designing high performance modems is to achieve the highest data transfer rate possible over the channel used (normally the PSTN) and avoid the expense of using dedicated conditioned private telephone lines. The V.32 recommendation describes a full-duplex (simultaneous transmission and reception) synchronous modem that operates on the Public Switched Telephone Network (PSTN). The V.32 modem communicates at a rate of 9600 bits/s and may utilize either quadrature amplitude modulation (QAM) or Trellis Code Modulation (TCM). Higher performance (lower bit-error-rates) may be

achieved using TCM. In TCM, four-bit symbols (bauds) modulate a carrier frequency of 1800Hz with a modulation rate of 2400 bauds/s. The modulation of 4-bit symbols at a rate of 2400 symbols/s yields the 9600 bits/s specification. These 4-bit symbols are transmitted using 32-state trellis-encoded QAM. The trellis encoding provides an extra bit per symbol for forward error correction. This additional bit dramatically increases the noise performance of the modem. Characteristics of V.32 and V.32bis modems are summarized in Figure 18.9.

### **V.32 / V.32bis MODEM CHARACTERISTICS**

- 9600 bits/second Bit Rate on PSTN (V.32)
- 14400 bits/second Bit Rate on PSTN (V.32bis)
- 1800Hz Carrier Frequency (Transmit and Receive)
- 4 Bits/Symbol, 2400Hz Symbol Rate
- 32-QAM, Trellis Coded, 4 Bit Data + Redundancy Bit
- Transmit/Receive Isolation Using Echo Cancellation
- Extensive Use of DSP Techniques

**Figure 18.9**

A simplified block diagram for a V.32 modem is shown in Figure 18.10. The diagram shows that the bulk of the signal processing is done digitally. Both

the transmit and receive portions of the modem subject the digital signals to a number of DSP algorithms which can be run efficiently on modern processors.

### V.32 MODEM SIMPLIFIED BLOCK DIAGRAM

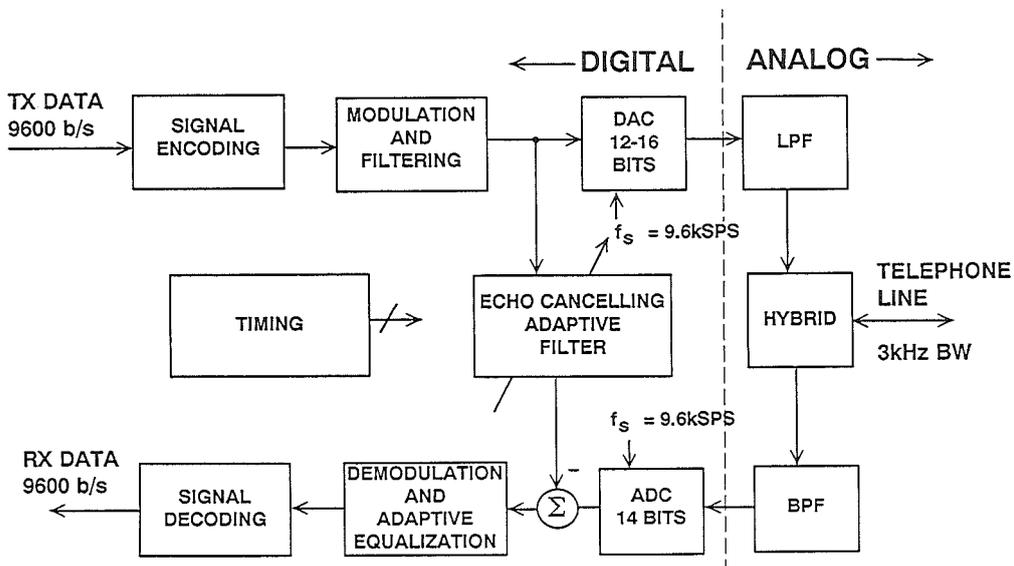


Figure 18.10

#### V.32 Modem Transmitter

A block diagram of the V.32 transmitter is shown in Figure 18.11. The input serial bit stream is first scrambled. Scrambling takes the input bit stream and produces a pseudo-random sequence. The purpose of the scrambler is to whiten the spectrum of the transmitted data. Without the scrambler, a long series of identical symbols could cause

the receiver to lose carrier lock. Scrambling makes the transmitted spectrum resemble white noise, to utilize the bandwidth of the channel more efficiently, makes carrier recovery and timing synchronization easy, and makes adaptive equalization and echo cancellation possible.

## V.32 MODEM TRANSMITTER

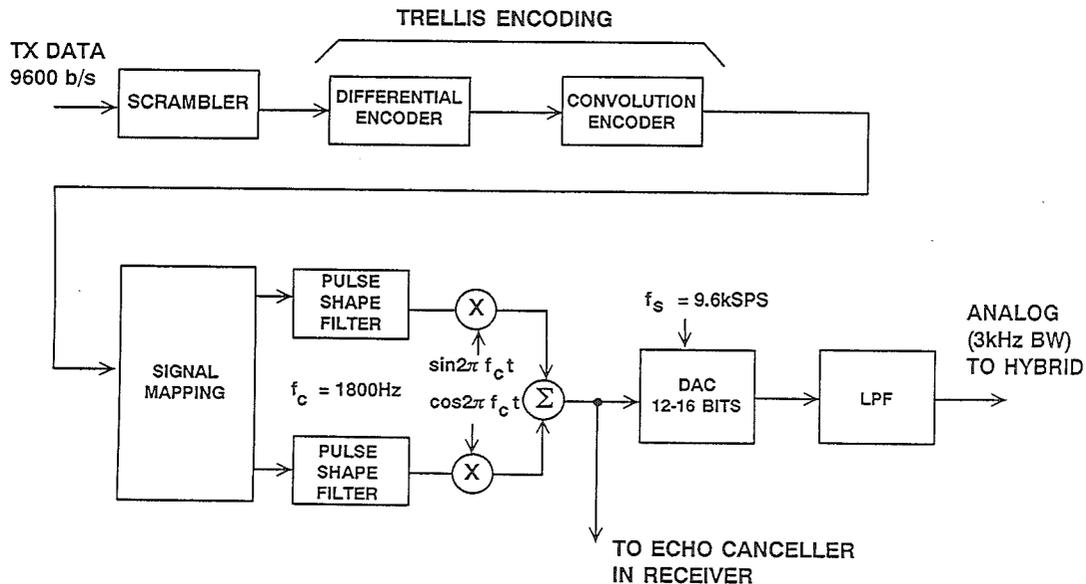


Figure 18.11

The scrambled bit stream is divided into groups of four bits. The first two bits of each 4-bit group are first differentially encoded and then convolutionally encoded. This produces a 5-bit trellis-coded symbol in which the extra bit is a redundantly coded bit.

The 5-bit symbols are then mapped into the signal space using trellis-coding as defined in the V.32 recommendation. The signal space mapping produces two coordinates, one for the real part of the QAM modulator and one for the imaginary part. A diagram of the resulting V.32 signal constellation is shown in Figure 18.12.

Used prior to modulation, the digital pulse shaping filters attenuate frequencies above the Nyquist frequency that are generated in the signal mapping process. These filters are designed to have zero crossings at the appropriate frequencies to cancel intersymbol interference. The pulse shape filter is based on the impulse response of a raised cosine function as shown in Figure 18.13. The value  $T$  is equal to the reciprocal of the symbol rate (2400 symbols/second). For a sampling rate of 9600Hz and a symbol rate of 2400Hz, a 17-tap FIR filter can be used.

V.32 MODEM SIGNAL CONSTELLATION

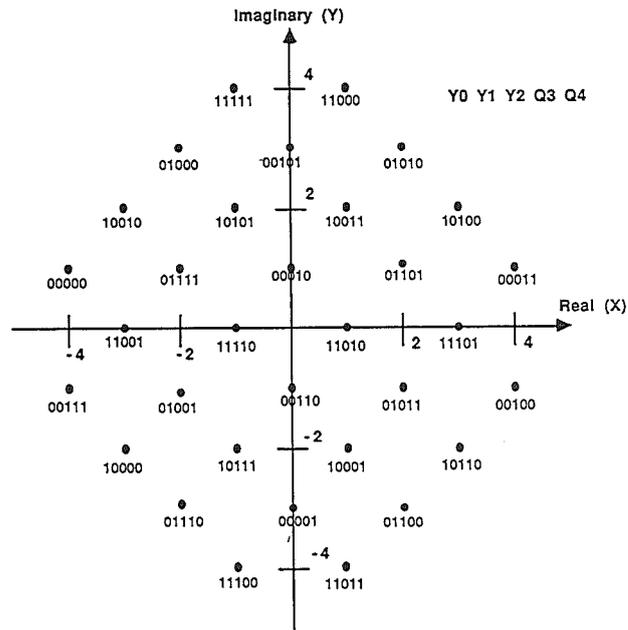


Figure 18.12

PULSE SHAPING FILTER IMPULSE RESPONSE

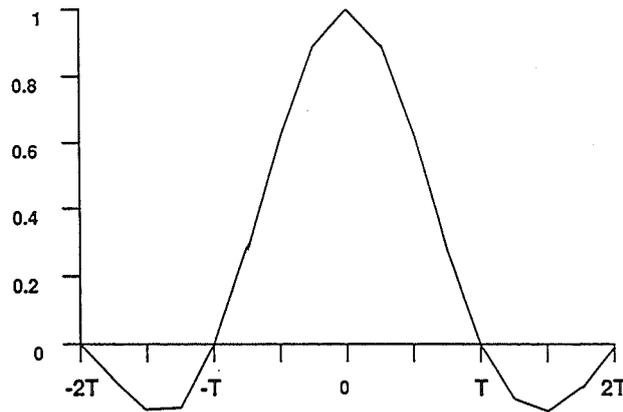


Figure 18.13

The modulation for the V.32 coding scheme is quadrature amplitude modulation (QAM). Modulation is easily implemented in modern DSP processors. The process of modulation requires the access of a sine or cosine value, the access of an input symbol (x or y coordinate) and a multiplication. The parallel architecture of the ADSP-2101 permits all three operations to be performed in a

single 80ns cycle (60ns for the ADSP-2116).

The output of the digital QAM modulator drives a 12- to 16-bit DAC which is updated at 9.6kSPS. The output of the DAC is passed through a 3.5kHz analog lowpass filter and to the 2-wire telephone line for transmission over the PSTN.

### V.32 Modem Receiver

A block diagram of the V.32 modem receiver is shown in Figure 18.14. The receiver is made up of several functional blocks: the input antialiasing filter and ADC, a demodulator, an adaptive equalizer, a Viterbi decoder, an echo canceller, a differential decoder, and a descrambler. The receiver DSP algo-

gorithms are both memory-intensive and computation-intensive. The ADSP-21XX-family of DSP processors address both needs, providing program memory RAM (for both code and data) on chip, data memory RAM on chip, and an instruction execution rate of up to 16.67MIPS.

## V.32 MODEM RECEIVER

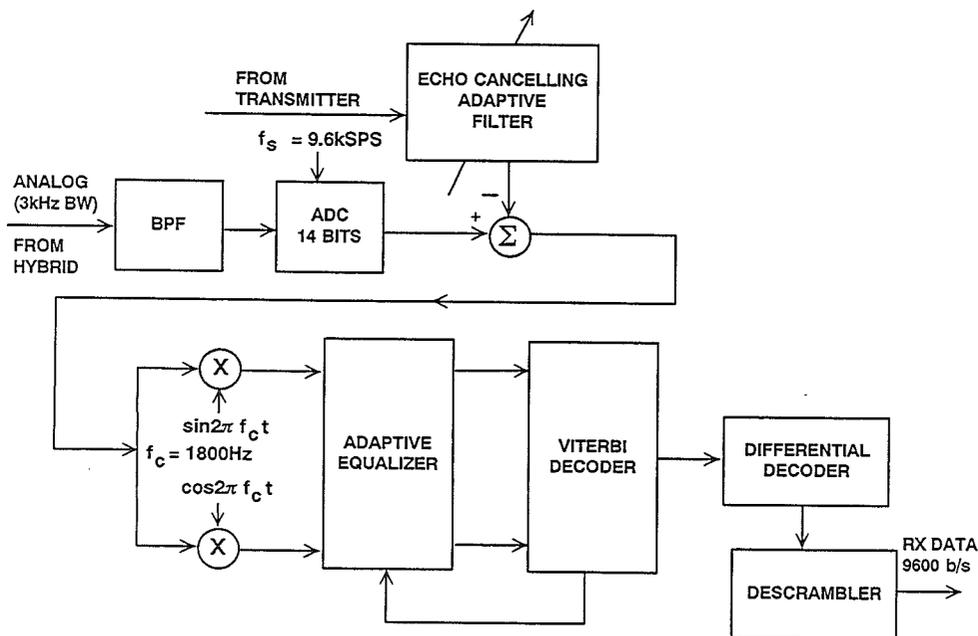


Figure 18.14

The antialiasing filter and ADC in the receiver need to have a dynamic range from the largest echo signal to the smallest received signal. The received signal can be as low as  $-40\text{dBm}$ , while the near-end echo can be as high as  $-6\text{dBm}$ . In order to insure that the analog front end of the receiver does not contribute any significant impairment to the channel under these conditions, an instantaneous dynamic range of  $80\text{dB}$  (14 bits) and an SNR of  $72\text{dB}$  is required.

In order to compensate for amplitude and phase distortion in the telephone channel, equalization is required to recover the transmitted data at an acceptably low bit error rate. In order to respond to rapidly changing conditions on the telephone line, adaptive equalization is required for the V.32 modem receiver. An adaptive equalizer can be implemented digitally in an FIR filter whose coefficients are continuously updated based on current line conditions. A 64-tap fractionally spaced equalizer provides the performance necessary for V.32 applications.

Separation between the transmit and receive signal in the V.32 modem is accomplished using echo cancellation. Echo cancellation is mandatory since both the calling and the answering modem use the same carrier frequency of  $1800\text{Hz}$ . Both near-end and far-end echo must be canceled in order to yield reliable communication. Echo cancellation is achieved by subtracting an estimate of the echo return signal from the actual received signal. The predicted echo is determined by feeding the transmitted signal into an adaptive filter with a transfer function that

approximates the telephone channel. The adaptive filter commonly used in echo cancellers is the FIR filter (chosen for its stability and linear phase response), where the taps are determined using the least-mean-square (LMS) algorithm during a training sequence executed prior to full-duplex communications. The echo canceller must be able to cancel  $16\text{ms}$  of echo. At  $9600$  samples/second, a 154-tap FIR filter is required to cancel the echo. Assuming that the canceller and frequency shifter have converged during the training period, about 200 cycles are required to cancel an echo in a V.32 modem.

The most common technique for decoding the received data is Viterbi decoding. Named after its inventor, the Viterbi algorithm is a general-purpose technique for making an error-corrected decision. Viterbi decoding provides a certain degree of error correction by examining the received bit pattern over time to deduce the value that was the most likely to have been transmitted at a particular time. Viterbi decoding is computation-intensive. A history for each of the possible symbols sent at each symbol interval has to be maintained. For the V.32 modem, the symbol history spans 20 symbol intervals. At each symbol interval, the length of the path backward in time from each possible received symbol to a symbol sent some time ago is calculated. After 20 symbol intervals, the symbol that has the shortest path back to the original signal is chosen to be the current decoded symbol. A complete description of Viterbi decoding and its implementation on the ADSP-2100 family of DSP processors is given in Reference 2.

The AD28msp01 PSTN Signal Port for V.32 Modems

The AD28msp01 is a complete analog front end for high performance modems. The AD28msp01 contains a 16 bit sigma-delta ADC and DAC and is capable of sampling rates of 7.2, 8.0, and 9.6kSPS with SNR and THD performance of 84dB. The extensive

support of bit, baud, and convert clocks allow the AD28msp01 to support many modem standards such as the V.32 and V.32bis. A block diagram is shown in Figure 18.15, and key specifications are summarized in Figure 18.16.

AD28msp01 PSTN SIGNAL PORT BLOCK DIAGRAM

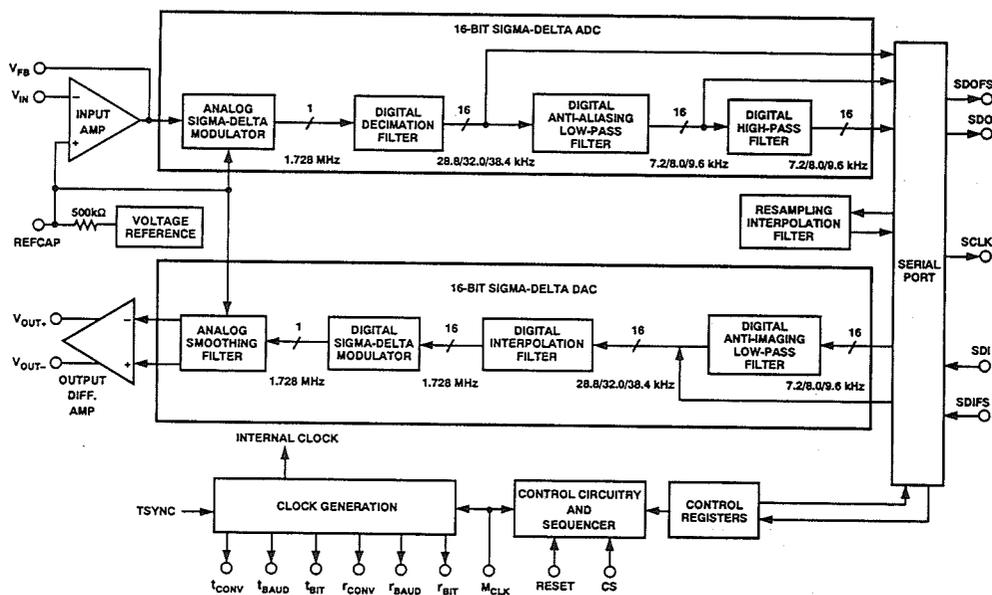


Figure 18.15

## AD28msp01 INTEGRATED MODEM ANALOG FRONT END KEY SPECIFICATIONS

- 16 Bit Sigma-Delta ADC and DAC
- On-Chip Antialiasing and Anti-Imaging Filters
- On-Chip Clock Generation Circuitry
- 80 dB THD and SNR
- Programmable Sampling Frequency of 7.2, 8.0, and 9.6kSPS
- DSP Compatible Serial Port
- Single +5V Supply, 350mW Power Dissipation
- 28 Pin DIP/SOIC

Figure 18.16

### The AD20msp500-Series Of Software Programmable PSTN Communications Chipsets And The ADAT-DSI01 DataPump Algorithm Toolkit

These two packages (Figure 18.17) form a good example of what Analog Devices' Signal Computing technology provides to solve a systems design problem. The chipsets are key building blocks for a variety of low-cost modems and

“datapumps.” They consist of the AD28msp01 analog signal port for PSTN (public switched telephone network), plus a member of Analog Devices' ADSP-2100 fixed-point DSP family.

## SIGNAL COMPUTING SOLUTION FOR HIGH PERFORMANCE MODEMS

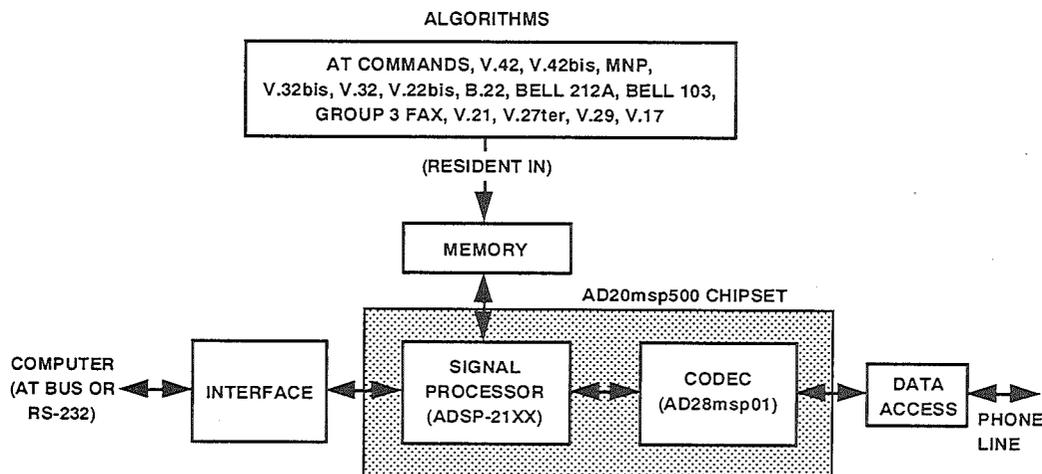


Figure 18.17

The AD28msp01 signal port (previously described) is designed specifically for echo-canceling V.32 and V.32bis modem designs, while the DSP processor provides processing power to implement algorithms for these standards—plus all fallback standards, and fax-, data-compression-, and error-correction functions. No microcontroller is used—all functionality is defined and implemented by software; thus the range of functions can be easily upgraded or stripped back (to meet the market needs of the system designer), and any repairs of software defects are easily made.

The toolkit, developed by Digicom Systems, Inc., provides all the software and documentation needed to implement the modem using the chipset. The

algorithms can be used “as is” for a standard design—or augmented for applications where customized signal processing algorithms are needed. The toolkit provides the datapump algorithms (which represent telecom standards) as modules; and only the desired modules need be included in the final product.

The ADMK-100 Modem Chipset Development Kit is a design kit developed by Digicom Systems, Inc., and is available from Analog Devices. This kit contains all schematics, layout, parts list, DSP object code, and other software necessary to build a complete low-cost modem using the AD20msp500-series of chipsets. A sample modem is also included in the kit.

## ADMK-100 MODEM MANUFACTURING KIT

- AD20msp500-Series Modem Chipset
- Parts List, Schematics, PC Board Layout
- DSP Object Code, License Agreement
- Sample Stand-Alone Modem

Figure 18.18

### Digital Telephone Answering Machine Solution Using Signal Computing From Analog Devices

The ADDS-CSDK-100 is a Manufacturing Kit for the design of digital telephone answering machines. The kit provides an answering machine development tool program, a demonstration board, and complete production information (gerber files, schematics, and user's guide). The development tool software allows developers to prototype

their digital answering machine. The tool outputs an EPROM file that contains the DSP object code to run the answering machine. The EPROM is coded to run on the AD20msp700 (ADSP-21XX compatible) DSP. Key features of the answering machine manufacturing kit are summarized in Figure 18.19.

## ADDS-CSDK-100 DIGITAL TELEPHONE ANSWERING MACHINE DESIGN KIT

- Complete Set of Hardware and Software Tools for Development of Compressed-Speech Digital Answering Machine Including Demo Board
- High Quality Speech Coding Algorithms based on RPE-LTP-LPC Coding
- Supports DTMF, Busy Tone, and Ring Detection
- Synthetic Voice Announces Time Stamp and DTMF Phone Number
- Functions: Record, Play, Delete, Memo, Cue, Review, Skip, Save, Remote
- 5 to 50 Minutes of Voice Recording Using 4 to 16Mbit DRAM or ARAM
- Voice Activity Detection for Pause Compression to Optimize Memory Usage
- Minimal Glue Logic, No ASIC Required

Figure 18.19

### DIGITAL MOBILE RADIO OVERVIEW

*Walt Kester*

The rapidly growing number of cellular mobile phones in the United States has created significant system performance problems, especially in crowded metropolitan areas such as New York and Los Angeles. Call blocking during rush hour, flaws in call processing (disconnects and misconnects), and undesirable interchannel crosstalk are only a few. In addition, the current system lacks privacy and security, and data transmission over a mobile link is almost impossible at rates above 1200 bits/s. These factors have led to the search for a more efficient and robust system based on digital techniques. Several digital approaches are being considered in the United States, while the Pan-European Digital Cellular Radio System (also known as *Groupe Speciale Mobile*, or GSM) is already in use throughout Europe and much of the rest of the world.

The current system in the United States is a cellular system based on Frequency Division Multiple Access (FDMA). A region is broken up into cells, with each cell having its own base station and its own group of assigned frequencies (see Figure 18.21). Because the radius of each cell is small (10 miles, for example) low power transmitters and receivers can be used. The cellular system lends itself to frequency reuse, since cells which are far enough apart can utilize the same band of frequencies without interference. The base stations must be linked together with an elaborate central control network so that a call may be handed-off to another cell when the signal strength from the mobile unit becomes too low for the current cell to handle.

## PROBLEMS WITH CURRENT ANALOG CELLULAR RADIO

- Call Blocking During Busy Hours
- Misconnects and Disconnects due to Rapidly Fading Signals
- Lack of Privacy and Security
- Data Transmission Limited to 1200 bits/s

Figure 18.20

## CELLULAR RADIO FREQUENCY REUSE

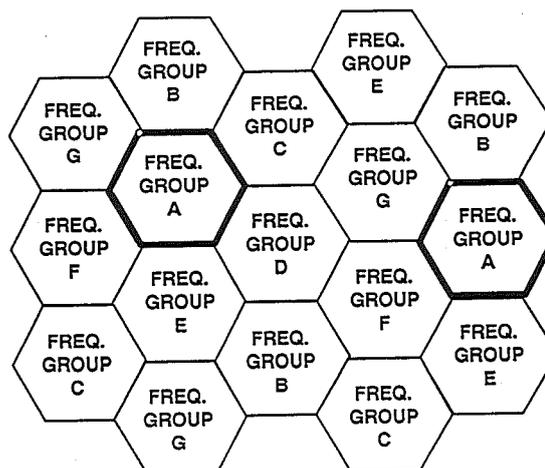


Figure 18.21

The frequency spectrum allocation for cellular radio in the United States is approximately 825 to 850MHz and 870 to 895MHz. Conventional architectures (both analog and digital) are channelized. The total spectrum is divided up into a large number of relatively narrow channels, defined by a carrier frequency. The carrier frequency is frequency-modulated with the voice signal using analog techniques. Each

full-duplex channel requires a pair of frequencies, each with a bandwidth of approximately 30kHz. A user is assigned both frequencies for the duration of the call. The forward and reverse channel are widely separated, to help the radio keep the transmit and receive functions separated. The 40MHz allocated to cellular service can therefore be divided up into 666 frequency pairs, each serving one full-duplex circuit.

### **U.S. FREQUENCY DIVISION MULTIPLE ACCESS (FDMA) ANALOG MOBILE RADIO SYSTEM**

- Uses 825-850MHz and 870-895MHz Spectrum
- 30kHz Transmit, 30kHz Receive
- Analog Frequency Modulation (FM)
- Approximately 700 Users Capacity

**Figure 18.22**

Time Division Multiple Access (TDMA) allocates bandwidth on a time-slot basis. In the proposed United States TDMA system, the entire 30kHz channel is assigned to a particular transmission, but only for a short period of time. A 3:1 multiplexing scheme means that three conversations can take place with TDMA using the same amount of bandwidth as one analog cellular conversation does. Each transmit/receive sequence occurs on time slots lasting 6.7ms. The TDMA system relies on an extensive amount of DSP technology to reduce the coded speech bit-rate as well as to prepare the digital data for transmission over the analog medium. The TDMA approach has been chosen for the Pan-European GSM system and will be discussed later in more detail.

The second digital approach being considered in the United States is called Code Division Multiple Access (CDMA). This technique has been used in secure

military communications for a number of years under the name of *spread spectrum*. In spread spectrum, the transmitter transmits in a pseudo-random sequence of frequency hops over a relatively wide frequency range. The receiver has access to the same random sequence and can decode the transmission. The effect of adding additional users on the system is to decrease the overall signal to noise ratio for all the users. With this technique, the effect of allowing more calls than the normal capacity is to increase the bit-error rate for all users. New callers can keep coming in, interference levels will rise gradually, until at some point the process will become self-regulating: the quality of the voice link will become so bad that users will cut short or refrain from making additional calls. No one is ever blocked in the conventional sense, as they are in FDMA or TDMA systems when all channels or slots are full.

## DIGITAL MOBILE RADIO APPROACHES

- Time Division Multiple Access (TDMA) - User Allocation Based on Time Slots: At Least 3X More Capacity than FDMA
- Code Division Multiple Access (CDMA) - Base on Spread Spectrum Technology: More Users Cause Graceful Degradation in Bit-Error Rate
- Both TDMA and CDMA Make Extensive Use of DSP in Speech Encoding and Channel Coding for Transmission

Both TDMA and CDMA systems make extensive use of DSP algorithms in both speech encoding and in preparing the signal for transmission. In the receiver, DSP techniques are used for demodulation and decoding the speech signal. The remainder of this section will

concentrate on speech processing and channel coding as they relate to the Pan-European GSM system. This will serve to illustrate the fundamental principles which are applicable to all digital mobile radio systems.

**The GSM System**

Figure 18.24 shows a simplified block diagram of the GSM Pan-European Digital Cellular Telephone System. The *speech encoder and decoder* and *discontinuous transmission* function will be described in detail. Up conversion and downconversion portions of the system

contain a digital modem similar to the V.32 device previously discussed. Similar modem functions are performed digitally in the GSM system such as equalization, convolutional coding, Viterbi decoding, modulation and demodulation.

**GSM PAN-EUROPEAN  
DIGITAL CELLULAR PHONE SYSTEM**

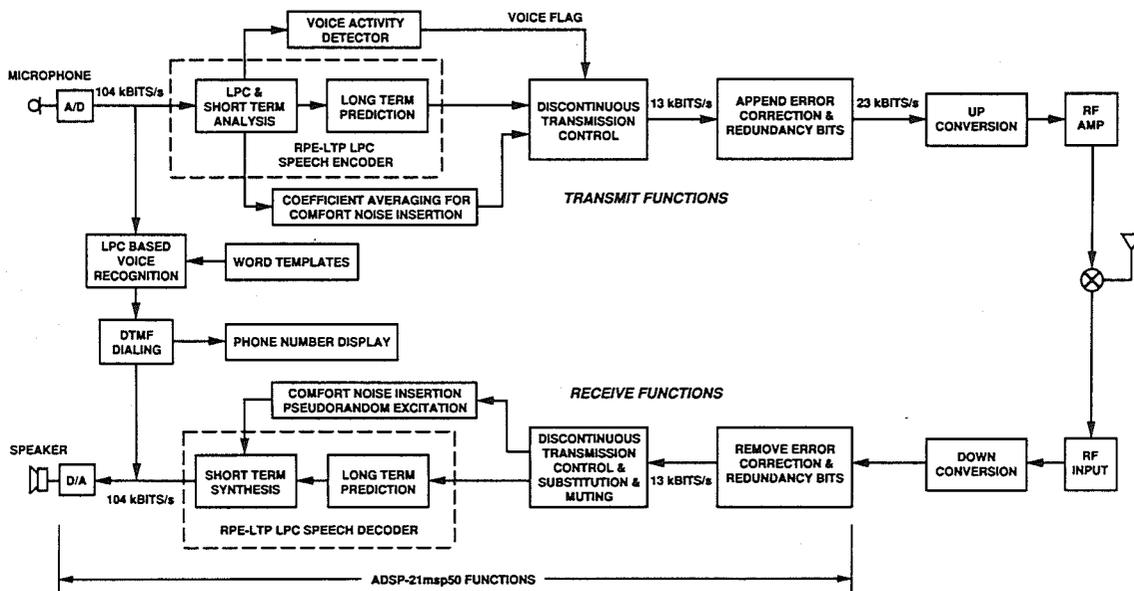


Figure 18.24

## Speech Codec

The standard for encoding voice has been set in the T-Carrier digital transmission system. In this system, speech is logarithmically encoded to 8 bits at a sampling rate of 8kSPS. The logarithmic encoding and decoding to 8 bits is equivalent to linear encoding and decoding to 13 bits of resolution. In the GSM system 13-bit linear, 8kSPS encoding produces a bit-rate of 104kb/s. The Speech Encoder portion of the GSM system compresses the speech signal to 13kb/s, and the decoder expands the compressed signal at the receiver. The terms *codec* and *transcoder* are both often used to refer to the entire encoding and decoding speech compression function. The speech encoder is based on an enhanced version of linear predictive coding (LPC). The LPC algorithm uses a model of the human vocal tract that represents the throat as a series of concentric cylinders of various diameters. An excitation (breath) is forced into the cylinders. This model can be mathematically represented by a series of simultaneous equations which describe the cylinders.

The excitation signal is passed through the cylinders, producing an output signal. In the human body, the excitation signal is air moving over the vocal cords or through a constriction in the vocal tract. In a digital system, the

excitation signal is a series of pulses for vocal excitation, or noise for a constriction. The signal is input to a digital lattice filter. Each filter coefficient represents the size of a cylinder.

An LPC system is characterized by the number of cylinders used in the model. The GSM system uses eight cylinders so eight reflection coefficients are required.

Early LPC systems worked well enough so the encoded speech could be understood, but often the quality was too poor to recognize the voice of the speaker. The GSM LPC system employs two advanced techniques that improve the quality of the encoded speech. These techniques are *regular pulse excitation* (RPE) and *long term prediction* (LTP). When these techniques are used, the resulting quality of encoded speech is nearly equal to that of logarithmic pulse code modulation (companded PCM as in the T-Carrier system).

The actual input to the speech encoder is a series of 13-bit samples of uniform PCM speech data. The sampling rate is 8kHz. The speech encoder operates on a 20ms window (160 samples) and reduces it to 76 coefficients (260 bits total), resulting in an encoded data rate of 13kb/s.

## SPEECH COMPRESSION IN THE GSM SYSTEM

- Input Data: 13bit Samples at 8kSPS = *104kbits/s*
- Output Data for Each 20ms Window: 76 Filter Coefficients, 260 bits Total = *13kbits/s*

Figure 18.25

### Discontinuous Transmission (DTX)

Discontinuous transmission (DTX) allows the system to shut off transmission during the pauses between words. This reduces transmitter power consumption and increases the overall GSM system's capacity.

Low power consumption prolongs battery life in the mobile station and is an important consideration for hand-held portable phones. Call capacity is increased by reducing the interference between channels, leading to better spectral efficiency. In a typical conversation each speaker talks for less than 40% of the time, and it has been estimated that DTX can approximately

double the call capacity of the radio system.

The required DTX functions are summarized in Figure 18.26.

The voice activity detector (VAD) is located at the transmitter; its job is to distinguish between speech superimposed on the background noise and noise with no speech present. The input to the voice activity detector is a set of parameters computed by the speech encoder. The VAD uses this information to decide whether or not each 20ms frame of the encoder contains speech.

## DISCONTINUOUS TRANSMISSION (DTX) FUNCTIONS

- Voice Activity Detection (VAD) to Detect Speech
- Comfort Noise Insertion (CNI) to Synthesize Artificial Car Noise During Pauses Between Words
- Output Muting When Lost Speech Frames Are Received

Figure 18.26

Comfort noise insertion (CNI) is performed at the receiver. The comfort noise is generated when the DTX has switched off the transmitter; it is similar in amplitude and spectrum to the background noise at the transmitter. The purpose of the CNI is to eliminate the unpleasant effect of switching between speech with noise, and silence. If you were listening to a transmission without CNI, you would hear rapid alternating between speech in a high-noise background (i.e. in a car), and silence. This effect greatly reduces the intelligibility of the conversation.

When DTX is in operation, each burst of speech is transmitted followed by a *silence descriptor* (SID) frame before the transmission is switched off. The SID serves as an end of speech marker for the receive side. It contains characteristic parameters of the background noise

at the transmitter, such as spectrum information derived through the use of linear predictive coding.

The SID frame is used by the receiver's comfort noise generator to obtain a digital filter which, when excited by pseudo-random noise, will produce noise similar to the background noise at the transmitter. This comfort noise is inserted into the gaps between received speech bursts. The comfort noise characteristics are updated at regular intervals by the transmission of SID frames during speech pauses.

Redundant bits are then added by the processor for error detection and correction at the receiver, increasing the final encoded bit rate to 22.8kb/s. The bits within one window, and their redundant bits, are interleaved and spread across several windows for robustness.

The ADSP-21msp50 Mixed Signal Processor shown in Figure 18.27 can perform all of the above tasks within the 20ms sampling window because of its optimized DSP architecture and the special on-chip peripherals associated with it. The sigma-delta converters provide the necessary interface to the speaker and microphone. The parallel host interface port communicates with a host processor, which is responsible for loading the ADSP-21msp50 with the appropriate programs during power-up, dialing, and actual conversation phases of a complete call. The ADSP-21msp50 has 1K words of (16-bit) data memory static RAM and 2K words of 24-bit

program memory static RAM on chip. The device operates at a 13MHz clock rate and has a low power mode and a power down mode (less than 1mW in power down). The ADSP-21msp50 combines the core ADSP-2100 architecture (three computational units, data address generators, and a program sequencer) with two serial ports, a programmable timer, host interface port, an analog interface (shown in Figure 18.28), and extensive interrupt capabilities. Key features of the ADSP-21msp50 are summarized in Figure 18.29, and the benchmark performance in the GSM system is shown in Figure 18.30.

### ADSP-21msp50 BLOCK DIAGRAM

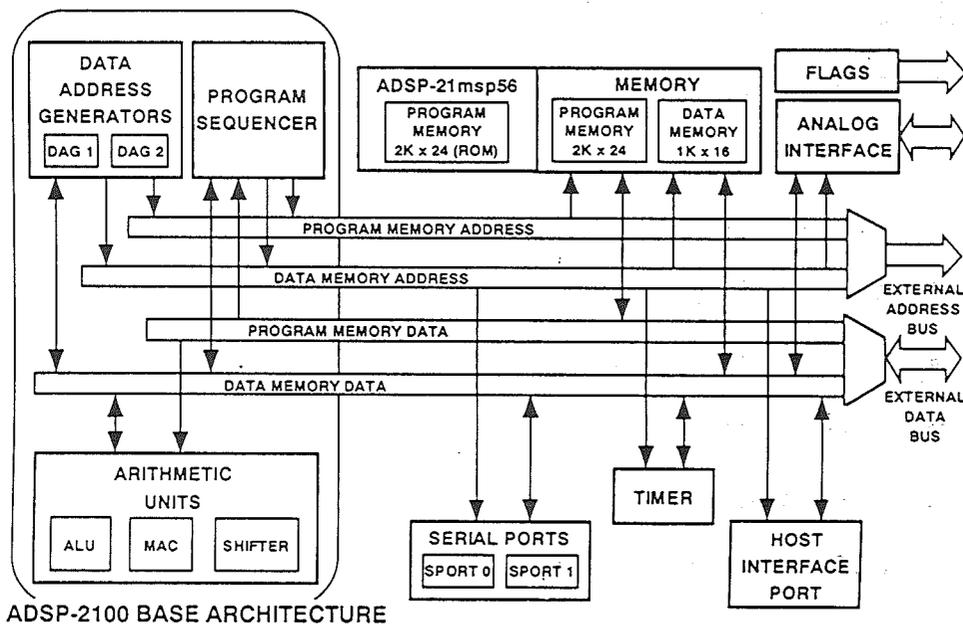


Figure 18.27

## ADSP-21msp50 ANALOG INPUT/OUTPUT INTERFACE

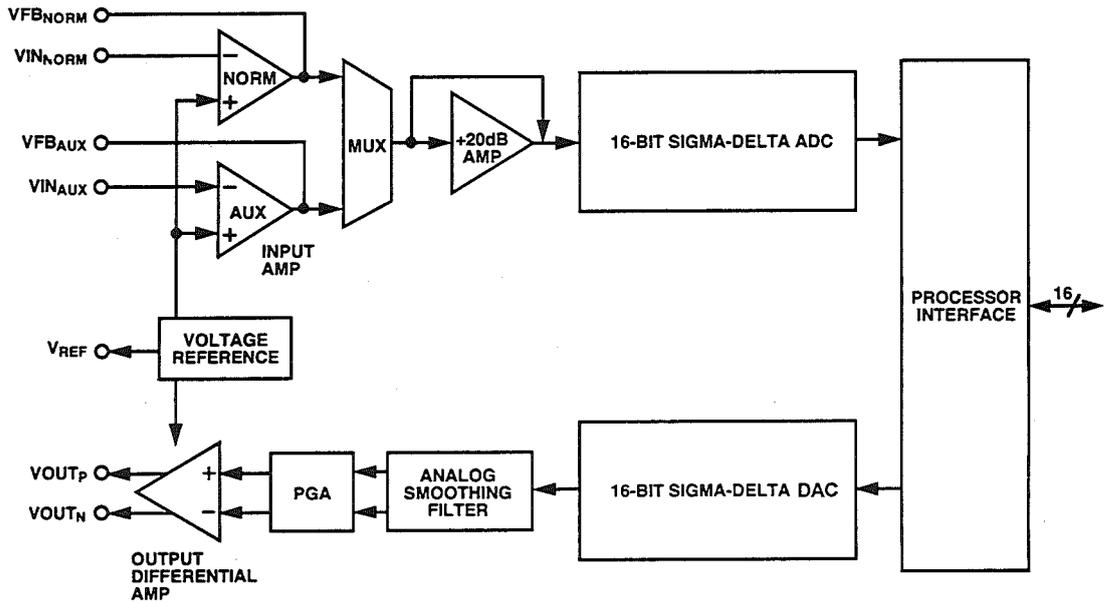


Figure 18.28

## ADSP-21msp50 MIXED SIGNAL PROCESSOR KEY SPECS

- On-Chip 16-Bit Sigma-Delta ADC and DAC
- 65dB SNR and THD
- 8kSPS Sampling Frequency, 1MHz Clock (125X Oversampling)
- 2K Words Program Memory Ram (24-bits)
- 1K Words Data Memory Ram (16-bits)
- 13MIPS Performance
- Host Interface Port
- ADSP-2100 Family Compatible Instruction Set
- Low Power and Power Down Mode

Figure 18.29

### ADSP-21msp50 GSM BENCHMARKS

Function	Cycle Count Maximum Worst Case	Time Required out of 20ms Window	Processor Loading
RPE-LTP LPC Encoder	49300	3.8ms	19.0%
RPE-LTP LPC Decoder	14400	1.1ms	5.5%
Voice Activity Detector	2141	0.17ms	0.9%
Total Functions	65841	5.07ms	25.4%
Free			74.6%

Internal Program Memory Required: 1988 words

Internal Data Memory Required: 964 words

Figure 18.30

The AD28msp02 Voiceband Signal Port is a complete I/O function for voiceband applications and requires an external

DSP processor. A block diagram is shown in Figure 18.31, and key specifications in Figure 18.32.

## AD28msp02 VOICEBAND SIGNAL INPUT / OUTPUT PORT

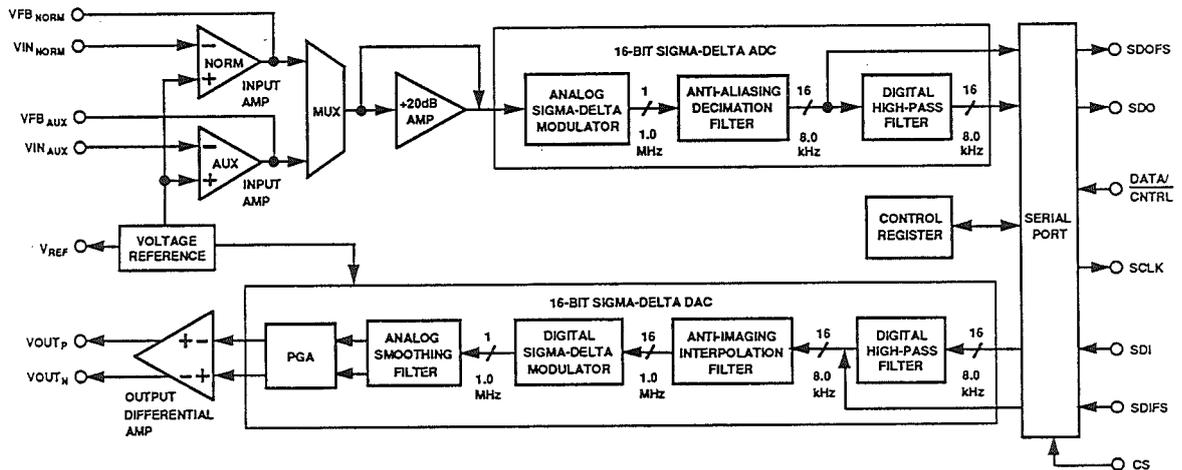


Figure 18.31

## KEY FEATURES OF THE AD28msp02 VOICEBAND SIGMA-DELTA CODEC

- 16 bit Sigma-Delta ADC
- 16 bit Sigma-Delta DAC
- On-Chip Antialiasing and Smoothing Filters
- 8kSPS Sampling Rate, 128x Oversampling Ratio
- On-Chip Voltage Reference
- 65dB SNR and THD
- Easy Interface to DSP Chips
- 24-pin DIP/SOIC Package
- Single +5V Supply, 100mW Power Dissipation
- Ideal for Voiceband Applications

Figure 18.32

### GSM System Upconversion and Downconversion

A block diagram of the GSM system with particular emphasis on the upconversion and downconversion circuitry is shown in Figure 18.33. The transmit data coming from the speech processor contains error correction and redundancy bits. The bit rate at this point in the system is 23kb/s. The channel coder and filters prepare the data to fit the TDMA format of the GSM system. Figure 18.34 shows how each 200kHz of frequency spectrum contains data from 8 users. Each user is assigned a time slot of 0.577ms during which time a burst of 156 data bits are

transmitted at a modulation frequency of approximately 270kHz. Modulation is accomplished using Gaussian Minimum Shift Keying (GMSK), a form of frequency shift keying which minimizes spectral leakage. The modulation is done digitally and converted into an I and Q signal. The modulator outputs drive two 10-bit DACs whose filtered output drives the RF modulators. The DACs are oversampled by a factor of 16 in order to simplify the anti-imaging analog filter requirements. The combined I and Q signal drives the RF amplifier, filter, and the antenna.

### GSM BLOCK DIAGRAM: UP/DOWN CONVERSION DETAILS

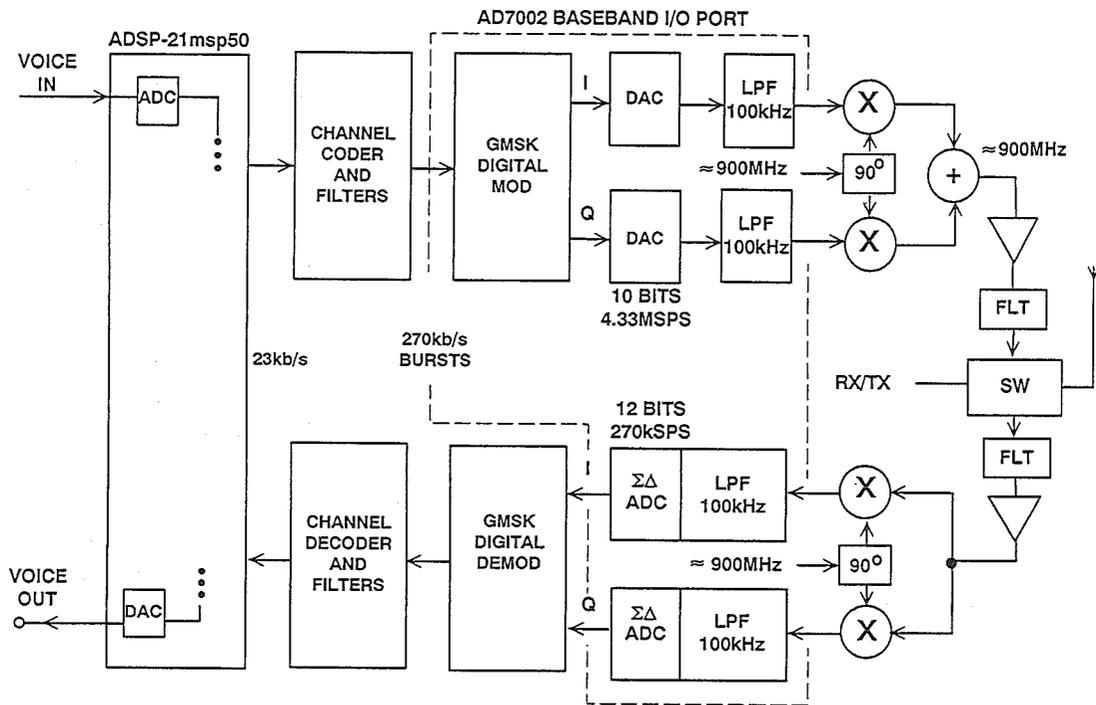


Figure 18.33

## GSM FREQUENCY / TIME ALLOCATIONS

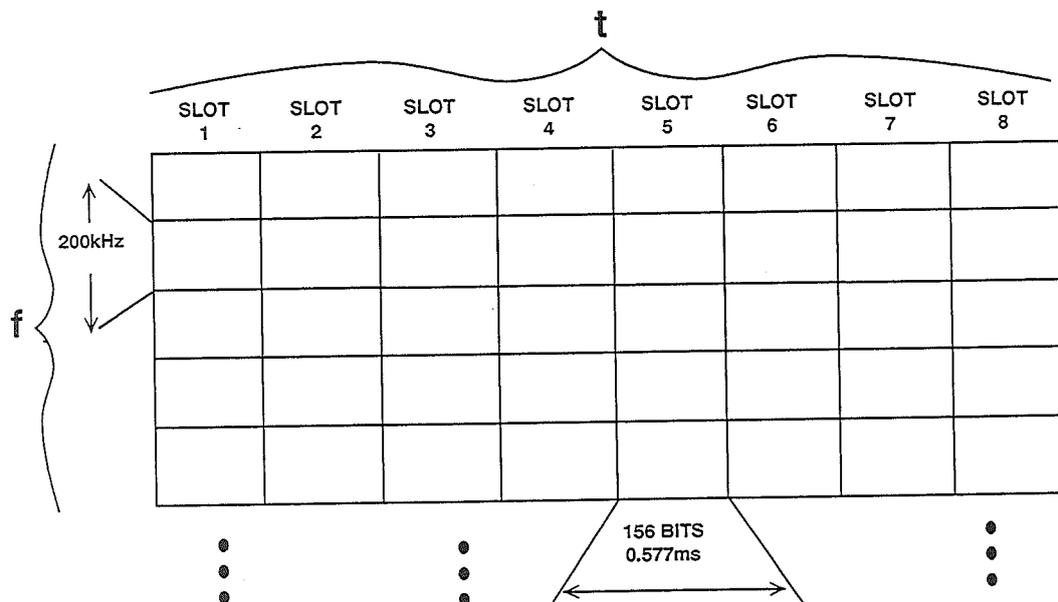


Figure 18.34

The received signal is filtered, amplified, and fed to an I/Q RF demodulator which recovers the I and Q signals. The baseband I and Q signals are converted by two 12-bit DACs at an effective sampling rate of 270kSPS. The I and Q signals are then demodulated by the GMSK digital demodulator. The 270kb/s burst is sent to the channel decoder and filters and then to the speech processor.

The AD7002 is a complete GSM Baseband I/O Port which performs the functions shown in Figure 18.35. The transmit path contains two 10-bit oversampled (16X) DACs followed by

fourth-order anti-imaging filters. The DACs are driven by a digital modulator containing a GMSK-coded ROM. The receive path contains two high-performance 12 bit sigma-delta ADCs having a throughput rate of 270kSPS. The sigma-delta ADCs contain a 288-tap FIR filter having linear phase response and a 3dB point of 122kHz. Three auxiliary DACs are included for such functions as AFC, AGC and carrier shaping. The device dissipates approximately 100mW and has flexible power-down or sleep modes. A block diagram is shown in Figure 18.35 and key specifications are summarized in Figure 18.36.

## AD7002 GSM BASEBAND I / O PORT

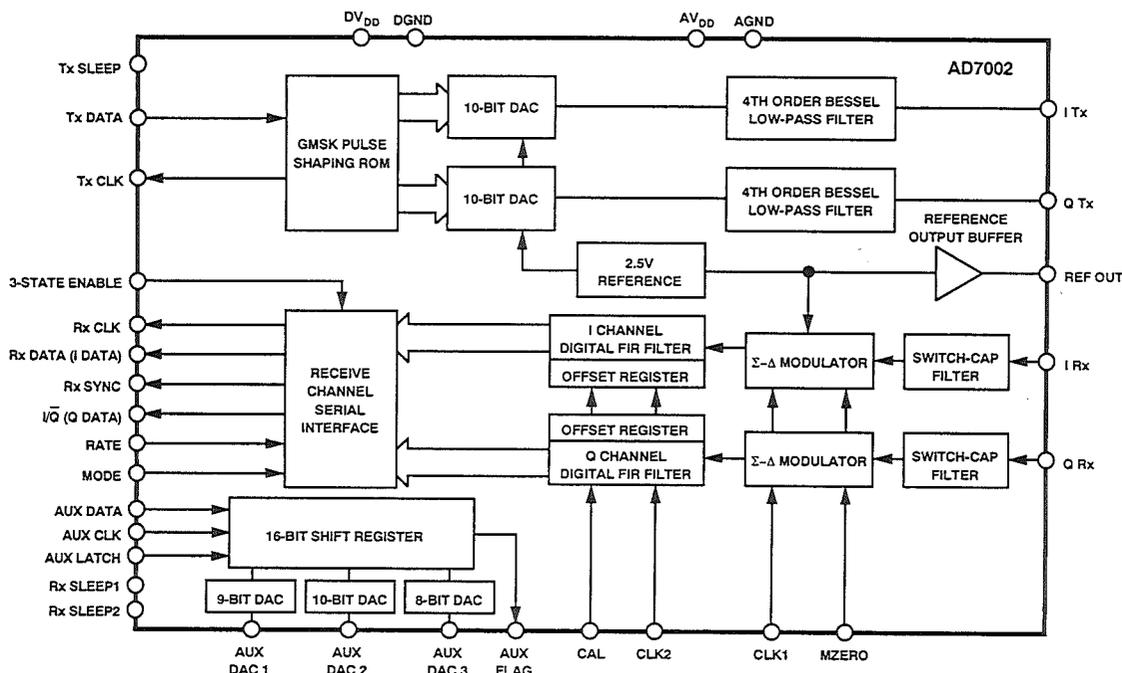


Figure 18.35

## AD7002 GSM BASEBAND I/O PORT KEY SPECIFICATIONS

- **Transmit Path:** GMSK I/Q Digital Modulator  
Dual 10 Bit, 4.33MSPS Oversampled DACs  
Dual Anti-Imaging Filters
- **Receive Path:** Dual 12 Bit 270kSPS Sigma-Delta ADCs  
288-Tap 100kHz Linear Phase FIR Filter
- **3 Auxiliary DACs for AFC, AGC**
- **Low Power: 100mW**
- **Sleep Mode**

Figure 18.36



## AD7001 GSM BASEBAND I/O PORT KEY SPECIFICATIONS

- **Transmit Path:** Dual 2.16MSPS 10-bit DACs with latches  
Dual Output Anti-Imaging Filters
- **Receive Path:** Single 8-bit 2.16MSPS ADC  
Receive Difference Amplifier  
Programmable Gain Amplifier
- **Single Serial Auxiliary 8-bit DAC for AFC, AGC, etc.**
- **Power Down Modes**

Figure 18.38

The AD7011 is a complete, low power, CMOS,  $\pi/4$  DQPSK modulator designed to perform the baseband conversion of I and Q transmit waveforms in accordance with the American Digital Cellu-

lar Telephone System (TIA IS-54). A functional block diagram is shown in Figure 18.39, and key specifications are given in Figure 18.40.

## AD7011 $\pi/4$ DQPSK BASEBAND TRANSMIT PORT FOR AMERICAN DIGITAL CELLULAR TELEPHONE (TIA IS-54)

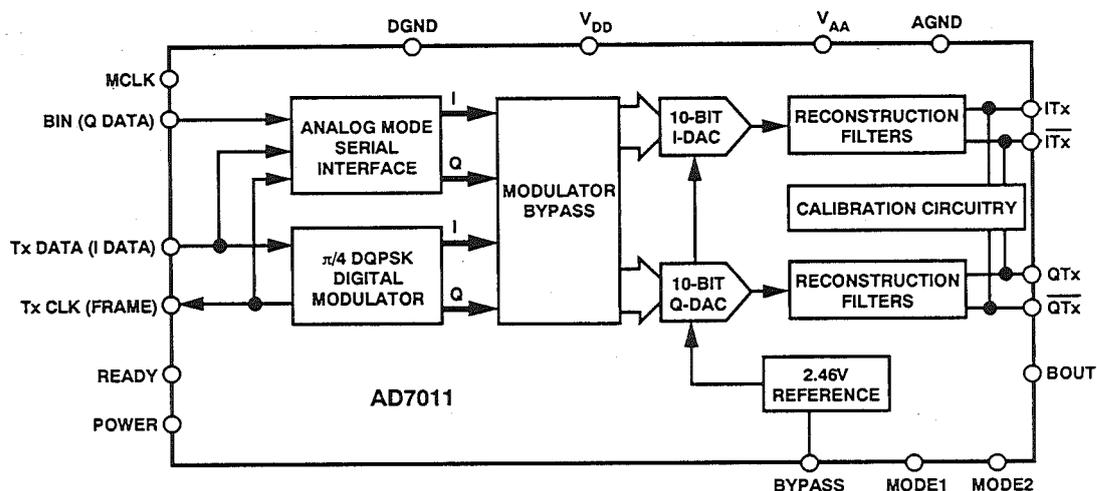


Figure 18.39

## AD7011 $\pi/4$ DQPSK BASEBAND TRANSMIT PORT FOR AMERICAN DIGITAL CELLULAR TELEPHONE (TIA IS-54) KEY SPECIFICATIONS

- Single +5V Operation, Low Power
- On-Chip  $\pi/4$  DQPSK Modulator
- Modulator Bypass Analog Mode
- Two 10-bit DACs
- On-Chip 4th Order Reconstruction Filters
- 30mW Typical Power Dissipation, 10 $\mu$ A in Power-Down Mode

Figure 18.40

The AD7013 is a companion part to the AD7011. The AD7013 is a TIA IS-54 baseband receive port. This device is designed to perform the baseband conversion of I and Q waveforms in the

American Digital Cellular Telephone System. A functional block diagram of the AD7013 is shown in Figure 18.41, and key specifications are given in Figure 18.42.

### AD7013 TIA IS-54 BASEBAND RECEIVE PORT

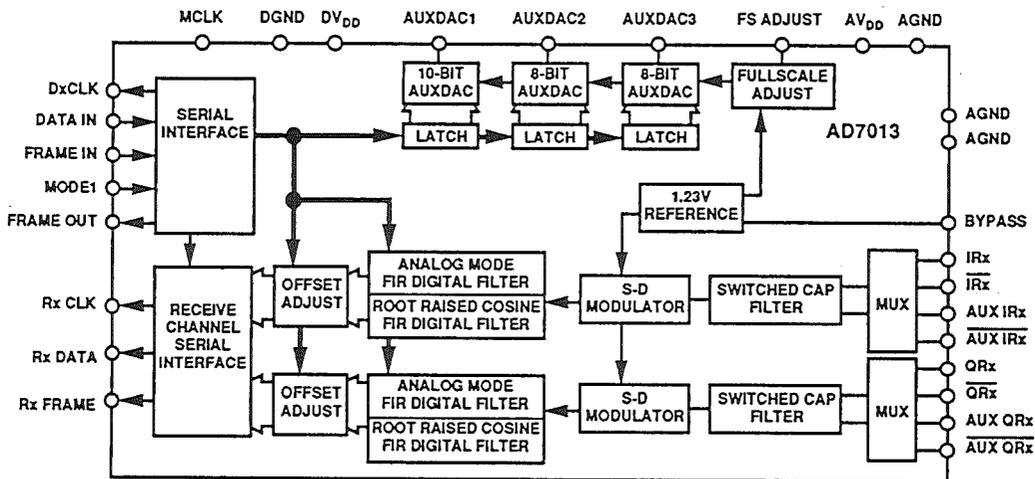


Figure 18.41

### AD7013 TIA IS-54 BASEBAND RECEIVE PORT KEY SPECIFICATIONS

- Single +5V Supply Operation
- Differential or Single-Ended Analog Inputs
- Auxiliary Set of Analog I and Q Inputs
- Two Sigma-Delta ADCs
- Choice of Two Digital FIR Filters
- Three Auxiliary DACs
- Less Than 5 $\mu$ A in Power-Down Mode

Figure 18.42

The AD7010 is a complete CMOS  $\pi/4$  DQPSK Baseband Transmit Port designed to operate in accordance with the Japanese digital cellular telephone

system (JDC). A functional block diagram is shown in Figure 18.43, and key specifications are given in Figure 18.44.

### AD7010 JAPANESE DIGITAL CELLULAR TELEPHONE (JDC) $\pi/4$ DQPSK BASEBAND TRANSMIT PORT

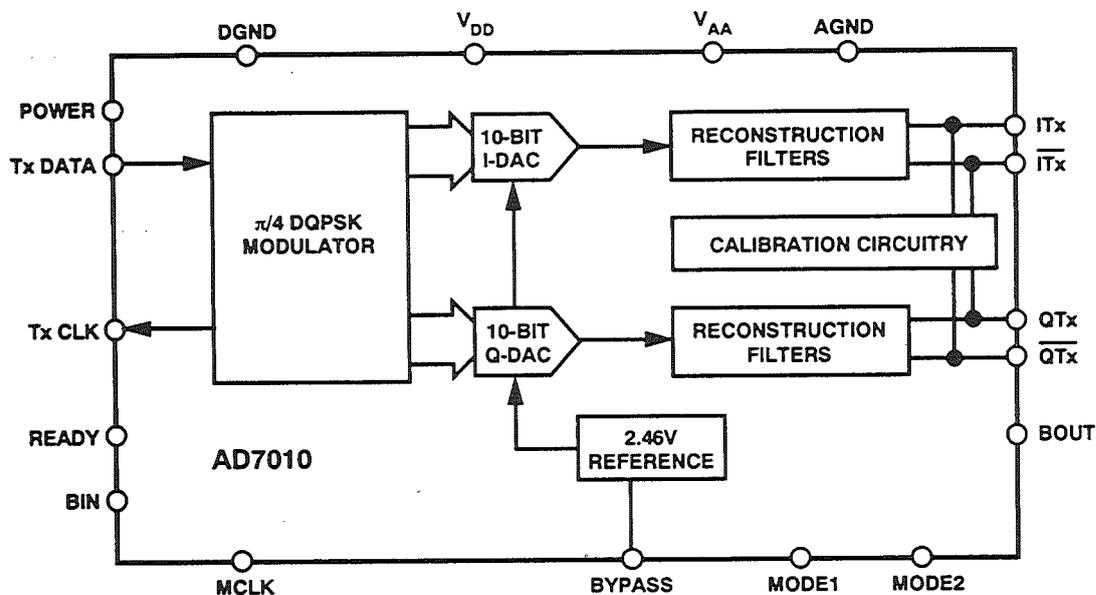


Figure 18.43

### AD7010 (JDC) $\pi/4$ DQPSK BASEBAND TRANSMIT PORT KEY SPECIFICATIONS

- Single +5V Supply
- On-Chip  $\pi/4$  DQPSK Modulator
- Two 10-Bit DACs (I and Q Channels)
- Two Reconstruction Filters
- Differential Analog Outputs
- Low Power: 30mW Typical, 5 $\mu$ A in Power-Down Mode

Figure 18.44

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