SECTION 13

INTERFACING TO HIGH SPEED ADCs

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SECTION 13

INTERFACING TO HIGH SPEED ADCs

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In previous sections, the amplification and transmission of high speed signals has been discussed in detail. The important characteristics of ADCs were reviewed in order to aid in specifying the appropriate converter for the signal being processed. In this section we examine the actual ADC interface. In addition to the selection of the drive amplifier, there are a number of other issues which are important to the successful application of high speed ADCs.

The input to most high speed ADCs requires an appropriate drive amplifier to buffer the signal and provide gain and offset capability. The ADC user must be able to supply a clean sampling clock which controls the conversion rate. Some high speed monolithic ADCs require an external voltage reference. Proper techniques must be used to handle the ADC output data, especially at high rates. Finally, and probably the most important, good layout, signal routing, power supply generation and decoupling, and grounding techniques must be followed in order to achieve the specified performance levels required.

SUCCESSFUL SYSTEMS REQUIRE PROPER INTERFACING WITH THE ADC

- Selection of Drive Amplifier
- Supplying External Reference Voltage if Required
- Capturing ADC Output Data
- Generation of Sampling Clock
- Proper Layout and Signal Routing
- Power Supply Generation, Filtering, Decoupling
- Proper Use of Ground Planes and Grounding Techniques

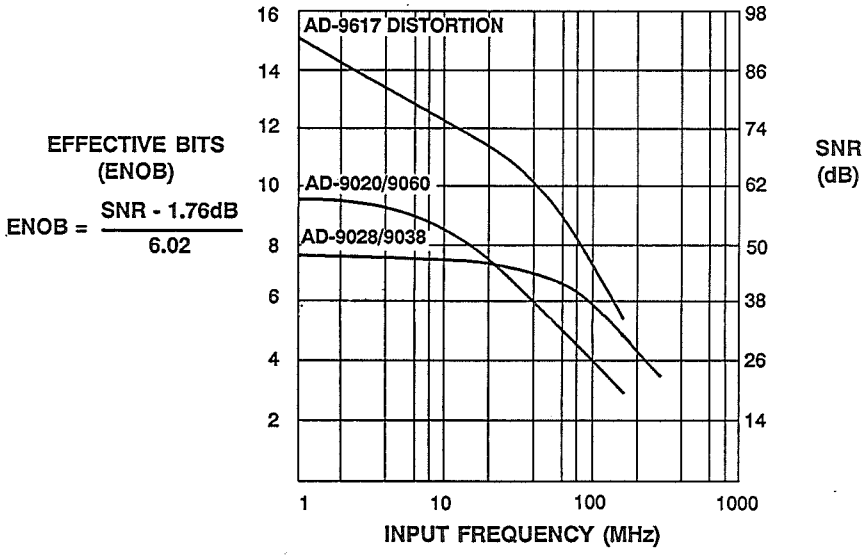
Figure 13.1

DRIVING THE HIGH SPEED ADC INPUT AND GENERATING REFERENCE VOLTAGES

Selecting the appropriate drive amplifier for a high speed ADC involves many of the considerations discussed in the section on amplification. The ac characteristics of ADCs are specified in terms of SNR, ENOBs, and distortion. The drive amplifier, therefore, should have a performance which is better than that of the ADC so that maximum dynamic performance is obtained. The second consideration involves understanding the analog input circuit of the ADC and its effect on the amplifier. Flash converters generally present a varying capacitive load to the amplifier which may cause instability. Subranging ADCs usually present rather benign loads to the drive amplifier because of their internal track-and-hold. Regardless of the ADC selected, the data sheet should always be consulted for recommended drive amplifiers.

High bandwidth, low distortion amplifiers such as the AD9617 are usually selected to drive high speed ADCs. Figure 13.2 shows the dynamic characteristics of two flash converters along with the distortion performance of the AD9617. Notice that the distortion performance of the AD9617 is better than the ADCs over the usable input bandwidths of the flash converters.

FLASH ADC AND OP AMP DYNAMIC PERFORMANCE



FLASH ADC	RESOLUTION	SAMPLING RATE
AD9020	10 BITS	40 MSPS
AD9060	10 BITS	60 MSPS
AD9028/9038	8 BITS	250 MSPS

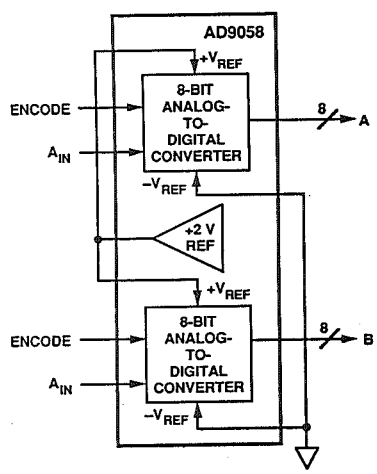
Figure 13.2

We will now consider some of the other important high speed ADC interface considerations by examining a few actual application circuits.

A simplified block diagram of the AD9058 dual 8 bit, 50MSPS flash converter and an application diagram for a quadrature receiver is shown in Figure 13.3. The AD9058 is ideal for applications which require matched converters in order to achieve optimum performance. Since both ADCs are on the same chip, dc and ac matching are both excellent. The matching between the aperture delay of the two converters is better than 200ps. Crosstalk rejection between the two channels at 3MHz is greater than 50dBc. The AD9058 has an internal +2V reference voltage which makes the device easy to use. Low power (<1W max) makes the AD9058 a cost effective solution for systems requiring two or more ADCs.

SIMPLIFIED BLOCK DIAGRAM OF AD9058 DUAL 8-BIT, 50MSPS FLASH CONVERTER AND QUADRATURE RECEIVER APPLICATION

BLOCK DIAGRAM



QUADRATURE RECEIVER

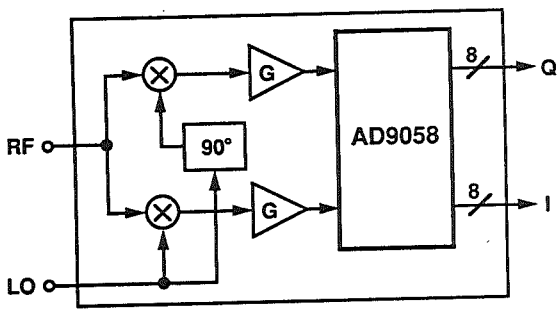


Figure 13.3

A typical interface circuit for the AD9058 is shown in Figure 13.4. The analog input range is established by the voltages applied at the voltage reference inputs $+V_{REFA}$, $+V_{REFB}$, and $-V_{REFA}$, $-V_{REFB}$. In applications requiring matched ADCs such as in quadrature receivers, $+V_{REFA} = +V_{REFB}$, and $-V_{REFA} = -V_{REFB}$. Because the reference voltages for each of the two ADCs are brought out on separate pins, it is possible to use different references for each of the two converters.

TYPICAL INTERFACE CIRCUIT FOR THE AD9058 DUAL FLASH CONVERTER USING INTERNAL VOLTGAGE REFERENCE

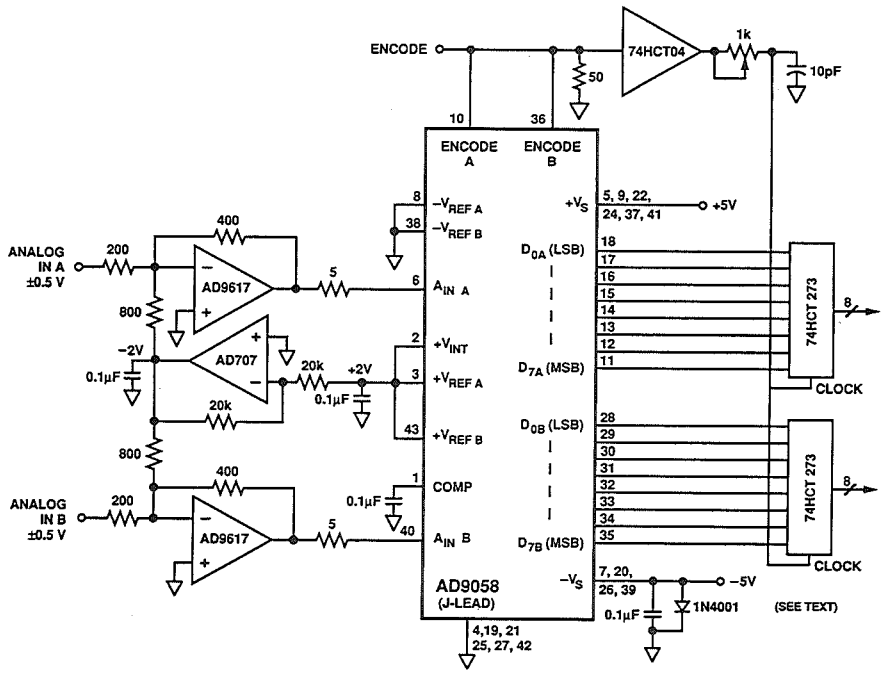


Figure 13.4

The AD9058 can operate from 0V to +2V using the internal bandgap voltage reference, or anywhere between –1V and +2V using external references. Input range is limited to 2V p-p when using external references. Using the internal voltage reference connected to both ADCs as shown in Figure 13.4 reduces the number of external components required to create a complete data acquisition system. The input ranges of the ADCs are positive unipolar in this configuration, ranging from 0V to +2V. The temperature coefficient of the internal reference is typically 150µV/°C which limits the drift to 11mV (1.4LSBs) over a 0 to +70°C temperature range.

A good low distortion amplifier such as the AD9617 (–67dBc at 20MHz) is used to buffer and amplify the signal to each ADC. The diagram shows that the bipolar signals of ±0.5V are amplified to 2V p-p by the pair of AD9617s. The op amps also serve to level shift the bipolar input signals to unipolar positive signals at the ADC inputs. The AD707 buffers the internal +2V reference and applies –2V to each of the 800Ω resistors. The corresponding 2.5mA removed from the inverting inputs of the op amps provides the required 1V positive offset at their outputs. The 5Ω series resistors isolate the AD9617 outputs from the 10pF input capacitance. This value of resistance ensures op amp stability without degrading the 175MHz input bandwidth of the AD9058.

The diode shown between ground and $-V_S$ is normally reverse biased and is used to prevent latchup. Its use is recommended for applications in which power supply sequencing might allow $+V_S$ to be applied before $-V_S$; or the $+V_S$ supply is not current limited. If the negative supply is allowed to float (the +5V supply is powered up before the

–5V supply), substantial +5V supply current will attempt to flow through the substrate ($+V_S$ supply contact) to ground. If this current is not limited to <500mA, the device may be destroyed. The diode prevents this potentially destructive condition from occurring.

The AD9058 may be used with external references as shown in Figure 13.5, where both inputs to the AD9058 are configured for ±1V operation. The AD580 provides an external +2.5V reference with a temperature coefficient as low as 25µV/°C for the M-grade. This limits the overall temperature drift of the reference to about 2mV (0.25LSBs) over the 0 to +70°C temperature range. The 10kΩ potentiometers allow independent adjustment of the positive and negative reference voltages. The dual AD708 low-drift op amp along with the 2N3904 and 2N3906 transistors are used to buffer the potentiometer outputs to the AD9058 reference voltage inputs. The lower half of the AD708 inverts the polarity to supply the negative reference. The ±0.125V input signals are amplified by the low-distortion AD9618 op amps configured for a gain of 8.

AD9058 INTERFACE CIRCUIT USING EXTERNAL VOLTAGE REFERENCE

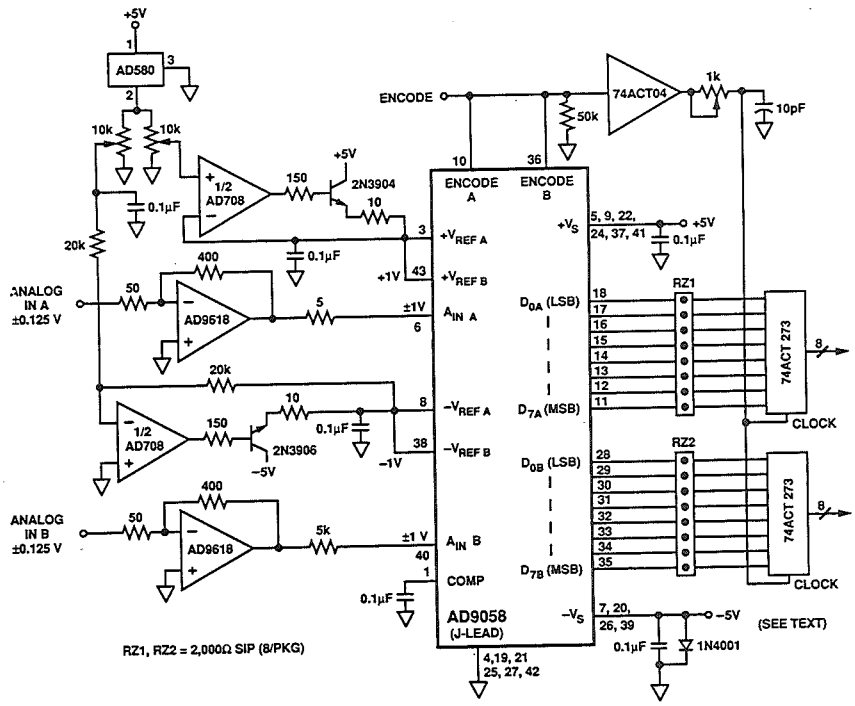


Figure 13.5

CAPTURING HIGH SPEED ADC OUTPUT DATA

A timing diagram for the AD9058 is shown in Figure 13.6. The AD9058 provides latched data outputs with no pipeline delay. To conserve power and reduce internal signal-dependent noise, the parallel data outputs have relatively slow rise and fall times. When designing system timing, it is important to observe set-up and hold times on the external latches; and the intervals when the ADC output data is changing.

Figure 13.5 shows 2kΩ pull-down resistors on each of the D_0 - D_7 output data bits. When operating at conversion rates higher than 40MSPS, these resistors help equalize rise and fall times and ease latching the output data into external latches. The 74ACT logic family devices have short set-up and hold times and are the recommended choices for speeds of 40MSPS or greater. The latch strobe may generated from the sampling clock by adding sufficient delay (if required) to center the latch strobe edge at the midpoint of the data-valid region.

Many flash converters and other ADCs, such as the AD9048 8 bit, 35MSPS ADC have one or more built-in pipeline delays associated with the output data. The block diagram of the AD9048 in Figure 13.7 shows an internal latch following the encoding logic. This latch introduces a one-clock-cycle pipeline delay, or *latency* in the output data as shown in Figure 13.8. This should not be a problem in most systems as long as the delay is known.

AD9058 FLASH CONVERTER TIMING DIAGRAM

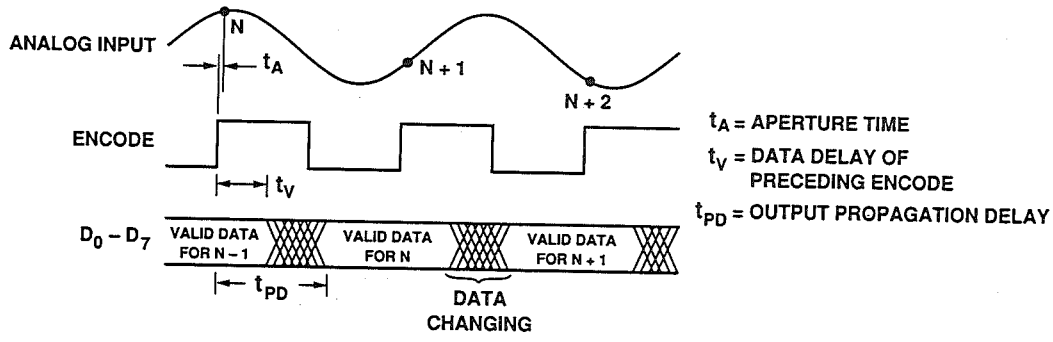


Figure 13.6

AD9048 8-BIT, 35MSPS FLASH CONVERTER HAS ONE CLOCK-CYCLE PIPELINE DELAY IN THE OUTPUT DATA DUE TO THE INTERNAL LATCH

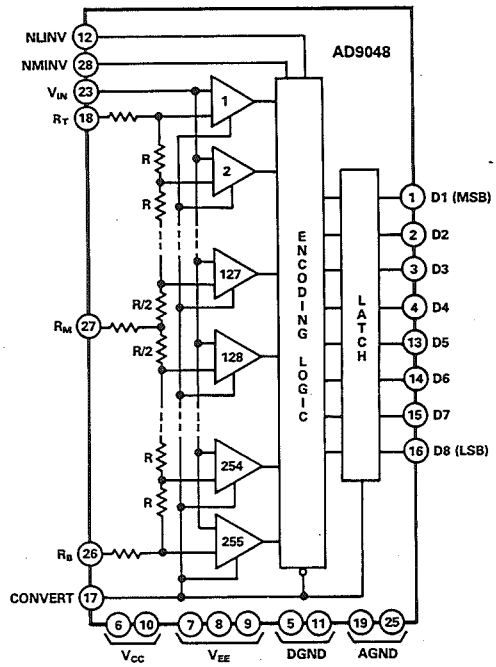


Figure 13.7

AD9048 TIMING DIAGRAM SHOWS PIPELINE DELAY (LATENCY) IN THE OUTPUT DATA

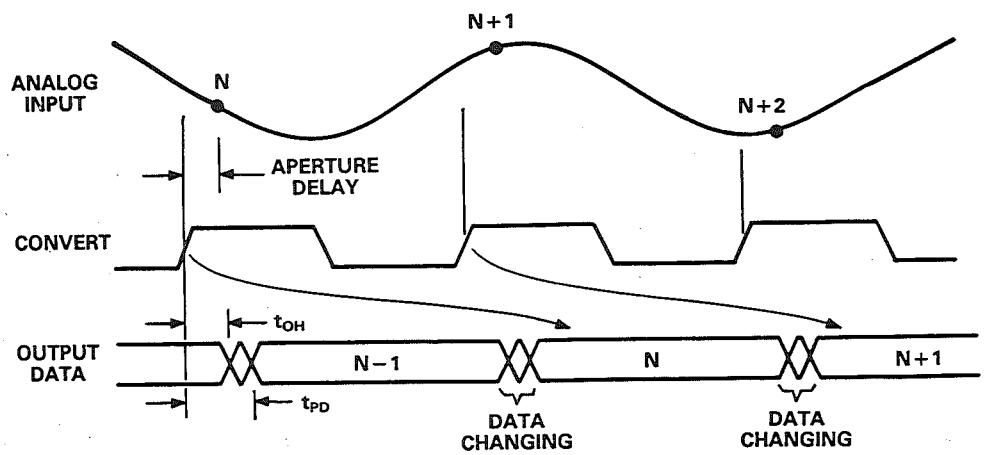


Figure 13.8

Some subranging ADCs, in fact, have several clock cycles of latency. A block diagram of the AD872 12 bit, 10MSPS ADC is shown in Figure 13.9. The conversion is implemented using a 4-stage pipelined multiple flash architecture with error correction. The timing diagram for the device is shown in Figure 13.10. Note that there are three clock-cycle delays in the output data. If the ADC is used inside a servo loop this delay should be considered when calculating loop stability. Also, because the converter is working on three conversions simultaneously, major disruptions to the device (such as a large glitch on the supplies or reference) may corrupt three data samples.

AD872 12-BIT, 10MSPS PIPELINED ADC ARCHITECTURE

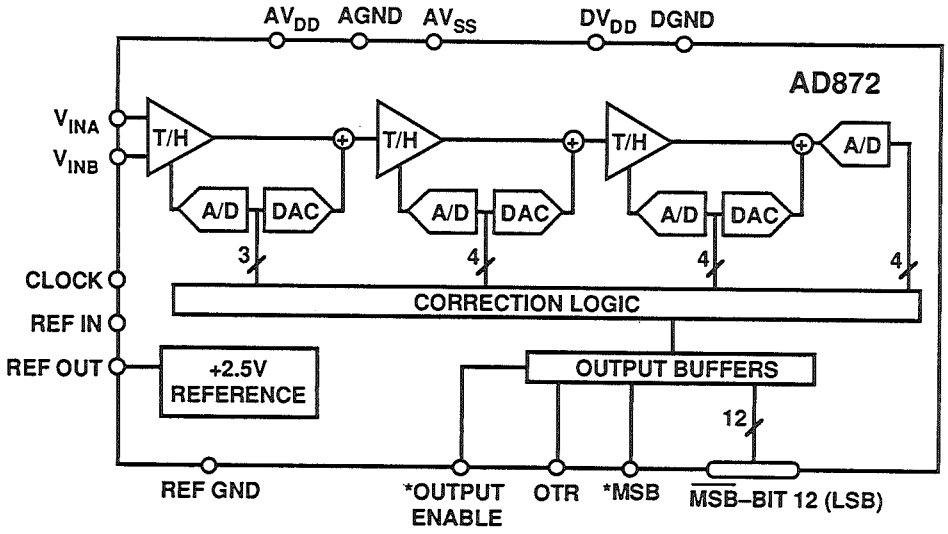


Figure 13.9

AD872 TIMING DIAGRAM SHOWS 3 CLOCK-CYCLE LATENCY

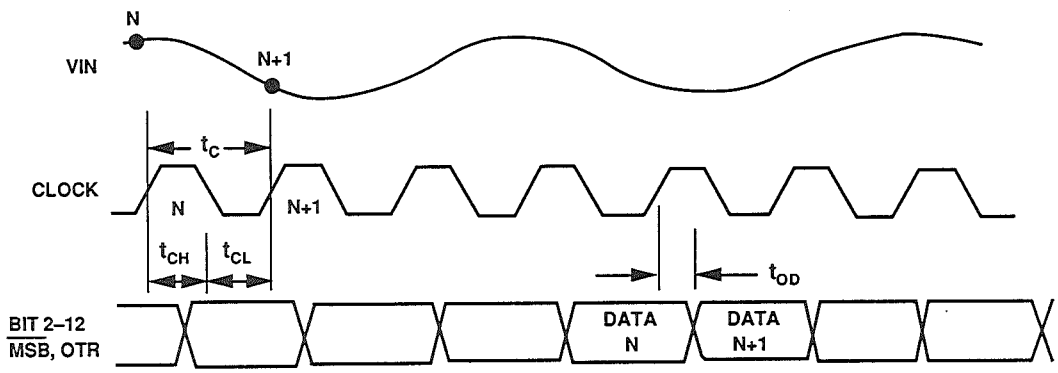


Figure 13.10

DEMULTIPLEXING HIGH SPEED ADC OUTPUTS

In most high speed applications, the output data from the ADC must be downloaded into a buffer memory for further processing. In order to avoid costly high speed, high power memory, the demultiplexing scheme shown in Figure 13.11 may be used to reduce the data output rate. This will allow low cost CMOS memory to be used for storage of the bulk of the data.

High speed flash converters may provide on-chip demultiplexing for easing the requirements on the buffer memory interface. For example, the AD9032 8 bit, 300MSPS ADC is presented to the output of the ADC on two 8 bit ports. The data rate for each port is therefore 150MSPS for a sampling clock frequency of 300MSPS. The data on each port can be further demultiplexed externally for eventual storage in CMOS memory.

DEMULTIPLEXING HIGH SPEED ADC OUTPUTS FOR STORAGE IN SLOWER MEMORIES

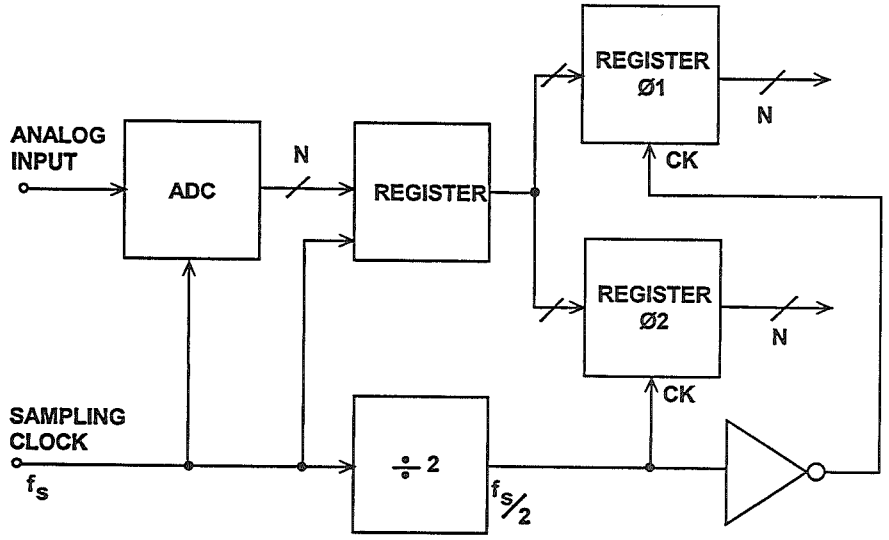


Figure 13.11

DEALING WITH 16-BIT PRECISION SAMPLING ADCS

ADCs with 16-bit resolution and sampling rates of 100kSPS or more have become very popular in real-time DSP applications. These converters present special challenges to the design engineer because they combine all the problems associated with high-speed and wide bandwidth with those problems associated with dc precision. Achieving low noise performance is perhaps the biggest challenge.

An example of a 16-bit sampling ADC is the AD7884/AD7885 166kSPS converter shown in Figure 13.13. The ADC contains an internal SHA and utilizes a recursive subranging architecture with digital error correction. Power dissipation is 250mW. The AD7884 has a 16-bit parallel output structure, while the AD7885 has a byte reading structure. Typical dynamic performance (FFT output and ENOB) is shown in Figure 13.14.

16-BIT SAMPLING ADCs

- Same Issues As High Speed ADCs: Grounding, Layout, Etc.
- Noise May Greatly Impair Performance @ 16 Bits
- Autocalibration Usually Required to Maintain Accuracy Over Extended Temperature Ranges
- Monolithic Solutions Require External Support Circuitry: Voltage References, Input Buffers, Clock Generators
- High Performance Hybrids Offer Complete Solutions at Higher Cost And Power

Figure 13.12

AD7884 16-BIT, 166kSPS ADC BLOCK DIAGRAM

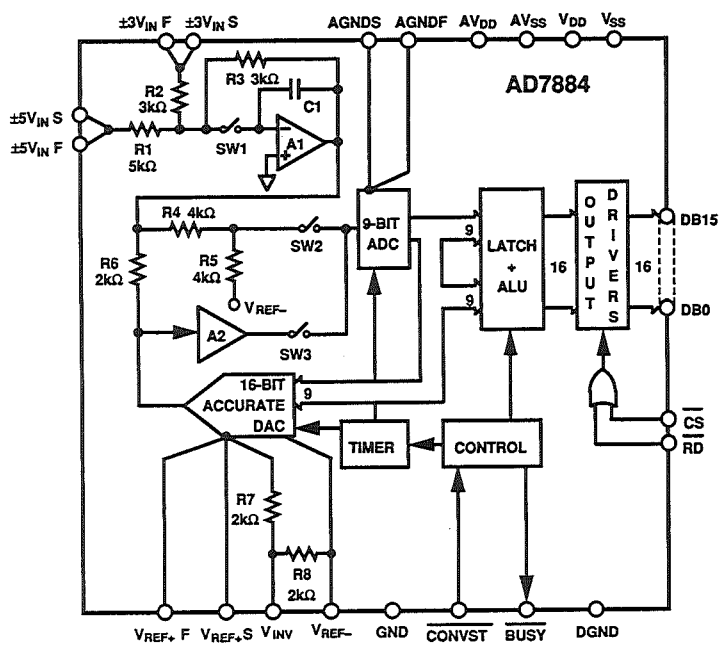


Figure 13.13

AD7884 / AD7885 ADC FFT OUTPUT AND EFFECTIVE BIT PERFORMANCE

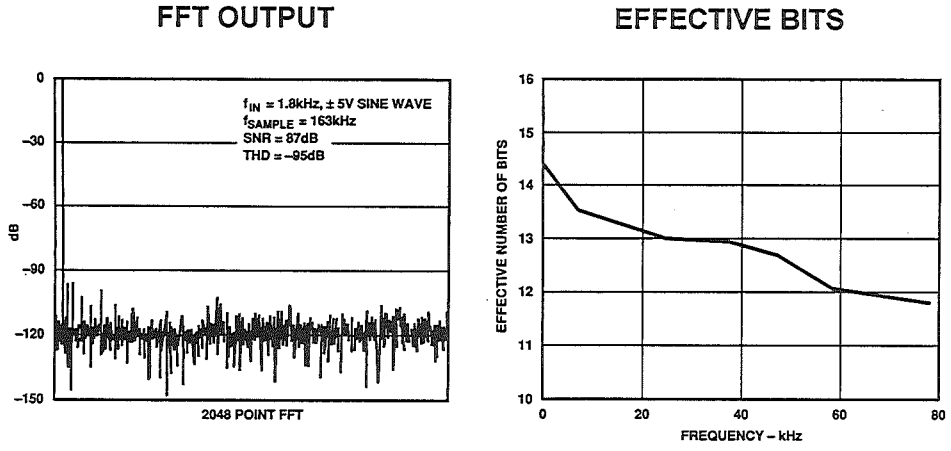


Figure 13.14

Precision 16-bit sampling ADCs such as the AD7884/AD7885 may very well behave differently from their 12-bit counterparts for dc inputs. Ideally, a fixed dc input to an ADC should result in the same output code for repetitive conversions (of course, the dc input should be centered between the transition regions of the two adjacent codes). In the past, ADCs were analyzed for code transition noise using a DAC to reconstruct the analog signal. A very slow ramp voltage was applied to the ADC, so that each code transition could be observed. With a precision 16-bit sampling ADC, however, this test will probably produce some unfamiliar results. In a high-resolution sampling converter, for a given input voltage, there will probably be a range of output codes which may occur. This is because of unavoidable circuit noise within the wideband circuits in the ADC. If a dc signal is applied to the precision sampling ADC and several thousand outputs are recorded, a distribution of codes such as that shown in Figure 13.15 may result.

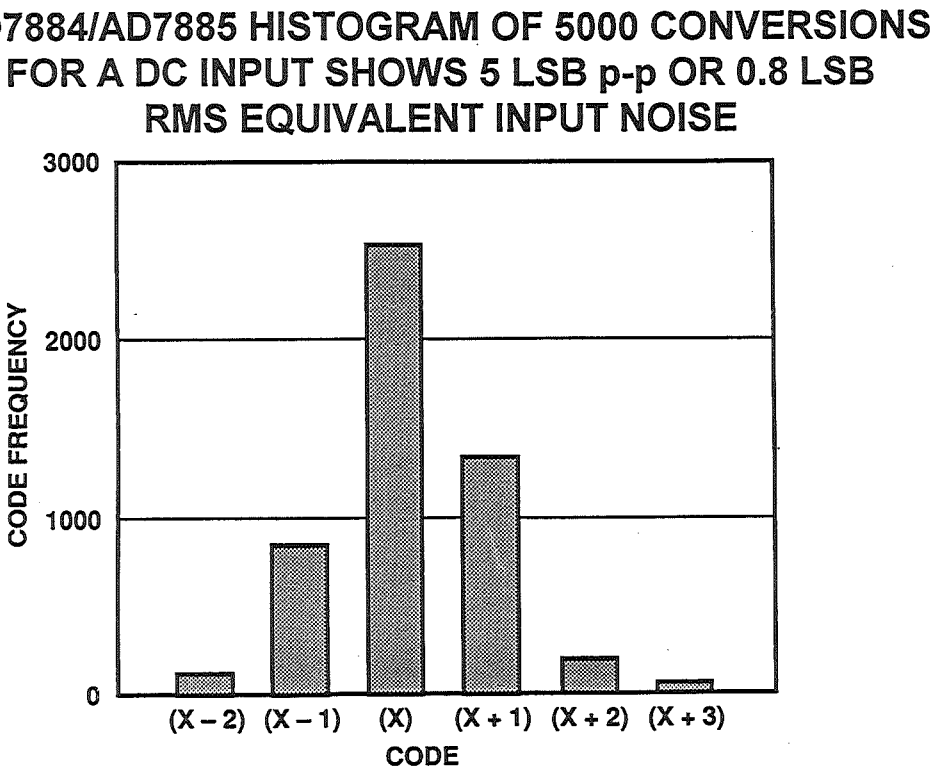


Figure 13.15

The correct code appears most of the time, but adjacent codes appear as well with reduced probability. If a Gaussian probability distribution is fitted to the histogram, the standard deviation is approximately equivalent to the equivalent input rms noise of the ADC. The actual specification on the ADC data sheet may be given in terms of a histogram or may be converted into an equivalent input rms noise voltage. In Figure 13.15, the peak-to-peak noise is about 5 LSBs, corresponding to 5/6 = 0.8 LSBs rms (Peak-to-peak values may be converted into rms values by dividing by 6). For a 6V peak-to-peak input range, this corresponds to 74μV rms equivalent input noise.

This noise may come from several sources. For example, a 1MΩ resistor generates 158μV rms noise over a 1MHz single-pole bandwidth (the equivalent noise bandwidth is 1.57MHz). One LSB for the AD7884 operating with a 6V peak-to-peak input range is 92μV. This illustrates the importance of keeping the source impedances low. Some of the internal ADC noise is generated in the wideband SHA. Sampling ADCs generally have input bandwidths which exceed the Nyquist frequency of one-half the sampling rate. (The AD7884/AD7885 has an input bandwidth which exceeds 1MHz, even though the maximum sampling rate is 166kSPS). These wide bandwidth front ends are required in order to minimize gain and phase distortion at the signal frequencies. A certain amount of unavoidable noise is generated in the SHA and the other wideband circuits within the ADC which cause the sample-to-sample variation in output codes for dc inputs. In addition, good layout, grounding, and decoupling techniques are essential to prevent additional external noise from coupling into the ADC adding to the inherent equivalent input noise.

The AD7884/AD7885 ADC is designed to operate with an external low noise +3V reference such as the AD780. Figure 13.16 shows the analog input and the reference voltage interfaces to the AD7884/AD7885 for a typical single channel application.

Several external components are needed for the reference and for signal conditioning. The analog input buffer should be chosen depending upon the bandwidth of the input signal. For wide bandwidth applications (up to 80kHz), the AD845, AD847, or AD744 is suitable. For lower bandwidth applications it is possible to use slower op amps such as the AD711.

The VREF(+) input is driven by the AD780 reference which is configured for a 3V output range. The AD780 output is decoupled directly to ground with a 10μF capacitor to absorb the transient voltages generated by the on-chip DAC.

The VREF(–) input is driven with a high speed amplifier like the AD845, AD847, AD827 (dual), or the AD744. The wide bandwidth is needed to handle the transients produced by the on-chip DAC. Likewise, AGNDF is also driven by a high speed op amp which is sensed to AGNDS. Again, either the AD845, AD847, AD827, or the AD744 may be used.

If the AD744 is used in any of the above circuits, a 5.6pF capacitor should be connected between the compensation pins (pin 5 and pin 8) for stability.

The AD676 is a multipurpose 16-bit 100kSPS parallel output ADC which utilizes a switched-capacitor, charge redistribution architecture. Overall performance is optimized by digitally correcting internal nonlinearities through on-chip autocalibration. A block diagram of the AD676 is shown in Figure 13.17.

INPUT AND REFERENCE INTERFACE TO THE AD7884/AD7885

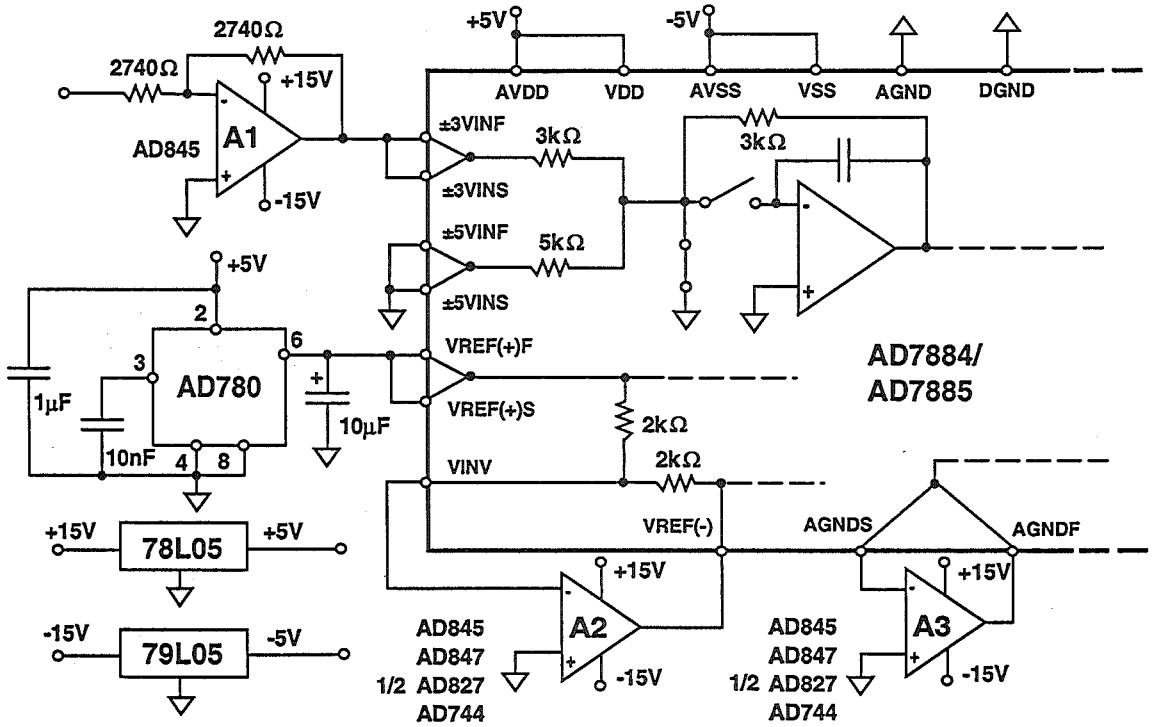


Figure 13.16

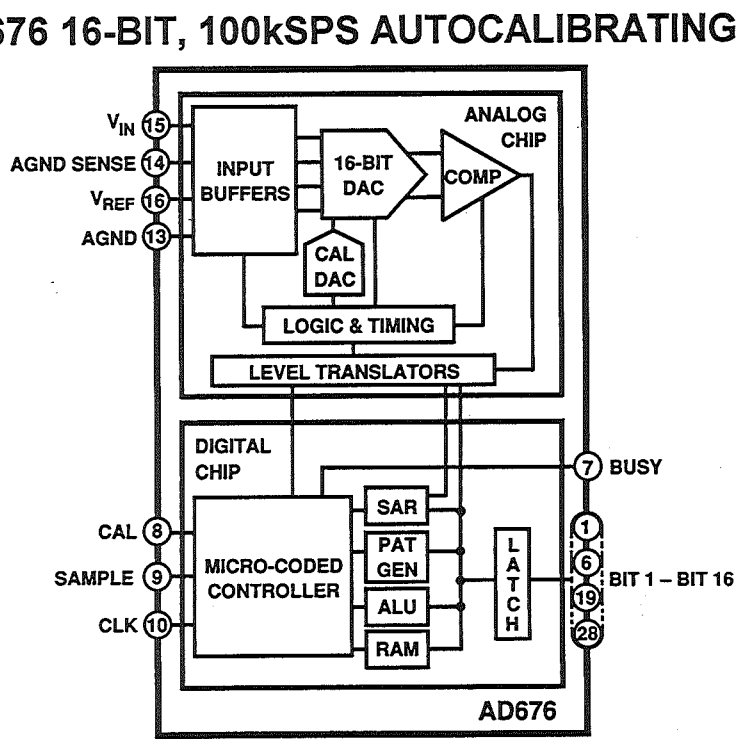


Figure 13.17

The AD676/AD677 employs a successive approximation technique to determine the value of the analog input voltage. However, instead of the traditional laser trimmed resistor ladder approach, this device uses a capacitor array, charge redistribution technique. Binary-weighted capacitors subdivide the input sample to perform the actual analog to digital conversion. The capacitor array eliminates variation in the linearity of the device due to temperature-induced mismatches of resistor values. Since a capacitor array is used to perform the data conversion, the SHA function is included without the need for additional circuitry.

Initial errors in capacitor matching are eliminated by an autocalibration circuit. This circuit employs an on-chip microcontroller and a calibration DAC to measure and compensate capacitor mismatch errors. In the calibration mode, each individual code (65,536 total) is checked for INL and DNL errors. When an error is detected, a correction value is stored in RAM. In normal operation, the ADC actually outputs the coded input plus the correction factor for that output code. The autocalibration routine may be invoked at any time. The complete autocalibration cycle requires approximately 50ms when sampling at 100kSPS. Autocalibration ensures high performance while eliminating the need for any user adjustments.

Designing with high resolution ADCs requires careful attention to board layout. Trace impedance is a significant issue. A 1.22mA current through a 0.5Ω trace will develop a voltage drop of 0.6mV, which is 4 LSBs at the 16-bit level for a 10V fullscale span.

The AD676 provides an Analog Ground Sense (AGND SENSE) pin that can be used to compensate for small voltage drops (<100mV) in the analog signal of the return line as shown in Figure 13.18. The AGND SENSE pin is used to remotely sense the ground potential of the signal source, and is especially useful if the signal has to be carried some distance to the ADC. Figure 13.18 also shows how the signal wires should be shielded in a noisy environment to avoid capacitive coupling. The AGND and DGND of the AD676 should be both tied together at the device and connected to the PCB Analog Ground Plane.

The AD676 is available in a 28-pin plastic DIP or a 28-pin side-brazed ceramic package. A serial output version, the AD677, is available in a 16-pin 300mil wide ceramic or plastic package. Both devices are specified for both ac and dc parameters. Typical S/(N+D) and effective bit performance is shown in Figure 13.19.

Like the AD7884/AD7885 ADC, the AD676/AD677 generates a certain amount of equivalent internal noise. The histogram for a dc input is shown in Figure 13.20. Notice that the peak-to-peak noise is approximately 3 LSBs, corresponding to 0.5 LSBs rms.

AD676 AGND SENSE PIN CONNECTIONS FOR SHIELDED TWISTED PAIR CABLE

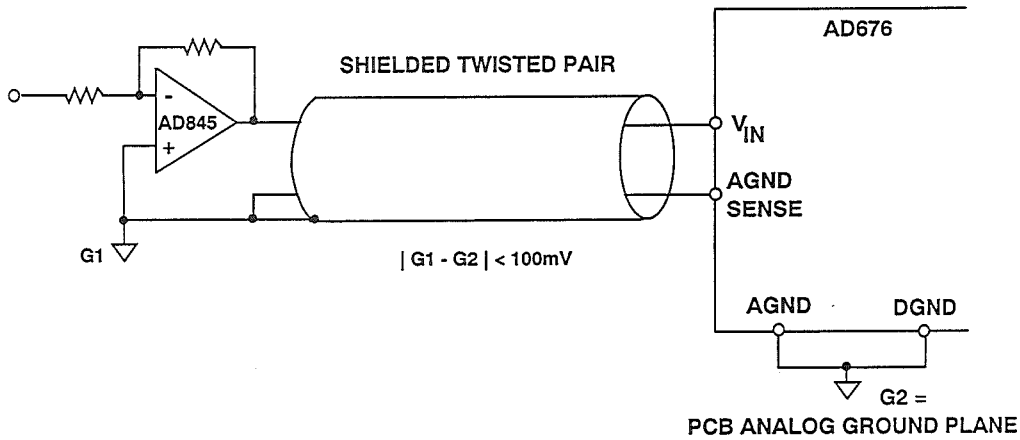


Figure 13.18

AD676 16-BIT, 100kSPS SAMPLING ADC S/N + D AND EFFECTIVE BIT PERFORMANCE

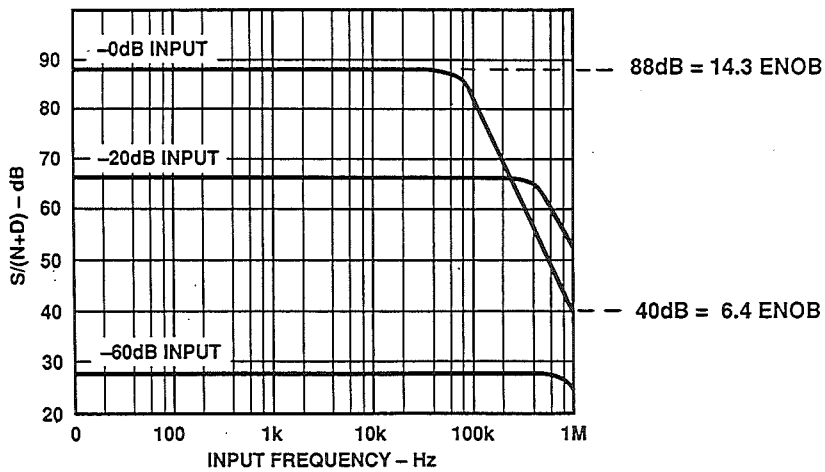


Figure 13.19

AD676 DISTRIBUTION OF CODES FROM 1000 CONVERSIONS FOR A DC INPUT SHOWS 3 LSBs p-p, OR 0.5 LSBs RMS EQUIVALENT INPUT NOISE

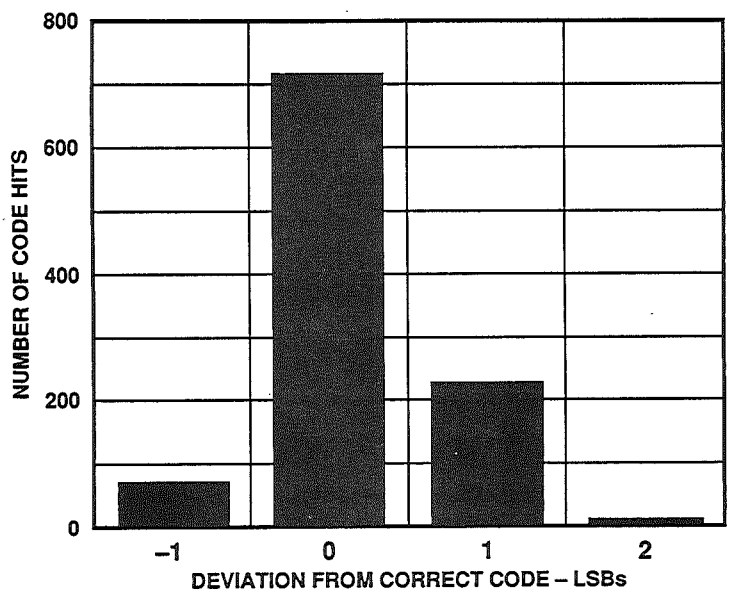


Figure 13.20

A simplified schematic of the input circuit of the AD676 is shown in Figure 13.21. All of the inputs (V_{in}, V_{ref}, and AGND SENSE) produce transient load currents which must be absorbed by their respective drivers. When a conversion cycle begins, each analog input is connected to an internal, discharged 50pF capacitor which then charges to the voltage present at the corresponding pin. The capacitor is disconnected when the SAMPLE line is taken LOW, and the stored charge is used in the subsequent conversion. In order to limit the demands placed on the external source by this high initial charging current, an internal low-accuracy buffer amplifier is connected between the input and this capacitance for a few hundred nanoseconds. During this time the input pin exhibits typically 20kΩ| |10pF and ±40μA bias current.

Next, the input is switched directly to the now precharged capacitor and allowed to fully settle. During this time, the input appears as a 50pF capacitor. Once the sample is taken, the input is internally floated so that the external input source sees a very high input resistance and a parasitic input capacitance of only 2pF. As a result, the input to the AD676/AD677 applies transient currents and transient impedances to the output of the drive amplifer.

The drive amplifier for the AD676 must therefore have fast settling time, low distortion and 16-bit dc accuracy. The AD797 low distortion bipolar op amp is an excellent choice for this application. Key specifications are summarized in Figure 13.22. Typical voltage noise and THD are shown in Figure 13.23.

AD676 EQUIVALENT INPUT CIRCUIT

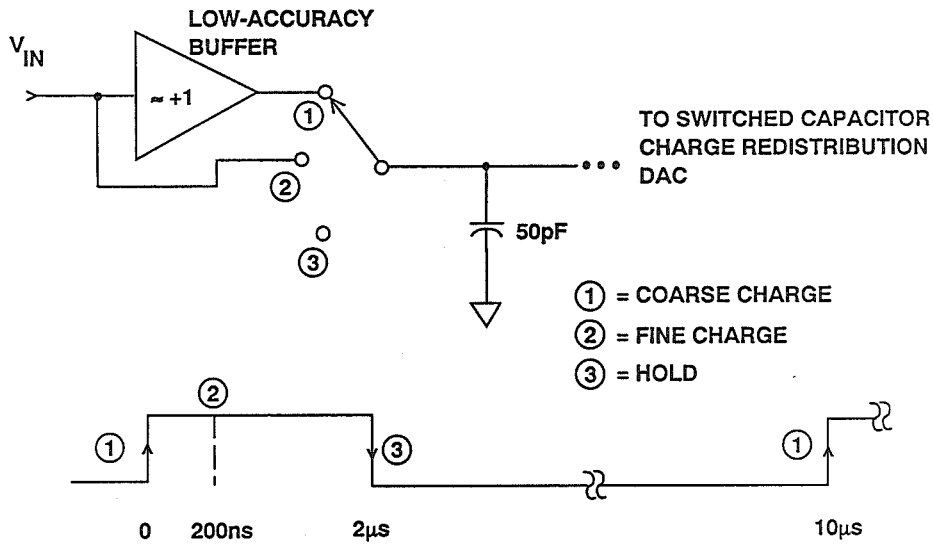


Figure 13.21

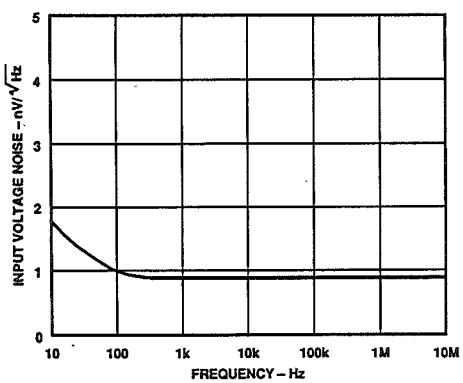
AD797 PRECISION LOW DISTORTION BIPOLAR OP AMP KEY SPECIFICATIONS

- 0.1mV Input Offset Voltage
- 0.2μV/°C Offset Voltage Drift
- 100nA Input Offset Current
- 1,000,000 dc Open Loop Gain
- 100MHz Gain Bandwidth Product
- 110dB THD @ 20kHz, 3Vrms into 600Ω
- 0.9nV/$\sqrt{Hz}$, 2pA/$\sqrt{Hz}$ Input Noise at 1kHz

Figure 13.22

AD797 ULTRA-LOW-NOISE OP AMP VOLTAGE NOISE AND THD PERFORMANCE

VOLTAGE NOISE



THD

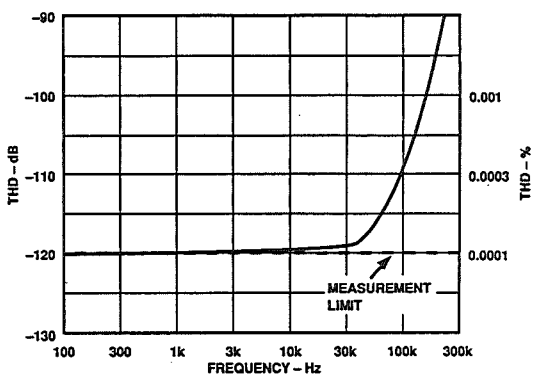


Figure 13.23

Figure 13.24 shows the calculations for the total output noise of the AD797 over the 1MHz input bandwidth of the AD676. The total noise is computed to be only 7μV rms compared to the theoretical 16-bit quantization noise (10V fullscale range) of 44μV rms.

If the application requires a FET input amplifier, the AD845 may be used as a drive amplifier for the AD676 yielding a total output noise of 30μV rms as shown in Figure 13.25.

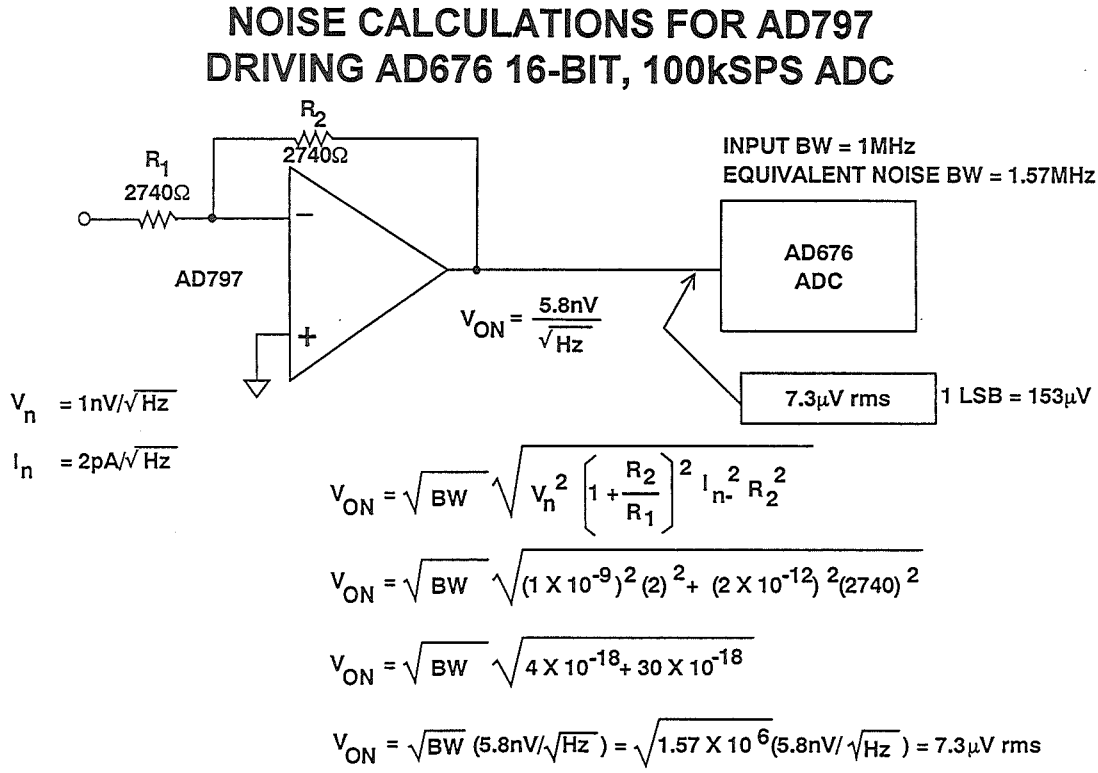
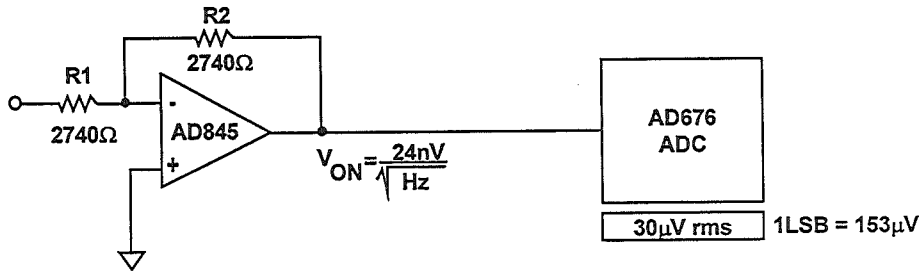


Figure 13.24

AD845 DRIVING AD676 16-BIT, 100kSPS ADC

AD845 SPECS: $V_N = 12nV/\sqrt{Hz}$
$I_N = 0.1pA/\sqrt{Hz}$

AD676 SPECS: INPUT BW = 1MHz
EQUIVALENT NOISE BW = 1.57MHz



$$V_{ON} = \sqrt{BW}\sqrt{V_N^2\left(1+\frac{R_2}{R_1}\right)^2 + I_{N-}^2 R_2^2}$$

$$V_{ON} = \sqrt{BW}\sqrt{(12\times10^{-9})^2(2)^2 + (0.1\times10^{-12})^2(2740)^2}$$

$$V_{ON} = \sqrt{BW}\sqrt{576\times10^{-18} + 0.075\times10^{-18}}$$

$$V_{ON} = \sqrt{BW}\,(24nV/\sqrt{Hz}) = \sqrt{1.57\times10^6}\,(24nV/\sqrt{Hz}) = 30\mu V\ rms$$

Figure 13.25

Both the AD7884/AD7885 and the AD676/AD677 ADCs require an external voltage reference. This is because the IC processes which are typically used for precision sampling converters do not support 16-bit accurate (or better) voltage reference circuits. The reference voltage establishes the fullscale range of the ADC, and the overall dc accuracy and stability of the ADC can be no better than that of the reference. Standard monolithic reference voltage values are 2.5V and 3V (AD780), and 5V (AD586) and 10V (AD587).

The entire voltage reference function is available in ICs which utilize laser trimmed thin film resistors for excellent accuracy and low drift. Standard dc specifications for such a voltage reference are output current capability, line regulation, load regulation, output voltage tolerance, and output voltage change with temperature. AC specifications include turn-on settling time, transient load current settling time, and noise. Selecting voltage references based on dc requirements is relatively straightforward. Evaluating its noise performance deserves further discussion because noise on the ADC reference voltage input usually translates directly into increased internal noise levels and degraded SNR performance.

Most voltage references specify peak-to-peak noise in a 0.1Hz to 10Hz bandwidth. For instance, the AD586 (a 5V buried zener reference with on-chip output buffer) specification in this bandwidth is 4μV peak-to-peak. In most sampling ADC applications, however, the wideband noise is usually of more concern. For the AD586, the unfiltered noise in a 1MHz bandwidth is approximately 200μV peak-to-peak, corresponding to 200/6 = 33μV rms. This value is usually larger for bandgap voltage references such as the REF-02 (800μV peak-to-peak). Regardless of the type of reference chosen, proper exter-

nal filtering can virtually eliminate the wideband noise.

Some voltage references, such as the AD586, have a pin brought out designated as the noise reduction pin (see Figure 13.26). Connecting an external capacitor between ground and this pin forms a single-pole lowpass filter with an internal 4000Ω resistor. For instance, an external 1μF capacitor produces a single-pole corner frequency of approximately 40Hz. This filter virtually eliminates the broadband buried-zener noise, but the output buffer amplifier (approximate bandwidth is 1MHz) still produces approximately 160μV peak-to-peak noise in the 1MHz bandwidth. The large capacitor also greatly increases startup time.

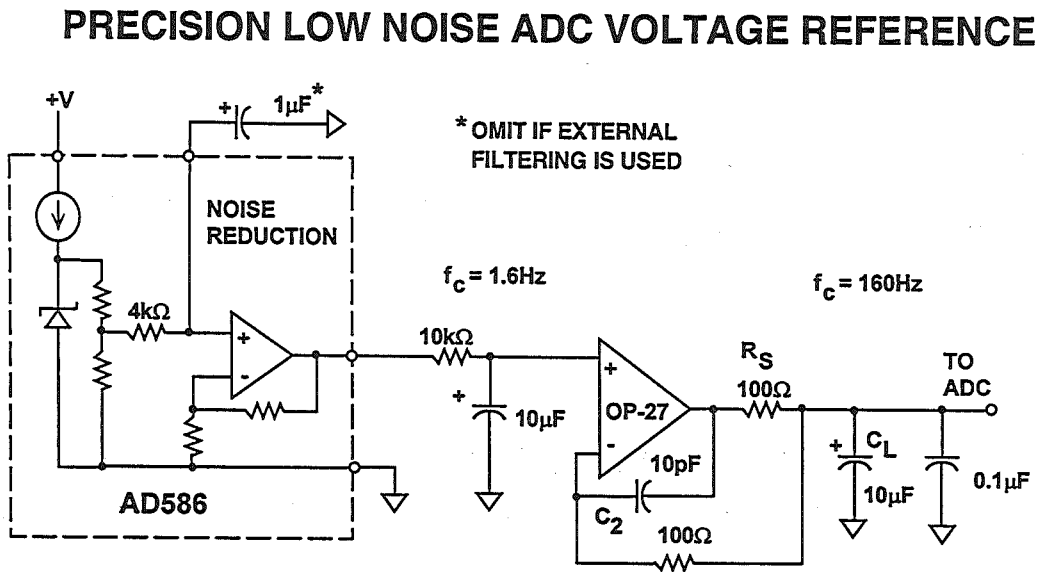


Figure 13.26

If low noise is required, adding a large capacitor on the reference output (10μF) will reduce the noise. This, however, may not produce the expected results for two reasons. First, the voltage reference output buffer amplifier has a low closed-loop output impedance on the order of a few ohms at low frequencies. The additional large capacitor does little to reduce this impedance further. Second, loading the output of the internal op amp with a large capacitor may cause the op amp to become unstable and to oscillate or ring under transient load conditions. (This is not the case with the AD780 2.5V/3V reference which is designed to be stable regardless of the capacitive load).

The ideal solution in precision applications is to use an external filter such as the one shown in Figure 13.26. The 10kΩ resistor and the 10μF capacitor form a single-pole passive filter which has a corner frequency of 1.6Hz, and reduces the noise to approximately the value specified in the 0.1 to 10Hz frequency band (4μV peak-to-peak for

the AD586 and the AD780). This passive filter is followed by a precision low noise buffer amp such as the OP-27 (V_n= 3nV/√Hz). The large load capacitor (C_L = 10μF) serves two purposes. First, it forms a lowpass filter with R_S having a corner frequency of approximately 160Hz. This reduces the output voltage noise of the op amp to a negligible value. Second, it provides additional reference voltage stability by acting as a charge reservoir to any transient load current. This amount of capacitance is a heavy load on any op amp; therefore, R_S and C_2 compensate for the pole introduced by C_L and the op amp's output resistance. This compensation scheme ensures that the buffer circuit recovers and settles from the output transients quickly without the long settling tails that might produce conversion errors. The 0.1μF capacitor in parallel with C_L is to keep the output impedance low at high frequencies, where the large 10μF electrolytic capacitor becomes less effective. When using external filtering, do not decouple the noise reduction pin with a capacitor. The capacitor will increase the refrence startup time.

In applications where filtering the voltage reference noise is not required, the decoupling capacitors on the ADC reference voltage input terminal may be eliminated completely. Simply buffer the voltage reference output with a precision low noise high bandwidth amplifier which has sufficient transient load settling time, such as the AD845 as shown in Figure 13.27. This approach will minimize the need for additional components, but dc precision and noise performance will be sacrificed.

WIDEBAND BUFFER AMPLIFIER ELIMINATES THE NEED FOR LARGE DECOUPLING CAPACITORS

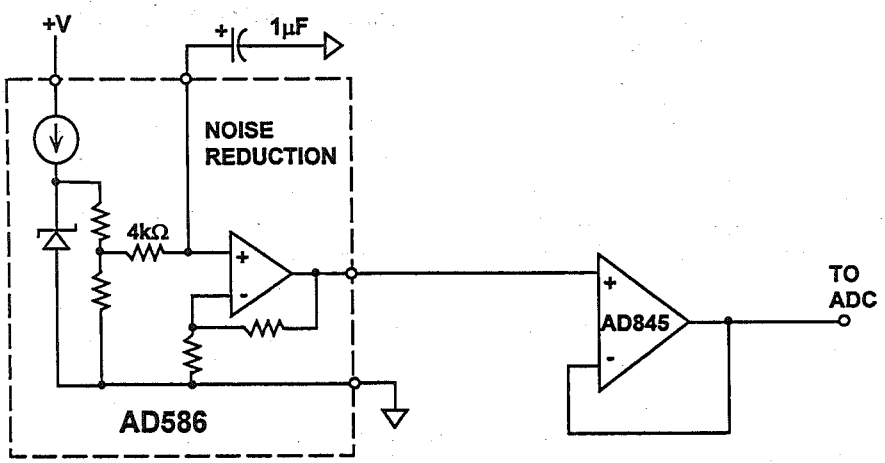


Figure 13.27

The AD1385 is a 16 bit, 500kSPS hybrid sampling ADC which contains on-board autocalibration circuits. The device is both ac and dc specified over the full temperature range of –55°C to +125°C. A block diagram of the device is shown in Figure 13.28.

The AD1385 architecture includes a low noise, low distortion track/hold, a three pass digitally corrected subranging ADC, and autocalibrating circuitry for excellent linearity. A complete linearity calibration requires 15ms. Precision thin film resistors and a proprietary DAC contribute to the outstanding dynamic and static performance. The AD1382 is a similar device, but is factory calibrated to meet full specifications from +10°C to +40°C.

Figure 13.29 shows the FFT output of the AD1385 at 25°C before and after autocalibration. Recalibration is recommended whenever the device's temperature has changed by more than 15°C. Performance degrades gracefully with temperature changes, resulting in small but gradual decreases in SNR and increases in distortion which may be eliminated by recalibration. The first FFT plot in Figure 13.30 was obtained by calibrating the AD1385 at +25°C and then elevating the case temperature to +125°C. The second FFT plot shows the AD1385 performance after recalibration at +125°C.

AD1385 16-BIT, 500kSPS ADC BLOCK DIAGRAM

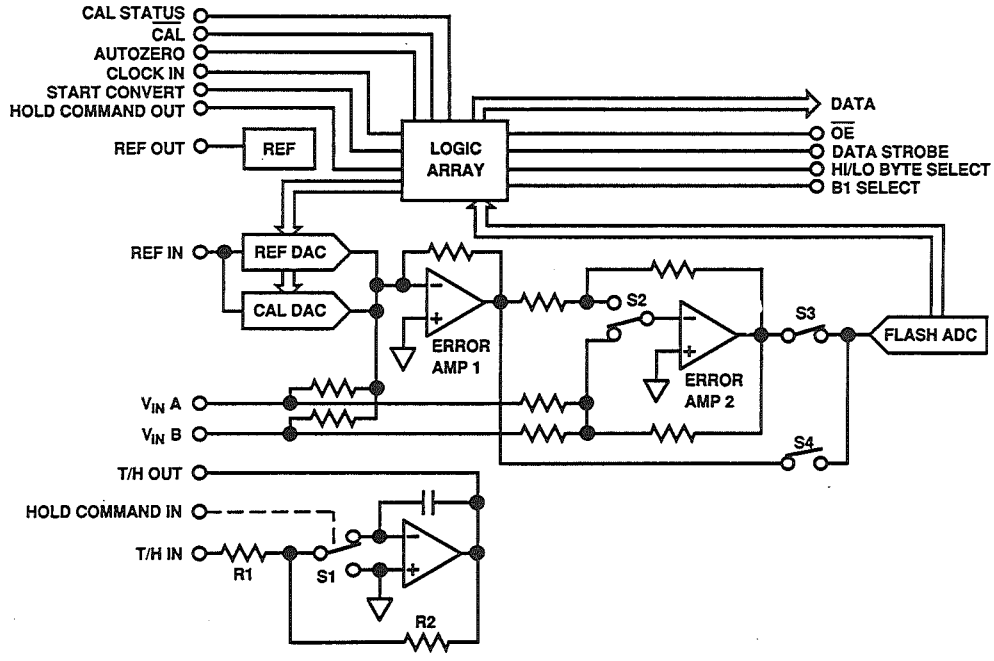


Figure 13.28

AD1385 ADC FFT OUTPUT AT +25°C BEFORE AND AFTER AUTO-CALIBRATION

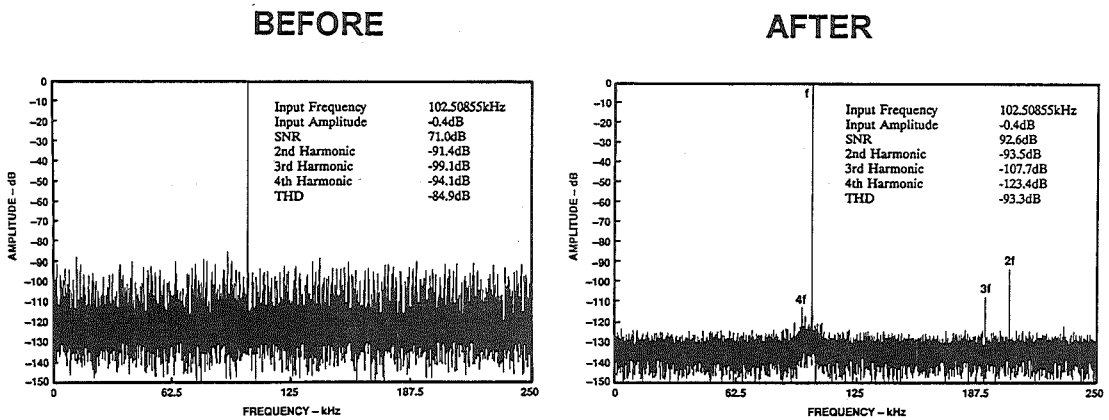


Figure 13.29

AD1385 ADC FFT OUTPUT AT +125°C BEFORE AND AFTER AUTO-CALIBRATION

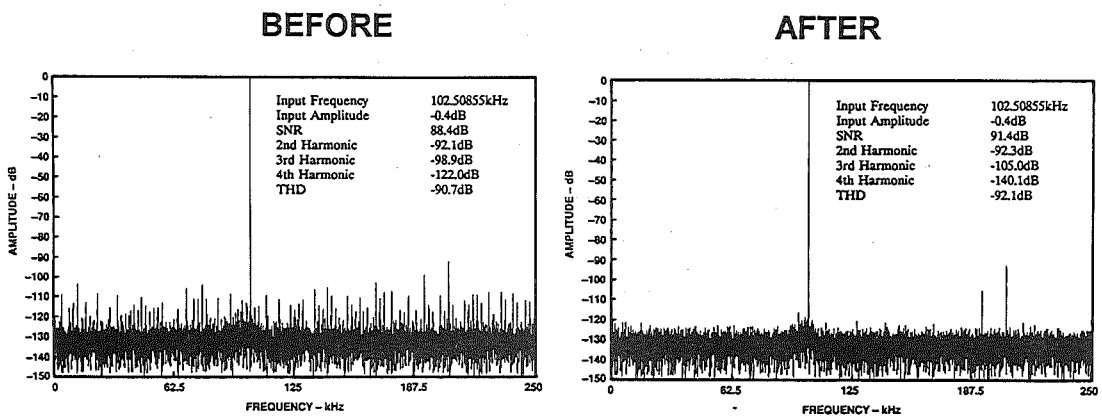


Figure 13.30

The AD1385 also has an Autozero function which may be used to digitally correct internal offsets in the track/hold and the ADC circuit. To use the Autozero function, the track/hold input must be connected to a zero reference prior to the zeroing conversion. This connection is external to the AD1385 and must be provided by the user. When the Autozero feature is enabled, the AD1385's digital out is forced to indicate exactly zero when its input is at the zero point, nominally 0V. Autozero operates by storing the digital result of a zeroing conversion and subtracting it from all subsequent conversion results. This reduces the maximum nonsaturating input of the AD1385 by a small amount at one end of its range depending on the magnitude and polarity of the offset.

DATA OUTPUT CONSIDERATIONS FOR PRECISION SAMPLING DSP ADCS

Precision sampling ADCs usually will have either parallel data outputs (one pin per bit), or a single serial output data line. The parallel case will be considered first.

Many parallel output sampling ADCs offer three-state outputs which can be enabled or disabled using an *output enable* pin on the IC. While it may be tempting to connect these three-state outputs directly to a backplane data bus, severe performance-degrading noise problems may result for the following reasons. All ADCs have a small amount of internal stray capacitance between the digital outputs and the analog input (typically 0.1 to 0.5pF). Every attempt is made during the design and layout of the ADC to keep this capacitance to a minimum. However, if there is excessive overshoot and ringing and possibly other high frequency noise on the digital output lines (as would probably be the case if the digital outputs were connected directly to a backplane bus) this digital noise will couple back into the analog input through the stray capacitance. The effect of this noise is to decrease the overall ADC SNR and ENOB. Any code-dependent noise will also tend to increase the ADC harmonic distortion.

The best approach to eliminating this potential problem is to provide an intermediate three-state output buffer latch which is located close to the ADC data outputs. This latch serves to isolate the noisy signals on the data bus from the ADC data outputs, thereby minimizing any coupling back into the ADC analog input.

The ADC data sheet should be consulted regarding exactly how the ADC data should be clocked into the buffer latch. Usually, a signal called *conversion complete*, or *busy* is provided from the ADC for this purpose.

It is also a good idea not to access the data in the intermediate latch during the actual conversion time of the ADC. This practice will further reduce the possibility of corrupting the ADC analog input with noise. The manufacturer's data sheet timing information should indicate the most desirable time to access the output data.

Figure 13.31 shows a simplified parallel interface between the AD676 16 bit, 100kSPS ADC (or theAD7884) and the ADSP-2101 microcomputer. (Note: the actual device pins shown have been relabled to simplify the following gen-

eral discussion). In a realtime DSP application (such as in digital filtering) the processor must complete its series of instructions within the ADC sampling interval. Note that the entire cycle is initiated by the sampling clock edge from the sampling clock generator. Even though some DSP chips offer the capability to generate lower frequency clocks from the DSP master clock, the use of these signals as precision sampling clock sources is not recommended due to potential excess timing jitter. It is preferable to generate the ADC sampling clock from a well-designed low noise crystal oscillator circuit as has been previously described.

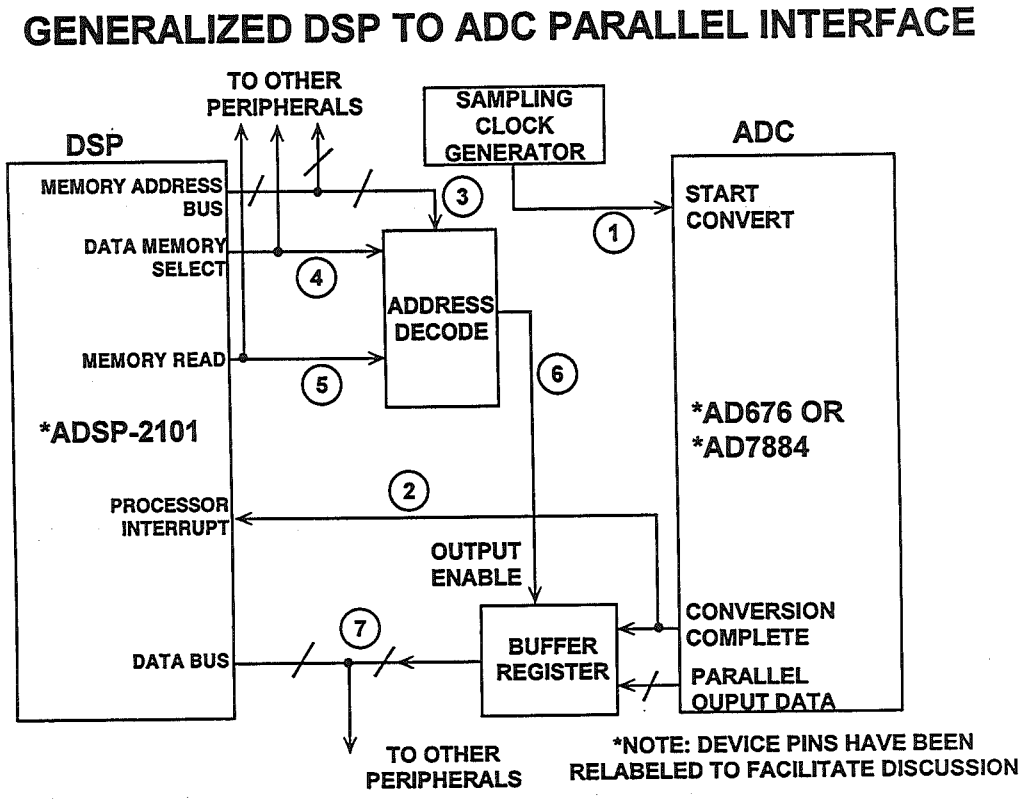


Figure 13.31

The sampling clock edge initiates the ADC conversion cycle. After the conversion is completed, the ADC *conversion complete* line is asserted which in turn interrupts the DSP. The DSP then places the address of the ADC which generated the interrupt on the *data memory address* bus and asserts the *data memory select* line. The *read* line of the DSP is then asserted. This enables the external three-state ADC buffer register outputs and places the ADC data on the *data bus*. The trailing edge of the *read* pulse latches the ADC data on the *data bus* into the DSP internal registers. At this time, the DSP is free to address other peripherals which may share the common data bus.

Because of the high-speed internal DSP clock (50MHz for the ADSP-2101), the width of the *read* pulse may be too narrow to properly access the data in the buffer latch. If this is the case,

adding the appropriate number of programmable software wait states in the DSP will both increase the width of the *read* pulse and also cause the *data memory select* and the *data memory address* lines to remain asserted for a correspondingly longer period of time. In the case of the ADSP-2101, one wait state is one instruction cycle, or 80ns.

ADCs which have a serial output (such as the AD677, AD776, and AD1879) are interfaced to the serial port of many DSP chips as shown in Figure 13.32. The sampling clock is generated from the low-noise oscillator. The ADC output data is presented on the *serial data* line one bit at a time. The *serial clock* signal from the ADC is used to latch the individual bits into the serial input shift register of the DSP serial port. After all the serial data is transferred into the serial input register, the serial port logic generates the required processor interrupt signal. The advantages of using serial output ADCs are the reduction in the number of interface connnections as well as reduced noise because of fewer digital runs. In addition, SAR and Sigma-Delta ADCs are inherently serial-output devices. The number of peripheral serial devices permitted is limited by the number of serial ports available on the DSP chip.

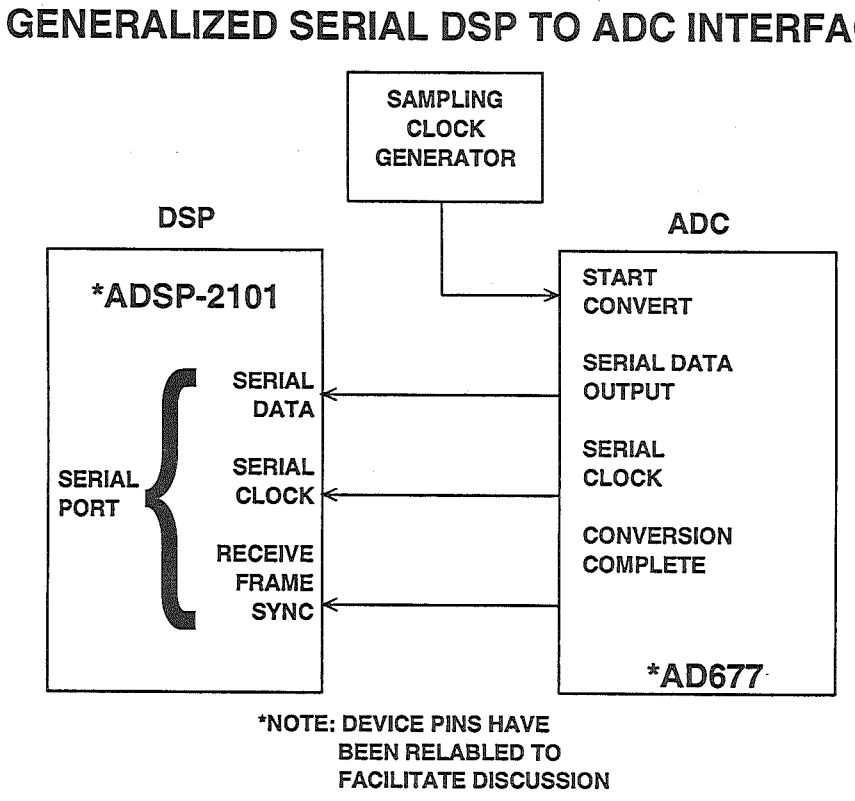


Figure 13.32

PROTECTING THE ADC INPUT FROM OVERDRIVE AND PREVENTING LATCHUP

Most ADCs will tolerate moderate out-of-range signals in the order of 50% or so without damage to the input circuit. The exception to this are certain flash converters which have unipolar negative input ranges. This will be discussed shortly.

For example, an ADC with an input range of ±5V should tolerate an input signal up to ±7.5V. It is usually true, however, that the overvoltage recovery time of an ADC increases as the input signal moves further out of range.

It may be desirable, therefore, to clamp the ADC input so that the input signal is limited to small overrange values. This is especially true if large out-of-range signals are frequently expected. Clamping therefore not only protects the internal ADC input circuits from damage, but also reduces the overvoltage recovery time.

Because the clamping circuit is in the signal path (between the drive amplifier and the ADC), care must be taken to insure that the clamp circuit does not degrade the system performance for normal in-range signals.

The circuit shown in Figure 13.33 utilizes low capacitance (1.2pF), low leakage (100nA @ 15V reverse bias) Schottky diodes (1N5712) to clamp the ADC input to adjustable levels. The series resistor must be chosen so that the drive amplifier output current is limited to acceptable values for overrange signals. A single Schottky diode is capable of withstanding up to 50mA of forward current for short periods of time. If additional current-handling capability is required, two diodes may be paralleled at the expense of additional capacitance and reverse leakage current.

ADJUSTABLE POSITIVE AND NEGATIVE CLAMP CIRCUIT

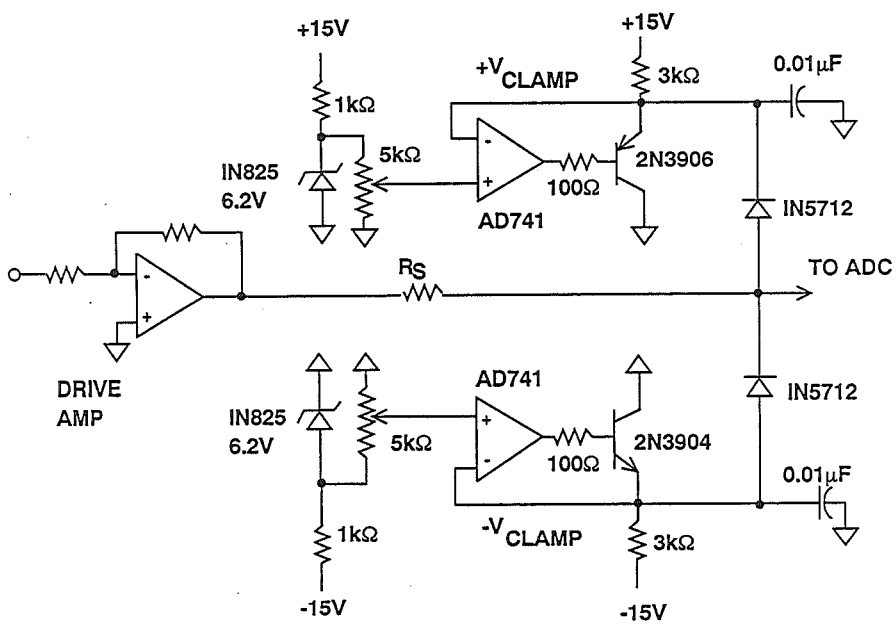


Figure 13.33

Other conditions of temporary overvoltage may occur because of power supply sequencing. Several possibilities will be discussed briefly.

Figure 13.34 shows an op amp powered by ±15V supplies driving an ADC which is powered by ±5V supplies (typical of many high speed ADCs). If the op amp supplies are brought up before the ADC supplies, an overvoltage condition on the ADC input may cause latch up and destroy the device. In addition, the analog input voltage to a CMOS ADC should never exceed the supply voltages, or a latch-up condition may occur. The diodes shown in the figure will protect against this condition. In fact, some CMOS ADCs have the protection diodes on-chip.

PROTECTION AGAINST LATCH-UP AND DAMAGE DUE TO SUPPLY SEQUENCING

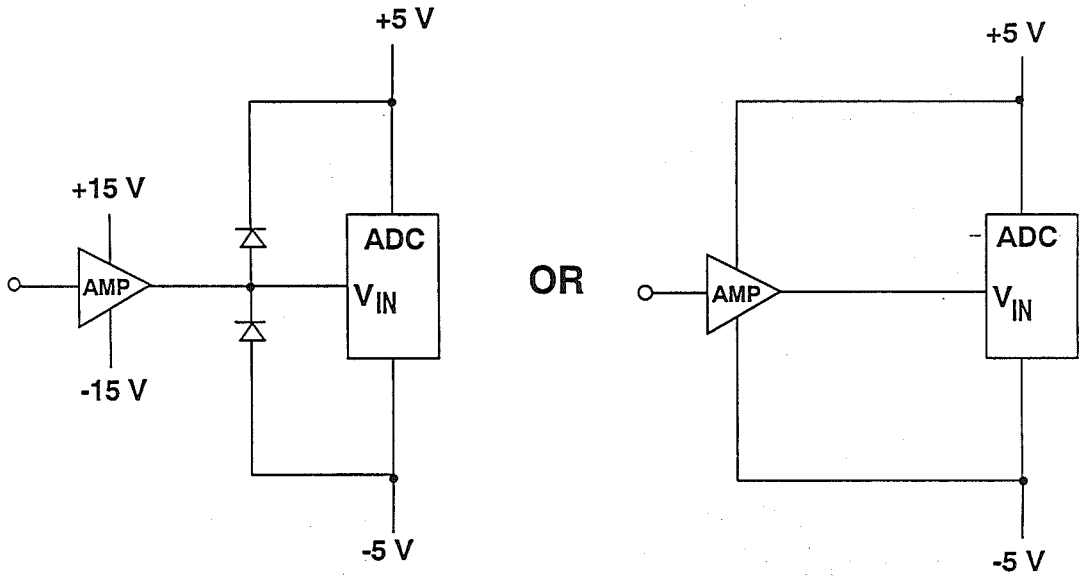


Figure 13.34

An alternative is also shown in Figure 13.34. If a ±5V supply op amp is chosen, then both the ADC and the op amp may be powered from the same supplies, thereby eliminating the potential latch-up problem. It should be noted that many op amps have specifications for both ±15V and ±5V supply operation. If a ±15V op amp must be used, the ±5V for the CMOS ADC may be derived from a three-terminal voltage regulator as shown in Figure 13.35. This is relatively efficient because most CMOS ADCs are low power devices. This scheme also has the advantage of isolating the ADC from the noise on the ±5V supplies in a system which is used to power digital circuitry.

USING 3-TERMINAL REGULATORS AS ADC SUPPLIES

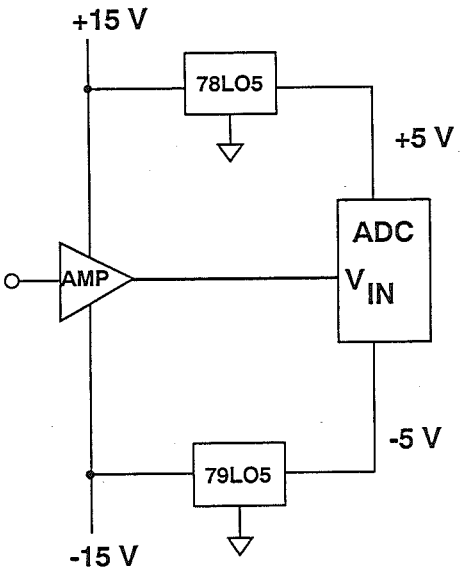


Figure 13.35

Many flash converters are designed to operate on a single –5.2V power supply and have a negative input voltage range of 0 to –2V. If the input goes positive, the substrate silicon diode begins to conduct. Any amount of forward current above a few mA may permanently degrade the performance of the flash converter. Input Schottky diodes should be installed as shown in Figure 13.36 to prevent this condition. Most amplifiers suitable for driving flash converters (such as the AD9617) operate on dual 5V supplies and can deliver 50 to 100mA of output current. The series resistor should be chosen to limit this current to an acceptable level. Two diodes should be paralleled if more than 50mA current is expected from the drive amplifier.

PROTECTING FLASH CONVERTER INPUTS WITH SCHOTTKY DIODES

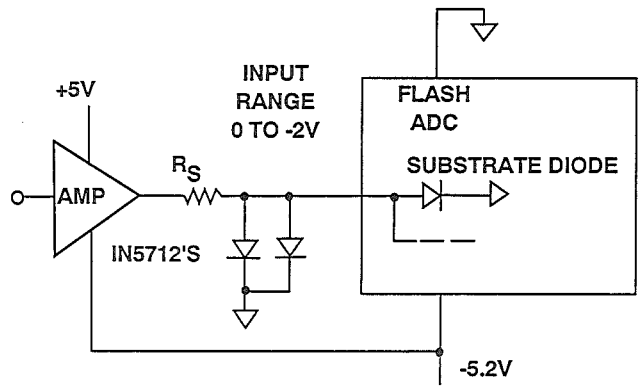


Figure 13.36

SAMPLING CLOCK GENERATION

Many users of sampling ADCs fail to understand the critical nature of the sampling clock signal. The tendency is to focus more on the ADC aperture jitter specification, when in reality, ADC dynamic errors due to noise and jitter on the sampling clock input may far exceed those caused by the internal ADC aperture jitter itself.

Aperture jitter, t_a, is simply the rms value of the sample-to-sample variation in the precise point in time at which the input signal is sampled. This rms time jitter produces a corresponding rms voltage error which is proportional to the slew rate of the input signal. The effect of broadband time jitter is to degrade the overall SNR of the ADC.

Aperture jitter for an ADC is usually attributed to the SHA. The ADC aperture jitter, unfortunately, is certainly not the only possible source for this error. In a practical ADC, the sampling clock is often phase and amplitude modulated by some unwanted external sources; the sources can be wideband random noise, oscillator phase noise, power line noise, or digital noise due to poor layout, bypassing, and grounding techniques. Phase jitter on the input sinewave produces the same effect as jitter on the sampling clock.

The effects of even small amounts of timing jitter are shown in Figure 13.37, where SNR and ENOB are plotted as a function of fullscale input sinewave frequency for various amounts of rms timing jitter using the above formula. For example, in order to achieve 12 bit SNR (74dB) on a 10MHz fullscale input sinewave, the rms jitter can be no more than 3ps rms.

EFFECTS OF APERTURE JITTER ON SNR AND ENOB

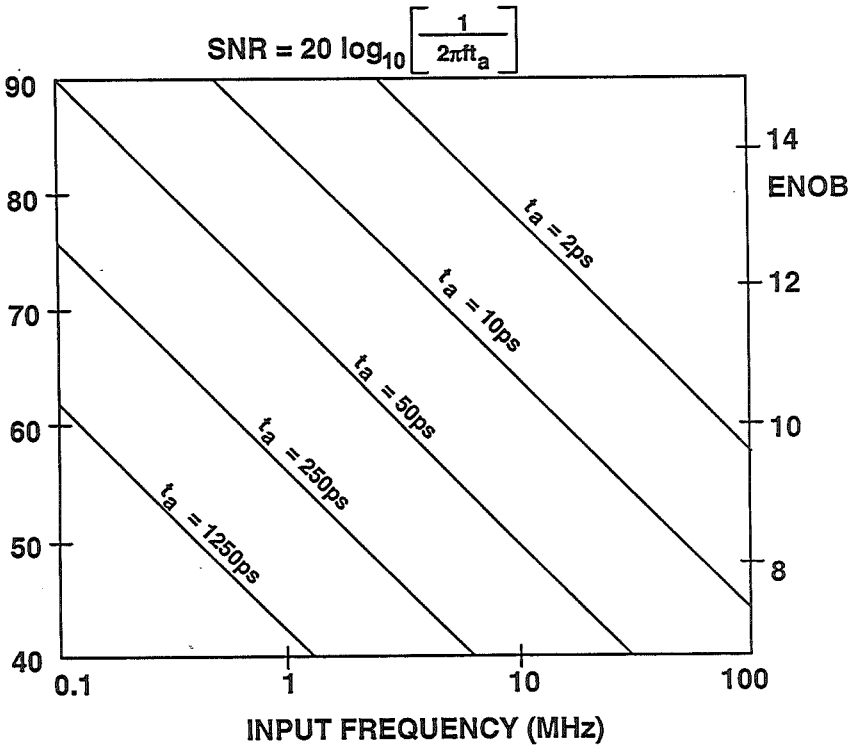


Figure 13.37

The total rms timing jitter will probably consist of two frequency components: narrowband and broadband. The sampling clock oscillator will probably have narrowband phase noise. The effect of narrow-band phase noise centered about the sampling frequency is to produce similar phase noise about the fundamental sinusoid frequency in an FFT of the digitized sinusoid. The high-speed logic circuits in the sampling clock path may introduce broadband noise on the pulse edges which in turn causes broadband jitter due to sample-to-sample variations in the precise times at which the internal logic thresholds are crossed. ECL logic gates have an effective bandwidth greater than 300MHz, and a typical 100K ECL gate has an effective rms timing jitter of approximately 7ps rms.

A detailed mathematical analysis of broadband and narrowband timing jitter is much beyond the scope of this discussion, however their effects may be observed directly in the FFT analysis of a sinusoid. The narrowband phase noise will show up as a widening of the main lobe of the fundamental sinusoid, while the broadband jitter will cause an overall increase in the noise floor.

The sampling clock generator must have low phase noise, therefore RC and relaxation oscillators should be ruled out completely. A crystal oscillator is much preferred. The crystal oscillator should not be constructed out of logic gates, capacitors, and resistors, however, but should be built around discrete bipolar and FET devices in the circuits recommended by the crystal

manufacturer. The crystal oscillator output put should then be filtered as shown in Figure 13.38. The bandpass filter following the crystal oscillator serves to remove any frequency skirts around the sampling frequency. The lowpass filter then removes any harmonics of the sampling clock frequency which may not have adequately been attenuated by the bandpass filter. The pure sinewave output then drives a low-jitter wideband comparator which converts the sinewave into a digital signal. Use a TTL comparator such as the AD9696 if the ADC requires TTL inputs, or an ECL comparator such as the AD96685 if ECL inputs are required.

The sampling clock circuits themselves should be isolated as much as possible from the noise present in the digital portions of the system. Separate decoupled power supplies may also be required for optimum results. It is extremely important that the digital outputs of the ADC not be allowed to couple into the sampling clock signal. Coupling will cause an increase in the harmonic distortion of ADC due to signal-dependent digital transients coupling into the sampling clock. On the other hand, the sampling clock is itself a digital signal. It has the potential for causing noise in the analog portion of the system. It should therefore be isolated from both the analog and digital portions of the system. As we will see in the next section, the sampling clock generator circuits should be referenced and decoupled to the analog ground plane.

GENERATING PRECISION LOW-JITTER ADC SAMPLING CLOCKS

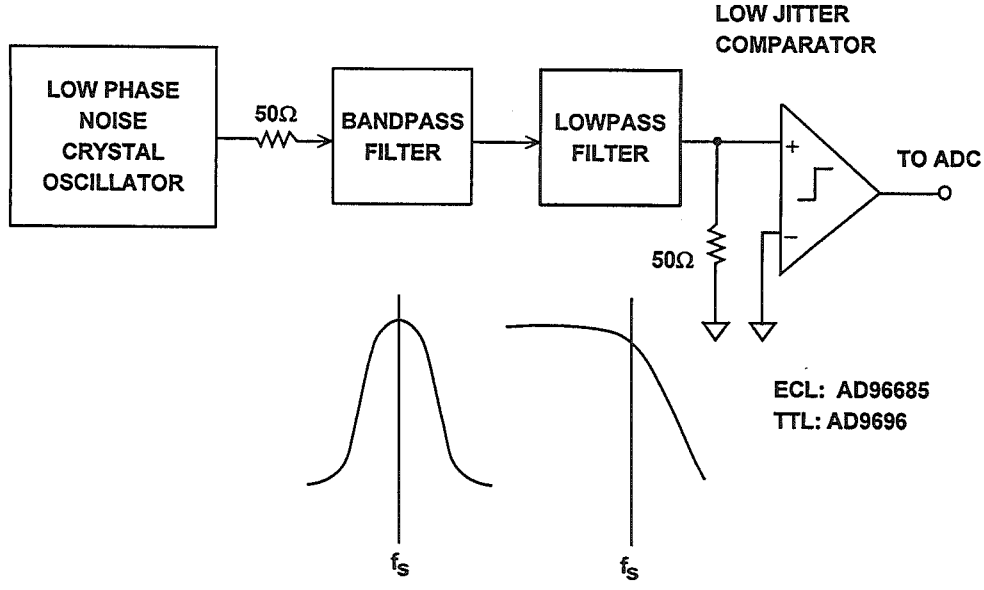


Figure 13.38

POWER SUPPLIES, GROUND PLANES, DECOUPLING, AND LAYOUT

The switching-mode power supply offers low cost, small size, high efficiency, high reliability and the possibility of operating from a wide range of input voltages without adjustment. Unfortunately, these supplies produce noise over a broad band of frequencies, and this noise occurs as conducted noise, radiated noise, and unwanted electric and magnetic fields. When used to supply logic circuits, even more noise is generated on the power supply bus. The noise transients on the output lines of switching supplies are short-duration voltage spikes. Although the actual switching frequencies may range from 10 to 100kHz, these spikes can contain frequency components that extend into the hundreds of megahertz.

Because of the wide variations in the noise characteristics of commercially available switching supplies, they should always be purchased in accordance with a specification-control drawing. Although specifying switching supplies in terms of rms noise is common practice, you should also specify the peak amplitudes of the switching spikes under the output loading conditions you expect in your system. You should also insist that the switching-supply manufacturer inform you of any internal supply design changes that may alter the spike amplitudes, duration, or switching frequency. These changes may require corresponding changes in the external power-supply filtering networks.

SWITCHING-MODE POWER SUPPLIES

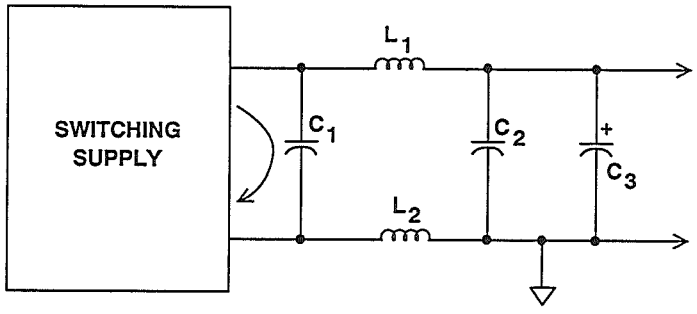
- Generate Conducted and Radiated Noise as Well as Electric and Magnetic Fields (HF and LF)
- Outputs Must be Adequately Filtered if Powering Sensitive Analog Circuits
- Optimum Filter Design Depends on Power Supply Characteristics. Beware of Power Supply Design Changes.
- Use Faraday Shields to Reduce HF Electric and HF Magnetic Fields
- Physically Isolate Supply from Analog Circuits
- Temporarily Replace Switching Supply with Low-Noise Linear Supply or Battery when Suspicious of Switching Supply Noise

Figure 13.39

Filtering switching supply outputs that provide several amps and generate voltage spikes having high frequency components is a challenge. For this reason, you should place the initial filtering burden on the switching supply manufacturer. Even so, external filtering such as shown in Figure 13.40 should be added. The series inductors isolate both the output and common lines from the external circuits. Because the load currents may be large, make sure that the inductors selected do not saturate. Split-core inductors or large ferrite beads make a good choice. Because the switching power supplies generate high and low frequency electric and magnetic fields, they should be physically separated as far as possible from critical analog circuitry. This is especially important in preventing the inductive coupling of low frequency magnetic fields.

Proper power supply decoupling techniques must be used on each PC board in the system. Figure 13.41 shows an arrangement which will ensure minimum problems. The power supply input (usually brought into the PC board on multiple pins) is first decoupled to the large-area low-impedance ground plane with a good quality, low ESL, ESR tantalum electrolytic capacitor. This capacitor bypasses low frequency noise to the ground plane. The ferrite bead reduces high frequency noise to the rest of the circuit. You should then place one low-inductance ceramic capacitor at each power pin on each IC. Ideally, you should use surface-mount chip capacitors for minimum inductance, but if you use leaded ceramics, be sure to minimize the lead lengths by mounting them flush on the PC board. Some ICs may require an additional small tantalum electrolytic capacitor (usually between 1 and 5μF). The data sheets for each IC should provide appropriate recommendations, but when in doubt, put them in!

FILTERING A SWITCHING SUPPLY OUTPUT



- C_1 MUST HAVE LOW INDUCTANCE AND BE CLOSE TO THE SUPPLY TO MINIMIZE HF CURRENT LOOPS AND RESULTANT HF MAGNETIC FIELDS
- C_2 IS ALSO LOW INDUCTANCE, C_3 IS ELECTROLYTIC
- IF THE SWITCHING SUPPLY IS INTERNALLY GROUNDED, L_2 SHOULD BE OMITTED

Figure 13.40

PROPER POWER SUPPLY DECOUPLING AT EACH IC ON THE PC BOARD IS CRITICAL TO ACHIEVING GOOD HIGH SPEED SYSTEM PERFORMANCE

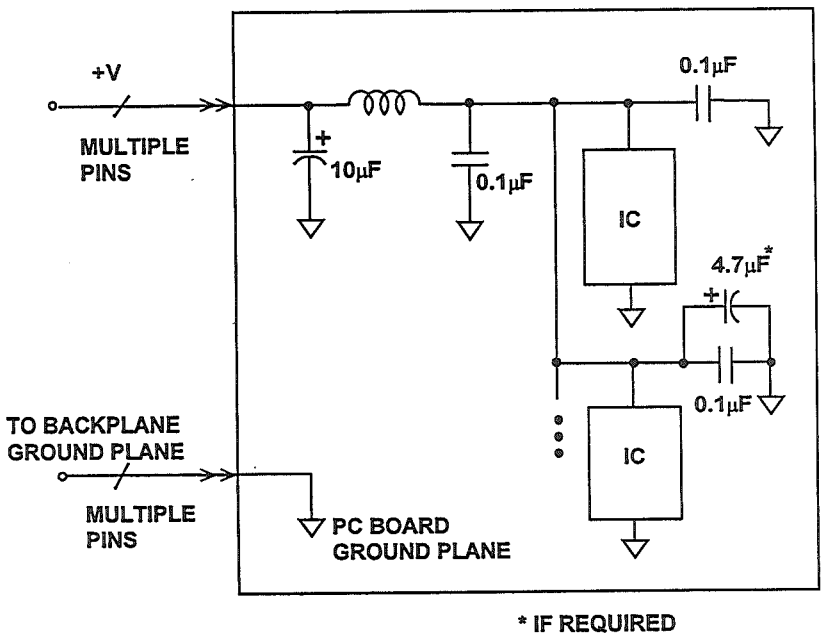


Figure 13.41

If a double-sided PC board is used, one side should be dedicated entirely (at least 75% of the total area) to the ground plane. The ICs are mounted on this side, and connections are made on the opposite side. Because of component interconnections, however, a few breaks in the ground plane are usually unavoidable. As more and more of the ground plane is eaten away for interconnections, its effectiveness diminishes. It is therefore recommended that multilayer PC boards be used where component packing density is high. Dedicate at least one entire layer to the ground plane.

When connecting to the backplane, use a number of pins (30 to 40%) on each PC board connector for ground. This will ensure that the low impedance ground plane is maintained between the various PC boards in a multicard system.

In practically all high speed systems, it is highly desirable to physically separate sensitive analog components from noisy digital components. It is usually a good idea to also establish separate analog and digital ground planes on each PC board as shown in Figure 13.42. The separate analog and digital ground planes are continued on the backplane using either motherboard ground planes or "ground screens" which are made up of a series of wired interconnections between the connector ground pins. The ground planes are joined together at the system *star ground* , or *single-point ground*, usually located at the common return point for the power supplies. The Schottky diodes are inserted to prevent significant accidental dc voltages from developing between the two ground systems.

SEPARATING ANALOG AND DIGITAL GROUNDS IN A MULTICARD, STAR GROUND SYSTEM

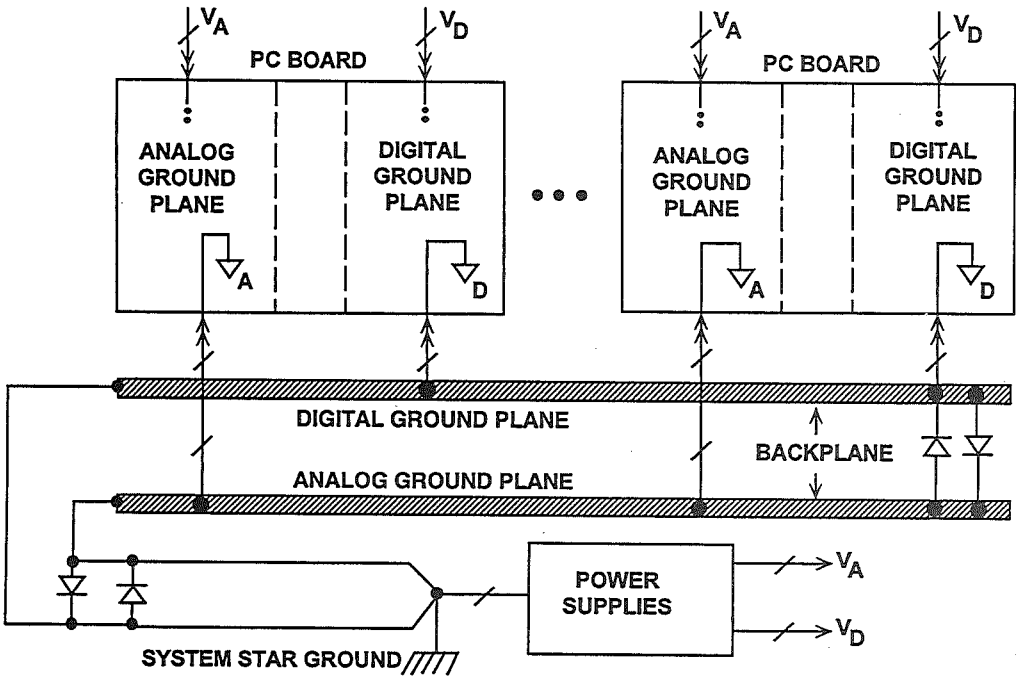


Figure 13.42

PROPER GROUNDING OF ADCs, DACs, AND MIXED SIGNAL ICs

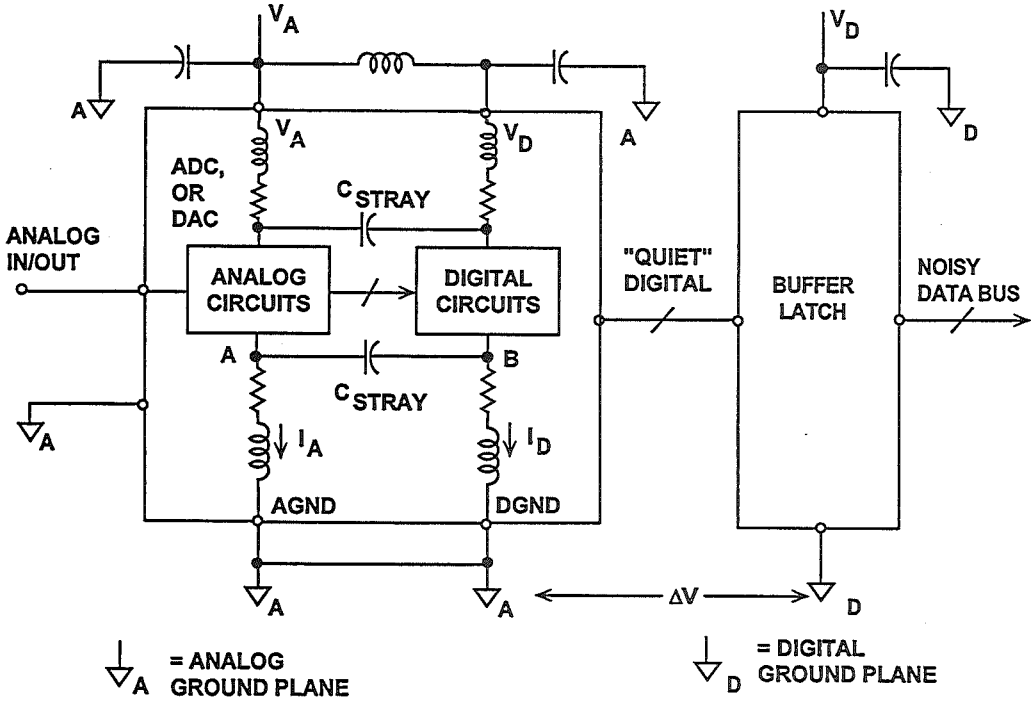


Figure 13.43

Sensitive analog components such as amplifiers and voltage references are referenced and decoupled to the analog ground plane. *The ADCs and DACs (and even some mixed-signal ICs) should be treated as analog circuits and also grounded and decoupled to the analog ground plane.* At first glance, this may seem somewhat contradictory, since a converter has an analog and digital interface and usually pins designated as analog ground (AGND) and digital ground (DGND). The diagram shown in Figure 13.43 will help to explain this seeming dilemma.

Inside an IC that has both analog and digital circuits, such as an ADC or a DAC, the grounds are usually kept separate to avoid coupling digital signals into the analog circuits. Figure 13.43 shows a simple model of a converter. There is nothing the IC designer can do about the wirebond inductance and resistance associated with connecting the pads on the chip to the package pins except to realize it's there. the rapidly changing digital currents produce a voltage at point B which will inevitably couple into point A of the analog circuits through the stray capacitance, C_{STRAY}. In addition, there is approximately 0.2pF unavoidable stray capacitance between every pin of the IC package! It's the IC designer's job to make the chip work in spite of this. However, in order to prevent further coupling, the AGND and DGND pins should be joined together externally to the *analog* ground plane with minimum lead lengths. Any extra impedance in the DGND connection will cause more digital noise to be developed at point B; it will, in turn, couple more digital noise into the analog circuit through the stray capacitance.

It is true that this arrangement will inject a small amount of digital noise on the analog ground plane. These currents should be quite small, and can be minimized by ensuring that the converter input/or output does not drive a large fanout. Minimizing the fanout on the converter's digital port will also keep the converter logic level transitions relatively free from ringing, and thereby minimize any potential coupling into the analog port of the converter. The logic supply pin (V_D) can be further isolated from the analog supply by the insertion of a small ferrite bead as shown in Figure 13.43. The internal digital currents of the converter will return to ground through the V_D pin decoupling capacitor (mounted as close to the converter as possible) and will not appear in the external ground circuit. It is always a good idea (as shown in Figure 13.43) to place a buffer latch adjacent to the converter to isolate the converter's digital lines from any noise which may be on the data bus. Even though a few high speed converters have three-state outputs/inputs, this isolation latch represents good design practice.

The buffer latch and other digital circuits should be grounded and decoupled to the digital ground plane of the PC board. Notice that any noise between the analog and digital ground plane reduces the noise margin at the converter digital interface. Since digital noise immunity is of the orders of hundreds or thousands of millivolts, this is unlikely to matter.

POWER SUPPLY, GROUNDING, AND DECOUPLING POINTS

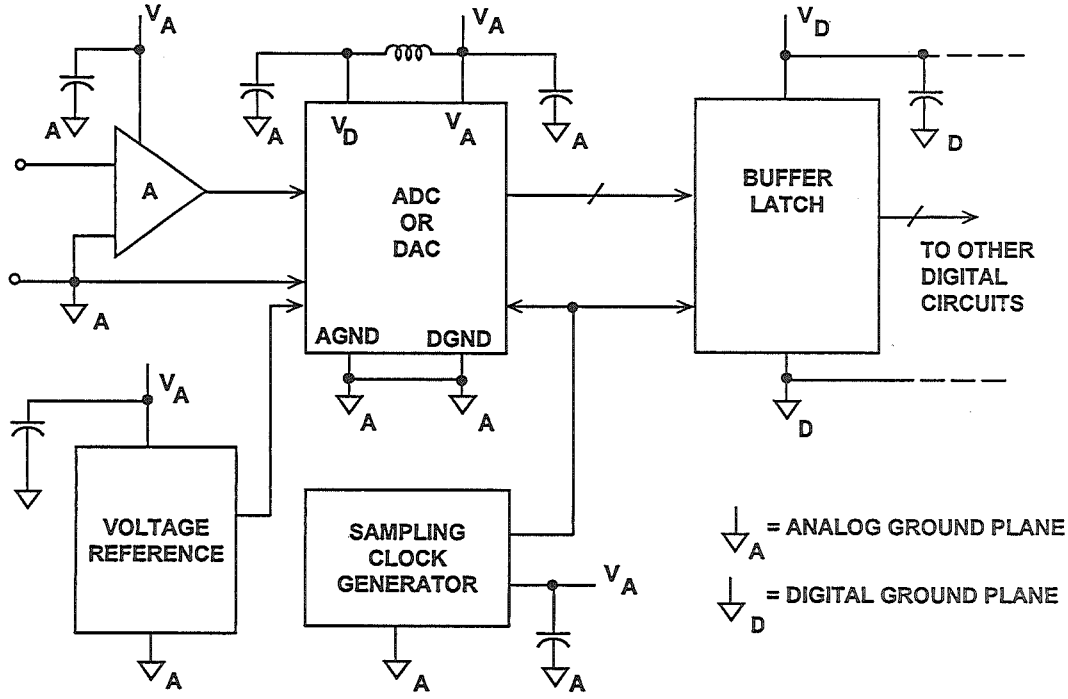


Figure 13.44

The sampling clock generation circuitry should also be grounded and heavily-decoupled to the analog ground plane. As previously discussed, phase noise on the sampling clock produces aperture jitter and a corresponding degradation in system SNR.

Separate power supplies for analog and digital circuits are also highly desirable. The analog supply should be used to power the converter. If the converter has a pin designated as a digital supply pin (V_D), it should either be powered from a separate analog supply, or filtered as shown in the diagram. All converter power pins should be decoupled to the analog ground plane, and all logic circuit power pins should be decoupled to the digital ground plane. If the digital power supply is relatively quiet, it may be possible to use it to supply analog circuits as well, but be very cautious.

A clean, analog-grade supply can be generated from a 5V logic supply using a differential LC filter with separate power supply and return lines as shown in Figure 13.45. The supply output is virtually free of any glitch noise as evident in the scope photo shown in Figure 13.46, which compares the input and output sides of the filter. All capacitors were selected from commonly available types. Lower noise can be attained using low ESR (Equivalent Series Resistance) type electrolytic and tantalum capacitors. The circuit as shown can handle 100mA of load current without the risk of saturating the ferrite core. Higher current capacity can be achieved using larger ferrite cores.

DIFFERENTIAL LC FILTER TURNS NOISY LOGIC SUPPLIES INTO NOISE-FREE ANALOG SUPPLIES

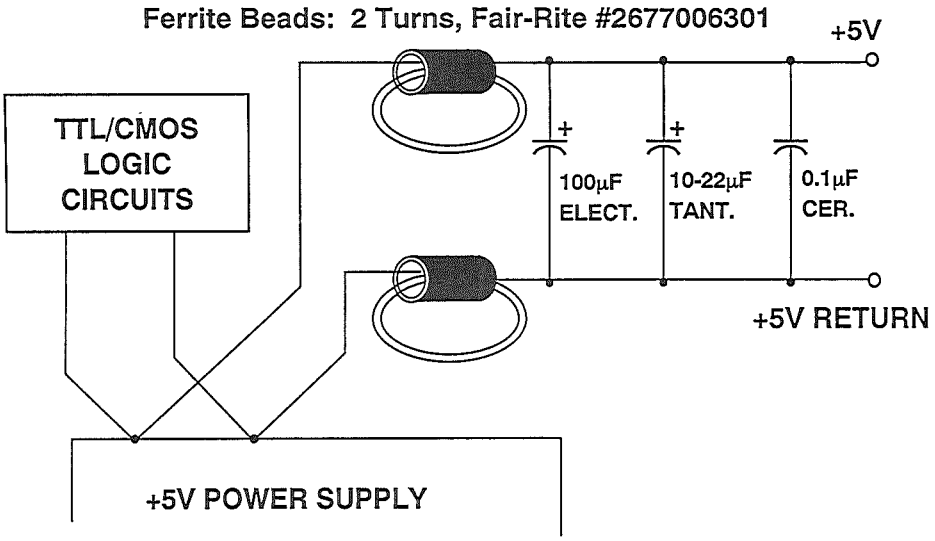
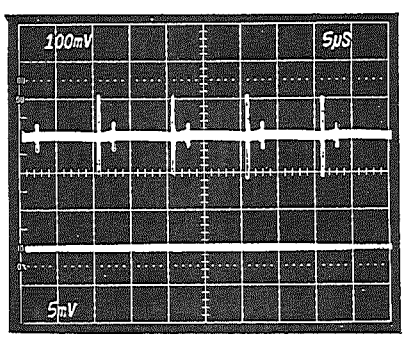


Figure 13.45

LC FILTER VIRTUALLY ELIMINATES ALL GLITCH NOISE

BEFORE FILTER

AFTER FILTER



100mV / div.

5mV / div.

HORIZONTAL SCALE: 5µs / div.

Figure 13.46

It is evident that we can minimize noise by paying attention to the system layout and preventing different signals from interfering with each other. High level analog signals should be separated from low level analog signals, and both should be kept away from digital signals. We have seen elsewhere that in waveform sampling and reconstruction systems the sampling clock (which is a digital signal) is as vulnerable to noise as any analog signal, but is as liable to cause noise as any digital signal, and so must be kept isolated from both analog and digital systems.

If a ground plane is used, as it should in be most cases, it can act as a shield where sensitive signals cross. Figure 13.48 shows a good layout for a data acquisition system where all sensitive areas are isolated from each other and signal paths are kept as short as possible. While real life is rarely as tidy as this the principle remains a valid one.

There are a number of important points to be considered when making signal and power connections. First of all a connector is one of the few places in the system where all signal conductors must run parallel - it is therefore a good idea to separate them with ground pins (creating a faraday shield) to reduce coupling between them.

SIGNAL ROUTING IN MIXED SIGNAL SYSTEMS

- Physically separate analog and digital signals.
- Avoid crossovers between analog and digital signals.
- Be careful with sampling clock and ADC/DAC analog runs.
- Use lots of ground plane.
- Use microstrip techniques at high frequencies for controlled impedances.
- Use surface mount components in high frequency systems to minimize parasitic capacitance and inductance.

Figure 13.47

A PC BOARD LAYOUT SHOWING GOOD SIGNAL ROUTING

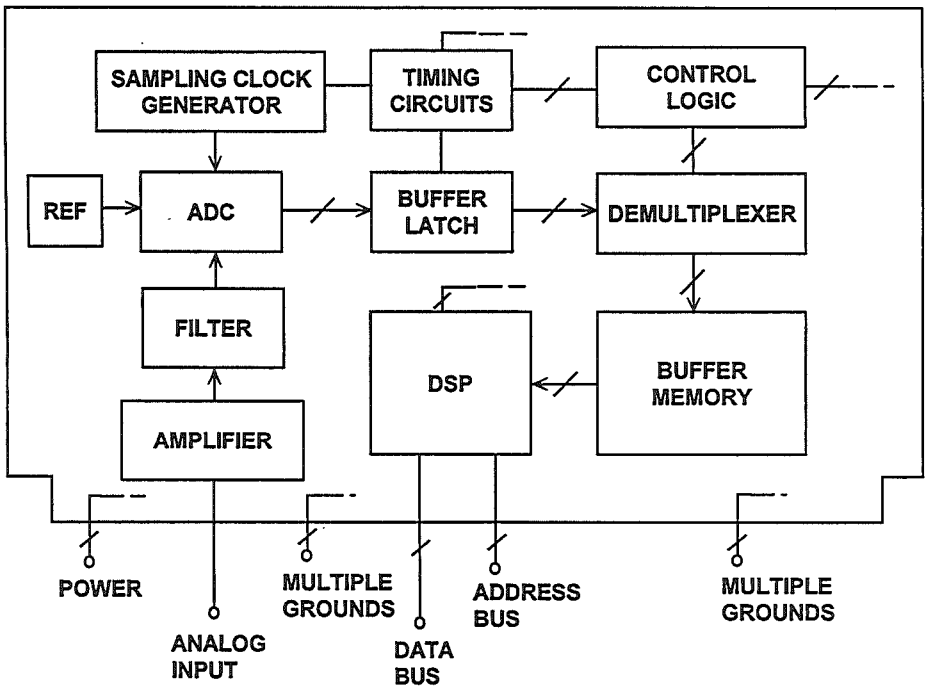


Figure 13.48

13

EDGE CONNECTIONS

- Separate sensitive signal by ground pins.
- Keep down ground impedances with multiple (30-40% of total) ground pins.
- Have several pins for each power line.
- Critical signals such as analog or sampling clocks may require a separate connector (possibly coax), or microstrip techniques.

Figure 13.49

Multiple ground pins are important for another reason: they keep down the ground impedance at the junction between the board and the backplane. The contact resistance of a single pin of a PCB connector is quite low (of the order of 10 mOhms) when the board is new - as the board gets older the contact resistance is likely to rise, and the board's performance may be compromised. It is therefore well worthwhile to afford extra PCB connector pins so that there are many ground connections (perhaps 30-40% of all the pins on the PCB connector should be ground pins). For similar reasons there should be several pins for each power connection, although there is no need to have as many as there are ground pins.

SOCKETS

It is tempting to mount expensive ICs in sockets rather than soldering them in circuit - especially during circuit development. Engineers would do well not to succumb to this temptation.

USE OF SOCKETS WITH HIGH PERFORMANCE ANALOG CIRCUITS

- DON'T! (If at all possible)
- Use "Pin sockets" or "Cage jacks" such as Amp Part No: 5-330808-3 or 5-330808-6 (Capped & uncapped respectively).
- Always test the effect of sockets by comparing system performance with and without the use of sockets.
- Do not change the type of socket or manufacturer used without evaluating the effects of the change on performance.

Figure 13.50

Sockets add resistance, inductance and capacitance to the circuit and may degrade performance to quite unacceptable levels. When this occurs, though, it is always the IC manufacturer who is blamed - not the use of a socket. Even low profile, low insertion force sockets cannot be relied upon to ensure the performance of high performance (high speed or high precision or, worst of all, both) devices. As the socket ages and the board suffers vibration, the contact resistance of low insertion force sockets is very likely to rise. Where a socket must be used the best performance is achieved by using individual pin sockets (sometimes called "cage jacks") to make up a multi-pin socket in the PCB itself.

It really is best not to use IC sockets with high performance analog and mixed signal circuits. If their use can be avoided it should be. However at medium speeds and medium resolutions the trade-off between performance and convenience may fall on the side of convenience. It is very important, when sockets are used, to evaluate circuit performance with and without the socket chosen to ensure that the type of socket chosen really does have minimal effect on the way that the circuit behaves. The effects of a change of socket on the circuit should be evaluated as carefully as a change of IC would be and the drawings should be prepared so that the change procedures for a socket are as rigorous as for an IC - in order to prevent a purchase clerk who knows nothing of electronics from devastating the system performance in order to save five cents on a socket.

PROTOTYPING HIGH PERFORMANCE ANALOG CIRCUITRY

As we have seen, circuit board layout is part of the circuit design of all high performance analog circuits. Prototyping techniques derived from the "node" theory, while ideal for logic breadboarding at low and medium speeds, are quite unsuitable for any analog circuits, or even for very fast digital ones. Vector board and wire wrap prototyping will tell an engineer nothing about the behavior of a properly laid out version of the analog circuit.

The best technique for analog prototyping is to use a prototype of the final PCB - certainly no design is complete until the final PCB layout has been proved to give the required performance. This approach may be a little limiting where a number of different possibilities are to be evaluated, or for a multicard system.

In this case components should be mounted on a board having a continuous copper ground plane (ideally on both sides of the board, though while convenient, this is not essential), with ground connections made to the plane and short point to point wiring made above and below it. The overall component placing and signal routing should be as close as possible to the planned final layout.

As we have already indicated, IC sockets can degrade the performance of analog ICs. While directly soldered components are ideal for prototyping, an IC socket made of pin sockets mounted in the ground plane board may be acceptable (clear the copper, on both sides of the board, for about 0.5 mm around each ungrounded pin socket - solder the grounded ones to ground on both sides of the board).

PROTOTYPING MIXED SIGNAL CIRCUITRY

- NEVER use vector boards or wire-wrap for the analog parts of the system (they can be invaluable for data buses and address lines in the digital part).
- Wherever possible avoid the use of sockets for analog ICs.
- Use a prototype of your final PCB layout as early as possible.

Figure 13.51

Allowing wiring to float in the air can be a little tricky. There is a breadboarding system which is conceptually very similar to that described above but which provides adhesive PC pads which stick to the ground plane and allow more rigid component mounting and wiring. This system is manufactured by Wainwright Instruments and is known as "Minimount" in Europe and "Solder Mounts" in the USA. The manufacturer's and distributors' addresses are given in Reference 1 at the end of this section.

Manufacturer's evaluation boards are also useful in system prototyping since they have already been optimized for best performance. Analog Devices offers many evaluation boards for a wide array of products. They offer the designer an excellent starting point for the layout.

When the prototype layout is transferred to a CAD system for PCB layout it is important to disable, or at any rate override where necessary, any automatic routing or component placing software. The criteria used by such software are more closely related to "node" theory and aesthetically pleasing rows of components (which, admittedly, are also easier on automatic component placing machinery) than to optimizing stray inductance and capacitance and minimizing common ground impedances.

ADDITIONAL PROTOTYPING HINTS

- Pay *equal* attention to signal routing, component placing and supply decoupling in *both* the prototype and the final design.
- Verify performance as well as functionality at each stage of the design.
- For "freehand" prototyping use a copper-clad board, mount components to it by their ground pins and wire the remaining connections point-to-point (use Wainwright Instruments' Minimount/Solder Mount adhesive PC pads if aerial point-to-point wiring seems too fraught with peril).

Figure 13.52

REFERENCES

1. Wainwright Instruments, Inc., 7770 Regents Rd., #113, Suite 371, San Diego, CA 92122, Tel. 619-558-1057. Wainwright Instruments GmbH, Widdersberger Strasse 14, DW-8138 Andechs-Frieding, Germany. Tel: +49-8152-2245, Fax: +49-8152-5174.

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