SECTION 11

VIDEO SIGNAL TRANSMISSION AND PROCESSING

- DRIVING CAPACITIVE LOADS WITH WIDEBAND OP AMPS:
  OUT-OF-LOOP RESISTIVE COMPENSATION FOR DRIVING CAPACITIVE LOADS, IN-THE-LOOP RESISTIVE COMPENSATION FOR DRIVING CAPACITIVE LOADS, USING OP AMPS WITH INTERNAL CAPACITIVE-LOAD COMPENSATION

- CABLE DRIVING AT VIDEO FREQUENCIES

- VIDEO SIGNAL PROCESSING:
  DIFFERENTIAL GAIN AND PHASE SPECIFICATIONS, VIDEO LINE DRIVERS, HIGH SPEED DIFFERENTIAL SIGNAL TRANSMISSION, VIDEO LINE RECEIVERS USING THE AD830 ACTIVE FEEDBACK AMPLIFIER TOPOLOGY, A COMPOSITE VIDEO SYNC TIP DC RESTORER, A VIDEO SYNC STRIPPER CIRCUIT

- MAINTAINING TRANSMISSION LINE IMPEDANCES ON THE PC BOARD

SECTION 11

VIDEO SIGNAL TRANSMISSION AND PROCESSING

Walt Kester, Walt Jung, Dave Whitney

Transmission of high speed analog signals over any distance is difficult for a number of reasons. Even a few pF of stray capacitance on the output of a high speed op amp may cause ringing and perhaps instability. For example, the capacitance of a 10 mil wide PC board trace over a ground plane (G-10 epoxy board, 60mils thick) is approximately 1.3pF/inch. Ground noise between ground planes on different PC boards makes uncorrupted transmission of single-ended signals between them difficult. This section is divided into three major areas: driving capacitive loads, driving coaxial cables, and differential signal transmission techniques.

DRIVING CAPACITIVE LOADS WITH WIDEBAND OP AMPS

Walt Jung, Walt Kester

Capacitive loading should be looked at in any driver-circuit application, however benign. Signal lead capacitance can build up quickly, even for short runs on a single PC board, and can cause high speed op amps to oscillate.

A follower-connected op amp with capacitive load is the classic case of a potential stability disaster (see Figure 11.1). For example, if the op amp has an open-loop phase shift of 135° (corresponding to a phase margin of 45°) near its unity-gain frequency, and if the pole formed by the output impedance of the op amp and the load capacitance produces an additional phase shift of 45°, severe peaking or even oscillation will result. The follower connection tends to maximize this tendency, because it involves 100% feedback.

CAPACITIVE LOADING ON OP AMP GENERALLY REDUCES PHASE MARGIN AND MAY CAUSE INSTABILITY, BUT INCREASING THE NOISE GAIN OF THE CIRCUIT IMPROVES STABILITY

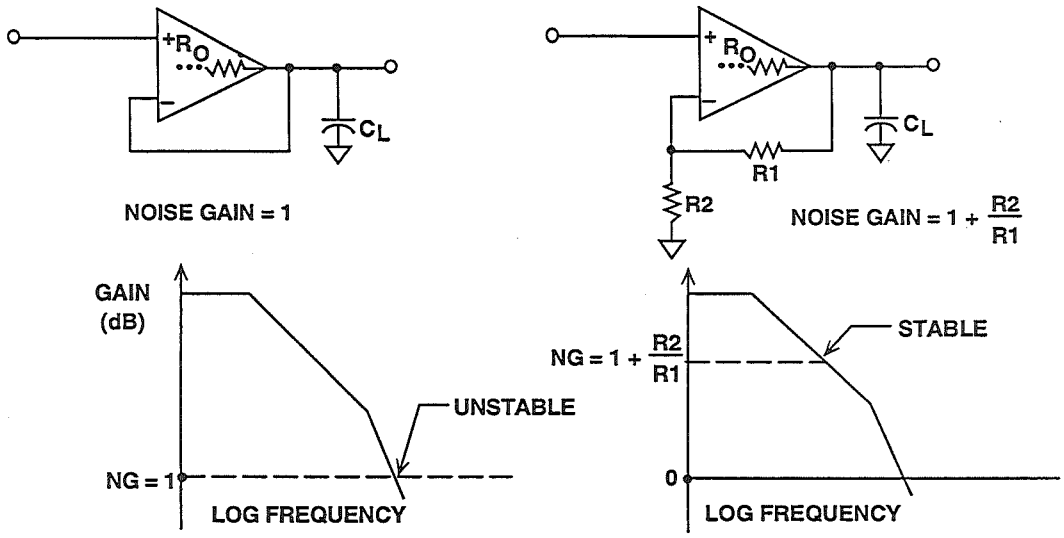


Figure 11.1

Operating at higher noise gains (reduced feedback) will also help stability of a standard voltage feedback op amp, following general feedback theory, because phase lag in generally lower at the lower unity-loop-gain frequencies. Therefore, inverters or higher-gain followers (with attenuated inputs, if necessary) will have less tendency to oscillate or peak.

Current feedback op amps, on the other hand, are generally optimized to operate with a fixed value of feedback resistor. The closed-loop bandwidth is relatively constant regardless of the value of closed-loop gain provided this feedback resistor remains unchanged. The bandwidth can be reduced, however, by increasing the value of the feedback resistor, which decreases the sensitivity to capacitive loading.

OUT-OF-LOOP RESISTIVE COMPENSATION FOR DRIVING CAPACITIVE LOADS

Walt Jung

Another method for compensating for capacitive loading is to isolate the amplifier output from the capacitive load, using a series resistor which is outside the feedback loop as shown in Figure 11.2.

OPEN-LOOP SERIES RESISTANCE ISOLATES CAPACITIVE LOAD FOR THE AD845 VOLTAGE FEEDBACK OP AMP (CIRCUIT BANDWIDTH = 3.5MHz)

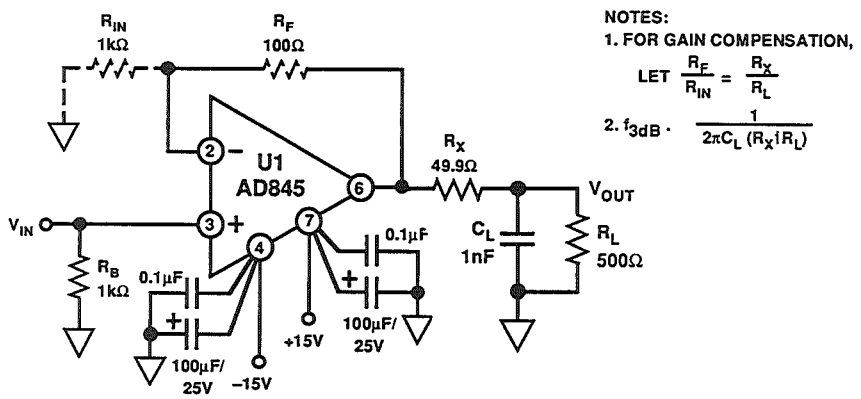


Figure 11.2

CABLE CAPACITANCE

- All Interconnections are Really Transmission Lines Which Have a Characteristic Impedance (Even if Not Controlled)
- The Characteristic Impedance is Equal to $\sqrt{L/C}$, where L and C are the Distributed Inductance and Capacitance
- Correctly Terminated Transmission Lines Have Impedances Equal to Their Characteristic Impedance
- Unterminated Transmission Lines Behave Approximately as Lumped Capacitance at Frequencies << $1/t_p$, where t_p = Propagation Delay of Cable

Figure 11.3

The load on the amplifier looks like a resistance, R_X, at frequencies above $1/(2\pi R_X C_L)$. Although it slightly reduces the amplifier's open-loop gain, it does not introduce additional loop phase lag, and the circuit's stability is less sensitive to C_L. However, the resistance, R_X, causes a voltage drop proportional to load current, and it must be small compared to R_L to minimize low frequency error. R_X is typically 10-100Ω, which, for loads ≥ 1kΩ, produces small (<1dB) dc errors.

For low impedance loads, such as 500Ω for R_L, a series resistance, R_X,) of 50Ω produces a 9% gain error, which often requires correction for unity overall gain, either locally or elsewhere in the system. It can be achieved locally by using feedback resistors in the same ratio, R_X/R_L; accuracy of the overall gain will depend on whether R_L is constant. If the circuit is already connected for gain, the required correction means revising resistance values for a $(1 + R_X/R_L)$ gain increase.

This technique (like almost all others to isolate capacitive loads) also causes a loss of frequency response, a loss likely to be serious with high speed amplifiers. For the example shown in Figure 11.2, the effective bandwidth will be about 3.5MHz, well below the basic 16MHz bandwidth of the AD845 op amp. In essence, the bandwidth will be limited to $1/[2\pi C_L(R_X \| R_L)]$.

In addition to reducing circuit bandwidth, the outside-the-loop series-R_X method can limit the slew rate. In general, the inherent slew rate of the amplifier will be reduced to $I_{O\ max}/C_L$. For example, while the AD845 has a basic slew rate of 100V/μs, the ±50mA

output-current limits cause the circuit slew rate to fall to about 50V/μs with C_L = 1nF. The slew rate is subject to the amplifier's short-circuit current limit, which usually varies inversely with temperature. This general limitation will apply to any capacitively loaded amplifier and is particularly acute in high slew rate devices.

Unlike voltage feedback op amps, current feedback (or transimpedance) op amps require an optimum value of R_F for flat frequency response and maximum bandwidth. For the AD811 at a gain of +1, it is 750Ω as shown in Figure 11.4. For other current feedback op amps, the optimum R_F value may be different. In all cases, the device data sheet should be consulted.

OPEN-LOOP SERIES RESISTANCE ISOLATES CAPACITIVE LOAD FOR AD811 CURRENT FEEDBACK OP AMP (CIRCUIT BANDWIDTH = 13.5MHz)

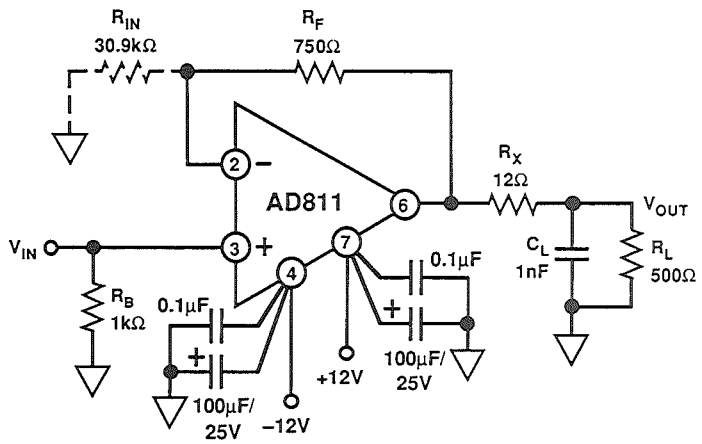


Figure 11.4

The AD811 op amp permits R_F to be increased to improve capacitive load handling for R_X = 0, but with less-flat frequency response. With R_X = 12Ω, as shown, response is optimized into a 1nF load. The AD811 has major benefits in this application, since the bandwidth is 13.5MHz compared to 3.5MHz for the AD845 circuit in Figure 11.2. The ±150mA short-circuit output drive of the AD811 increases the circuit's slew rate to 150V/μs (much less than its unloaded 2500V/μs spec, but much more than that of Figure 11.2. As in the previous example, R_{in} may be added to compensate for the gain loss due the divider action of R_X and R_L.

IN-THE-LOOP RESISTIVE COMPENSATION FOR DRIVING CAPACITIVE LOADS

Walt Jung

In-the-loop resistive compensation is the most flexible and accurate general way to isolate/compensate capacitive loads. It is flexible; in principle, it applies to any unity-gain stable op amp, in inverting or noninverting operation. It is accurate; the isolation resistor is included within a dc feedback loop for excellent low frequency gain accuracy, independent of the load and limited principally by the circuit's gain resistors (assuming adequate op amp gain). Unfortunately, like other techniques discussed thus far, it also reduces bandwidth and slew rate.

Figure 11.5 illustrates the principle. In this circuit, a noninverting gain-of-2 stage, resistor R_X isolates the capacitive load C_L. Unlike Figures 11.2 and 11.4, the feedback return is taken from the *load* side of R_X, enclosing it within the loop. This automatically corrects gain errors caused by loading at the lower frequencies. the gain expression is like that of a standard noninverting op amp stage.

Dynamically, capacitor C_F provides compensation for the additional lag introduces by the R_X-C_L combination. For a given set of values, C_F can be adjusted to cancel much of the destabilizing effect of C_L and provide a well-damped step response, countering the tendency towards overshoot, ringing, or oscillation. Bandwidth is reduced; the closed-loop bandwidth of this stage is a function of R_F and C_F, as well as R_X and C_L. While several references suggest procedures for predicting C_F (see References 3 and 7), a practical approach is to select a close nominal value for C_F, then adjust it for optimum pulse response in the final circuit layout (see Reference 8).

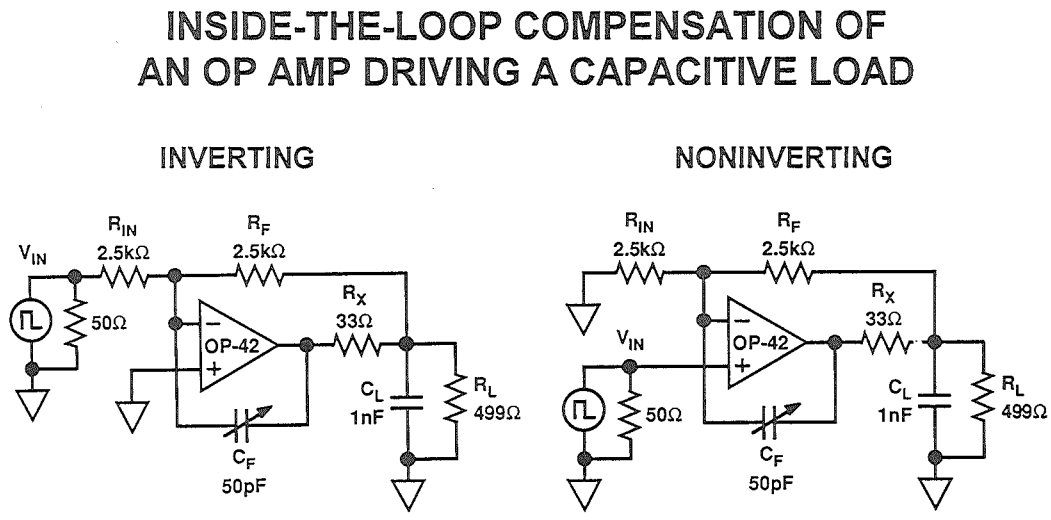


Figure 11.5

USING OP AMPS WITH INTERNAL CAPACITIVE-LOAD COMPENSATION

Walt Jung

Several Analog Devices' op amps have internal compensation for driving capacitive loads. Examples are the AD847, AD848, AD849, AD817, AD818, AD827, AD826, AD828, and the OP-160. The fundamental principle is the same and will be illustrated using the AD817 simplified schematic in Figure 11.6.

AD817 SIMPLIFIED SCHEMATIC ILLUSTRATES INTERNAL COMPENSATION FOR DRIVING CAPACITIVE LOADS

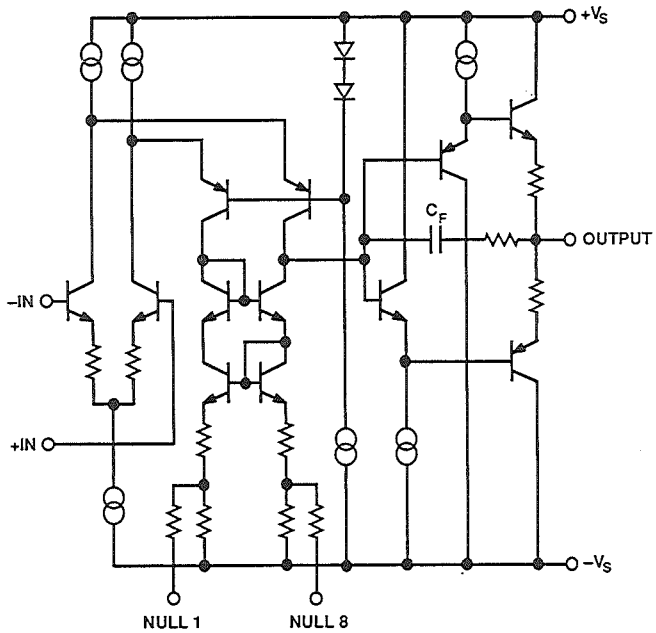
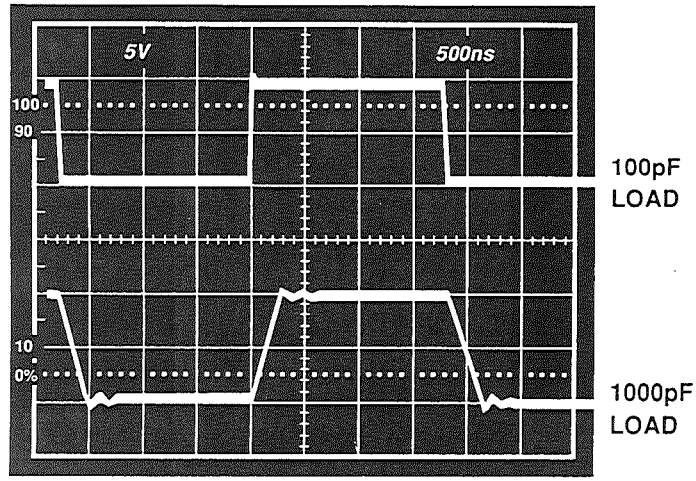


Figure 11.6

The AD817 consists of a degenerated NPN differential pair driving matched PNPs in a folded-cascode gain stage. The output buffer stage employs emitter followers in a class AB amplifier which delivers the necessary current to the load while maintaining low levels of distortion.

The capacitor, C_F, in the output stage mitigates the effect of capacitive loads. At low frequencies, and with low capacitive loads, the gain from the high-impedance compensation node to the output is very close to unity. In this case, C_F is bootstrapped and does not contribute to the overall compensation capacitance of the device. As the capacitive load is increased, a pole is formed with the output impedance of the output stage. This reduces the gain, and therefore, C_F is incompletely bootstrapped. Effectively, some fraction of C_F contributes to the overall compensation capacitance, reducing the unity gain bandwidth. As the load capacitance is further increased, the bandwidth continues to fall, maintaining stability of the amplifier. Figure 11.7 shows the AD817 pulse response for a 100pF load and a 1000pF load.

INTERNAL COMPENSATION MAKES THE AD817
STABLE WHEN DRIVING LARGE CAPACITVE LOADS



VERTICAL SCALE: 5V/div.
HORIZONTAL SCALE: 500ns/div.

Figure 11.7

Some caveats are also associated with internal compensation, however. As with passive compensation techniques, bandwidth decreases as the device slows down to prevent oscillation as load current flows. The compensation network has its greatest effect when enough output current flows to produce voltage across C_F. Conversely, at small signal levels the effect of the network on speed is much less, so greater ringing may actually be possible for some circuits for low-level signals. Because the circuit is based on a nonlinear principle, the internal network affects distortion and the ability to drive loads; this factor affects amplifier performance in video applications. Though it does not by any means make the AD847 or AD817 unusable for video, it does not permit the very lowest levels of distortion and differential gain and phase achieved by otherwise comparable amplifiers.

CABLE DRIVING AT VIDEO FREQUENCIES
Walt Kester

The capacitive-load compensation techniques described above are hardly a perfect solution to the line-driving problem. Perhaps the best and most foolproof way to drive a long line (which might otherwise present substantial capacitive load) is to use a transmission line. This has been the standard for signal distribution in video and RF systems for years. When properly driven and terminated, bandwidth limitations are greatly reduced.

A transmission line correctly terminated with pure resistance (no reactive component) does not look capacitive. It has a controlled distributed capacitance per foot (C) and a controlled distributed

inductance per foot (L). The characteristic impedance of the line is given by the equation $Z_0 = \sqrt{(L/C)}$. Coaxial cable is the most popular form of single-ended transmission line and comes in characteristic impedances of 50Ω, 75Ω, and 93Ω. Because of skin effect, it exhibits a loss which is a function of frequency as shown in Figure 11.8 for several popular coaxial cables (Reference 4). Skin effect also affects the pulse response of long coaxial cables. The response to a fast pulse will rise sharply for the first 50% of the output swing, then taper off during the remaining portion of the edge. Calculations show that the 10 to 90% waveform risetime is 30 times greater than the 0 to 50% risetime when the cable is skin effect limited (Reference 4).

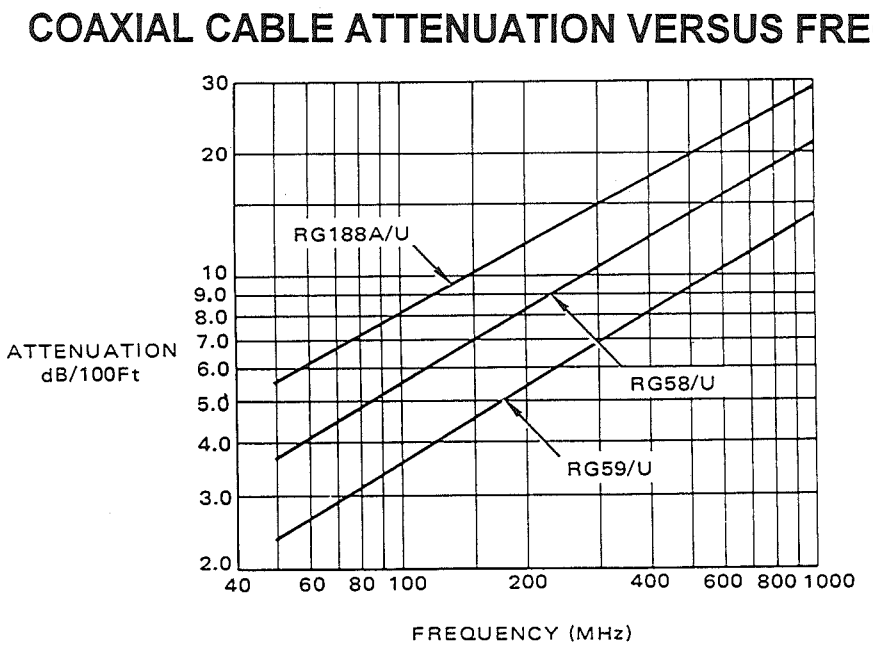


Figure 11.8

To illustrate the behavior of a high speed op amp driving a coaxial cable, consider the circuit of Figure 11.9. The AD9617 drives 4 feet of high-quality Belden 9223 50Ω cable which is terminated in the characteristic impedance of 50Ω. The pulse response is also shown on Figure 11.9. The output of the cable was measured by connecting the test fixture directly to the 50Ω input of a 400MHz Tektronix 2465B oscilloscope. The 50Ω resistor termination is actually the input of the scope. The 50Ω load is not a perfect termination (the scope input capacitance is about 2pF), so some of the pulse is reflected back to the source. When the reflection reaches the low impedance source, it is reflected out-of-phase back to the load. The delay of the cable is about 1.6ns/foot, and you can see this small reflection which occurs about 13ns after the leading and trailing edge of the pulse. This is equal to the round-trip delay of the cable. In the frequency domain, the cable mismatch will cause a loss of bandwidth flatness at the load.

PULSE RESPONSE OF AD9617 DRIVING 4 FEET OF LOAD-TERMINATED COAXIAL CABLE

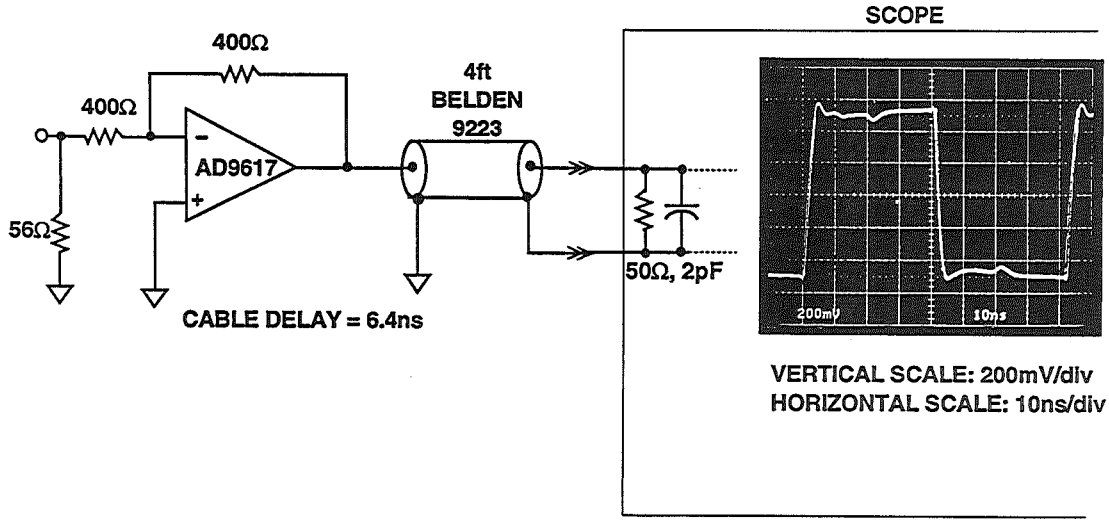


Figure 11.9

Figure 11.10 shows the coaxial cable with both a source and a load termination. This is the preferred way to drive a transmission line because the reflection from the load impedance mismatch is largely absorbed by the source termination resistor. The disadvantage is that there is a 2× gain reduction because of the voltage division between the source and load terminations. But source and load terminations in conjunction with a low-loss cable ensure the best bandwidth flatness.

Now, let us replace the 4feet of coaxial cable with an uncontrolled-impedance cable (one that is largely capacitive with little inductance). Let us use a capacitance of 120pF to simulate the cable (corresponding to the total capacitance of 4 feet of coaxial cable whose distributed capacitance is about 30pF/foot). Figure 11.11 shows the output of the AD9617 driving a lumped 120pF capacitor. Notice the overshoot and ringing on the pulse waveform due to the capacitive loading. This illustrates the need to use good quality controlled-impedance coaxial cable in the transmission of high frequency signals.

PULSE RESPONSE OF AD9617 DRIVING 4 FEET OF SOURCE AND LOAD-TERMINATED COAXIAL CABLE

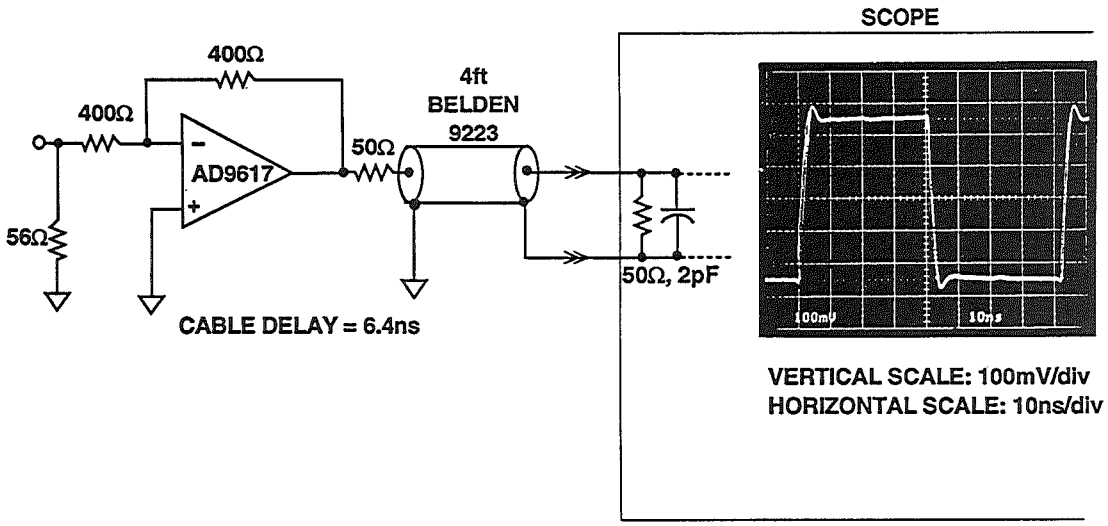


Figure 11.10

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PULSE RESPONSE OF AD9617 DRIVING 120pF ‖ 50Ω LOAD

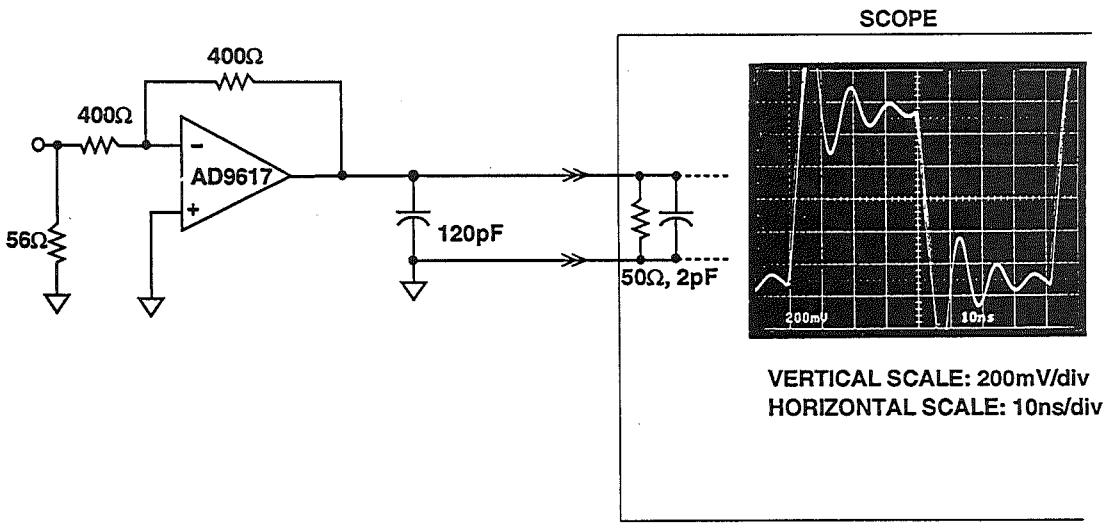

Figure 11.11

VIDEO SIGNAL PROCESSING

Walt Kester, Walt Jung, Dave Whitney

Before discussing a few professional video applications, we will review some basics regarding the video signal. The standard video format is the specification of how the video signal looks from an electrical point of view. Light strikes the surface of an image sensing device within the camera and produces a voltage level corresponding to the amount of light hitting a particular spatial region of the surface. This information is then placed into the standard format and sequenced out of the camera. Along with the actual light and color information, synchronization pulses are added to allow the receiving device - a television monitor, for instance - to identify where the sequence is in the frame data.

A standard video format image is read out on a line-by-line basis from left to right, top to bottom. A technique called *interlacing* refers to the reading of all even numbered lines, top to bottom, followed by all odd lines as shown in Figure 11.12.

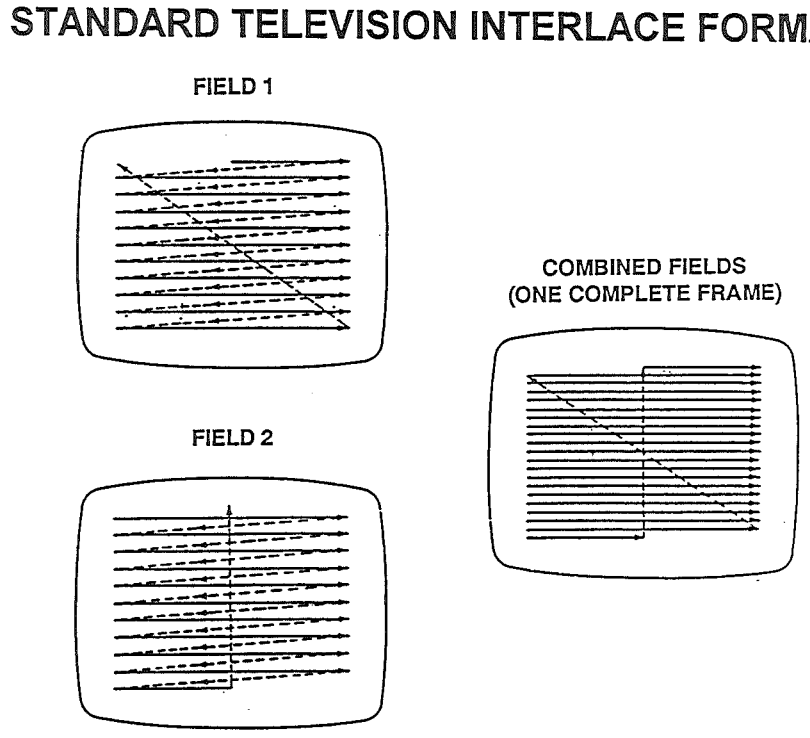

Figure 11.12

The television picture *frame* is thus divided into even and odd *fields*. Interlacing is used to produce an apparent update of the entire frame in half the time that a full update actually occurs. This results in a television image with less apparent flicker. Typical broadcast television frame update rates are 30 and 25 Hz, depending upon the line frequency.

The original black and white, or *monochrome*, television specification in the USA is the EIA RS-170 specification which prescribes all timing and voltage level requirements for standard commercial broadcast video signals. The standard American specification for color signals, NTSC, modifies RS-170 to work with color signals by adding color information to the signal which otherwise contains only brightness information.

A video signal comprises a series of analog television lines. Each line is separated from the next by a synchronization pulse called the *horizontal sync*. The fields of the picture are separated by a longer synchronization pulse called the *vertical sync*. In the case of a monitor receiving the signal, its electron beam scans the face of the display tube with the brightness of the beam controlled by the amplitude of the video signal. Whenever a horizontal sync pulse is detected, the beam is reset to the left side of the screen and moved down to the next line position. A vertical sync pulse, indicated by a horizontal sync pulse of longer duration, resets the beam to the top left point of the screen to a line centered between the first two lines of the previous scan. This allows the current field to be displayed between the previous one. A single line of an NTSC color video signal is shown in Figure 11.13, and the field timing diagram in Figure 11.14.

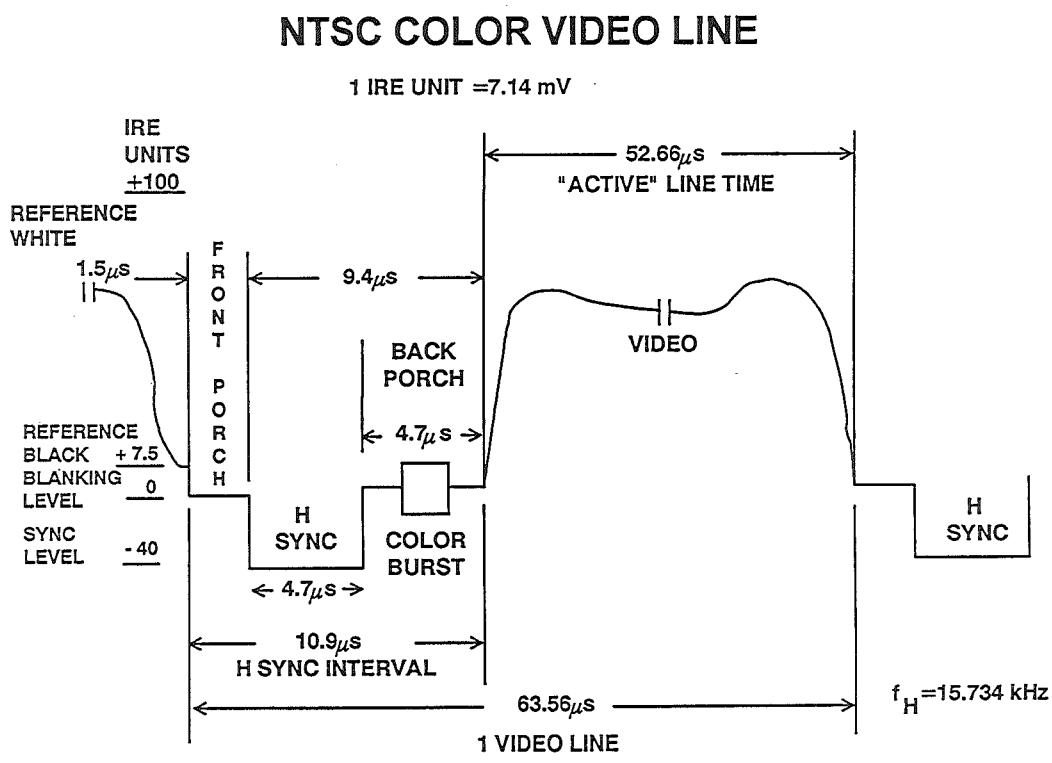

Figure 11.13

NTSC FIELD TIMING DIAGRAM

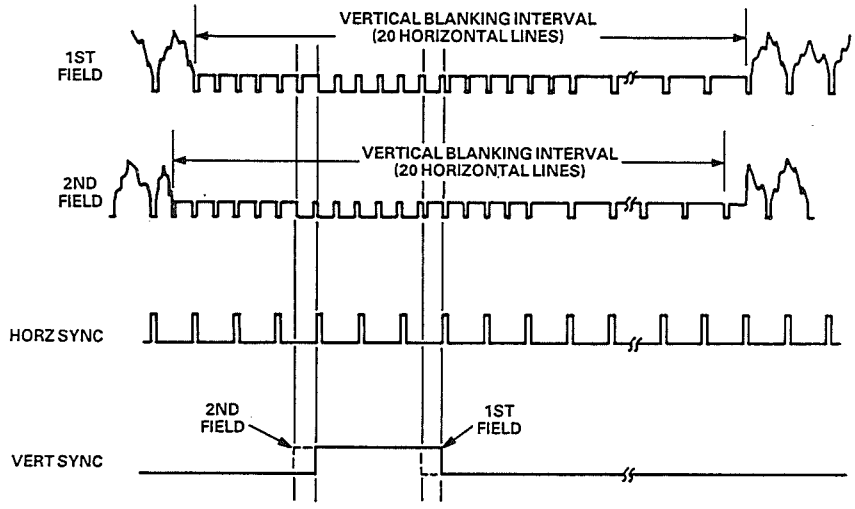

Figure 11.14

A simplified block diagram of the NTSC color processing system is shown in Figure 11.15. The three color signals (RGB: red, green, and blue) from the color camera are combined in a *matrix* unit to produce what is called the *luminance* signal (Y) and two color difference signals (I and Q). These *components* are further combined to produce what is called the *composite* color signal.

In the NTSC system (used in the U.S. and Japan), the color subcarrier frequency is 3.58MHz. The PAL system (used in the U.K. and Germany) and SECAM system (used in France), use a 4.43MHz color subcarrier. Comparisons between the NTSC system and the PAL system are given in Figure 11.16.

GENERATING THE COMPOSITE NTSC COLOR SIGNAL

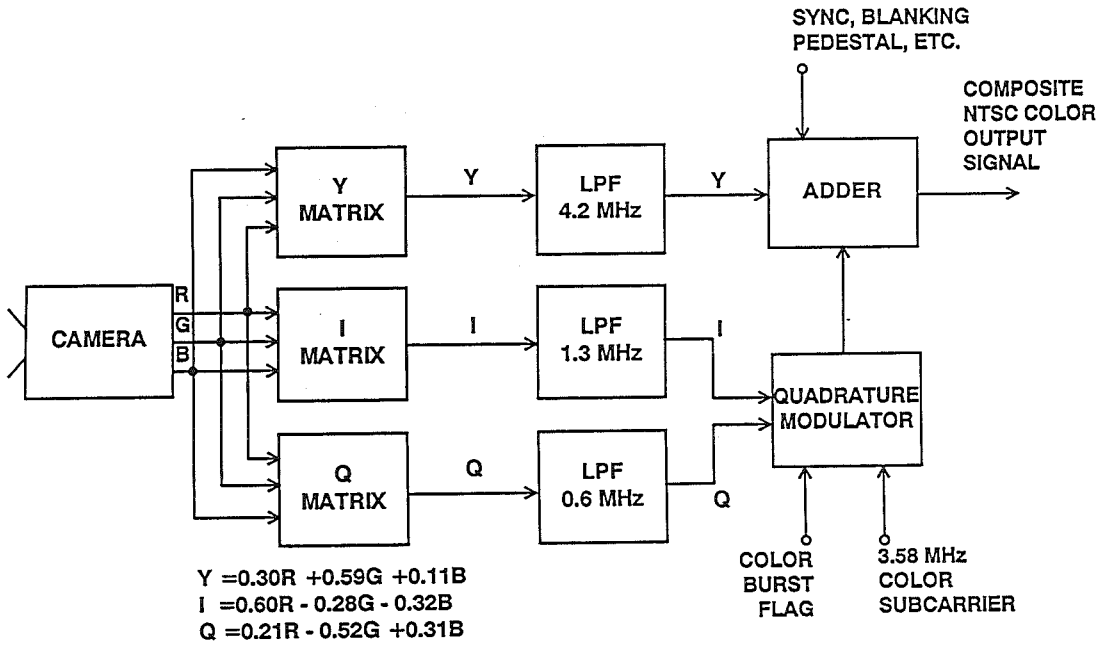

Figure 11.15

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NTSC AND PAL SIGNAL CHARACTERISTICS

	NTSC	PAL
Horizontal Lines	525	625
Color Subcarrier Frequency	3.58MHz	4.43MHz
Frame Frequency	30Hz	25Hz
Field Frequency	60Hz	50Hz
Horizontal Sync Frequency	15.734kHz	15.625kHz

Figure 11.16

High performance LSI circuits are now available which perform the majority of the complete RGB-to-composite conversion. Figure 11.17 shows a functional block diagram of the AD720 RGB to NTSC/PAL Encoder. This device provides separate chrominance, luminance, and composite video outputs and drives 75Ω reverse terminated cable at standard levels. The AD720 provides a complete, fully calibrated function, requiring only termination resistors, decoupling networks, a clock input at four times the subcarrier frequency, and a composite sync pulse. The AD720 has two control inputs: one input selects the TV standard (NTSC/PAL) and the other (ENCD) powers down most sections of the chip when the encoding function is not in use. All logical inputs are TTL and CMOS compatible. The chip operates from ±5V supplies.

AD720 RGB TO NTSC/PAL ENCODER FUNCTIONAL BLOCK DIAGRAM

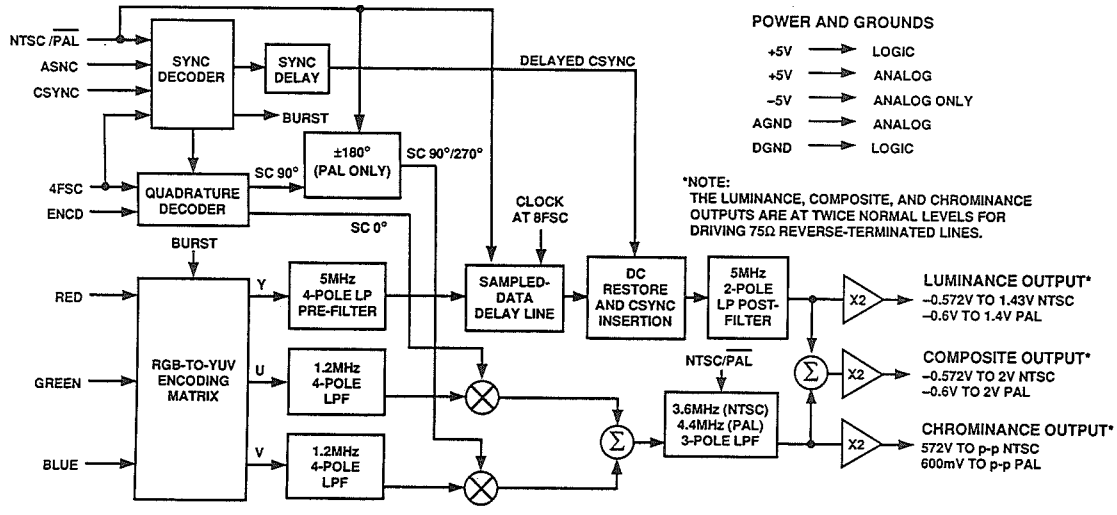


Figure 11.17

All required lowpass filters are on chip. After the input signals pass through a precision RGB to YUV encoding matrix, two on-chip filters limit the bandwidth of the U and V color-difference signals to 1.2MHz prior to quadrature modulation of the color subcarrier; a third lowpass filter at 3.6MHz (NTSC) or 4.4MHz (PAL) follows the modulators to limit the harmonic content of the output. Delays in the U and V chroma filters are matched by an on-chip

sampled-data delay line in the Y signal path; to prevent aliasing, a prefilter at 5MHz is included ahead of the delay line and a postfilter at 5MHz is added after the delay line to suppress harmonics in the output. These lowpass filters are optimized for minimum pulse overshoot. The AD720 is available in a 28 pin PLCC for the 0°C to +70°C commercial temperature range.

DIFFERENTIAL GAIN AND PHASE SPECIFICATIONS

Walt Kester

The color (or *chrominance*) information in the composite video signal is contained in the amplitude and phase of the subcarrier. The *intensity* or *saturation* of the color is determined by the amplitude of the subcarrier signal, and the precise color displayed (i.e. red, green, blue, and combinations) is determined by the phase of the subcarrier signal with respect to the phase of the color burst.

The chrominance signal modulates the luminance signal which determines the relative blackness or whiteness of the color. Therefore, in order to preserve color fidelity, it is important that the amplitude and phase of a constant-amplitude and phase color subcarrier remain constant across the entire range from black to white. Any variation of the *amplitude* of the color subcarrier from black to white levels is called *differential gain* (expressed in %), and any variation in phase with respect to the color subcarrier is called *differential phase* (expressed in degrees). Although several percent differential gain and several degrees differential phase is acceptable for home viewing purposes, individual components in the signal path (such as amplifiers, switches, etc.) must meet much tighter specifications. This is because the signal must pass through many circuits from the camera to the home. Individual professional video systems therefore have stringent requirements for differential gain and phase, usually limiting changes to less than 0.1% and 0.1°. These system specifications mandate even more stringent standards for individual components, with the differential gain and differential phase requirements for op amps approaching 0.01% and 0.01°.

Figure 11.18 shows a high resolution setup that uses a HP3314A waveform generator and a HP8753A network analyzer to measure differential gain and phase to better than 0.01% and 0.01° accuracy. The arbitrary waveform generator generates a staircase that simulates the luminance (picture level) portion of the video waveform. The network analyzer supplies the color subcarrier waveform, in this case a 4.43MHz color subcarrier. The network analyzer also measures the differences in the color subcarrier's phase and gain by comparing the output of the DUT and the reference signal returned by the HP11850 signal splitter. The 4.43MHz color subcarrier and the staircase signal are summed at the input to the op amp. This summing action superimposes the color subcarrier on the staircase, thus generating the standard video test waveform. The differential phase and gain is defined as the maximum difference in the phase or gain between any of the steps in the staircase waveform. Actual measurements taken on an op amp are shown in Figure 11.19.

PRECISION MEASUREMENT OF DIFFERENTIAL GAIN AND PHASE

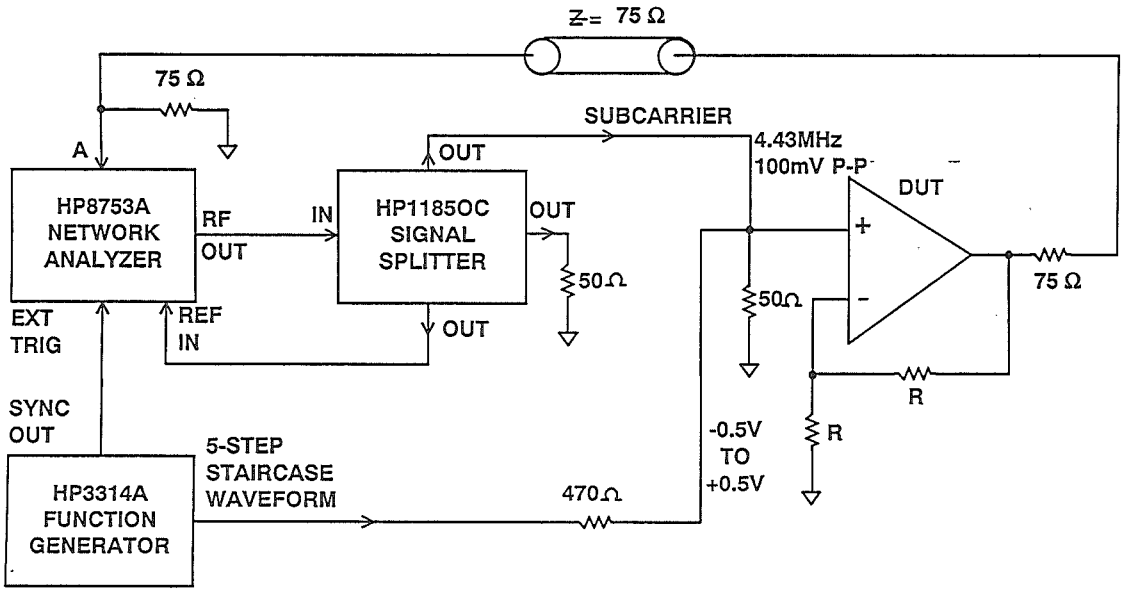


Figure 11.18

DIFFERENTIAL GAIN AND PHASE MEASURED WITH PRECISION TEST SET

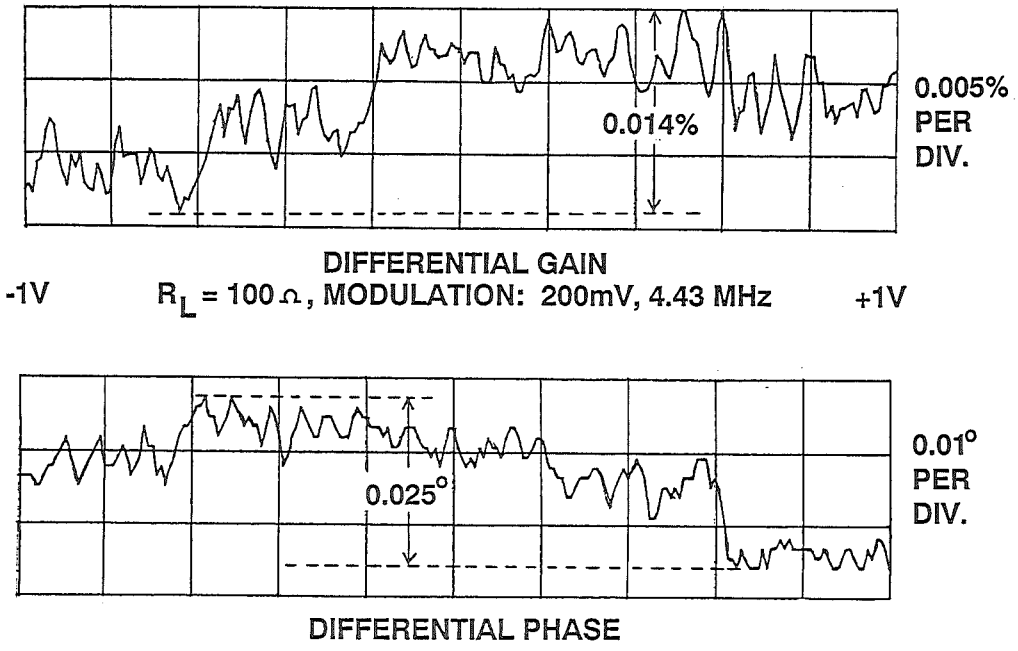


Figure 11.19

The op amp under test is shown connected as a gain-of-two amplifier driving a 75Ω reverse-terminated line. The 75Ω series termination resistor absorbs any reflections from the line termination mismatch. The 75Ω termination resistor and the 75Ω load form a voltage divider, so the net gain from the input to the DUT circuit to the load is unity.

VIDEO LINE DRIVERS
Walt Jung

The basic video line driver circuit of Figure 11.20 utilizes the low cost AD818 voltage feedback op amp. The stage gain is set at 2× by making R_F = R_{IN} = 499Ω. These values are chosen to be fairly low in order to maximize bandwidth. The AD818 is internally compensated for stable operation at a noise gain of 2 or greater, with a maximum bandwidth of over 50MHz. Quiescent current is only 6mA. As shown in Figure 11.20, the AD818 achieves its best differential gain and phase at higher supply voltages.

BASIC (GOOD) VIDEO LINE DRIVER USING THE AD818 OP AMP HAS 50MHz BANDWIDTH

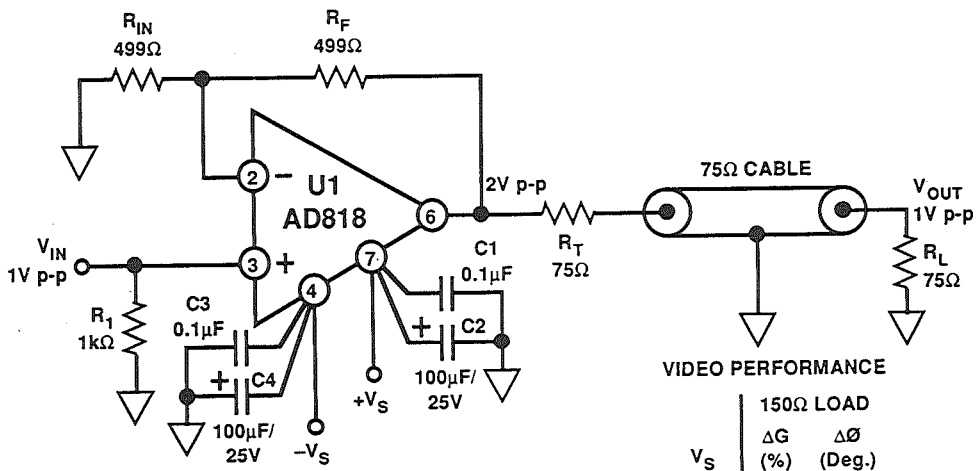
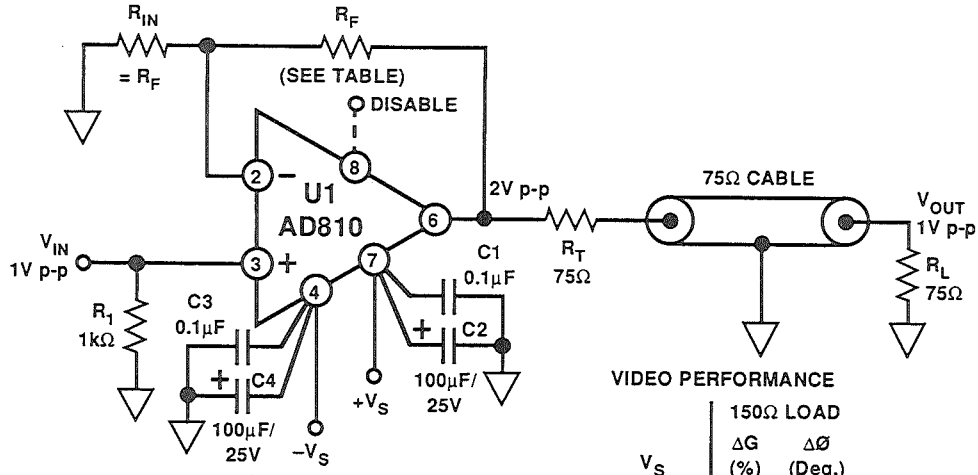


Figure 11.20

Figure 11.21 shows a higher-performance video line driver using the AD810 transimpedance amplifier. This circuit is also inexpensive, but it can perform better than the circuit of Figure 11.20 because of the AD810's appreciably higher slewrate and bandwidth, plus its higher output current. The AD810 has a 3dB bandwidth of 65MHz, and a 0.1dB bandwidth of 20MHz. Quiescent current is only 8mA. A unique feature of the AD810 is its power-down mode. The DISABLE pin is active-low to shut the device down to a standby current drain of 2mA, with 60dB input isolation at 10MHz. This permits on/off control of a single amplifier, or "wire or-ing" the outputs of a number of devices to achieve a multiplexing function.

HIGH PERFORMANCE (BETTER) VIDEO LINE DRIVER USING THE AD810 HAS DISABLE MODE, 65MHz BANDWIDTH (–3dB), AND 20MHz BANDWIDTH (–0.1dB)



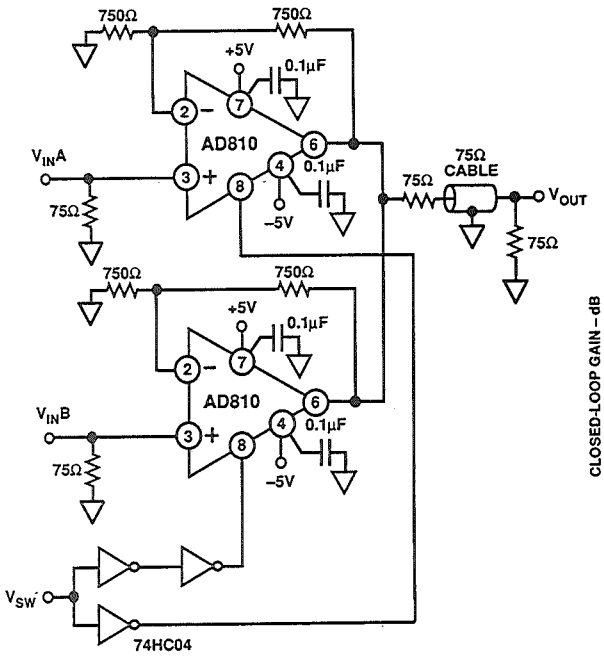
VIDEO PERFORMANCE

V_S	150Ω LOAD ΔG (%)	ΔØ (Deg.)
±5V R_F = 649Ω	0.04	0.05
±15V R_F = 750Ω	0.03	0.05

Figure 11.21

The outputs of two AD810s can be wired together to form a 2:1 multiplexer without degrading the flatness of the gain response. Figure 11.22 shows a recommended configuration which results in a –0.1dB bandwidth of 20MHz and OFF channel isolation of 77dB at 10MHz on ±5V supplies. The time to switch between channels is about 750ns when the disable pins are driven by open drain output logic. Adding pull-up resistors to the logic outputs or using complementary output logic (such as the 74HC04) reduces the switching time to about 180ns as shown in Figure 11.23. The switching time is only slightly affected by the signal level. The OFF channel feedthrough of the circuit is also shown in Figure 11.23.

A 2:1 VIDEO MULTIPLEXER USING AD810s HAS –0.1dB BANDWIDTH OF 20MHz AND SWITCHES IN 180ns



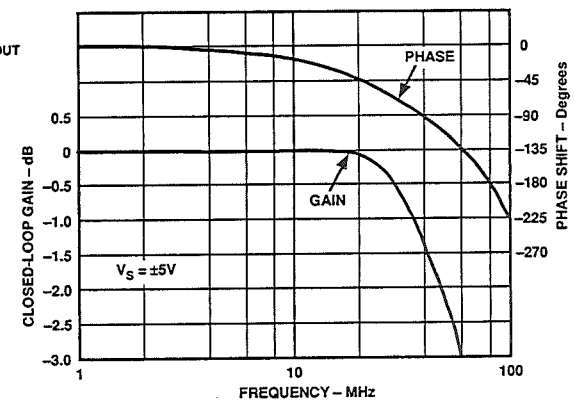
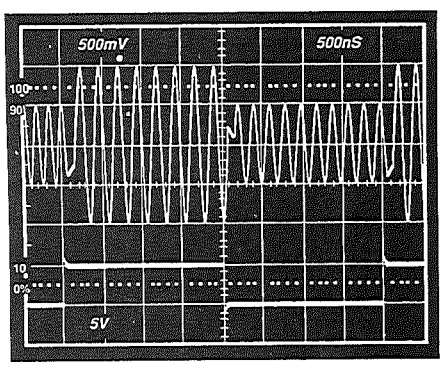


Figure 11.22

11

CHANNEL SWITCHING TIME AND OFF CHANNEL FEEDTHROUGH FOR THE 2:1 VIDEO MULTIPLEXER



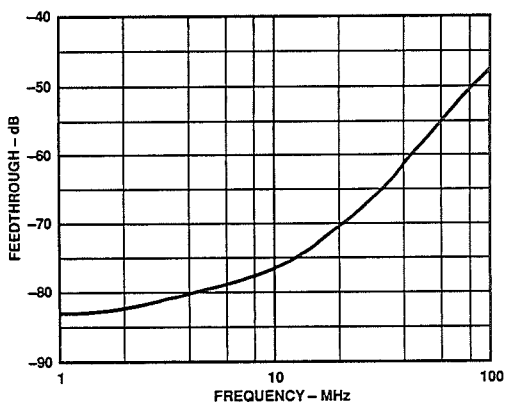


Figure 11.23

A multiplexer of arbitrary size can be formed by combining the desired number of AD810s together with the appropriate selection logic. Figure 11.24 shows a recommendation for a 4:1 multiplexer which may be useful for driving a low impedances (greater than 100Ω) such as the input to a video ADC. The output series resistors effectively compensate for the combined output capacitance of the OFF channels plus the input capacitance of the ADC while maintaining wide bandwidth. In the case illustrated, the –0.1dB bandwidth is about 20MHz with no peaking. Switching time and OFF channel isolation for the 4:1 multiplexer are about 250ns and 60dB at 10MHz, respectively.

A 4:1 VIDEO MULTIPLEXER USING AD810s HAS –0.1dB BANDWIDTH OF 20MHz AND SWITCHES IN 250ns

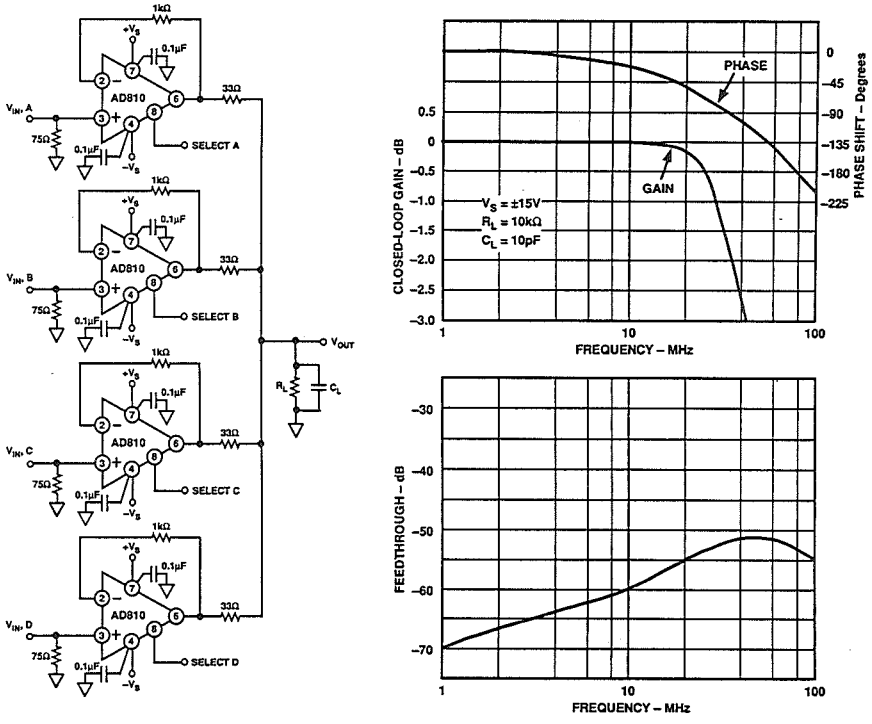
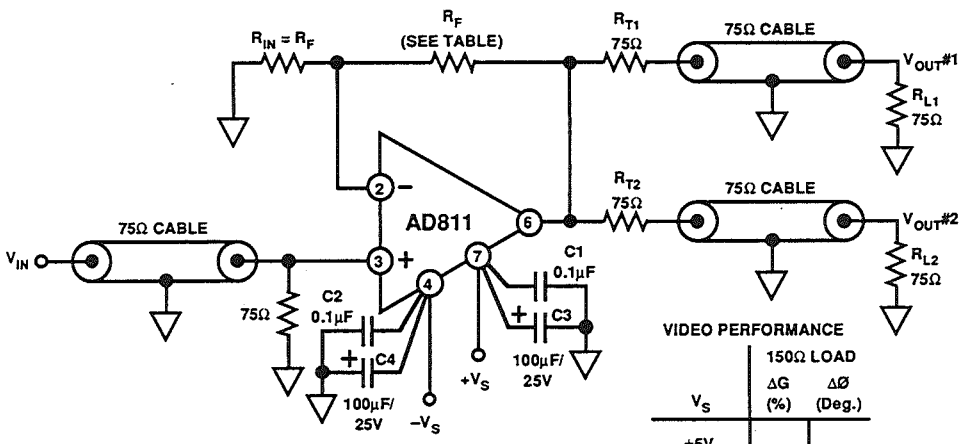


Figure 11.24

Figure 11.25 shows a very high performance video line driver using the AD811 transimpedance op amp as a gain-of-2 video buffer or line driver. This circuit also acts as a video distribution amplifier, driving two output lines.

HIGHER PERFORMANCE (EVEN BETTER) VIDEO LINE DRIVER/DISTRIBUTION AMPLIFIER USING AD811 HAS 120MHz BANDWIDTH (–3dB), AND 35MHz BANDWIDTH (–0.1dB)



VIDEO PERFORMANCE

	150Ω LOAD	
V_S	ΔG (%)	ΔØ (Deg.)
±5V R_F = 562Ω	0.015	0.18
±15V R_F = 649Ω	0.01	0.01

Figure 11.25

11

Construction of these video circuits should be in accordance with high speed rules. A solid, heavy copper ground plane should be used, and circuit layout should be compact with low capacitance, especially at the inverting input pin. In fact, the ground plane area immediately surrounding the inverting input pins should be etched away to ensure minimum stray capacitance at this critical node. In addition, the power supplies should be well bypassed. As a minimum, local low inductance/low ESR RF ceramic bypass capacitors should be used right at the device supply pins. These are 0.1μF surface mount chips (or other low inductance types). These capacitors should be augmented by local, short lead/large value low ESR electrolytics in the range of 47 to 100μF. These capacitors can be either tantalum, or aluminum types rated for high frequency (i.e., switching supply types).

HIGH SPEED DIFFERENTIAL SIGNAL TRANSMISSION

Walt Kester, Walt Jung

The transmission of high quality signals across noisy interfaces (either between individual PC boards or between racks) has always been a challenge to design engineers. Differential techniques using high common-mode-rejection-ratio (CMRR) instrumentation amplifiers largely solves the problem at low frequencies. At audio frequencies, products such as the SSM-2142 balanced line driver and SSM-2141/SSM-2143 line receiver offer outstanding CMRRs and the ability to transmit low-level signals in the presence of large amounts of noise.

The problem at video frequencies is twofold. First, video signals are generally single-ended and therefore don't adapt easily to balanced transmission line techniques. In addition, shielded twin-conductor coaxial cable with good bandwidth is usually somewhat bulky and expensive. Finally, designing high bandwidth, low distortion differential video amplifiers with high CMRRs at high frequencies is an extremely difficult task.

Even with the above problems, there are differential techniques available now which offer distinct advantages over single-ended methods. Some of these techniques make use of discrete components, while others utilize the latest in state-of-the-art video differential amplifiers.

Three solutions to the problem of differential transmission and reception are shown in Figure 11.26. The first represents the ideal case, where a balanced differential line driver drives a balanced twin-conductor coaxial cable which in turn drives a differential line receiver. This circuit, however, is difficult to implement fully at video frequencies for the reasons previously discussed.

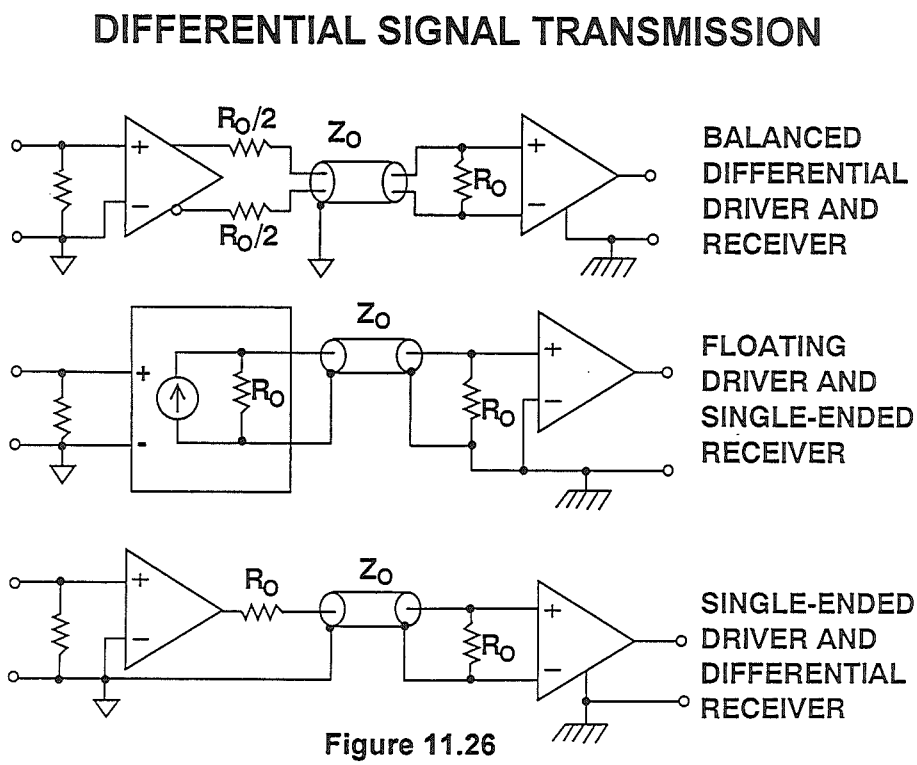


Figure 11.26

The second approach shown in Figure 11.26 uses a floating line driver (represented by the floating current source) to drive a single-conductor coaxial cable which is terminated at the receiving end in its characteristic impedance. Both the shield and the center conductor of the cable are driven by the floating line driver, and the cable is terminated at the receiving end. In this manner, noise between the two ground systems is isolated from the receiver output by the CMRR of the floating line driver.

The third and most often used approach makes use of a single-ended driver which drives a source-terminated coaxial cable. The shield of the coaxial cable is grounded at the transmitting end. At the receiving end, the coaxial cable is terminated in its characteristic impedance, but the shield is left floating. The common mode ground noise is rejected by the CMRR of the differential line receiver. The success of this approach depends upon the characteristics of the line receiver.

Figure 11.27 shows a practical implementation of the third approach in a single-ended 75Ω video transmission system.

SINGLE-ENDED DRIVER AND DIFFERENTIAL RECEIVER

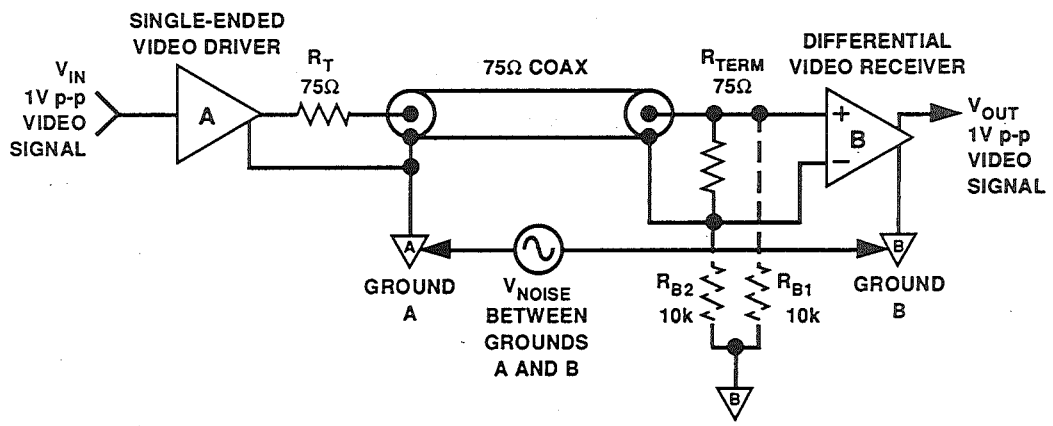


Figure 11.27

The noise between driver and receiver grounds is rejected by the CMRR of the differential video receiver. The coaxial line is terminated in its characteristic impedance at the receiver. Because neither end of the termination is connected directly to ground B, both inputs of receiver B see essentially the same common mode voltage, V_{NOISE}, which is rejected in proportion to B's CMRR. A

typical CMRR goal is 70dB or better for frequencies up to 10MHz. Return resistors, R_{B1} and R_{B2} may be needed to keep I_{bias} from developing excessive common-mode voltage across the amplifier inputs.

A low cost, medium-performance video line receiver, using a high speed op amp in a standard 4-resistor bridge instrumentation amplifier is shown in Figure 11.28. It is implemented using the AD818 op amp and low-resistance ac-trimmed resistors. Resistor matching is critical to good CMRR, so for highest noise rejection, a single-substrate dual-matched-pair thin-film network should be used. Matching of the ratios R1/R2 and R3/R4, to 1% gives a low-frequency CMRR of about 46dB. Above 1MHz, the bridge balance is dominated by ac effects, and C1 - C2 capacitive balance should be trimmed for best performance - a match that is essential for achieving CMRR above 40dB at high frequencies. This circuit, with its two 1kΩ input resistors, does load a 75Ω video line somewhat, and this loading should be taken into account.

SIMPLE VIDEO LINE RECEIVER USING THE AD818 OP AMP

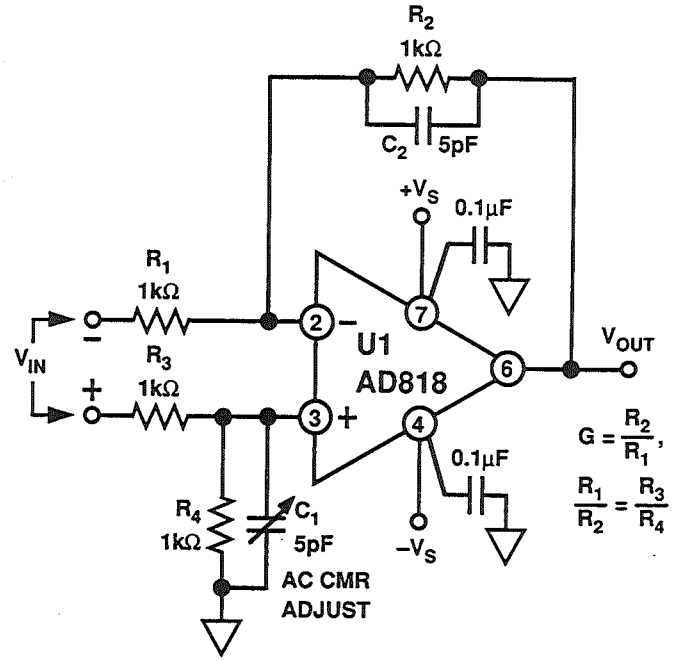


Figure 11.28

VIDEO LINE RECEIVERS USING THE AD830 ACTIVE FEEDBACK AMPLIFIER TOPOLOGY

Walt Kester

Full integration of the video line receiver eliminates the drawbacks of the simple line receiver approach and improves both performance and circuit flexibility. The AD830, shown in the circuit of Figure 11.29, is a two-input IC "active feedback amplifier" designed for this function. The signal from system "A" is received differentially by the AD830 and is reproduced relative to the ground in system "B". Common mode noise is rejected by the excellent CMRR of the AD830 (50dB at 10MHz). Key specifications for the AD830 are shown in Figure 11.30. CMRR and frequency response for the AD830 are shown in Figure 11.31.

DIFFERENTIAL LINE RECEIVER USING THE AD830

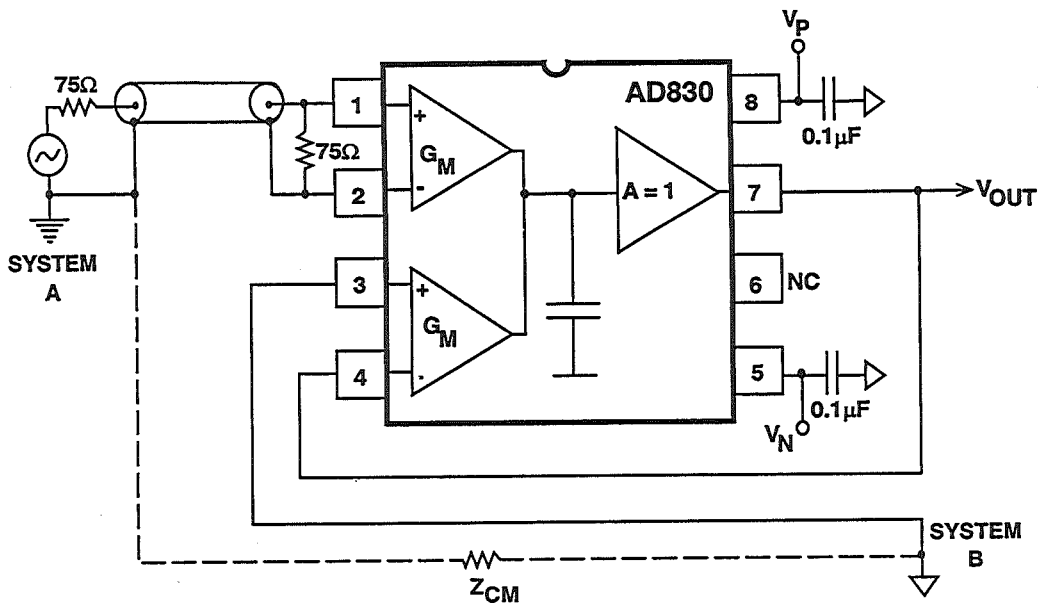


Figure 11.29

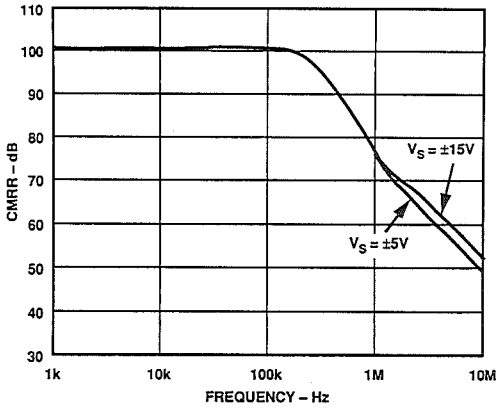
AD830 ACTIVE FEEDBACK VIDEO DIFFERENCE AMPLIFIER KEY SPECIFICATIONS

- Common Mode Voltage Range: ±11.5V
- Differential Voltage Range: ±2V
- CMRR: 60dB @ 4.43MHz, 50dB @ 10MHz
- Bandwidth: 50Mhz
- Distortion: -60dBc @ 4.43Mhz
- Differential Gain: 0.1%, Differential Phase: 0.1°

Figure 11.30

AD830 CMRR AND FREQUENCY RESPONSE (G = 1) FOR ±5V AND ±15V SUPPLIES

CMRR



FREQUENCY RESPONSE

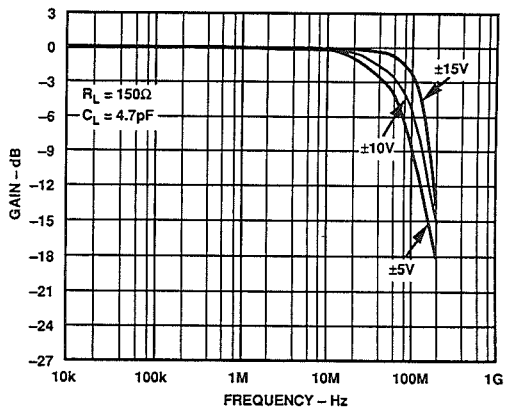


Figure 11.31

The AD830 represents Analog Devices' first amplifier product to embody a powerful new amplifier topology. Referred to as active feedback, the topology used in the AD830 provides inherent advantages in the handling of differential signals, differing system grounds, level shifting and low distortion, high frequency amplification. In addition, it makes possible the implementation of many functions not realizable with single op amp circuits and is often superior to op amp based equivalent circuits. For instance, you can use the AD830 to add or subtract two video signals with no external resistors.

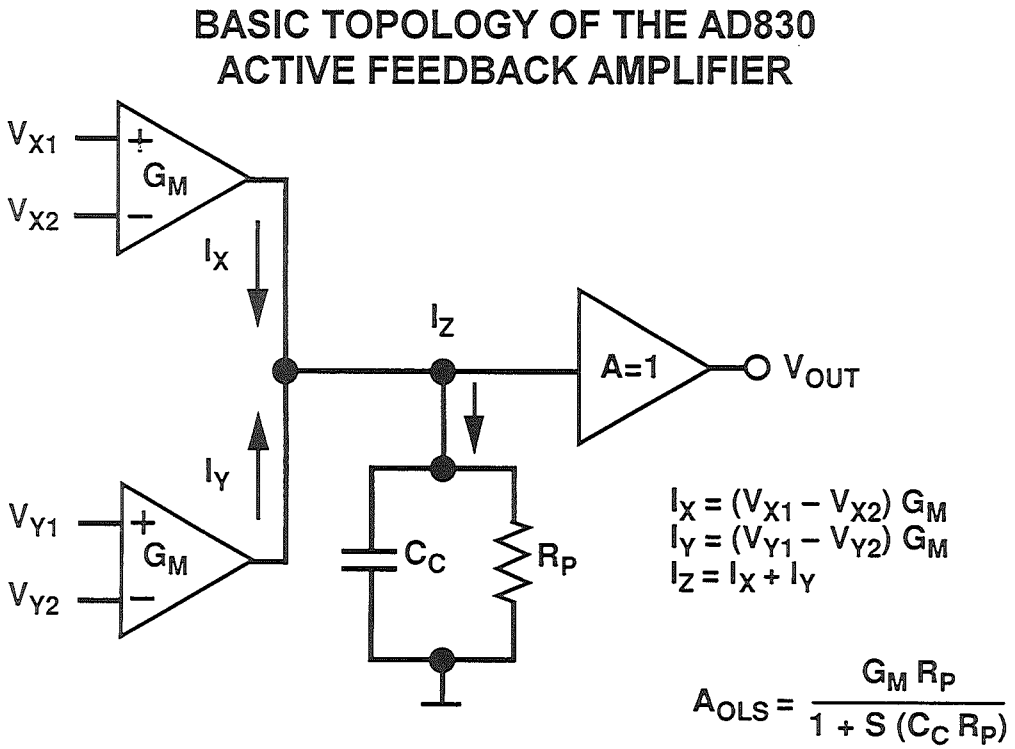
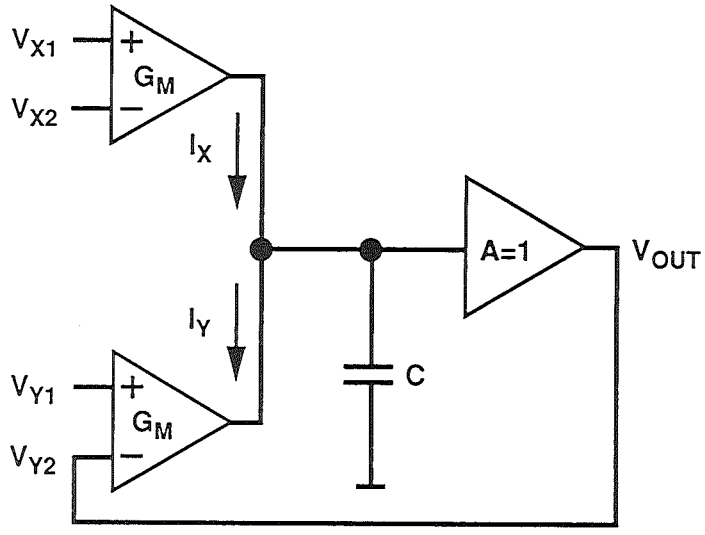


Figure 11.32

The AD830 topology, reduced to its elemental form, is shown in Figure 11.32. Nonideal effects such as nonlinearity, bias currents and limited input range are omitted from this model for simplicity. The key feature of this topology is the use of two, identical voltage-to-current converters, G_M, that make up input and feedback signal interfaces. They are labeled with inputs V_X and V_Y, respectively. These voltage to current converters inputs are fully differential; with high linearity, high input impedance, and wide common mode, small signal voltage range operation. The device can handle ±1V differential input signals in the linear mode. The inputs provide common-mode rejection, low distortion, and negligible loading on the source. The label, G_M, is meant to convey that the transconductance is a large signal quantity, unlike in the front end of most op amps. The two G_M stage current outputs I_X and I_Y, sum together at the high impedance node which is characterized by an equivalent

resistance and capacitance connected to an "ac" ground. A unity voltage gain stage follows the high impedance node to provide buffering from loads. Relative to either input, the open loop gain, A_{OL}, is set by the transconductance, G_M, working into the resistance, R_P, $A_{OL} = G_M \times R_P$. The unity gain frequency ω_{odB} for the open loop gain is established by the transconductance, G_M, working into the capacitance, C_C; $\omega_{odB} = G_M/C_C$.

CLOSED LOOP CONNECTION FOR THE BASIC AD830 TOPOLOGY



$$V_{X1} - V_{X2} = V_{Y2} - V_{Y1}$$

FOR $V_{Y2} = V_{OUT}$

$$V_{OUT} = (V_{X1} - V_{X2} + V_{Y1}) \frac{1}{1 + S(C_C/G_M)}$$

Figure 11.33

Precise amplification is accomplished through closed loop operation of the topology as shown in Figure 11.33. Voltage feedback is implemented via the Y G_M stage where the output is connected to the –Y input for negative feedback. An input signal is applied across the X G_M stage, either fully differentially or single-ended referred to common. It produces a current signal which is summed at the high impedance node with the output current from the Y G_M stage. Negative feedback nulls this sum to a small error current necessary to develop the output voltage at the high impedance node. the error current is usually negligible, so the null condition essentially forces the Y G_M output stage current to exactly equal the X G_M output current. Since the two transconductances are identical, the differential voltage across the Y inputs equals the negative of the differential voltage across the X input; $V_Y = -V_X$ or more precisely, $V_{Y2} - V_{Y1} = V_{X1} - V_{X2}$. This simple relationship provides the

basis to analyze any function possible with the AD830, including any feedback situation.

The bandwidth of the circuit is defined by the G_M and the capacitor C_C. The highly linear G_M stages give the amplifier a single pole response, excluding the output amplifier and loading effects. The bandwidth and general dynamic behavior is symmetrical (identical) for the noninverting and the inverting connections of the AD830. In addition, the input impedance and CMRR are the same for either connection. This is very advantageous and unlike the situation with a voltage or current feedback amplifier, where there is a distinct difference in performance between the inverting and noninverting gain stages. The practical importance of this cannot be overemphasized and is a key feature offered by the AD830 active feedback topology.

The AD830 is a flexible device which may be used in a number of configurations with excellent video performance. Figure 11.34 shows how the AD830 may be configured to provide instrumentation amplifier style amplification. The input signal is connected differentially to the internal V-to-I converter #1. The gain is set via the feedback resistors R2 and R1 in the same manner as a noninverting op amp circuit. The polarity of the gain is established by the relative connections at input pins 1 and 2. Inverting gain is set by reversing the connections to the input. As in a conventional voltage feedback op amp, the bandwidth decreases with increasing gain.

GAIN-OF-N INSTRUMENTATION AMPLIFIER USING THE AD830

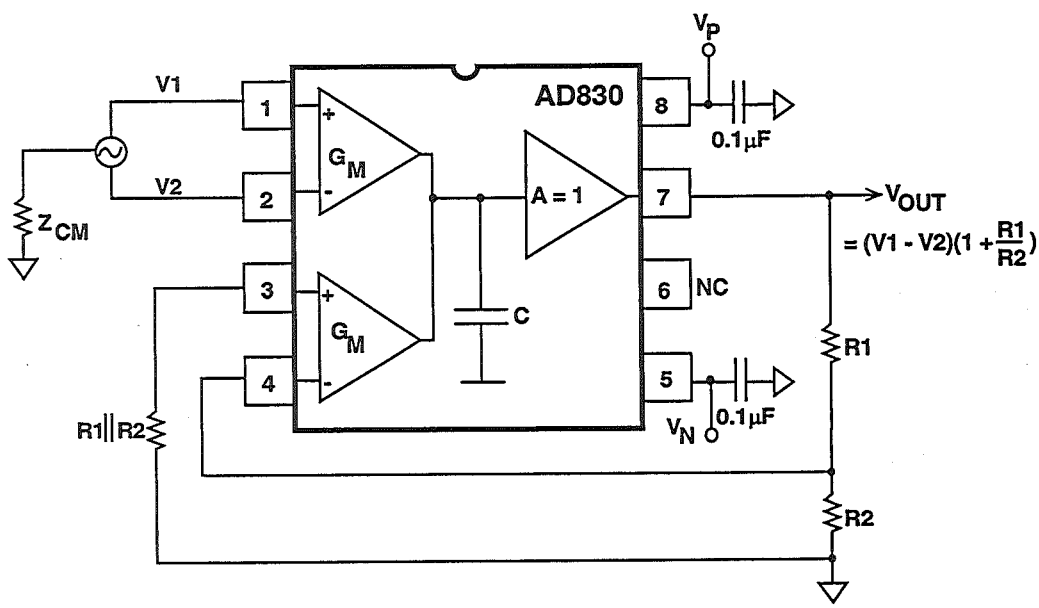


Figure 11.34

The video cable receiver/driver circuit shown in Figure 11.35 not only provides ground noise rejection, but also supplies a gain-of-two so that the AD830 output can drive a source and load terminated 75Ω cable without signal attenuation. The 499Ω resistors set the gain at 2, and the 249Ω resistor between pin 3 and ground cancels the offset due to the input bias currents.

VIDEO CABLE RECEIVER/DRIVER USING THE AD830

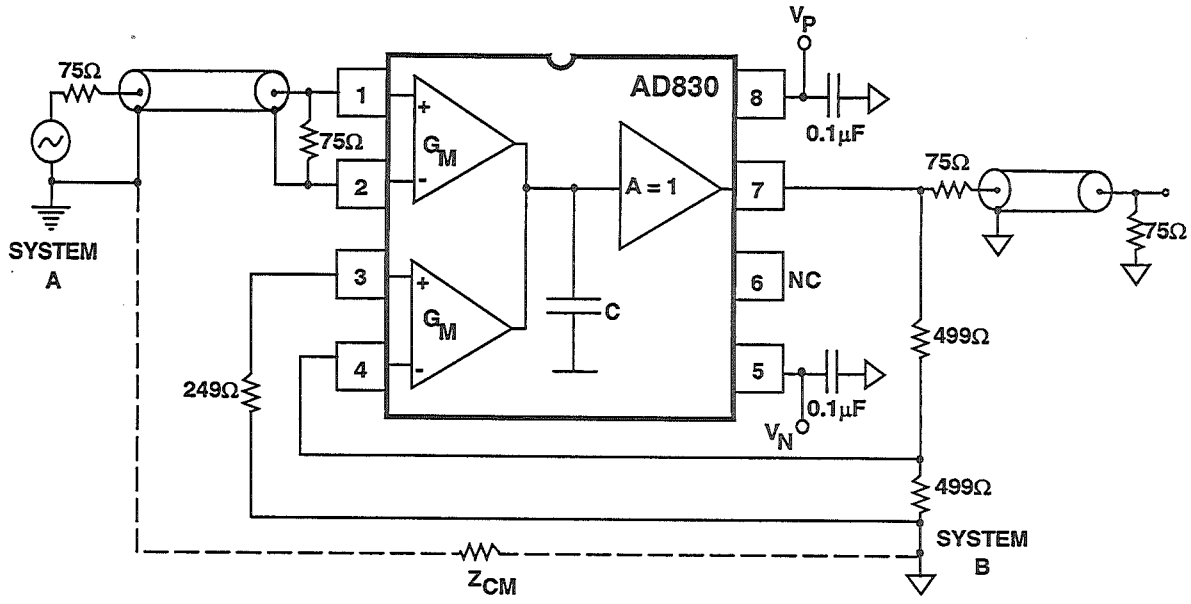


Figure 11.35

The video loop-through connection is a popular method of connecting different pieces of equipment. High input impedance differential amplifiers connect to taps along the distribution cable. The cable is terminated in its characteristic impedance at the source and at the far end. The AD830 makes an ideal choice for this loop-through amplifier because of its high input impedance and good common mode rejection at high frequencies. The high input impedance provides negligible loading on the cable. More significantly, the benign loading is maintained while the AD830 is powered down. Figure 11.36 shows a typical loop-through connection using the AD830.

VIDEO LOOP-THROUGH CONNECTION USING THE AD830

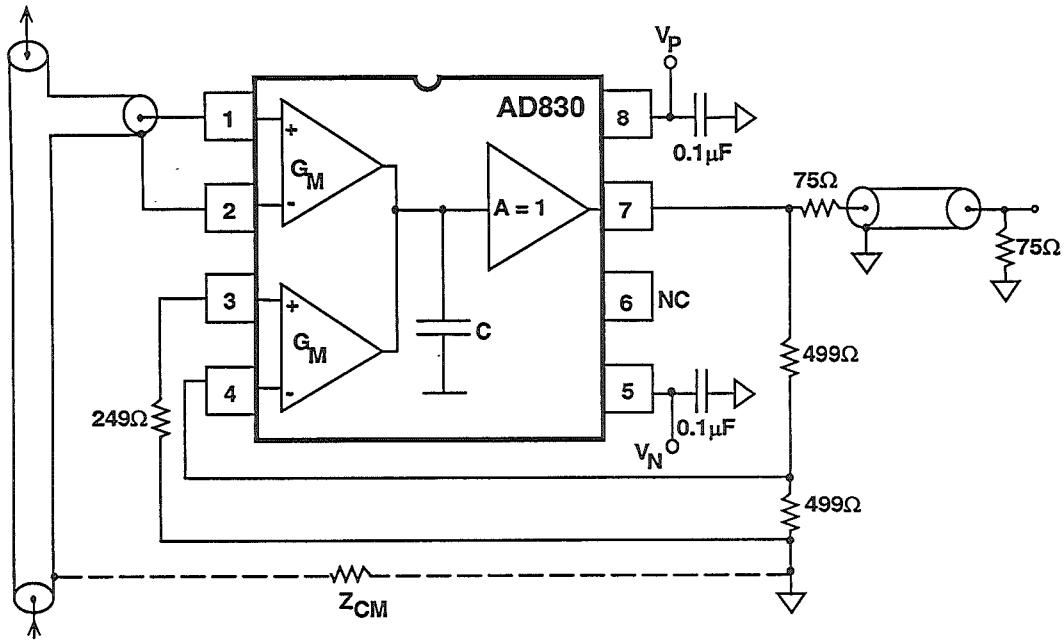


Figure 11.36

A COMPOSITE VIDEO SYNC TIP DC RESTORER

Walt Jung, Dave Whitney

A common video signal processing requirement is DC restoration, or clamping. When used with a composite NTSC video signal, sync tip clamping is commonly used. This fixes the most negative excursion of the signal to a fixed DC level, which is usually ground. With a constant input signal level, note that this operation also fixes the remainder of the signal with respect to ground. The circuit of Figure 11.37 is an example of a sync tip clamper, using 2 op amps and a pair of discrete transistors. With a standard NTSC composite video signal at the input, the circuit restores the signal to a ground reference, and makes the DC restored and buffered version available at the output, source terminated by 75Ω. This circuit is especially useful in driving an ADC, since ac coupling into the ADC requires additional range overhead and a corresponding loss of effective resolution.

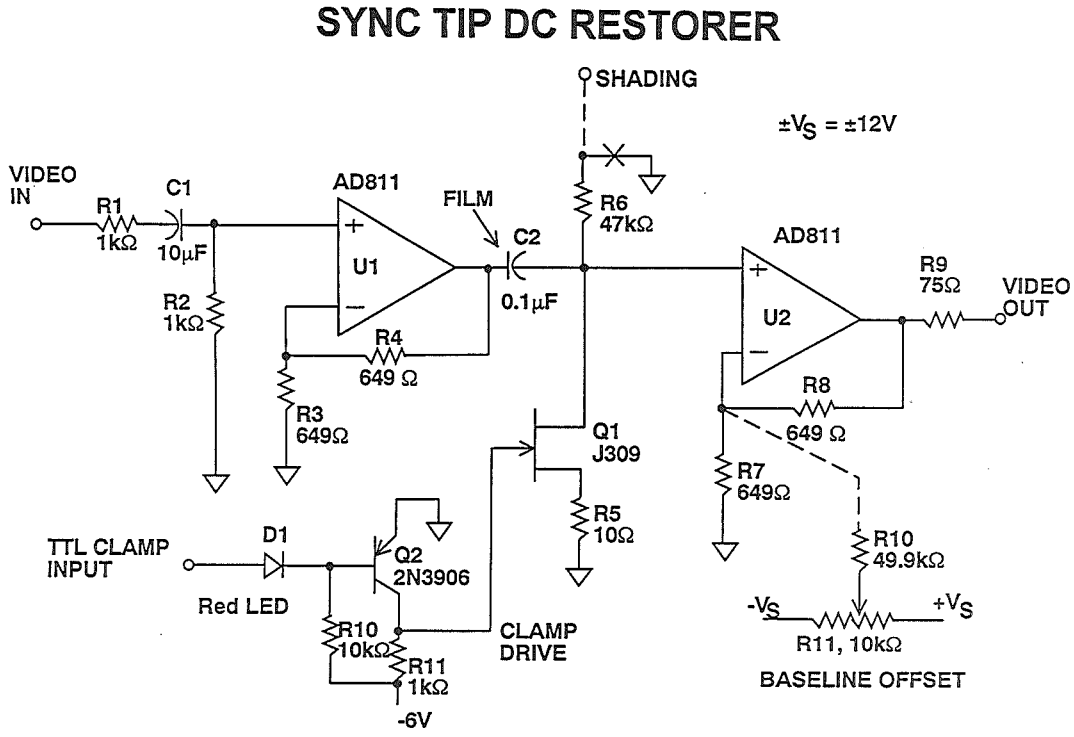


Figure 11.37

In operation, the U1 stage functions as an input line isolator and buffer. The signal at the input is divided by a factor of 2 by R_1 and R_2, and is AC coupled into U1. U1 is an AD811 configured as a wideband noninverting gain-of-two amplifier, by virtue of the R_4-R_3 ratio. With the values shown for R_4-R_3 and the use of ±10V (or more) DC supplies, the 0.1dB bandwidth will be more than 30MHz.

The output of U1 drives Q1, a shunt JFET switch through a film coupling cap, C_2. The N channel JFET is a low capacitance, high transconductance unit, chosen for 50Ω or less of on-resistance. The low capacitance allows it to be easily driven from U1, minimizing potential distortion of the signal. The low on-resistance of Q1 and high output current of the AD811 driver stage allows very fast charging of capacitor C_2 between sync tips, at a rate that will be limited to $I_{max(U1)}/C_2$ V/s. With a ±100mA output from the AD811 and a 0.1µF value for C_2, this allows maximum charging rates on the order of ±1 V/µs, applicable during the interval when switch Q1 is on (the clamp sample period). If this period is for example a 0.1µs time, then the circuit can correct ±100mV of baseline change for each clamp sample.

Since the overall video signal is on the order of 1Vp-p and corrections tend to be longer term, these design limits are conservative in practice. For example, for an interfering 60 Hz hum of 1 volt peak, the clamp circuit will see a maximum rate of change or slew rate of $SR = f \cdot 2\pi \cdot Vpeak$.

For 60Hz and 1V, the rate of change is 376.80V/s. In an NTSC 63.5µs line interval, the maximum change of this

hum signal is 376.80·63.5e-6 = 0.024V, which is correctable.

The clamp sample period drive signal is derived elsewhere, and is presented to this circuit as a TTL signal at D1-Q2. This signal is an active low TTL logic signal, and is timed to occur during the video waveform negative sync tips. The low state signal drives both Q2 and Q1 on, effectively connecting C_2 to ground through Q1-R_5, and so provides the DC reference path to ground described above.

During the remaining time period of a video line time, the switch Q1 is off due to the -6V bias from R_{11}. The bias current of U2 is the main DC load on the C_2-R_6 voltage node during this time, which will tend to ramp ±, slowly charging C_2 with the bias current of U2. Since this current could be as high as 5μA, the baseline ramp error in 50μs time could be (5e-6/0.10e-6)×50e-6 volts, or 2.5mV. However, this is not likely to be a problem, as the typical AD811 bias current is lower, and the video signal is appreciably larger in amplitude.

On the other hand, if an intentional ramp up or down waveform is desired, R_6 can optionally be returned to a variable DC voltage to achieve this effect (by breaking the ground at "X"). This will produce a horizontal shading (a black-to- white or white-to-black background).

Another option possible with the circuit is to introduce a variable DC baseline to the clamped signal, for example to provide a specific bias point for a following stage. The optional bias network consisting of resistor R_{10} and R_{11} can provide this function. The variable DC voltage from R_{11} injects a current through R_{10} which is added in voltage form at the output of U2, effectively allowing signal baseline offset of ±150mV about the DC clamping potential (which otherwise is ground). Note that if this feature is used, the value of R_7 may require some adjustment for exact gain, and that DC voltages ±Vs should be clean.

The output stage U2 is a second wideband AD811, configured as a 75Ω line driver. U2 presents the DC restored video signal to the output, with a level equal to the original input signal.

A VIDEO SYNC STRIPPER CIRCUIT
Walt Jung, Dave Whitney

Another common video signal processing requirement is the function of sync stripping. In a sync stripper, horizontal and vertical timing information is removed from the composite NTSC video signal and converted to logic levels for further processing. The circuit of Figure 11.38 is a self-contained sync stripper, using an AD811 op amp and a pair of discrete transistors. It is driven from an NTSC composite video signal and delivers TTL compatible positive going sync at the output.

SYNC STRIPPER GENERATES COMPOSITE SYNC

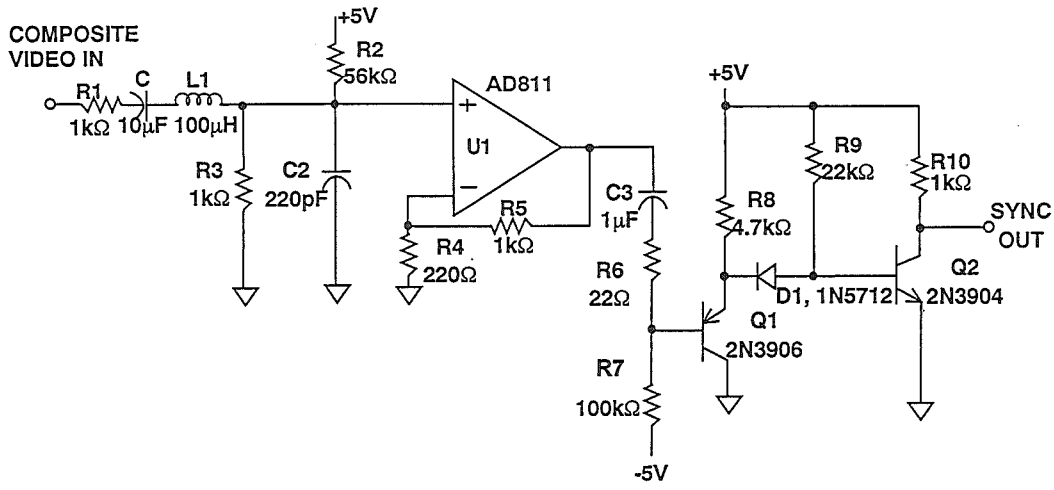


Figure 11.38

In this circuit the U1 stage performs three functions. First, components L_1-C_2 act as a low pass filter, removing the 3.58MHz chrominance components. U1, an AD811, also is an isolator with gain as well as a buffer to drive the following stage, which is a low input impedance sync tip clamp. The input signal is divided by a nominal factor of 2 by R_1 and R_2-R_3, and AC coupled to the input of U1. U1 is configured as a wideband times 6 amplifier, by the R_5-R_4 ratio. This yields an overall luminance signal gain of three times, from the input to C_3. With the gain values shown and ±5V (or more) DC supplies for U1, the stage can handle normal video signals without clipping at the output.

U1's output drives Q1, a PNP shunt clamp in an unusual configuration. In steady-state DC terms, Q1 is held in saturation by the bias current from R_7, where the emitter is close to ground. Since the AC signal driving Q1 through C_3 is a composite video signal with the sync tips the most negative limit, on a dynamic basis Q1 acts as a DC restorer. The negative going video waveform sync tips drive Q1 into hard saturation, and the more positive parts of the waveform bring it out of saturation, where it acts as a linear emitter follower. This action produces a DC restored composite video signal at the emitter of Q1, with the sync tips referred to ground.

The output of Q1 is coupled to the base of NPN switch Q2, through Schottky diode D1. The combination of this diode's forward drop and the V_{BE} of Q2 produce a switching threshold at the base of Q2 which, with consideration of

the signal levels, causes Q2 to switch on/off cleanly at about the sync tip 50% amplitude point.

The output from Q2 consists of clean, noise-free sync timing information, positive going during sync tips. This signal is TTL compatible, by virtue of the +5V supply to Q2 as shown. Practical hints in getting the most from this circuit involve some attention to good decoupling of the U1 stage. The high instantaneous currents during the sync tips can generate power supply and/or ground noise. Local bypassing of U1 with large capacitors to the logic supply ground will help to control this, as will a compact layout and the use of a ground plane.

MAINTAINING TRANSMISSION LINE IMPEDANCES ON THE PC BOARD
Walt Kester

In the previous section, we discussed methods for transmitting high speed signals across interfaces. It is equally important to maintain signal fidelity at the receiving end of the transmission line. In most applications, the actual termination point of the transmission line is on another PC board.

In some cases, it may be possible to bring the high speed analog signal into the PC board through an edge connector. The ground plane of the PC board should be connected to at least 20-30% of the connector pins. The analog signal(s) should be separated from other signals by ground pins.

EDGE CONNECTORS

- Separate Sensitive Signals by Ground Pins
- Keep the Ground Impedance Low with Multiple (20-30% of total) Ground Pins
- Have Several Pins for Each Power Line
- Critical Signals May Require a Separate Connector, Possibly Coaxial (BNC, SMA, SMB, SMC)

Figure 11.39

A much better solution is to bring the sensitive analog signal into the PC board via a separate coaxial cable connector. The most popular are the BNC types and the subminiature SMA, SMB, or SMC types. The smaller miniature types offer direct microstrip-to-coaxial interconnects with minimal impedance mismatch. Once the signal is on the PC board, it is a relatively simple matter to match the cable impedance.

Figure 11.40 shows the typical wire-over-ground plane line often used in prototypes. The characteristic impedance of this line is approximately 120Ω, but this may vary by as much as 40% depending upon the actual placement of the wire.

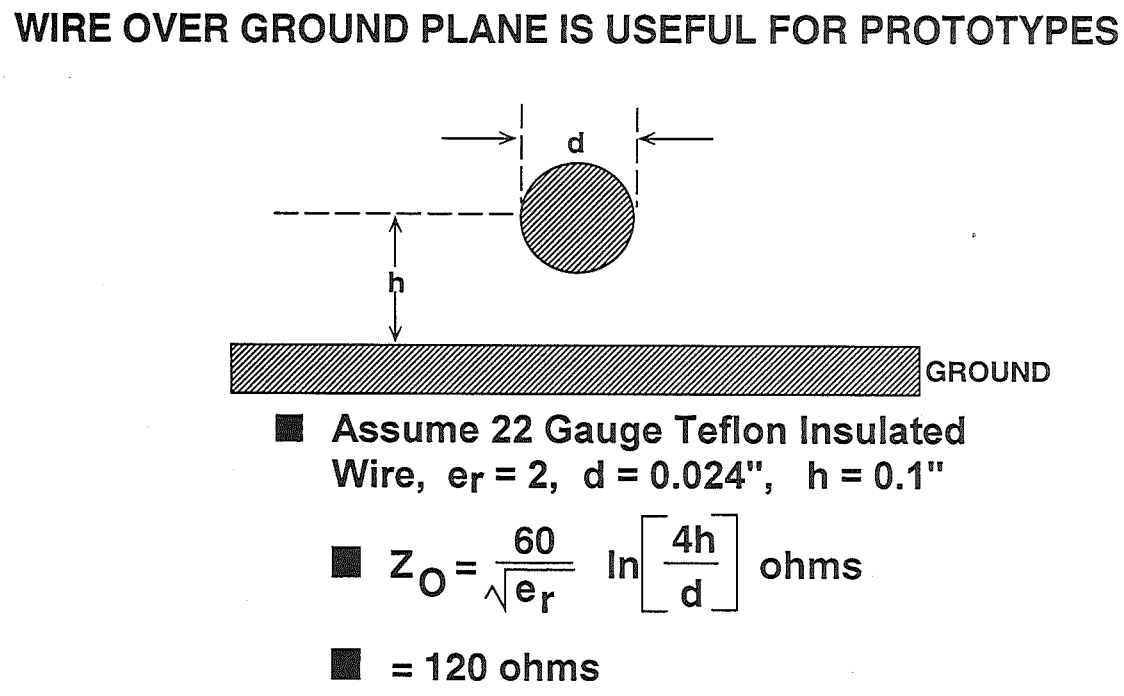
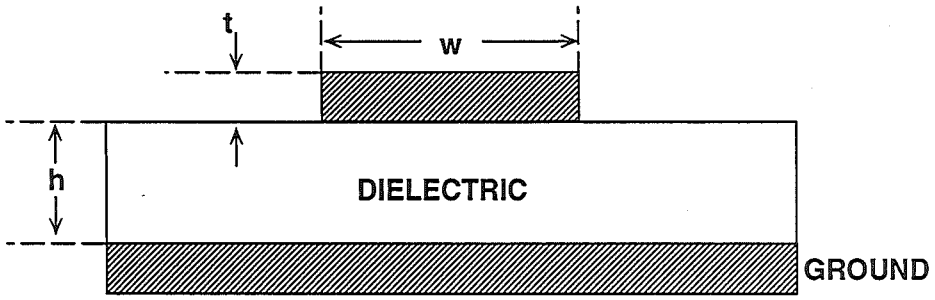


Figure 11.40

Microstrip techniques are easily implemented on a double-sided PC board, where one side of the board is dedicated primarily to ground plane, and the other side to the signal interconnects. The characteristics of typical microstrip lines are given in Figures 11.41, 11.42, 11.43, and 11.44.

In multilayer PC boards, strip line transmission line techniques are required as shown in Figure 11.45. The characteristics of typical strip lines are given in Figures 11.46 and 11.47. It is critically important that if a microstrip line is implemented on a PC board that there is no break in the ground plane underneath the line. Any break renders the whole exercise useless.

MICROSTRIP TRANSMISSION LINE FOR DOUBLE-SIDED PC BOARD



$$Z_O = \frac{87}{\sqrt{e_r + 1.41}} \ln \left[\frac{5.98h}{0.8w + t} \right]$$

$$t_{pd} = 1.017\sqrt{0.475e_r + 0.67} \quad \text{ns/ft}$$

$$t_{pd} = 1.73\text{ns/ft} \text{ for } e_r = 4.7$$

Figure 11.41

11

CAPACITANCE VERSUS LINE WIDTH AND DIELECTRIC THICKNESS FOR MICROSTRIP LINES

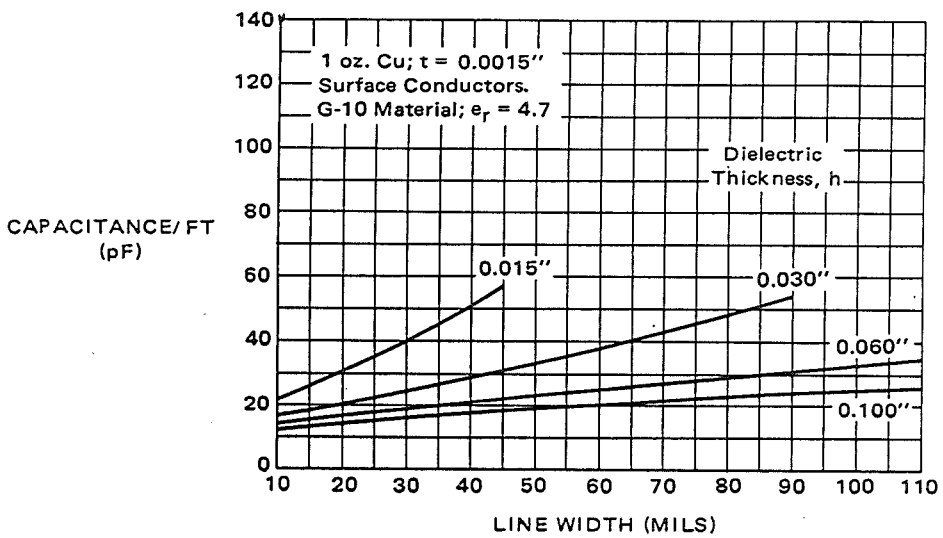


Figure 11.42

IMPEDANCE VERSUS LINE WIDTH AND DIELECTRIC THICKNESS FOR MICROSTRIP LINES

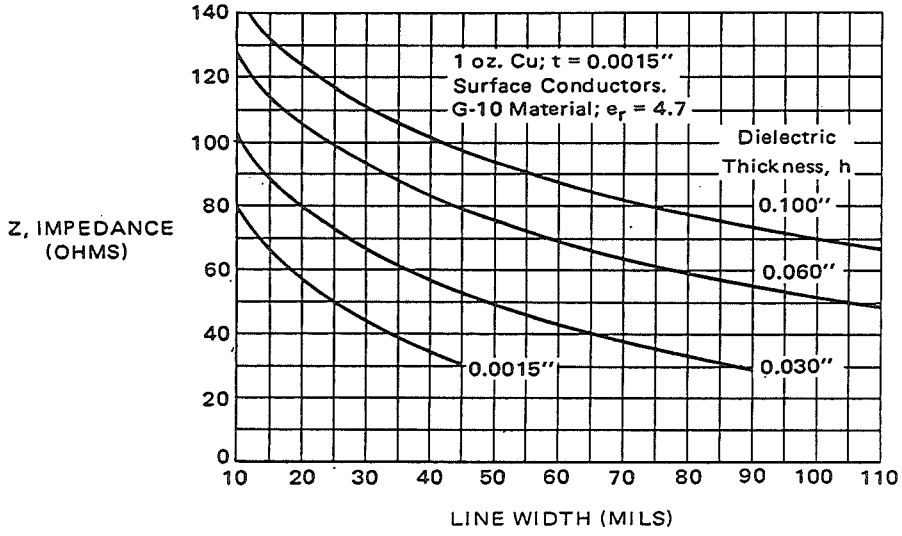


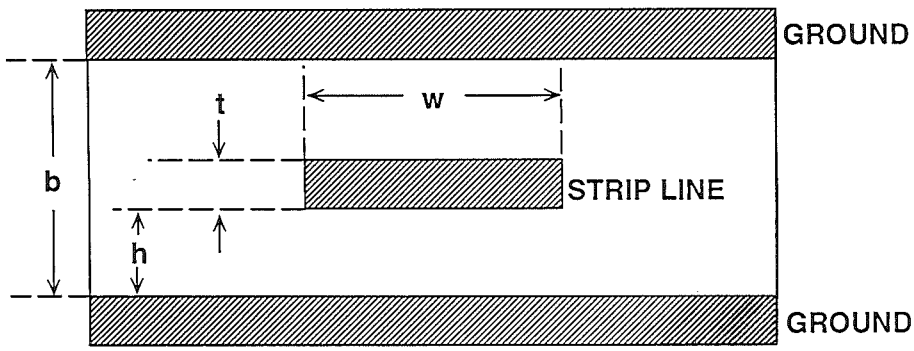
Figure 11.43

CHARACTERISTICS OF 1 OUNCE COPPER MICROSTRIP LINES ON 0.060 INCH THICK G-10 EPOXY PC BOARD

Characteristic Impedance	50Ω	75Ω	100Ω
Trace Width	105mils (2.67mm)	50mils (1.27mm)	25mils (0.63mm)
Distributed C	2.9pF/in (1.15pF/cm)	1.9pF/in (0.75pF/cm)	1.5pF/in (0.59pF/cm)
Distributed L	7.3nH/in (2.86nH/cm)	10.8nH/in (4.23nH/cm)	15nH/in (5.9nH/cm)
Prop. Delay	1.73ns/ft 0.144ns/in (0.057ns/cm)	1.73ns/ft 0.144ns/in (0.057ns/cm)	1.73ns/ft 0.144ns/in (0.057ns/cm)

Figure 11.44

STRIP LINE TRANSMISSION LINE FOR MULTILAYER PC BOARD



- $Z_O = \frac{60}{\sqrt{e_r}} \ln \left[\frac{4b}{0.67\pi w \left(0.8 + \frac{t}{w} \right)} \right]$
- $t_{pd} = 1.017\sqrt{e_r}$ ns/ft
- $t_{pd} = 2.2$ns/ft for $e_r = 4.7$

Figure 11.45

11

CAPACITANCE VERSUS LINE WIDTH AND SPACING FOR STRIP LINES

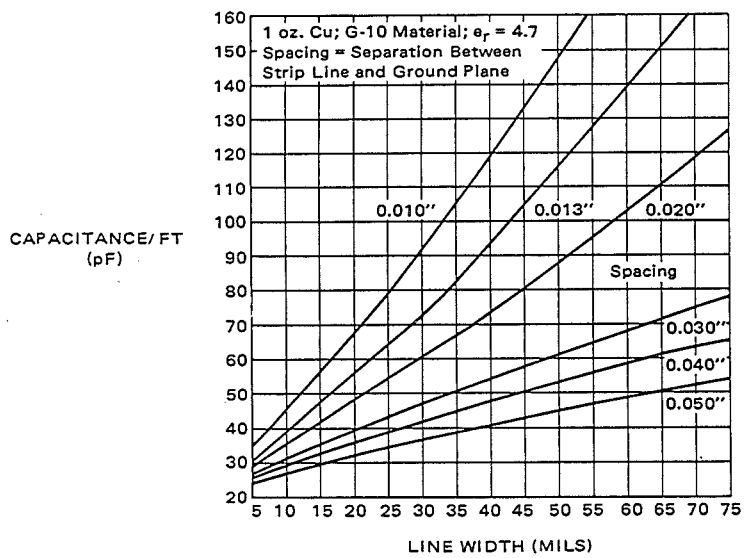


Figure 11.46

IMPEDANCE VERSUS LINE WIDTH AND SPACING FOR STRIP LINES

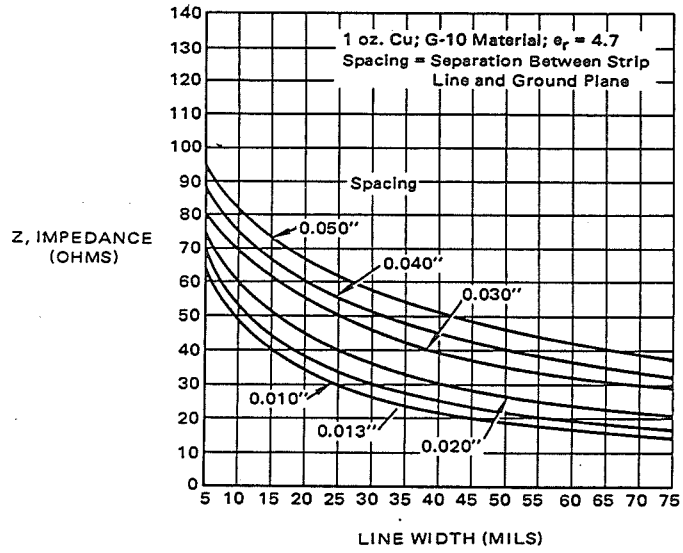


Figure 11.47

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