Memories

Chapter 6

INTRODUCTION

A digital memory is an array of binary storage elements organised so as to provide some means of external access. The memory array is arranged as a set of *memory words*, each of which consists of a number of single bit storage elements or *memory cells*. Typically, a memory word has a length of one, four or eight memory cells and can store 1 bit, 4 bits or 8 bits (or a *byte*) of information respectively. The contents of a particular memory word are accessed by specifying a unique memory address. Since the memory address is normally decoded from a binary number, there are usually 2^n memory words in an array. The *memory capacity*, which is measured in bits, is given by the product of the number of memory words and the number of memory cells in each word. Memory capacities are frequently defined in kilobits (kbits) where 1 kbit = 2^{10} = 1024 bits.

There are two basic ways of organising the memory array to allow external access to the store:

(i) *Serial or sequential access* where the time to access a particular memory word is not constant but depends on its position (or address) in the array.

(ii) *Random access* where the time to access a particular word is independent of its position.

The *access time* is defined as the time delay between providing a memory address and gaining access to the stored information (the *read* access time) or completing modification of the stored information (the *write* access time). The speed of operation of a

memory array is sometimes defined in terms of its *cycle time* which is the minimum allowable time interval between the initiation of successive memory access operations.

There are a number of different techniques for storing binary information. The memories commonly used in microprocessor systems are based on one of two storage techniques:

(i) Magnetic storage
(ii) Electronic storage.

Magnetic stores are non-volatile and retain the stored information when external power supplies are disconnected. There are two types: magnetic core memories and magnetic surface memories. Though the core memories have short access times (e.g., 400ns) they are uneconomic to manufacture for small memory capacity sizes. Typically, the smaller commercially available core memories have capacities of 32 kbits, and their application is usually limited to data and program store in relatively large microprocessor systems. Magnetic surface memories have longer access times (10ms to 50s) but provide a low-cost large-capacity non-volatile storage medium. Magnetic tape cassette and magnetic flexible disk memories are the most common secondary stores for data and programs in microprocessor systems.

Electronic or semiconductor stores are, with one exception, volatile and require the continuous connection of external power supplies if the stored information is to be retained. However, access times are short (30 ns to 500ns) and they have two major advantages over magnetic core memories:

(i) They can be manufactured at a comparable cost/bit for small capacity units (memory capacities range from 1 bit to 16 kbits per integrated circuit chip) which can be assembled to meet the exact storage requirements of a particular microprocessor application.

(ii) They are electrically compatible with the microprocessor chips and are more easily interfaced to the microprocessor system.

The use of semiconductor memories in microprocessor systems is widespread. In the remainder of the chapter attention is focussed on the various types of semiconductor memories. Memory cells

based on the more important manufacturing technologies are explained, different addressing and accessing schemes are described and the various microprocessor applications are discussed. Two examples are presented to illustrate the design of complete memory systems based on semiconductor memory chips.

SEMICONDUCTOR MEMORIES

Semiconductor memories fall into three categories:

(i) Read/write memory
(ii) Read-only memory
(iii) Read-mostly memory.

The contents of a read/write memory may be read out or modified an unlimited number of times under external control. The read and write access times are of similar length. In a read-only memory, the contents can be read out but, after they have been initially defined, they cannot be modified.

In a read-mostly memory, the contents may be read out but modified only with considerable difficulty. In this case the write access time is many orders of magnitude longer than the read access time. In addition, the number of times that the stored information can be modified is often limited.

THE BASIC READ/WRITE MEMORY CELL

Most read/write semiconductor memories are manufactured using either bipolar or metal-oxide-semiconductor (MOS) technology. Bipolar memory cells are *static* in that they retain the stored information as long as the power is applied to the circuit. MOS memory cells can be either static or *dynamic*. Even with the power applied, a dynamic memory cell can only store information for a limited period of time, typically 1 or 2ms, and requires its contents to be *refreshed* from time to time. Dynamic MOS memories have two important advantages over static memories.

(i) The *standby power*, which is the power consumed by the circuit when read or write access operations are not taking place, is much lower.

(ii) The number of transistors per memory cell is smaller. Thus larger capacity memory arrays can be manufactured on a single integrated circuit chip at lower cost.

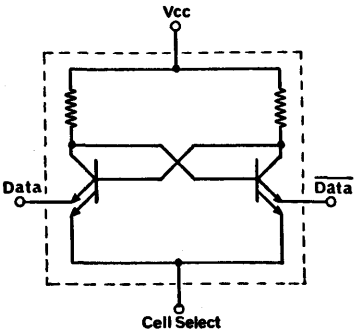

Figure 6-1a. Bipolar static memory cell

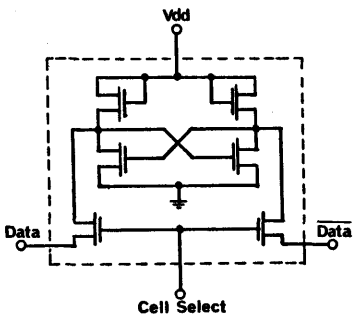

Figure 6-1b. MOS static memory cell

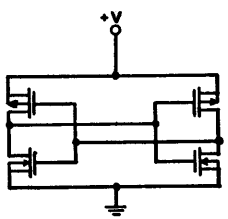

Figure 6-1c. Basic CMOS static memory cell

Figure 6-1. Static memory cells

A typical bipolar static memory cell is shown in Figure 6-1a. The two multiple-emitter transistors are cross-coupled to form a

simple bistable latch. The connections to the emitters allow the cell to be selected and data to be entered or read out. Figure 6-1b shows a simple P- or N-channel MOS static memory cell constructed entirely from MOS transistors. Two of the transistors are cross-coupled to form the bistable latch as before, whilst the others are used for loads and for the gating logic which allows access to the cell. In both of these types of static memory cells, the standby power consumption will be high (typically 500mW for a 1-kbit array) since one of the two cross-coupled transistors is conducting at all times. The storage element of a static memory cell based on a complementary MOS (or CMOS) circuit is shown in Figure 6-1c. By using pairs of PMOS and NMOS transistors, a bistable latch is formed which has negligible power dissipation on standby (typically 1mW for 1-kbit array).

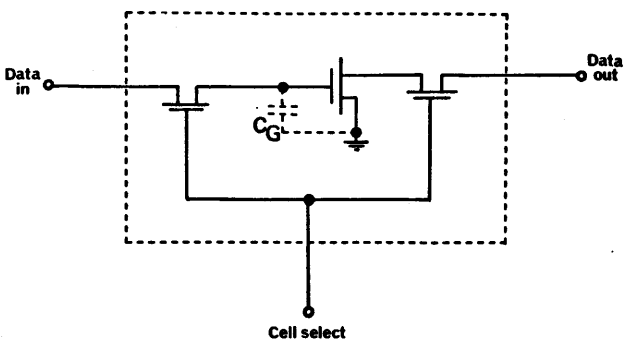

Figure 6-2. MOS dynamic memory cell

The MOS dynamic memory cell relies on the temporary storage of information as charge, or lack of it, on the gate capacitance of an MOS transistor. Figure 6-2 shows a typical design based on three MOS transistors per memory cell. Since the charge on the gate capacitance C_G will gradually leak away, the cell will require periodic refreshing of its contents. In addition, the data read-out operation destroys the contents of the memory and a data restore (read followed by write) operation is necessary to access each memory word. The periodic refresh operations, which are usually controlled by external logic, will reduce the availability of the memory for normal use. Typically, a dynamic memory is busy and unavailable for external data transfers for 1% to 5% of the time.

The restore operation which is performed automatically using on-chip logic will tend to lengthen the cycle time of the memory. Non-destructive read operations are possible in dynamic memory cells which are more complex and use more transistors than that shown in Figure 6-2. The read access time is thus reduced at the expense of a greater chip area per cell. In standby mode, power is consumed only during the refresh operations. The average standby power requirement is typically 2mW for a 1-kbit array.

ORGANISATION OF SERIAL-ACCESS READ/WRITE MEMORY ARRAYS

In a serial-access read/write memory, the sequence in which the information is loaded into the input of the memory will determine the order in which the stored information is available at the output of the memory. Access times are therefore dependent on memory location.

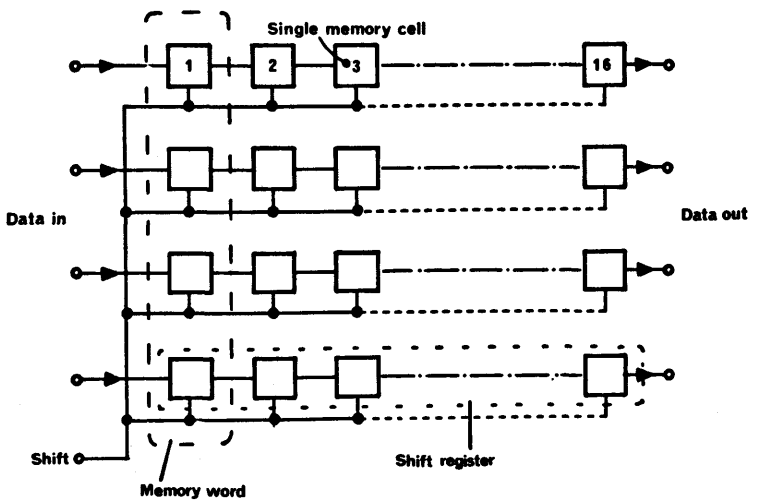

Figure 6-3. 16 x 4-bit FIFO

The First-In-First-Out (FIFO) memory. The memory consists of a number of shift registers equal to the number of cells in the memory word. As shown in Figure 6-3, each shift register which is formed by interconnecting a string of memory cells is clocked

from the same source. At every clock pulse the contents of each column of cells is transferred one position to the right. New information is entered into the first column of cells and the oldest information is read out from the last column of cells. The entry of new information will lead to the loss of old information from the memory. Both static and dynamic memory cells can be used in the construction of the shift registers and the shift operation is usually controlled by a multiphase clock.

Figure 6-4 shows a memory cell from a MOS static shift register which uses a three-phase clocking sequence. The new data is read into the left hand side and the old data is read out of the right hand side of the cell when ϕ_1 is high. The circuit operates dynamically during the shift operation and relies on gate capacitances for information storage. When ϕ_2 and ϕ_3 are high, the transistors are fully cross-coupled, the information is actively latched and the cell operates statically until the next clocking sequence begins. It is common for ϕ_2 and ϕ_3 to be generated on-chip from ϕ_1. The maximum clock rate will depend on the charging and discharging time constants of the circuit. There is no minimum clock rate. A typical MOS static shift register has a capacity of 2 kbits/chip and a maximum operating frequency of 2MHz.

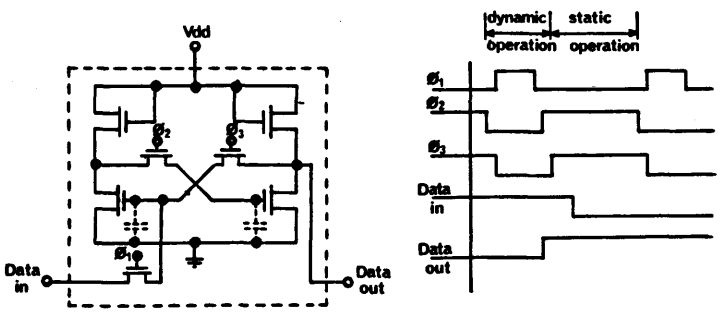

Figure 6-4. 3-phase MOS static shift register cell

Figure 6-5 shows a cell from a dynamic MOS shift register which uses a two-phase clocking sequence. The cell consists of two similar circuits interconnected as a master-slave combination. New data stored on C_{G1} is sampled when ϕ_1 is high and its inverse is stored on C_{G2}. The data output line is set to the inverse of the

data stored on C_{G2} during ϕ_2 to complete the shift operation. The standby power dissipation is low since the load transistors are switched on only when ϕ_1 or ϕ_2 are high. Periodic clocking is required to renew the charges on C_{G1} and C_{G2}. The minimum clock rate (typically 10kHz) will be determined by the rate of charge leakage from the gate capacitors. The maximum time that information can be retained in the memory will depend upon the length of the shift registers and the minimum clock rate.

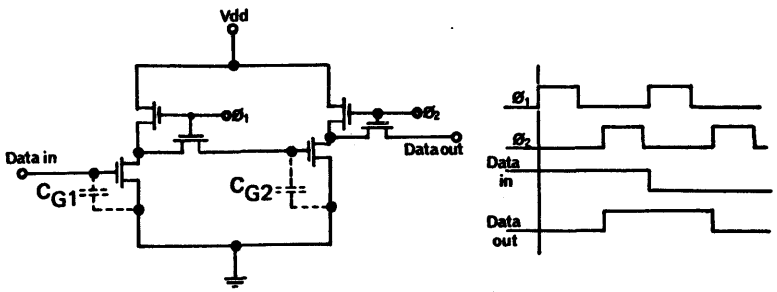

Figure 6-5. 2-phase MOS dynamic shift register cell

The recirculating memory. A recirculating memory is a FIFO memory with its output fed back into its input. As shown in Figure 6-6, some additional logic is required to allow new data to be gated into the memory. If the memory is constructed from dynamic shift registers, the recirculation operation provides a means of automatically refreshing the dynamic stores. In standby mode, the contents are continuously recirculated at a rate determined by the clock. In read or write mode the contents of the counter are compared with the address of the desired memory word until a match is found. The "write" or "read" control signal then gates the required data in or out of the memory. The access time varies according to memory location. It has a maximum value dependent on the length and clock rate of the memory.

As an example, a single chip serial memory fabricated with charge-coupled-device (CCD) technology, and consisting of 64 independent 256-bit recirculating shift registers, has a 16-kbit capacity and a 128μs maximum access time.

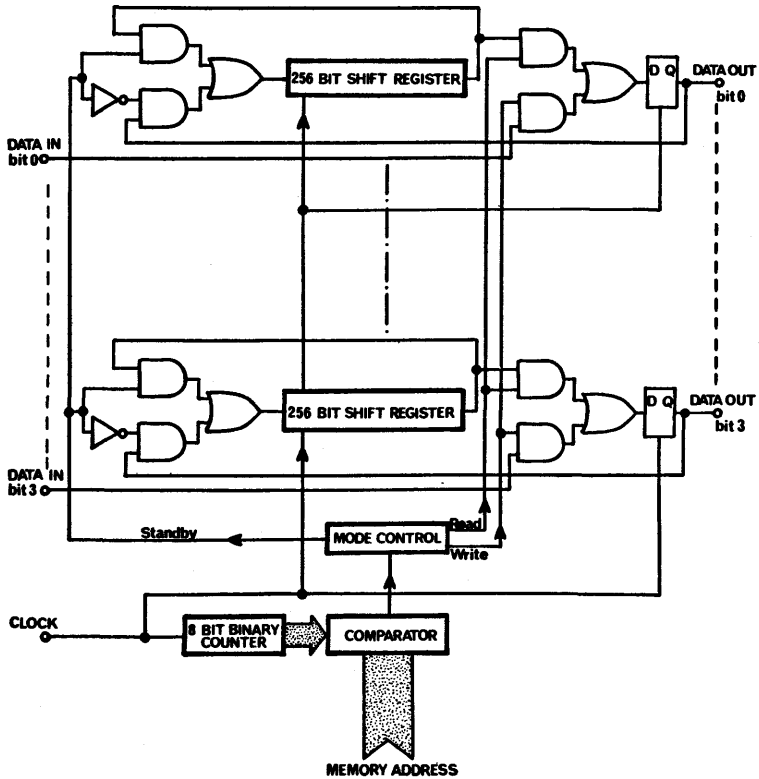

Figure 6-6. 256 x 4-bit recirculating memory

RANDOM-ACCESS READ/WRITE MEMORIES

In a random-access read/write memory, the availability of the stored information at the output of the memory is independent of the order in which the information was loaded into the memory. Access times are therefore independent of memory location.

The standard random-access read/write memory consists of a memory cell array with memory address decoders, data sense amplifiers, output buffers and access control logic, all on a single integrated-circuit chip. The term RAM is generally accepted to describe this type of memory although other types of random-

access memory are in common use (e.g., random-access read-only memory). Memory arrays are based on bipolar or MOS static memory cells or on MOS dynamic memory cells. Two ways of organising memory address decoding are discussed below.

Word organisation. A multibit memory word structure is used in the array as shown in Figure 6-7. A single binary address decoder is used to select simultaneously each of the memory cells in the particular memory word which has been addressed. The number of external connections to the integrated-circuit package is high and the technique is only used in small capacity memories.

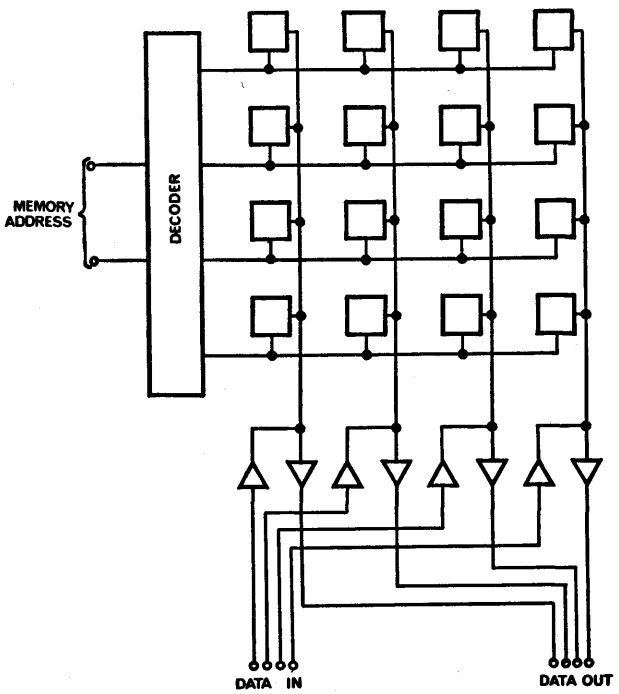

Figure 6-7. 4 x 4-bit word organised RAM

Co-incidence addressing. In larger memory chips the number of external connections is reduced by adopting a single bit memory word structure for the array. Two decoders are used to generate the X-select signal and the Y-select signal from the binary memory address. A particular memory cell is accessed when both of its X-

and Y-select lines are active at the same time. The logic to detect co-incidence of the select signals is either included as part of the memory cell (Figure 6-8) or is implemented using gating circuits external to the array (Figure 6-9).

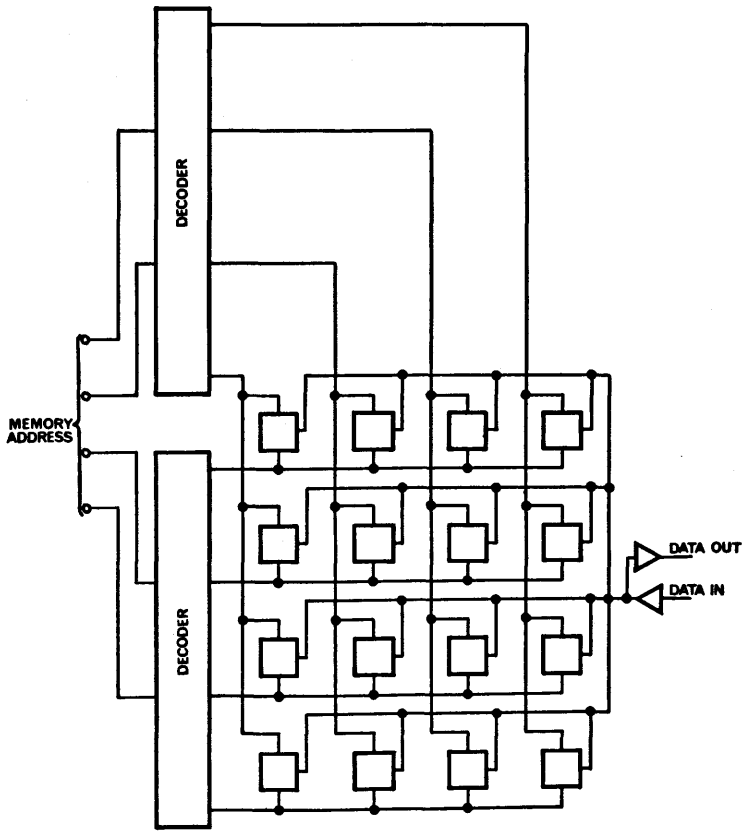

Figure 6-8. 16 x 1-bit RAM with coincidence addressing (cell detection)

Most of the commercially available RAM chips include chip-select logic and use three-state bidirectional data lines under control of a read/write select signal to simplify the design of large multi-chip memory systems. The number of words in a memory array may be increased by connecting the outputs of several memory chips in parallel as shown in Figure 6-10. The number of cells in each

memory word of an array may be increased by parallelling the address and chip select lines of several memory chips as shown in Figure 6-11.

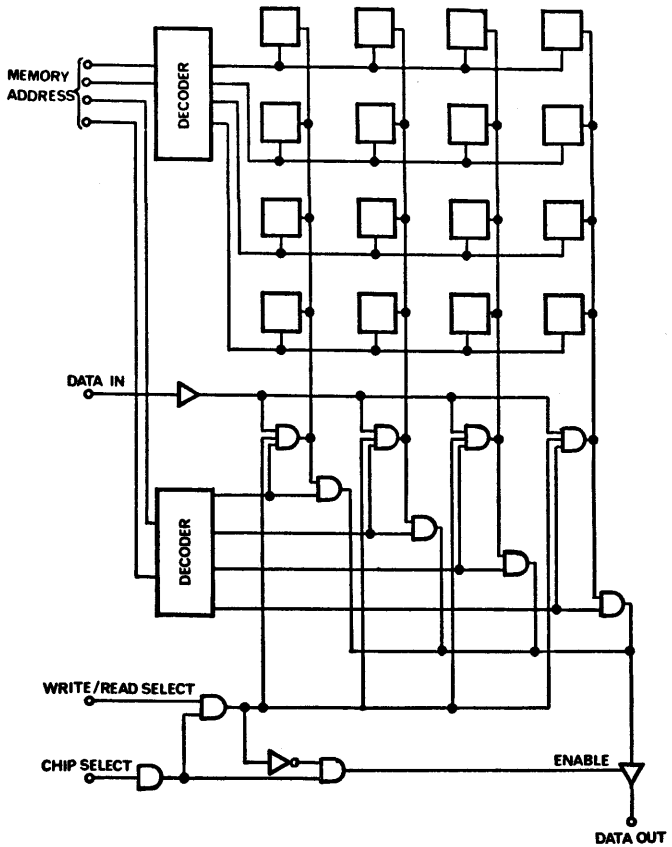

Figure 6-9. 16 x 1-bit RAM with coincidence addressing (external detection)

A typical bipolar static RAM chip has a capacity of 256 bits and an access time of 50ns. A typical MOS static RAM chip has a capacity of 2 kbits and an access time of 400ns.

MOS dynamic RAM chips have larger capacities (e.g., 4 kbits) and similar access times, but require additional external logic to control the refresh operation. In most cases, refreshing is accomp-

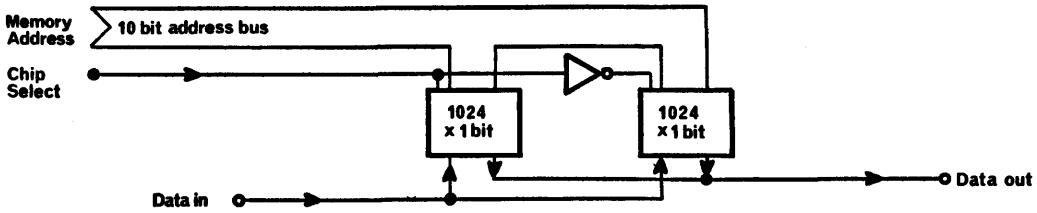

Figure 6-10. Extending the number of words in the memory (2048 x 1-bit RAM)

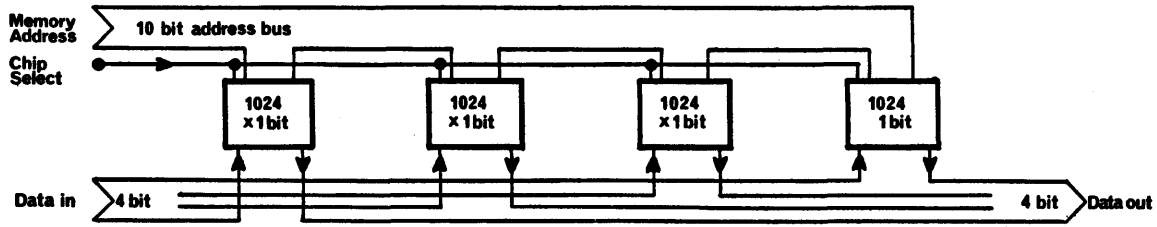

Figure 6-11. Extending the number of cells in the memory word (1024 x 4-bit RAM)

lished by performing a read or write operation, with the chip select disabled, on each column of the memory array in turn. The refresh operations must be organised so as to cause a minimum of interference with the normal memory access operations. The similarity between refresh and direct-memory-access may be noted. A number of refresh control schemes are used. Figure 6-12 shows the important elements of the external control logic and indicates the availability of the memory when using interleaved cycle-steal and burst-refresh control schemes. All the schemes are transparent to the microprocessor but only the interleaved refresh scheme does not delay the normal memory access operations. A more detailed description of a dynamic read/write memory system with cycle-steal refresh control is given later.

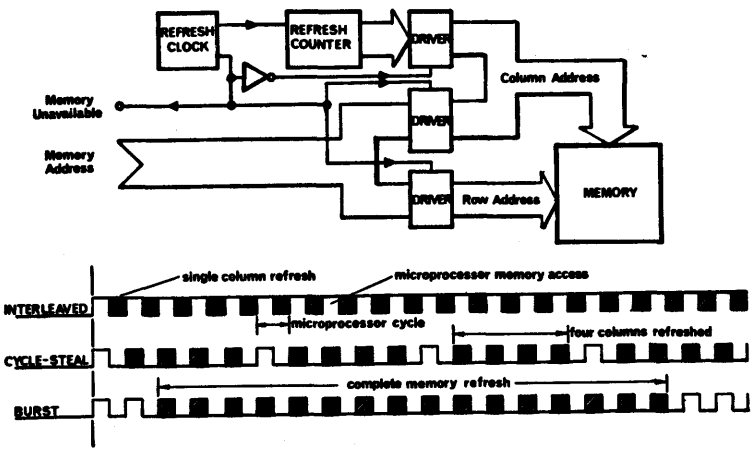

Figure 6-12. Refresh logic and timing

CONTENT-ADDRESSABLE READ/WRITE MEMORY

A content-addressable read/write memory (CAM) is a random-access memory with additional logic included at each memory cell to allow direct comparison of the contents of the cell with externally supplied data. The CAM has three modes of operation:

(i) Read
(ii) Write
(iii) Match

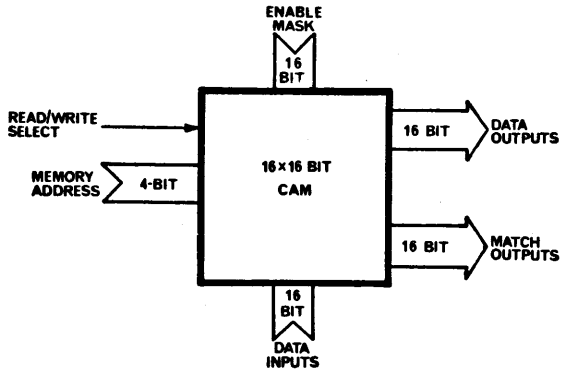

Figure 6-13. 16 x 16-bit content-addressable memory

In the "read" and "write" modes, the CAM functions in the same way as an ordinary random-access read/write memory. In the "match" mode, the additional cell logic is used to compare the information presented at the data input lines with the contents of the addressed memory word. Figure 6-13 shows the external connections to a simple 16 x 16-bit CAM. For each bit of the memory word, the results of the comparison are indicated at the match output lines. The bit enabling mask is used to determine which of the data input lines are to be compared with the contents of the memory word. Disabled data input lines are ignored. With additional external or on-chip logic, more sophisticated CAM's allow the bit comparison process to be made against the contents of every word in the memory in one operation.

The content-addressable memory provides a powerful tool for microprocessor applications involving data search operations.

READ-ONLY MEMORY

A read-only memory (ROM) is an array of memory cells whose contents are predetermined. The stored information is defined by the physical layout of the memory array circuits which then provide an involatile store. Each word of the memory can be accessed at random and its contents read out by selecting a unique binary address. ROM's use both word organised and coincidence

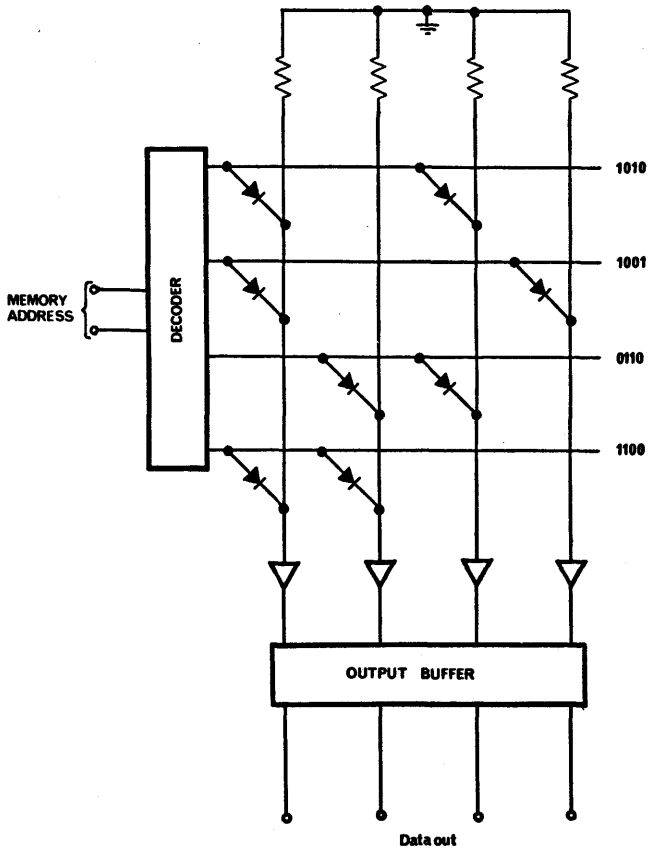

Figure 6-14. 4 x 4-bit diode matrix ROM

addressing schemes to decode the memory address. Although information cannot be written into the memory, the external characteristics of the ROM chip are functionally identical to those of the RAM chip. There are some ROM and RAM chips which are both electrically interchangeable and pin-compatible. The memory cell in a ROM array is simpler than that in a RAM array since its contents are unchangeable. Typically, the basic cell in a ROM array consists of a single diode or transistor. Figure 6-14 shows the layout of a small bipolar diode ROM using word addressing. The presence or absence of a diode at the nodes of the array determines the state of the memory cells. Similarly, the stored information in an MOS transistor ROM is determined by

the presence or absence of an electrical connection between the gate and the row select line at each node of the array, as shown in Figure 6-15. In a bipolar transistor ROM the stored information is determined by the presence or absence of an electrical connection between the emitter and load resistor, as shown in Figure 6-16.

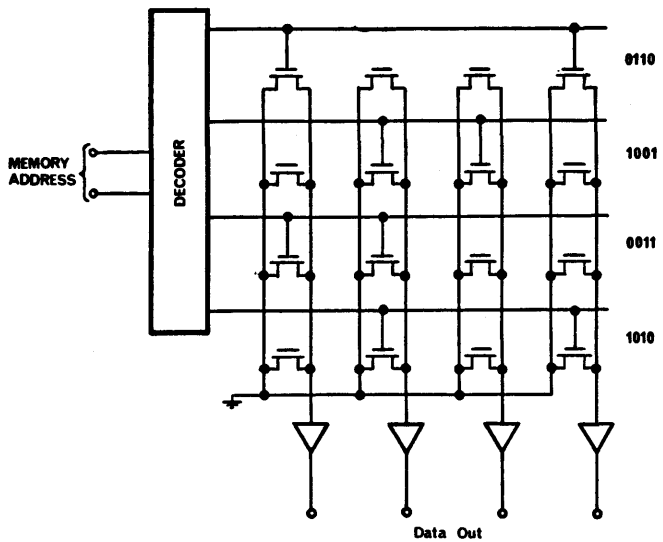

Figure 6-15. 4 x 4-bit MOS ROM

The bit pattern held in the ROM must be defined at the time of manufacture. Either a custom-designed integrated-circuit is manufactured or a standard integrated-circuit is manufactured and programmed at the last stage of fabrication with the desired bit pattern to produce a *mask-programmed* ROM. In the latter process, unconnected diodes or transistors are fabricated at every node position and then a special-purpose metalisation mask is used to interconnect the components according to the specified bit pattern. The mask-programmed ROM offers an economic method of manufacture when quantities are too small to consider custom-designed integrated-circuits.

Typically, single chip bipolar ROM's have 1 kbit capacity and 40ns access time, whilst MOS ROM's have 16 kbit capacity and 400ns access time.

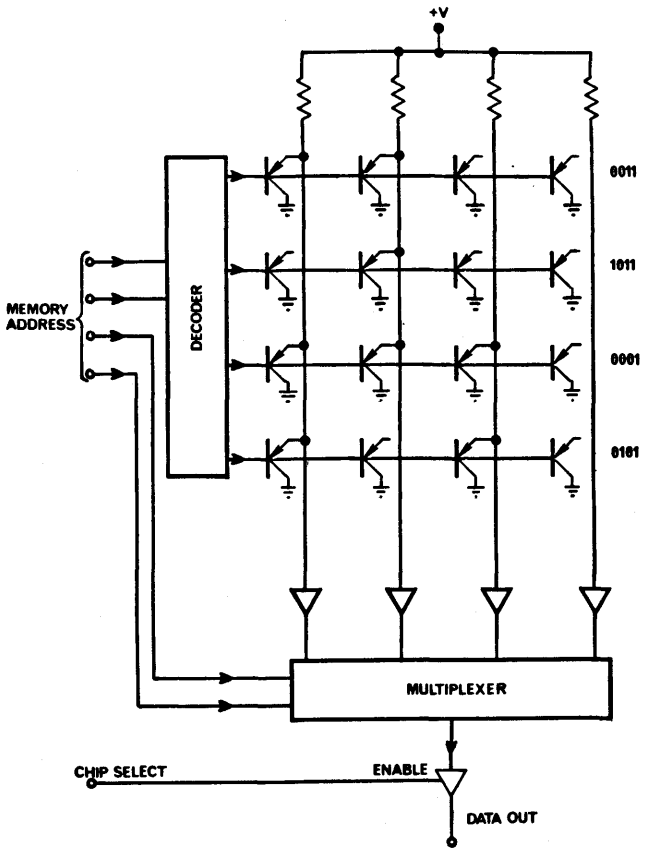

Figure 6-16. 16 x 1-bit bipolar transistor ROM

USER OR FIELD PROGRAMMABLE READ-ONLY MEMORY

The user programmable-read-only-memory (PROM) is a ROM chip whose contents can be specified after manufacture by external application of electrical signals. Two types of PROM's are in common use.

The fusible-link PROM. An integrated-circuit containing a bipolar or MOS ROM array is manufactured with all transistors fully interconnected so that the memory initially stores all 1's or all 0's in each of its cells. As shown in Figure 6-17, a critical interconnection is made at each node position by a fusible metallic or semi-

conductor link. The link can be destroyed to break the connection and change the state of the cell by application of an abnormally large current to the appropriate part of the memory circuit. The state of the cell cannot be modified once the associated link has been fused. The programming operation is performed in a special-purpose *PROM-programmer* which addresses a specified memory word and destroys the fusible links according to the bit pattern specified by the user. The programming of the entire contents of a 1-kbit PROM chip may take several minutes.

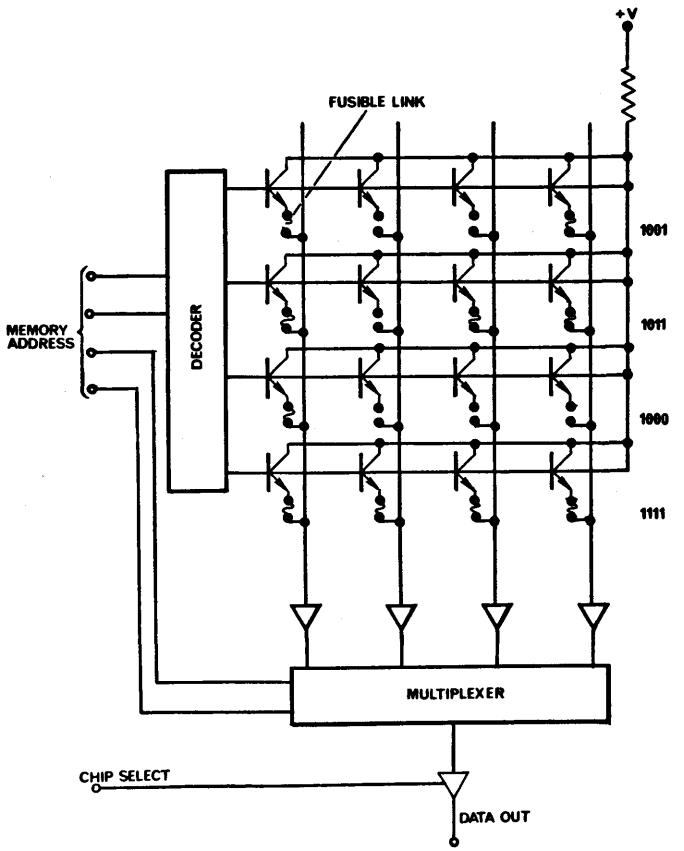

Figure 6-17. 16- x 1-bit fusible link ROM

The avalanche-induced PROM. The avalance-induced PROM is based on a bipolar ROM array and is manufactured with all

transistors fully connected. By applying large external voltages, avalanche breakdown can be induced through the base-emitter diode junction of the transistor in any particular cell. A large reverse current flows, the junction fuses and shorts out the base-emitter connection to change the state of the cell. The programming is performed in a special-purpose PROM programmer as before.

There is some doubt about the long-term stability of user programmable ROM's. Some evidence suggests that it is possible for fused links or transistor junctions to reform by a diffusion process over a long period of time. Reports of such occurrences are not common and manufacturers of PROM's claim reliable operation over several decades.

READ-MOSTLY MEMORY

One type of read-mostly memory which is widely used in microprocessor systems is the user reprogrammable read-only-memory (RePROM). The RePROM is a read-only memory which can be electrically programmed, erased and reprogrammed several times. The most common type is the floating-gate-avalanche-injection MOS (FAMOS) RePROM. In each memory cell the information is stored as the presence or absence of charge on the gate of a MOS transistor. With the power supplies disconnected, or under normal operating conditions, the gate is electrically isolated from the other parts of the circuit and no charge leakage can occur. Unlike the dynamic MOS memory, the FAMOS RePROM can retain the stored information for a long period of time (at least 5 to 10 years). During programming abnormally large voltages are applied to the circuit. Avalanche breakdown of a diode junction allows charge to be injected into the isolated or floating gate of a selected memory cell. The programming operation, which is performed in a special-purpose PROM programmer, might take 2 or 3 minutes to load the contents of an entire RePROM chip. Charge can be released from the floating gate, and the contents of the memory erased, by exposing the circuit to an ultra-violet light source. The integrated-circuit is mounted in a sealed package provided with a quartz window so that the user can erase the memory in the field. The time to complete erasure which depends

on the intensity of the UV light is typically 5 to 15 minutes. The number of times that the erasure and reprogramming operation can be performed successfully, though usually unspecified by the manufacturer, may be limited in practice.

FAMOS RePROM's are available which have capacities as high as 8 kbits/chip and read access times as low as 450ns.

THE PROGRAMMABLE-LOGIC ARRAY

The programmable-logic-array (PLA) is a general-purpose integrated-circuit which includes both read-only and read/write memory cells on the same chip. Initially the chip is fabricated with the various circuit elements unconnected. By specifying a final mask in the fabrication process, the PLA can be interconnected to perform special-purpose memory functions. The incorporation of combinational and sequential logic elements on the same chip provides a flexible and powerful semiconductor memory element.

USES OF MEMORY IN A MICROPROCESSOR SYSTEM

Memories play a fundamental role in all microprocessor systems and have a number of different uses. Each type of application has particular requirements which will determine the most suitable kind of memory. Some more of the important applications are discussed below.

Main-program memory. The size of the main-program memory will vary greatly depending on the microprocessor's application. Typical capacities range from 512 bytes to 16 kbytes. The basic requirements are:

(i) Non-volatile storage
(ii) A read access time compatible with the normal operating speed of the microprocessor.

The most common types of main-program memory are mask-programmed ROM, PROM, RePROM or ferrite core memories. Dynamic MOS RAM with a standby battery power supply to guard against power failure is also used. Programs are often deve-

loped in volatile static RAM chips which are subsequently replaced by pin-compatible PROM chips. RePROM has obvious advantages during program development.

Microprogram or control memory. The control memory of a single chip microprocessor is situated on the microprocessor chip itself. The main requirements are:

(i) Non-volatile storage
(ii) High speed
(iii) Low power consumption
(iv) Small chip area per cell.

The microcode will be stored in a ROM which is designed to meet these requirements and is fabricated using the technology of the microprocessor.

High speed and non-volatility are the important considerations when choosing a suitable external control memory for a bit-slice microprocessor. A mask-programmed bipolar ROM is commonly used.

Scratch-pad data memory. Scratch-pad memory is used as a temporary data or address store during the execution of an instruction or as a short-term intermediate store during the processing of data. In some microprocessors the scratch-pad is structured as a number of internal working registers. The main requirements here are:

(i) High speed
(ii) Low power
(iii) Small chip area per cell.

A dynamic MOS RAM is often used. A microprocessor using dynamic data storage has a minimum system clock frequency to ensure adequate refreshing of the data in the scratch-pad registers. The maximum number of machine cycles which may be stolen during DMA operations is also limited. There are no such restrictions in a microprocessor which uses a static RAM for the scratch-pad memory.

Some microprocessors use an external scratch-pad memory. The most important consideration here is speed and a bipolar static RAM is commonly used.

Main data memory. In most microprocessor applications, the size of the main data memory is small in comparison with the main program memory. In some applications, the internal scratch-pad memory will satisfy the entire data storage requirements. Large capacity high or medium speed data memories are sometimes required in microprocessor-based data acquisition systems where large quantities of data must be stored in relatively short time periods (e.g., a transient event recorder). In these applications MOS static RAM and ferrite core memories are frequently used. MOS dynamic RAM memory systems are also used; in particular, they find application in large capacity memory systems where the total power consumption and heat dissipation can be considerable.

In some systems, a small high-speed memory is used as a buffer store between the microprocessor and the slower large capacity main data store. Blocks of data can be transferred from the main data memory to the buffer or *cache* memory under external control so as to ensure that the high-speed memory always contains the data most relevant to the current microprocessor task. A bipolar static RAM is the obvious choice for cache memories.

Secondary data memory. A secondary memory or "backing store" is used as a long-term semi-permanent data store in a microprocessor system. The main requirements are:

(i) Non-volatile storage
(ii) Large capacity at low cost.

Access times from 5ms to 100ms are usually acceptable. The most common secondary data memories are magnetic tape cassette or magnetic flexible disk stores although the cost of semiconductor recirculating memory systems with battery driven standby supplies is becoming increasingly competitive.

I/O device memory. The microprocessor and its I/O devices usually communicate asynchronously. A temporary data store is often required to hold information during I/O operations. These I/O buffer memories, which are frequently included on the I/O interface chips, are usually of small capacity. In a memory-mapped microprocessor system, the I/O buffer memories are accessed in an identical manner to the main data memory. Most I/O buffer memories are based on the MOS static RAM.

Some output devices require a longer term data store of large capacity (8 or 16 kbytes) to hold the output data whilst it is presented to the outside world. MOS recirculating memories are common in devices which read out the stored data sequentially as, for example, in the character memory in a visual display unit (VDU). MOS static or dynamic RAM is used in I/O devices requiring random access to the stored data as, for example, in the character store of a line-printer.

Table 6-1 summarises the more important characteristics and lists the common applications of the different types of semiconductor memory used in microprocessor systems.

TABLE 6-1. SEMICONDUCTOR MEMORY CHARACTERISTICS

Type	Typical access time	Typical capacity chip	Standby Power	Volatile	Typical application
Recirulating	100μS	16k bits	medium	yes	character store
Bipolar Static RAM	50nS	256k bits	high	yes	scratch-pad
MOS Static RAM	300nS	2k bits	medium	yes	main data store
Dynamic RAM	300nS	4k bits	low	yes	main data store
Bipolar ROM	40nS	1k bits	high	no	control memory
MOS ROM	500nS	16k bits	medium	no	program memory

THE USE OF STATIC RAM IN A VOLATILE READ/WRITE MEMORY SYSTEM

A simplified block diagram of a 2-kbyte memory system is shown in Figure 6-18. The memory array consists of two banks of eight 1k x 1-bit static RAM chips. The ten low order bits of the address bus drive the memory address inputs of each RAM chip in parallel

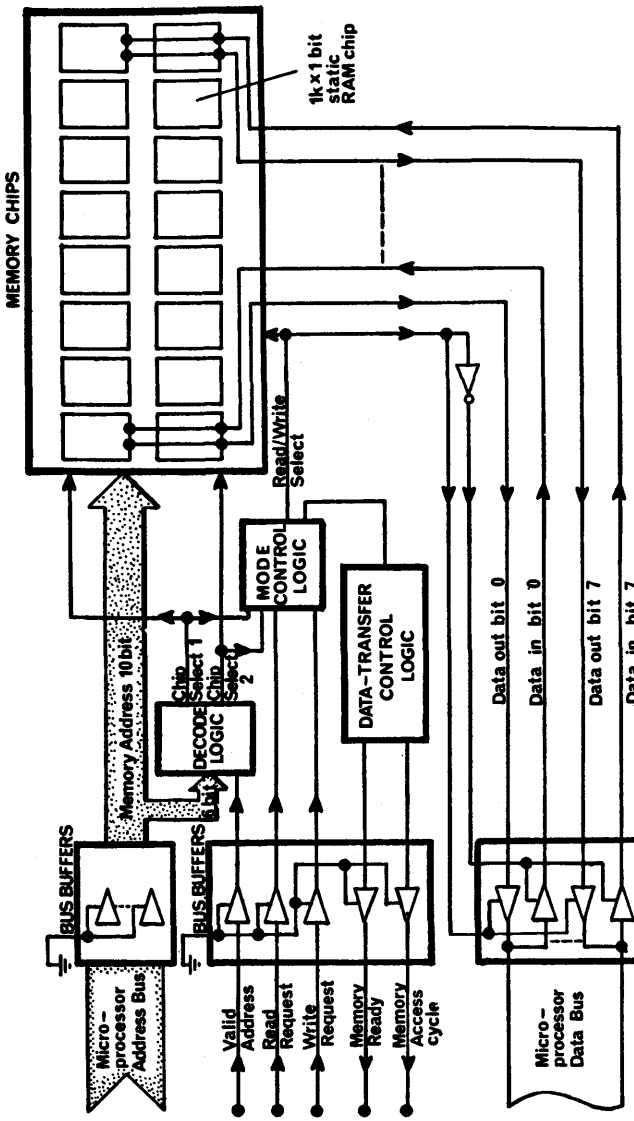

Figure 6-18. 2-kbyte volatile read/write memory system

through a set of bus buffers. The six high order bits of the address bus together with the "valid address" signal are decoded, according to the memory map of the microprocessor, to generate two chip select signals – one for each bank of eight memory chips. The bidirectional data bus is connected to the data-in and data-out lines of each RAM via bidirectional bus drivers. The mode select logic generates the read/write select signals for the RAM chips and controls the direction of data flow through the data bus drivers.

The design and operation of the data transfer control logic will depend upon the speed of the RAM and the requirements of the microprocessor which is connected to the memory. Some microprocessors demand synchronous operation of the memory; others provide for asynchronous operation.

Synchronous memory control. The microprocessor expects the memory to respond to a memory access request within a defined time interval. Data may be lost if the memory cannot respond in the required time. There are three ways of controlling data transfer when using a slow memory:

(i) The frequency of the system clock is reduced until the microprocessor and memory operating speeds are compatible. Additional data transfer control logic is not required.

(ii) The system clock period is lengthened during each memory access operation. The data transfer control logic generates a ' slow down" signal which causes the temporary reduction in the system clock rate.

(iii) Memory data transfer is treated in the same way as I/O data transfer under program or interrupt control. The data transfer control logic responds to and provides the necessary control signals to interact with the microprocessor during input-output operations.

Asynchronous memory control. After it has requested memory access, the microprocessor pauses with its operation suspended until a "memory ready" signal is received from the memory system. The data transfer control logic generates the "memory ready" signal from a delayed version of the "memory read/write request" signal. The delay is adjusted to suit the particular access time of the memory chips.

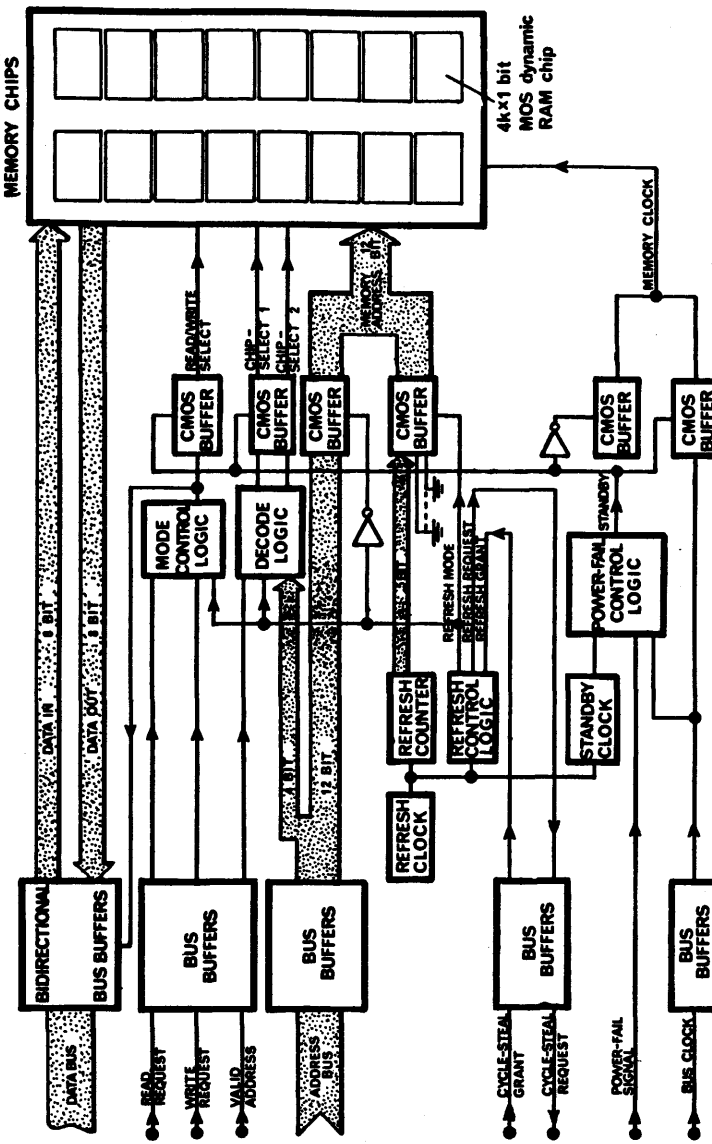

Figure 6-19. 8-kbyte non-volatile read/write memory system

THE USE OF DYNAMIC RAM IN A NON-VOLATILE READ/WRITE MEMORY SYSTEM

A simplified block diagram of a 4-kbyte memory system is shown in Figure 6-19. The system may be considered in the four sections given below.

The memory array. The array consists of two banks of eight 4k x 1-bit dynamic RAM chips. Each chip is organised as a 32-column by 128-row matrix of cells with the column address generated from the lower 5 bits of the memory address. Refresh is achieved by addressing a particular column of cells and initiating a memory-write operation with the chip select disabled. Each of the 32 columns of memory cells requires refreshing every 2ms.

Chip select and address decoding. During normal memory access operations, the twelve low order bits of the address bus drive the memory address inputs of each RAM chip. The four high order bits of the address bus, together with the "valid address" signal, are decoded to generate the two chip select signals.

During refresh, the column address is generated by the refresh counter, both of the chip select lines are disabled, and the memory write mode is selected.

During power failure, CMOS low-power buffers are used to isolate the memory array from the control signals which are normally derived from the microprocessor bus. The address multiplexer and other parts of the circuit which must remain active during a power failure are also realised using CMOS technology.

Refresh control. Refresh is performed on a cycle-steal basis, one column at a time, under control of the refresh control logic. The refresh clock increments the refresh counter and initiates a new refresh operation every 62.5μs. After gaining control of the memory by raising the refresh request signal, the control logic disables the chip select lines and initiates a memory-write operation using the contents of the refresh counter as the memory address. Memory control is then handed back to the microprocessor. The refresh logic, which must operate during power failure, is realised using CMOS circuitry.

Power-fail detection and control. The power-fail line is activated immediately a failure in the main power supplies of the microprocessor system is sensed. The power-fail logic allows completion of any current memory access or refresh operation before generating the "standby" signal which disables the chip and read/write select buffers and connects the standby clock to the memory array. The memory refresh control logic continues to operate normally as it derives its power from the standby supply. The total power consumption of the memory system during power failure is typically 200mW. If it obtains all voltage levels from a single 12-volt battery of 4.5 amp-hours capacity, the memory system could be supported in standby-mode for some 8 or 9 days.

SUMMARY

This chapter has presented an overview of memory systems rather than a detailed description of how they work. Hopefully it provides the microcomputer system designer with a guide to the various technologies at his disposal and some insight into their specific capabilities. For a more detailed description of memory technology the reader is referred to the bibliography at the end of this book.