SECTION VIII

FREQUENCY DOMAIN FUNCTIONS: PHASE LOCKED LOOPS

FREQUENCY DOMAIN FUNCTIONS: PHASE LOCKED LOOPS

BASIC PHASE LOCKED LOOP

PHASE DETECTORS:
Double Balanced Mixer, Digital Phase/Frequency Detector

PHASE DETECTION USING THE AD9901 PHASE/FREQUENCY DISCRIMINATOR

PLL MATHEMATICS AND DESIGN BASICS

USING THE AD9901 IN A PLL

USE OF DUAL MODULUS PRESCALERS

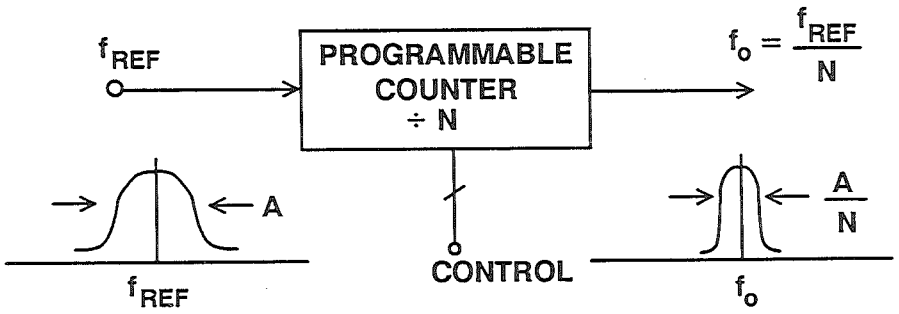
BASIC PHASE-LOCKED LOOP

High purity reference frequencies are key elements in communications equipment, radar systems, and instrumentation. Crystal oscillators followed by suitable filtering provide signals which have excellent stability and purity coupled with very low phase noise. Unfortunately, this requires one crystal oscillator per frequency, and hence this approach soon becomes expensive and bulky.

Frequency division is one technique commonly used to generate frequencies which are less than or equal to a single reference frequency. Prescalers, counters, and dual modulus type digital circuits are all in common use and available in silicon ICs. Galium arsenide digital circuits operate at frequencies up to about 2 GHz. High speed prescalers can be used ahead of conventional silicon circuits to provide cost effective solutions to high speed frequency division.

Digital frequency dividers are often treated as "noise-less" devices since the phase noise in the reference source is almost always greater than that of the divider itself.

Frequency dividers reduce the reference frequency in proportional steps, 1/2, 1/3, 1/4, 1/N. They also tend to proportionally compress the phase spectra as shown in Figure 8.1.

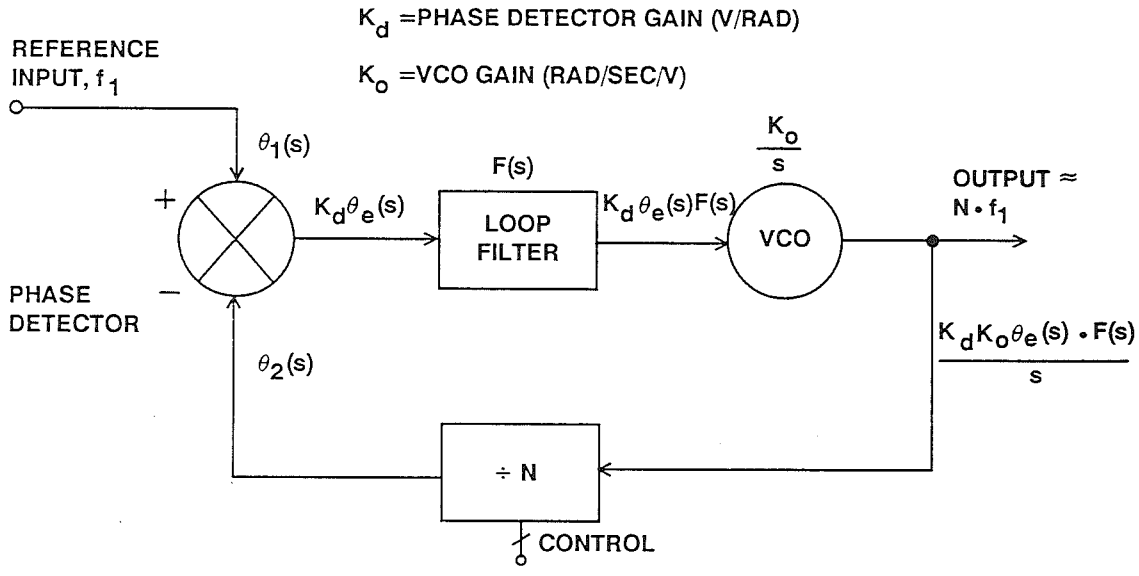


PROGRAMMABLE FREQUENCY DIVISION

Figure 8.1

The phase locked loop (PLL) as shown in Figure 8.2 makes use of a programmable frequency divider in the feedback loop to produce an output frequency which is a multiple of the input frequency. The basic elements of a PLL are the reference input source, loop filter, voltage controlled oscillator (VCO), digital divider, and the phase detector. Each element has a transfer function which can be expressed using Laplace transforms. The basic PLL is analyzed using standard feedback control theory as will be discussed later in this section.

In the most basic PLL, the divided VCO signal is compared to a reference frequency in the phase detector to generate an error signal which will retune the VCO so as to track the reference signal. Since the phase detector is really a multiplier, it produces a sum frequency component as well as a difference component. The loop filter eliminates the sum component as well as any out of band interfering signals present at the input. The proper loop filter design for a given PLL application involves a fairly complex series of tradeoffs and is the subject of much of the material contained in the recommended references at the end of this section. An elementary treatment of loop filter design is contained in this section.



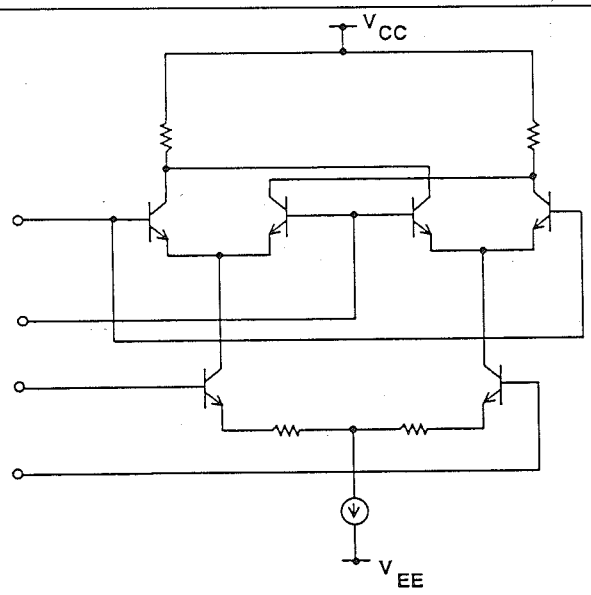
BASIC PHASE LOCKED LOOP

Figure 8.2

PHASE DETECTORS

The purpose of the phase detector is to generate an error signal which is used to retune the oscillator should its output deviate from the reference input signal. The two most common phase detector implementations are the analog mixer and a family of sequential logic circuits known as digital phase detectors.

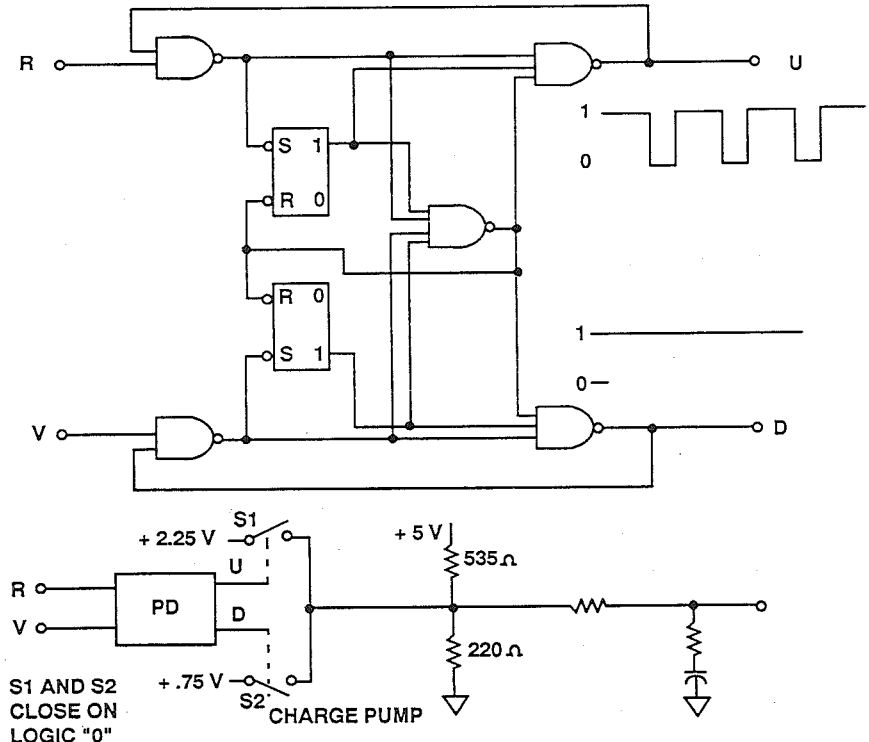
The phase detector is basically a double balanced analog mixer which has good noise rejection and phase response. A typical circuit implementation is shown in Figure 8.3. The phase detector has several important limitations when used in PLL applications. First, large steps in the loop frequency may cause the PLL to unlock and not regain lock. Second, the PLL may never achieve lock upon power up if the VCOs free running frequency is far enough away from PLLs operating frequency. Third, the PLL may lock on a harmonic of the VCO frequency.



DOUBLE BALANCED MIXER/PHASE DETECTOR
Figure 8.3

The digital phase/frequency detector circuit shown in Figure 8.4 solves many of the problems associated with the analog phase detector. The digital phase/frequency detector first pulls the VCO frequency close to the reference frequency. At this point, phase acquisition takes over and phase lock is achieved. This type of phase/frequency detector circuit has been implemented in IC form, such as the Motorola MC-4044, but also suffers from several limitations. Loop lockup occurs when all the negative transitions on R (the reference input) and V (the feedback input) coincide. Under these conditions both outputs U and D remain high. Unfortunately, this results in a so-called "dead zone" at phase lock which results in an increase in phase noise. When the input phases are differ-

ent, one output pulses, while the other output is locked low. The average value of the pulsating output waveform is proportional to the phase difference between the two inputs. This implies that the phase detector outputs must either drive a charge pump as shown in Figure 8.4 or a differential filter. This is required to convert the noncomplementary differential output to a single ended output suitable for driving the VCO. Figure 8.5 shows a typical phase gain plot for the Motorola MC-4044 when driving its internal charge pump. Although the dead zone at 0° phase difference may be avoided by offsetting the VCO input voltage by an appropriate amount, this results in a decrease in the linear phase detection operating range.



DIGITAL PHASE/FREQUENCY DETECTOR AND CHARGE PUMP

Figure 8.4

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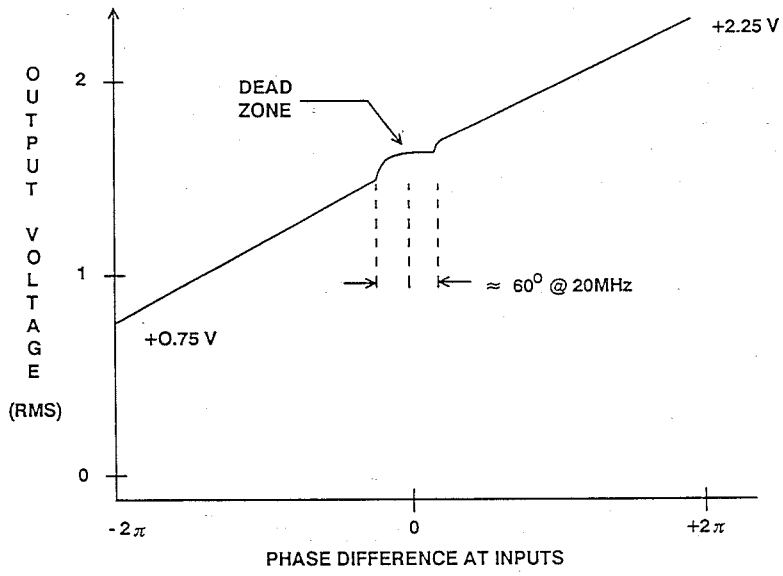


PHASE GAIN PLOT FOR DIGITAL PHASE/FREQUENCY DETECTOR AT 20MHz

Figure 8.5

PHASE DETECTION USING THE AD9901 PHASE/ FREQUENCY DISCRIMINATOR

The AD9901 is a digital phase detector. Figure 8.6 shows the straightforward sequential logic design of the AD9901. The main components include four "D" flip-flops, an exclusive-OR gate (XOR), and some combinational output logic. The circuit operates in two distinct modes; as a linear phase detector, and as a frequency discriminator. When the reference and oscillator are very close in frequency, only the phase detection circuit is active. If the two inputs are substantially different in frequency, the frequency discrimination circuit overrides the phase detector portion to drive the oscillator frequency toward the reference frequency.

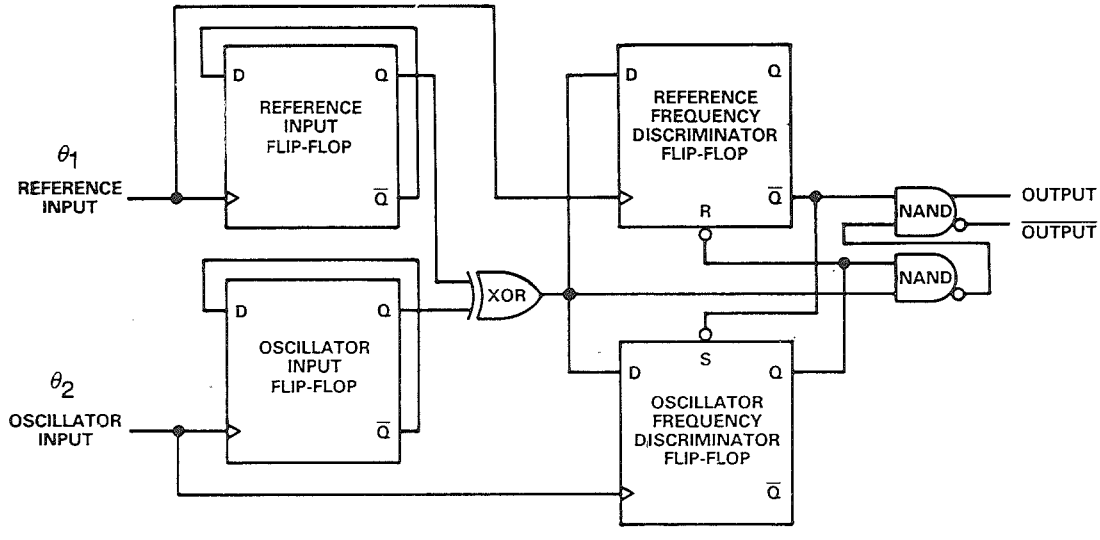
Its input signals are pulse trains, and its output duty cycle is proportional to the phase difference of the oscillator and reference inputs. Figures 8.7, 8.8 and 8.9 illustrate the input-output relationships at lock, with oscillator leading, and oscillator lagging respectively. This output pulse train is low-pass filtered to extract the mean value $K_d(\theta_1 - \theta_2)$, where K_d is a proportionality constant (phase gain).

At or near lock (Figures 8.7, 8.8 and 8.9) only the two input flip-flops and the exclusive-OR gate are active. The input flip-flops divide both reference and oscillator inputs by two. This insures that the inputs to the exclusive-OR are square waves, no matter what the input duty cycles might be. When the two square-waves are combined by the XOR, an output with 50% duty cycle results when the reference and the oscillator inputs are 180° out of phase. Any shift in the phase relationship of the input signals results in

a change in the output duty cycle. Near lock, the frequency discriminator flip-flops provide constant HIGH levels to gate the XOR output to the final output.

Near lock, the duty cycle of the AD9901 is a direct measure of the phase difference between the two input signals. The transfer function can be stated as $[K_d(\theta_1 - \theta_2)]$(V/rad), where K_d is the output voltage range of the AD9901 divided by 2π • (1.8V/2π = .285V/rad). Figure 8.10 shows the relationship of the mean value of the AD9901 output as a function of the phase difference of the two inputs. It is important to note that the slope of the transfer function is constant near its midpoint and does not exhibit the "dead zone" characteristic of other digital phase detectors (see Figure 8.5). The AD9901 avoids this "dead zone" by shifting it off to the endpoints of its transfer curve as indicated in Figure 8.10. The increasing gain at either end increases the effective error signal to pull the oscillator back into the linear region. This does not affect phase noise which is far more dependent upon lock region characteristics. It should be noted, however, that as frequency increases, the linear range is decreased. This effect is caused by the fixed propagation delay through the phase detector. This fixed delay is nominally 3.6 nsec. Therefore, the typical detection range can be found using the following equation:

$$\text{Detection Range} = F \cdot 360^\circ \left[\frac{1}{F} - 3.6\text{ns}\right].$$



AD-9901 PHASE/FREQUENCY DISCRIMINATOR BLOCK DIAGRAM

Figure 8.6

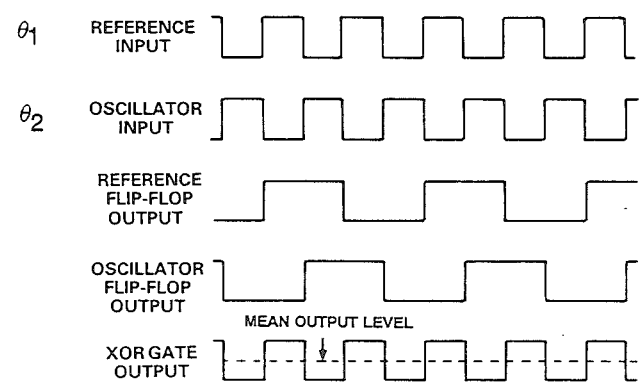
As an example, this yields 100° linear phase detection range for F = 200 MHz.

Away from lock, the AD9901 becomes a frequency discriminator. If the reference frequency and the oscillator frequency are significantly different, the appropriate Discriminator Flip-Flop Output Frequency will be clocked to logic LOW. This overrides the XOR output and holds the output at the appropriate level to pull the oscillator toward the reference frequency. Once the frequencies are within the linear range, the phase detector circuit takes over again. Because the AD9901 combines a frequency discriminator with the phase detector, the possibility of locking to a harmonic of the reference is eliminated.

The AD9901 can operate with ECL inputs when using a single -5.2V supply or TTL/CMOS when using a single +5V supply. A current setting resistor controls the current in the open collector differential pair output stage. The open collector outputs allow flexibility in varying the output voltage swing to match the amplifier and loop filter requirements. A functional circuit diagram of the AD9901 configured for TTL and ECL mode operation is shown in Figure 8.11. In the TTL mode, the output voltage swing is nominally +3.4V to +5V. In the ECL mode, the output voltage swing is nominally -1.8V to 0V. The output stage current is controlled by an external R_{SET} resistor, where $I_{LOAD} = 0.47V/R_{SET}$. Nominally R_{SET} = 47.5 ohms and R_{LOAD} = 182 ohms will yield an output voltage swing of 1.8Vp-p.

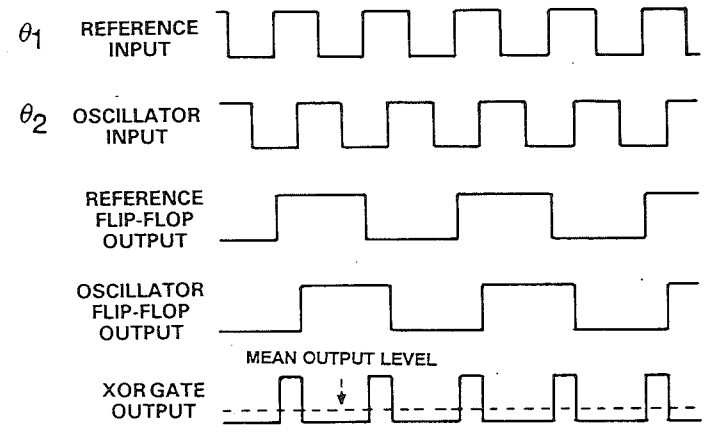
Since the AD9901 has complementary differential outputs, it can be used either single-ended or differentially. The output can be filtered with a passive filter thereby eliminating the need for a high frequency op amp, or the AD9901s output can be used in a fully differential mode.

Another shortcoming of previous phase detectors was the output stability over temperature. This has been eliminated in the AD9901 as has been previously described by the use of an internal bandgap reference in conjunction with external R_{SET} and R_{LOAD} resistors to control the output voltage swing. This gives a stable output voltage swing over temperature thus making a single ended output an alternative to a differential output.



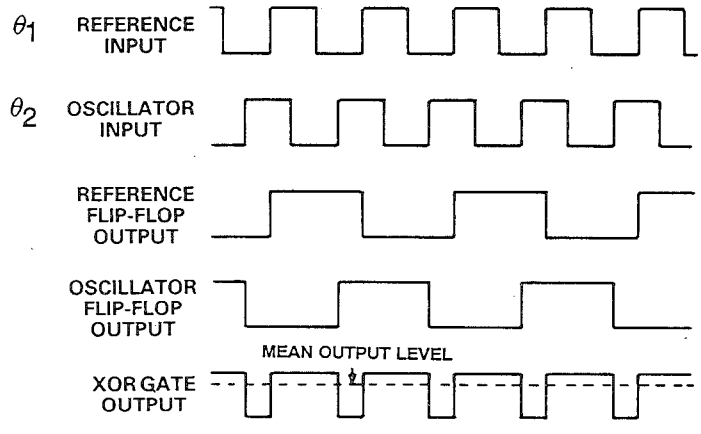
AD-9901 TIMING WAVEFORMS AT "LOCK"

Figure 8.7



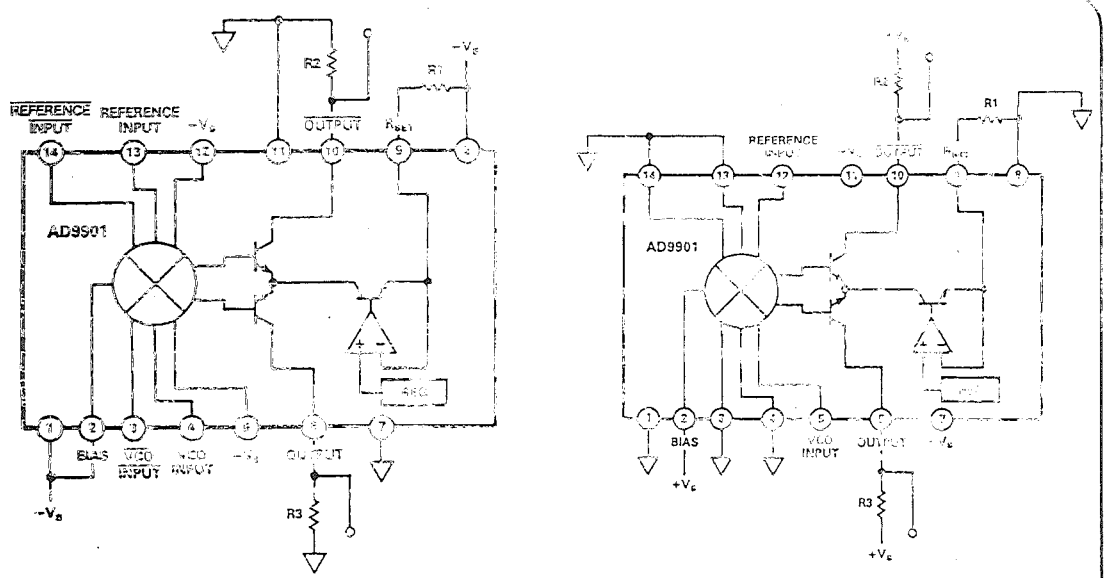
AD-9901 TIMING WAVEFORMS θ_1 LEADS θ_2

Figure 8.8



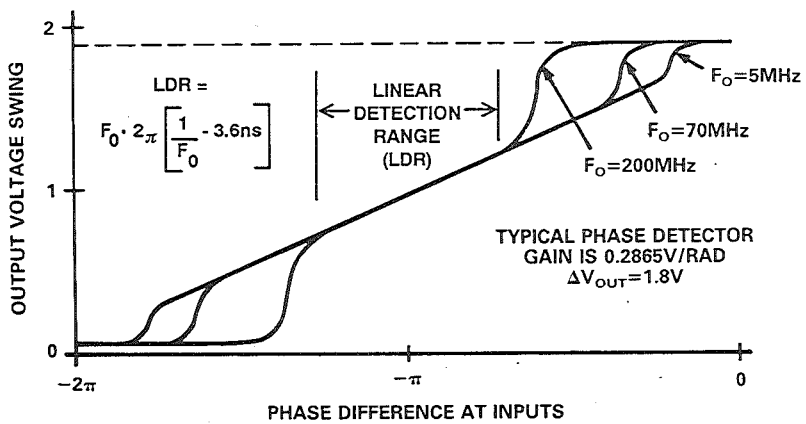
AD-9901 TIMING WAVEFORMS, θ_1 LAGS θ_2

Figure 8.9



ECL/TTL CONFIGURATIONS FOR AD-9901

Figure 8.10



PHASE GAIN PLOT FOR AD-9901

Figure 8.11

PLL MATHEMATICS AND DESIGN BASICS

PLLs are analyzed using feedback control theory with Laplace transforms used to represent transfer functions of the various elements in the loop. Refer to Figure 8.12 and obtain:

Phase error, $\theta_e(s)$:

$$\theta_e(s) = \theta_1(s) - \theta_2(s) \qquad (1)$$

$$\theta_2(s) = \frac{K_d K_o \cdot \theta_e(s) \cdot F(s)}{Ns} \qquad (2)$$

Combine (1) and (2) and solve for the phase error transfer function, $\frac{\theta_e(s)}{\theta_1(s)}$:

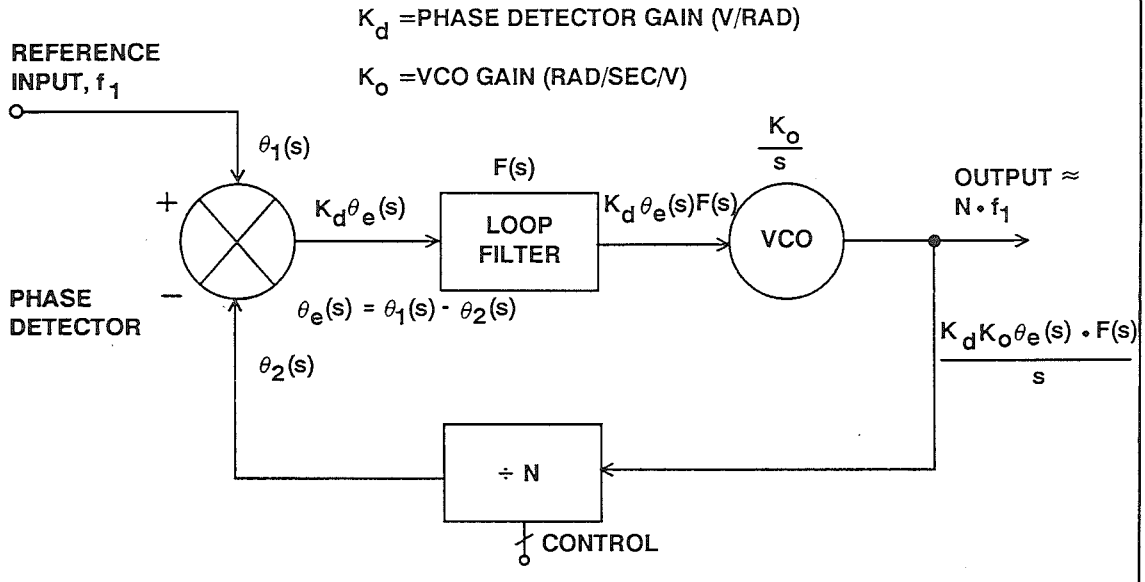
$$H_e(s) = \frac{\theta_e(s)}{\theta_1(s)} = \frac{Ns}{Ns + K_d K_o \cdot F(s)} \qquad (3).$$

Combine (2) and (3) and solve for the phase transfer function, $\frac{\theta_2(s)}{\theta_1(s)}$:

$$H(s) = \frac{\theta_2(s)}{\theta_1(s)} = \frac{K_d K_o F(s)}{Ns + K_d K_o F(s)} \quad , \quad (4)$$

where

K_d = Phase Detector Gain (V/rad)
K_o = VCO Gain (rad/sec/V)
F(s) = Loop Filter Transfer Function
N = Integer Divisor



BASIC PHASE LOCKED LOOP

Figure 8.12

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From the phase transfer function H(s), it is obvious that the basic loop without a filter is a first order (one pole) system. Let F(s) = 1 (i.e., an all pass filter), and

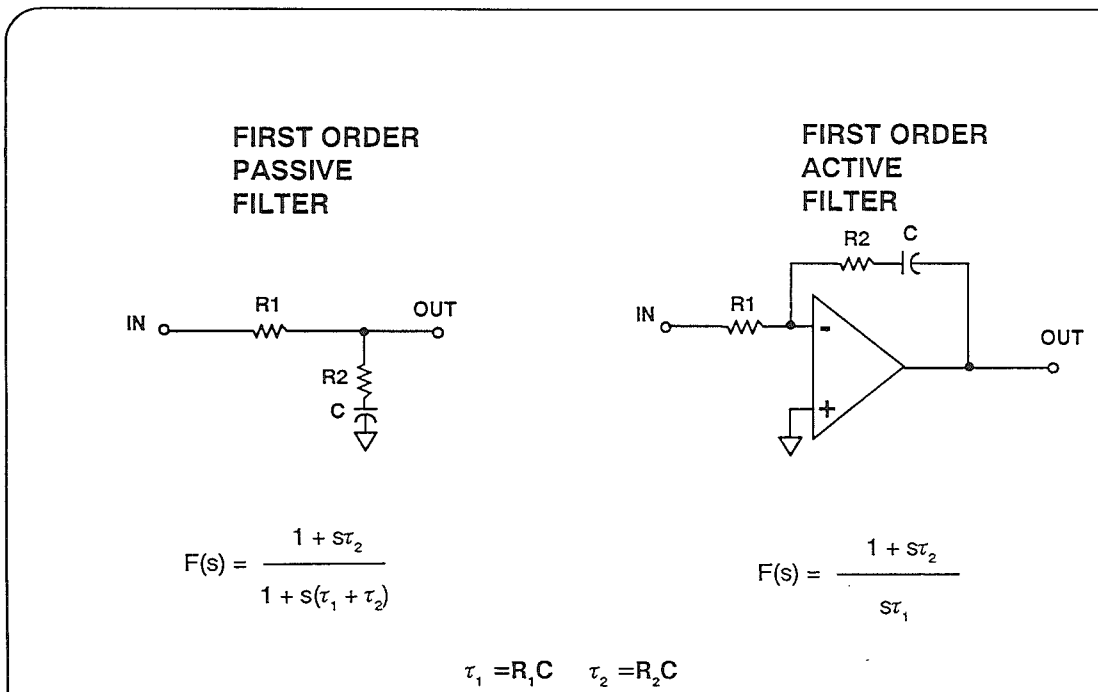
$$H(s) = \frac{K_d K_o}{Ns + K_d K_o}$$

Therefore, if we introduce a one pole loop filter, it is obvious that the PLL system becomes a second order system.

The most popular loop configuration is the second order loop, which is technically stable under all conditions. The second order loop gets one pole from the VCO and one pole from the loop filter. With the second order loop, the phase detector output is filtered before being used to control the VCO, thereby greatly reducing reference frequency sidebands in the VCO output.

Higher order loops should be used with caution since they become very difficult to stabilize. In fact, a second order loop can become unstable due to high frequency parasitics which may increase the loop order unintentionally.

The transfer functions F(s) are given in Figure 8.13 for the most popular passive and active first order loop filters, each having one pole and one zero. Recall that a first order loop filter will produce a second order unconditionally stable PLL.



FIRST ORDER PASSIVE AND ACTIVE LOOP FILTERS USED IN SECOND ORDER PLLs

Figure 8.13

The basic analysis and design of a PLL now centers around the optimization of the loop filter transfer function F(s) for the desired PLL characteristics. If the values of F(s) for the passive and active case from Figure 8.13 are substituted in the equation for H(s), we obtain the following results:

PASSIVE LOOP:

$$H_p(s) = \frac{N_p(s)}{s^2 + 2\delta\omega_n s + \omega_n{}^2} \quad \text{, where}$$

$$\omega_n = \left[\frac{K_o K_d}{N(\tau_1 + \tau_2)}\right]^{\frac{1}{2}} =$$

natural frequency

$$\delta = \frac{1}{2}\left[\frac{K_o K_d}{N(\tau_1 + \tau_2)}\right]^{\frac{1}{2}}\left(\tau_2 + \frac{N}{K_o K_d}\right) =$$

damping factor

$N_p(s)$ = Numerator Function of s

ACTIVE LOOP:

$$H_A(s) = \frac{N_A(s)}{s^2 + 2\delta\,\omega_n s + \omega_n 2} \quad \text{, where}$$

$$\omega_n = \left(\frac{K_o K_d}{N\tau_1}\right)^{\frac{1}{2}} =$$

natural frequency

$$\delta = \frac{\tau_2}{2}\left(\frac{K_o K_d}{N\tau_1}\right)^{\frac{1}{2}} =$$

damping factor

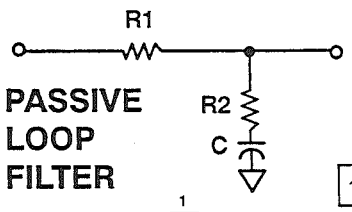
$N_A(s)$ = Numerator Function of S

The above equations were obtained by writing the transfer functions in normalized form as is often done in filter design. The natural frequency of the PLL (ω_n) is the frequency of a damped oscillation caused by a transient input. The damping factor of the PLL (δ) in conjunction with the natural frequency (ω_n) are the traditional servo loop parameters which dominate the PLL control voltage response characteristics. If $\delta = 1$, the system is critically damped. If $\delta < 1$, the system becomes oscillatory and tends to overshoot. In most practical systems, an optimally flat frequency-transfer characteristic is the goal. This implies $\delta = 1/\sqrt{2} \approx 0.7$. If $\delta >> 1$, the transfer function flattens out, and the dynamic response becomes sluggish. The second order PLL is actually a low pass filter for input signals whose frequency spectrum is between zero and approximately the natural frequency ω_n. This means that a second order PLL is able to track for phase and frequency modulations of the reference signal as long as the modulation frequencies remain within an angular frequency band roughly between zero and ω_n. Damping curves which show the relationship between ω_n, phase error and δ are given in Reference 2, p. 49 (Gardner). It should be noted, however, that these curves assume that $K_o K_d >> \omega_n$, the criterion for a high gain loop.

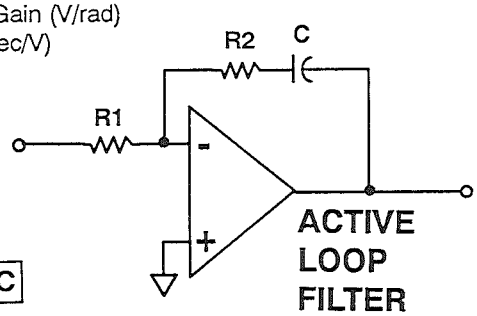
SECOND ORDER PLL DESIGN EQUATIONS

$$H(s) = \frac{\theta_2(s)}{\theta_1(s)} = \text{PHASE TRANSFER FUNCTION} = \frac{\text{NUMERATOR (s)}}{s^2 + 2\delta\omega_n s + \omega_n^2}$$

ω_n = Natural Frequency
δ = Damping Factor
K_d = Phase Detector Gain (V/rad)
K_o = VCO Gain (rad/sec/V)
N = Integer Divisor



PASSIVE LOOP FILTER



ACTIVE LOOP FILTER

$\tau_1 = R_1C \quad \tau_2 = R_2C$

$$\omega_n = \left[\frac{K_oK_d}{N(\tau_1 + \tau_2)}\right]^{\frac{1}{2}}$$

$$\delta = \frac{\omega_n}{2}\left[\tau_2 + \frac{N}{K_oK_d}\right]$$

If $K_oK_d >> \omega_n$
$K_oK_d\tau_2 >> N$
$\tau_1 >> \tau_2$

$$\omega_n \simeq \left(\frac{K_oK_d}{N\tau_1}\right)^{\frac{1}{2}}$$

$$\delta \simeq \frac{\omega_n\tau_2}{2}$$

$$\omega_n = \left(\frac{K_oK_d}{N\tau_1}\right)^{\frac{1}{2}}$$

$$\delta = \frac{\omega_n\tau_2}{2}$$

Figure 8.14

If $K_oK_d >> \omega_n$, and $K_oK_d\tau_2 >> 1$ (the criteria for a high gain passive loop), then the equations for ω_n and δ reduce to those of the active loop:

Active/Passive Loop, $K_oK_d >> \omega_n$
$K_oK_d\tau_2 >> N$
$\tau_1 >> \tau_2$

$$\omega_n \simeq \left(\frac{K_oK_d}{N\tau_1}\right)^{\frac{1}{2}}$$

$$\delta \simeq \frac{\tau_2}{2}\left(\frac{K_oK_d}{N\tau_1}\right)^{\frac{1}{2}} = \frac{\tau_2\omega_n}{2}$$

If the PLL is used for frequency synthesis, the damping factor δ is a function of the divider ratio N. If the divider ratio is variable in the range $N_{MIN} \le N \le N_{MAX}$,

$$\frac{\delta_{MAX}}{\delta_{MIN}} = \sqrt{\frac{N_{MAX}}{N_{MIN}}}$$

If N is changed by a factor of 100, δ varies by a factor of 10, which would be intolerable. The PLL would be underdamped or overdamped at the limits of its frequency range. In such applications, the loop filter time constants have to be switched in accordance with the instantaneous value of N in order to achieve a damping factor in the approximate range between 0.5 and 1.

USING THE AD9901 IN A PLL

A PLL which multiplies a 56 MHz reference frequency input to 112 MHz is shown in Figure 8.15. A FET Colpitts oscillator was chosen along with two MV1404 varactor diodes and a 100nH coil in the circuit shown. For this circuit, the output frequency versus varactor diode reverse bias voltage is plotted in Figure 8.16 (data obtained experimentally). Note that an operating point of 5.5V is optimum for an output frequency of about 110 MHz. The VCO gain can be calculated from Figure 8.16.

$$K_o = 115 \times 10^6 \text{ rad/sec/V.}$$

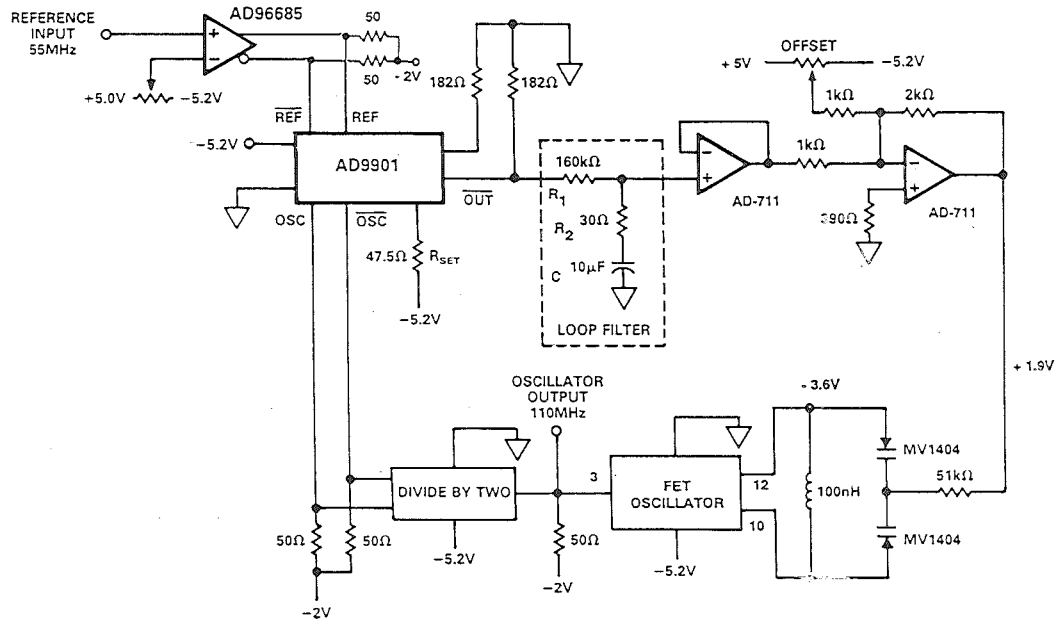
An output swing of 1.8V is chosen for the AD9901 operating in the ECL mode. R_{SET} is chosen to be 47.5Ω such that the output current is 9.9mA. With a 182Ω output resistor, the output swing is 1.8V. This low value for R_{LOAD} assures that the parasitic pole associated with the output capacitance of the AD9901 is minimized. The phase detector gain is next calculated:

$$K_d = \frac{1.7V}{2\pi \text{ rad}} = 0.286V/\text{rad}$$

Because the phase detector is used in ECL mode, its output swing is -1.8V to 0V. At phase lock, the nomimal mean output is therefore -0.9V. This must be matched to the VCO input range.

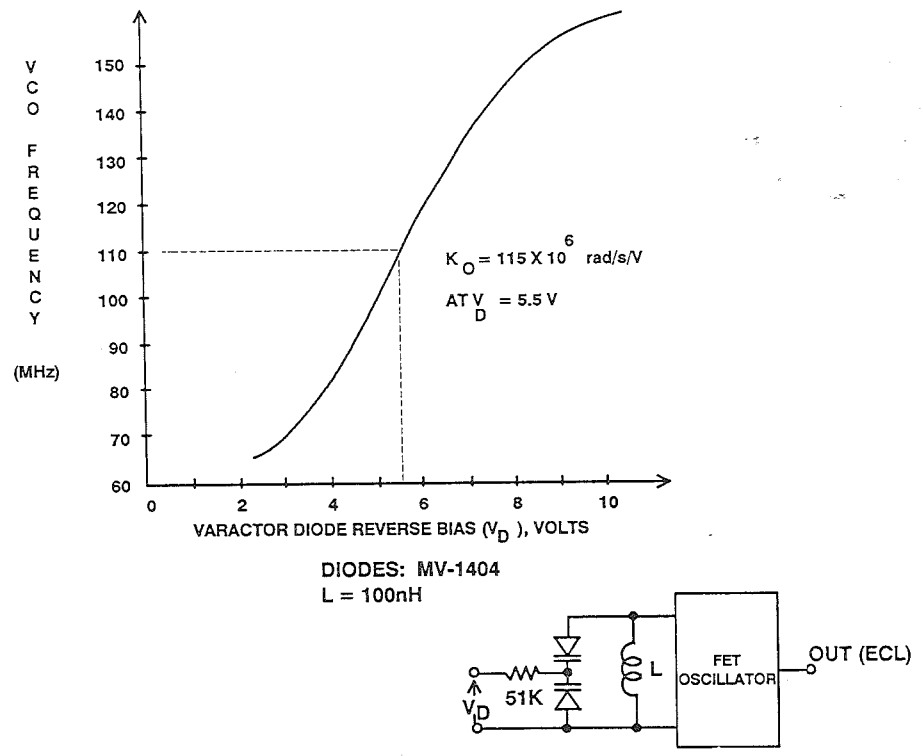
The optimum varactor diode reverse bias voltage was determined to be +5.5V for an output frequency of 110 MHz. The nominal input voltage for the FET oscillator is -3.6V. The input voltage to the 51kΩ resistor required to maintain the 5.5V varactor diode reverse bias is +5.5 - 3.6 = +1.9V.

8



PLL USING AD-9901 PHASE/FREQUENCY DISCRIMINATOR

Figure 8.15



VCO CHARACTERISTICS

Figure 8.16

Since the mean value of the AD9901 at lock is -0.9V, an inverting gain stage of -2 is used after the unity gain follower stage. An offset adjustment is provided to allow the user to vary the phase of the output signal versus the input signal. This is an easy way for the user to check the output linearity of the phase detector.

Another advantage of the complementary differential outputs of the AD9901 is the designer can choose which output (either increasing or decreasing) is correct for the application. Since an inverting gain stage was used, the inverting AD9901 output was chosen. This inverts the signal before the gain stage corrects the signal polarity.

A passive loop filter having a single pole is used to produce a second order PLL. The output of the loop filter is buffered by a unity gain follower before going to the inverting gain stage.

The final stage of the design is to calculate the natural frequency ω_n and the damping factor δ. From the damping curves, a damping factor of 0.7 allows the loop to settle to within 5% of its final value within one millisecond with less than 25% overshoot.

From the set of damping curves, p. 49, Ref. 2

$$\omega_n t = 4.5$$

For t = 1ms

$$\omega_n = 4.5 \text{ KHz}$$

The gain of the inverting stage is then lumped into the phase detector gain to give

$K_d = 0.286\text{V/rad} \times 2 = 0.572\text{V/rad.}$

With $K_o = 115 \times 10^6$ rad/sec/V, the equations

$$\omega_n \approx \left(\frac{k_o k_d}{N\tau_1}\right)^{\frac{1}{2}} \quad \text{and}$$

$$\delta \approx \frac{\tau_2 \omega_n}{2} \quad \text{with N = 2,}$$

are solved for τ_1 and τ_2 yielding:

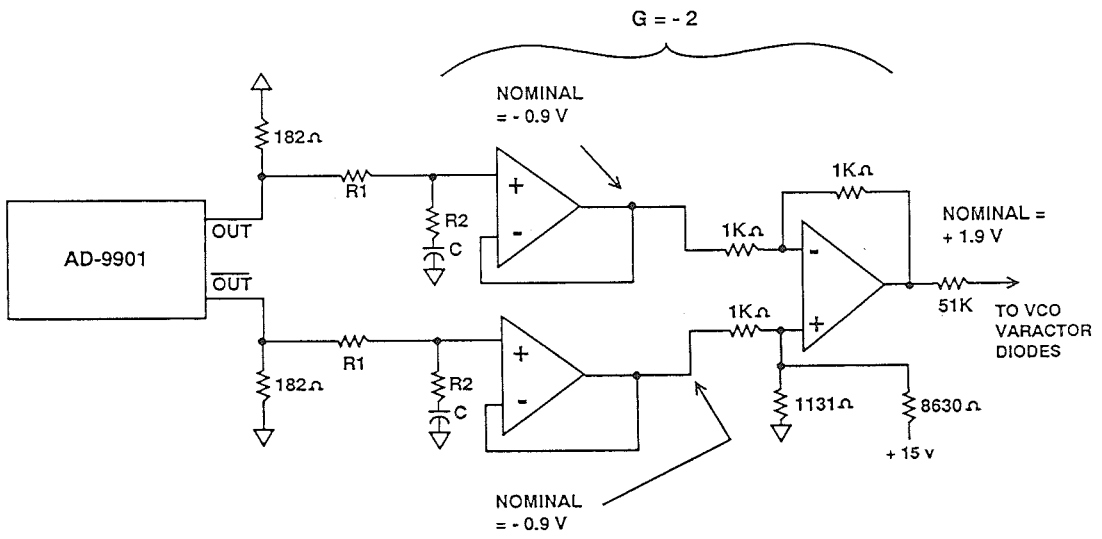
$\tau_1 = 1.624 \text{ sec} = R1 \cdot C$
$\tau_2 = 311 \times 10^{-6} \text{ sec.} = R2 \cdot C$

The following values are chosen for R1, R2 and C:

$C = 10\mu F$
$R1 = 160k\Omega$
$R2 = 30\Omega$

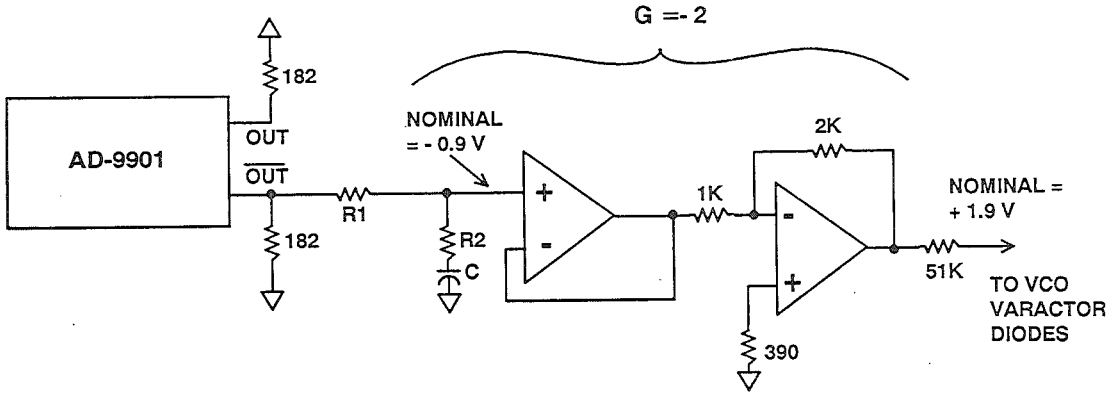
The design is now complete.

The outputs of the AD9901 can be used in the single ended or differential mode. Figure 8.17 shows the single ended configuration while Figure 8.18 shows the differential connection.



AD-9901 USED IN DIFFERENTIAL OUTPUT MODE

Figure 8.17



AD-9901 USED IN SINGLE-ENDED OUTPUT MODE

Figure 8.18

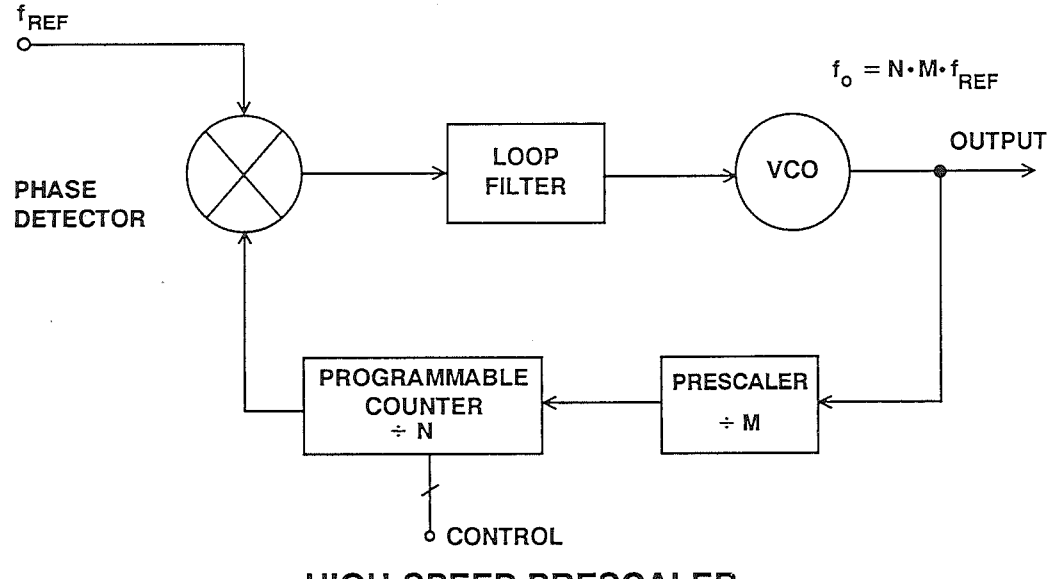
USE OF DUAL MODULUS PRESCALERS

In a PLL which does not use fractional division techniques (such as pulse swallowers), the output frequency is limited to integer multiples of the reference frequency, i.e., $f_o = N \cdot f_{REF}$. Flexible programmable counters can perform this function but often must be preceded by higher speed dividers called prescalers which bring the VCO frequency into the range of the programmable counter as shown in Figure 8.19. The use of a prescaler which divides the VCO output frequency by M limits the frequency resolution of the PLL to multiples of $M \cdot f_{REF}$ rather than f_{REF}.

High speed dual modulus prescalers as shown in Figure 8.20 solve this problem as follows. The modulus of the prescaler is controlled by a third counter causing it to alternate between M and M + 1. Assume all three counters have been set for the beginning of a cycle: the prescaler for division by M + 1, the modulus control counter for division by N_{MC}, and the programmable counter for division by N_{PC}. The prescaler will divide by M + 1 until the modulus control counter has counted down to zero. At this time, the all zero state is detected and causes the prescaler to divide by M until the programmable counter has also counted down to zero. When this occurs, a cycle is complete and each counter is reset to its original modulus in readiness for the next cycle. The output frequency is given by:

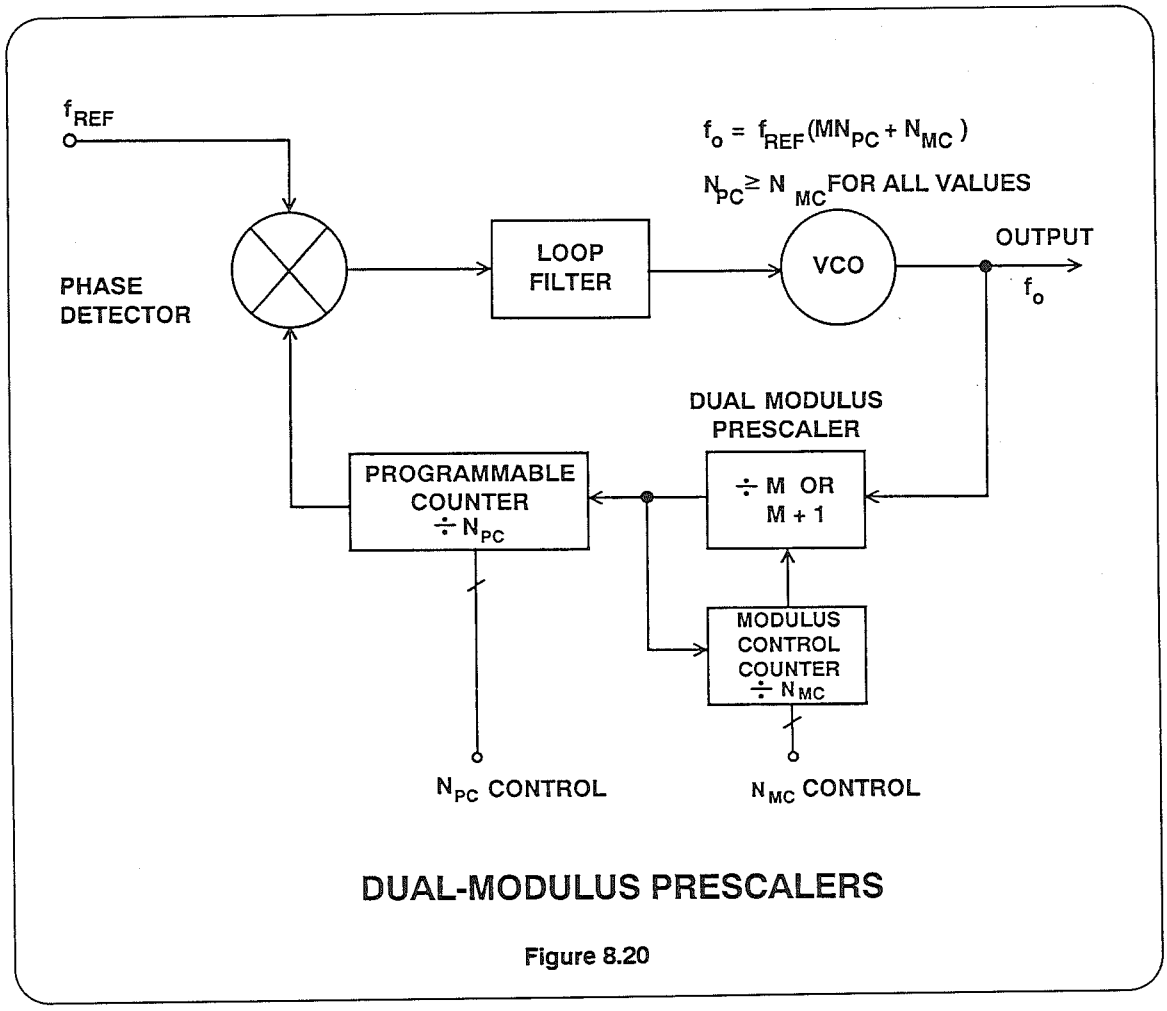
$$f_o = (MN_{PC} + N_{MC}) \cdot f_{REF}$$

Note that channels can be selected every f_{REF} by letting N_{PC} and N_{MC} take on suitable integer values, including zero, provided $N_{PC} \geq N_{MC}$ for all values.



HIGH-SPEED PRESCALER

Figure 8.19



DUAL-MODULUS PRESCALERS

Figure 8.20

PLL REFERENCES

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