SECTION VII

TIME DOMAIN FUNCTIONS: TIME DELAY GENERATORS

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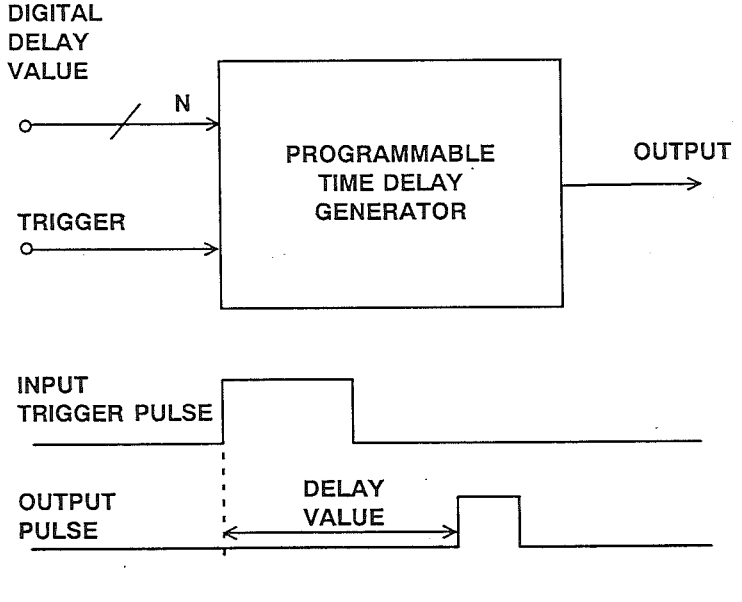
PROGRAMMABLE TIME DELAY GENERATION TECHNIQUES

There are numerous applications where it is desired to generate precise time delays under computer control as shown in Figure 7.1. A primary example is multiple channel deskewing in ATE systems. High pin count logic testers may have over one-hundred line drivers whose outputs must be routed to a remote testhead. Subnanosecond delay matching at the testhead is required for accurate delay measurements to be made on high speed ECL logic. Other applications for programmable delay generators are in pulse generators, timing circuits, multiple phase clock generators and arbitrary waveform generators.

High speed counters are often used to generate controlled delays but are not practical where subnanosecond resolution is required. Passive tapped delay lines offer precision but have limited resolution and delays can only be changed by switching taps. Hybrid delay lines (see Figure 7.3) which are a combination of passive and active elements offer digitally controlled step sizes of 100ps and fullscale delays of up to 20ns but are expensive and typically have high power dissipation (1 watt) thereby making them unsuitable for large volume high density applications.



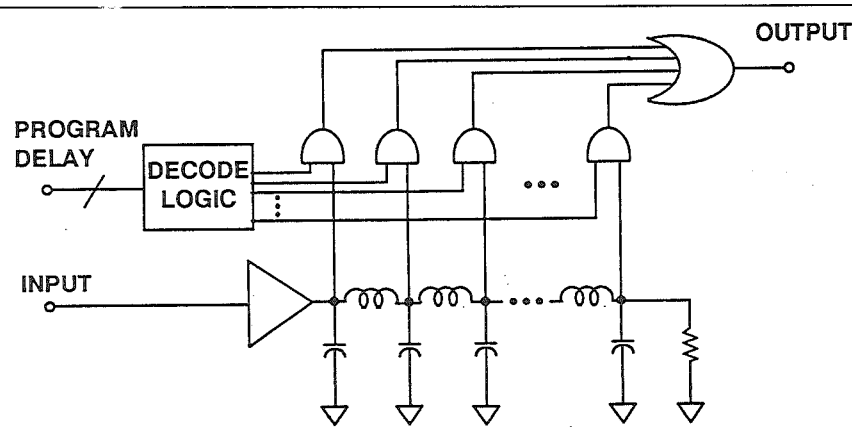
PROGRAMMABLE TIME DELAY GENERATOR

Figure 7.1

PROGRAMMABLE DELAY GENERATION

- High Speed Counters
  - 100ps Resolution Required 10 GHz Flip-Flop
- Passive Tapped Delay Lines
  - 100ps Resolution
  - Awkward to Switch Delay
- Hybrid Delay Lines
  - On Board Decoding Logic
  - 100ps Resolution
  - High Power
- Ramp/Comparator/DAC
  - 10ps Resolution, 8 BITS
  - Variable Full Scale Delays
  - Low Power, Low Cost IC

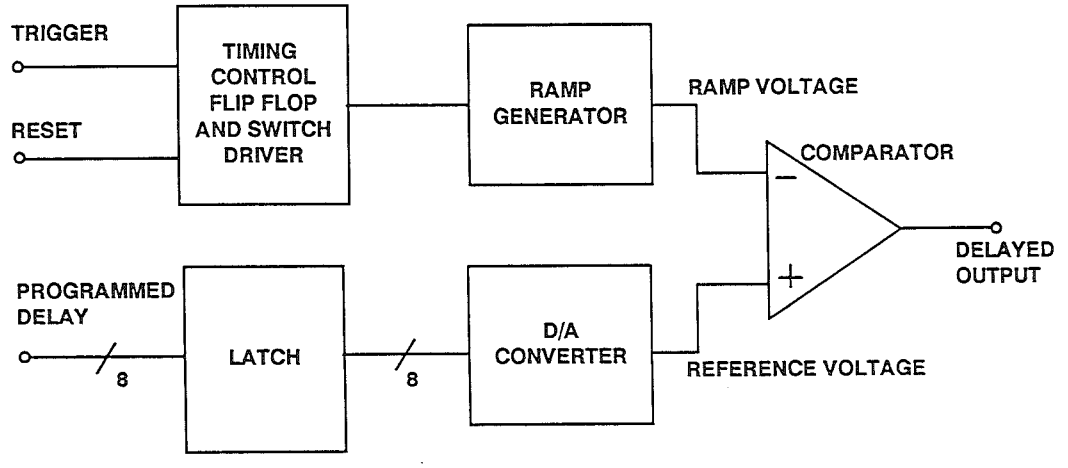
Figure 7.2



PROGRAMMABLE PASSIVE/ACTIVE HYBRID DELAY LINE

Figure 7.3

By far the most flexible approach to generating programmable delays is the ramp/comparator/DAC method shown in Figure 7.4. Upon the receipt of a trigger pulse, the ramp voltage generator is started. When the ramp voltage crosses the comparator threshold set by the DAC, the comparator output goes high, thereby generating a pulse edge which is delayed from the trigger pulse edge by an amount of time proportional to the DAC binary input. This approach to digital-to-time conversion (DTC) is not new, but recent advances in design and process techniques allow this function to be implemented in a single monolithic IC which offers not only precision but low power and cost.

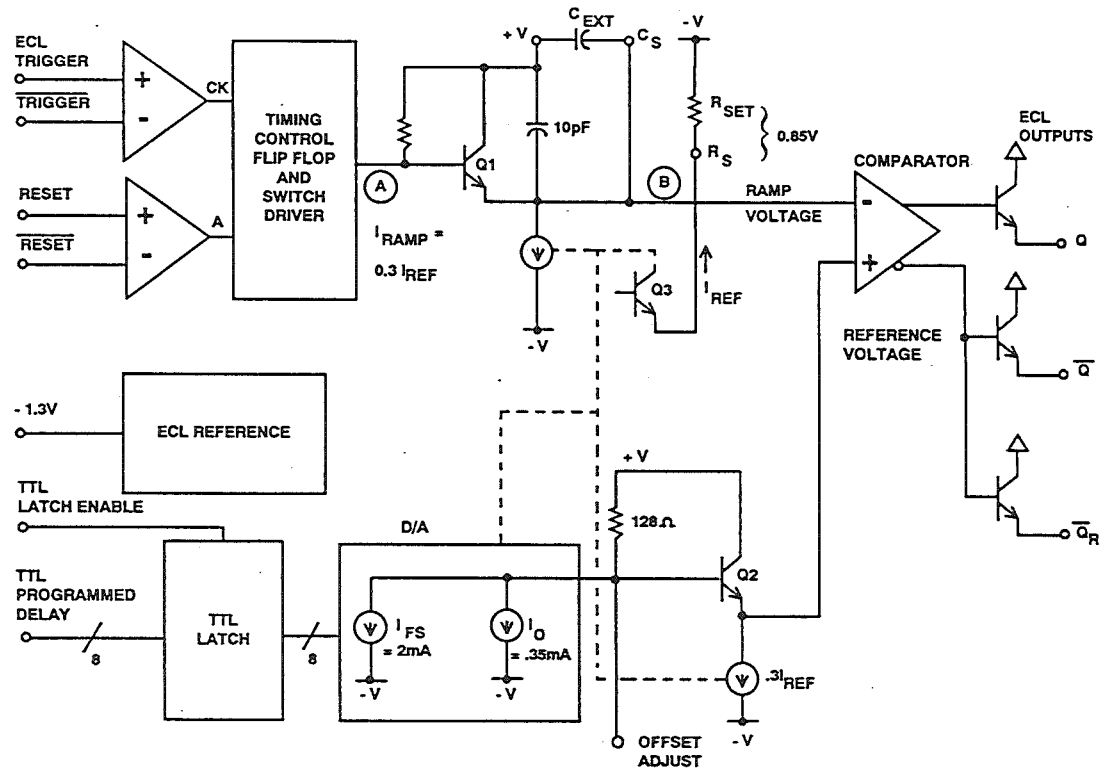


RAMP/COMPARATOR/DAC DELAY GENERATOR

Figure 7.4

AD9500 PROGRAMMABLE DELAY GENERATOR

A block diagram of the AD9500 DTC is shown in Figure 7.5. A positive going differential ECL pulse edge between the TRIGGER and the $\overline{\text{TRIGGER}}$ input causes the timing control flip flop and switch driver to force the base of Q1 negative, thereby causing the precision current source ($0.3I_{REF}$) to charge the capacitance ($10pF||C_{EXT}$) and creating a linear negative-going ramp voltage at Point B (the negative input of the comparator). The positive input reference voltage to the comparator is set by the 8-bit D/A converter after buffering by emitter follower Q2. When the ramp voltage crosses the programmed threshold, the Q output goes high while the $\overline{Q}$ and $\overline{Q}_R$ outputs go low. A differential RESET signal resets the timing control flip flop which returns Point A to +V and discharges the capacitance $10pF||C_{EXT}$ through the emitter of Q1. The RESET input is *level sensitive*



AD-9500 BLOCK DIAGRAM

Figure 7.5

and overrides the *edge sensitive* TRIGGER input (exactly like the reset input in a D flip flop). The reference current through Q3 is set by the external R_{SET} resistor with a minimum value of 250 ohms corresponding to I_{REF} = 3.4mA. I_{REF} is scaled to 0.3 I_{REF} which becomes the ramp current as well as the emitter current for Q2. Since Q1 and Q2 operate at the same current, their V_{BE} drops act as a common mode signal to the comparator inputs. The ramp charging current is given by:

$$I_{RAMP} = 0.3\, I_{REF} = 0.3\left(\frac{0.85V}{R_{SET}}\right) = \frac{0.255V}{R_{SET}}.$$

The slope of the ramp voltage becomes:

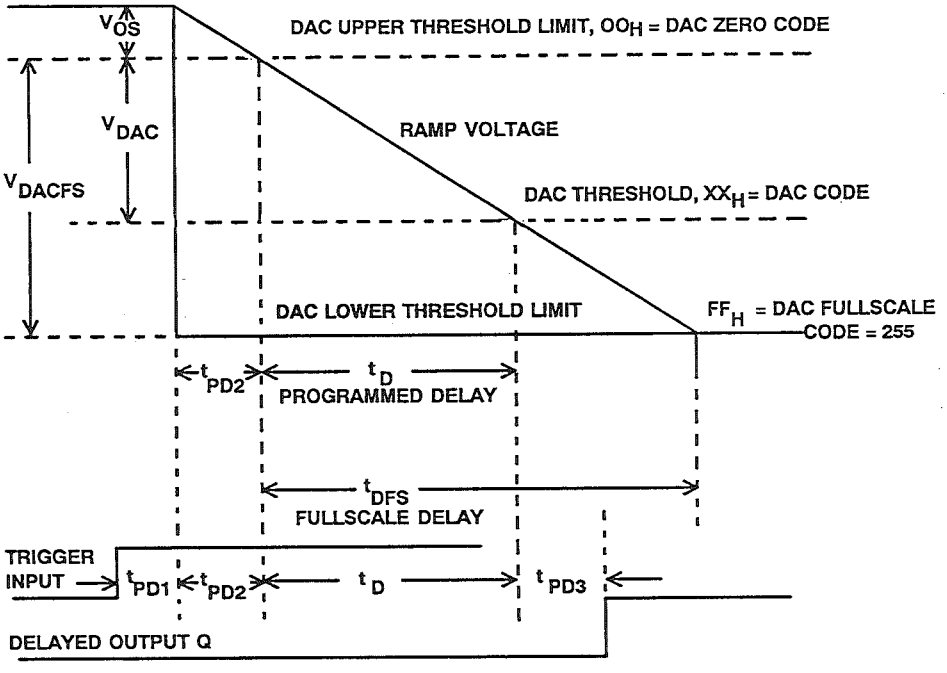
$$\frac{dV}{dt} = \frac{I_{RAMP}}{C_{EXT} + 10pF} = \frac{0.255V}{R_{SET}(C_{EXT} + 10pF)} \simeq \frac{\Delta v}{\Delta t}$$

The details of the ramp voltage and the various timing relationships are shown in Figure 7.6. Note that there is an initial

offset voltage of approximately 45mV across the 128 Ω resistor. This insures that the comparator is always off (Q output 0) at the start of the ramp. The offset also prevents the comparator from false triggering because of the small amount of ringing which occurs on the ramp voltage when it is reset.

The fullscale DAC current is set for 2mA corresponding to a fullscale DAC lower threshold limit (FF_H) of 256mV below the DAC upper threshold limit (OO_H). The DAC current is slaved to the reference current through Q3 to minimize the effects of temperature and device mismatch on the programmed delay t_D.

The programmed delay t_D is the time required for the ramp voltage to pass from the upper threshold limit OO_H to the DAC threshold voltage XX_H. The difference between these two levels is V_{DAC}.



t_{PD1} = INPUT DELAY (CONSTANT)

t_{PD2} = OFFSET DELAY (VARIABLE WITH t_{DFS})

t_{PD3} = OUTPUT DELAY (CONSTANT)

$t_{PD} = t_{PD1} + t_{PD2} + t_{PD3}$ = MINIMUM PROP. DELAY

TOTAL DELAY = $t_{PD} + t_D$

RAMP/TIMING RELATIONSHIPS

Figure 7.6

The previous equation can be rewritten:

$$\Delta v = \frac{0.255V \bullet R_{SET}\,(C_{EXT} + 10pF)}{\Delta v}.$$

The fullscale programmed delay t_{DFS} occurs when

$\Delta v = 256mV,$

$t_{DFS} = R_{SET}\,(C_{EXT} + 10pF).$

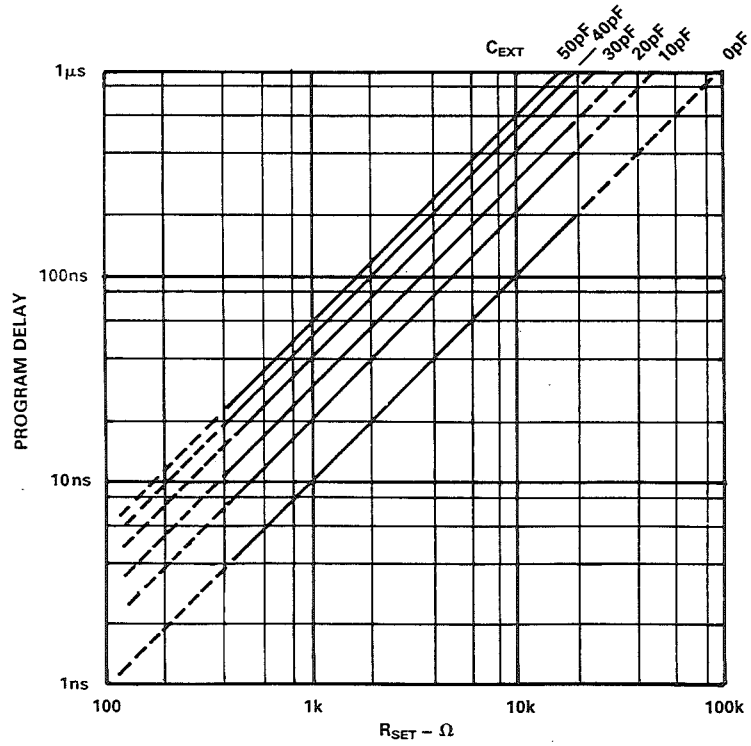
The graph of this function is shown in Figure 7.7. The program delay t_D can be written as

$$t_D = \frac{V_{DAC}}{V_{DACFS}} \bullet t_{DFS} = \frac{XX_H}{FF_H} \bullet R_{SET}\,(C_{EXT}+10pF).$$

The total delay through the AD9500 is the sum of the minimum propagation delay t_{PD} and the programmed delay t_D. The minimum propagation delay t_{PD} is made up of the fixed input delay t_{PD1}, the offset delay t_{PD2}, and the fixed output delay t_{PD3}. Note that the offset delay t_{PD2} is a function of the fullscale delay and is given by:

$$t_{PD2} = t_{DFS} \bullet \frac{V_{OS}}{V_{DACFS}} =$$

$$\frac{V_{OS}}{V_{DACFS}} \bullet R_{SET}\,(C_{EXT}+10pF)$$



TYPICAL PROGRAMMED DELAY RANGES

Figure 7.7

The minimum propagation delay t_{PD} becomes:

$$t_{PD} = t_{PD1} + t_{PD3} + t_{PD2}$$

$$t_{PD} = t_{PD1} + t_{PD3} + \frac{V_{OS}}{V_{DACFS}} \cdot R_{SET}\,(C_{EXT}+10pF)$$

The total delay then becomes:

$$\text{TOTAL DELAY} = t_{PD} + t_D$$

$$= t_{PD1} + t_{PD3} + \frac{V_{OS}}{V_{DACFS}} \cdot R_{SET}\,(C_{EXT}+10pF) + \frac{XX_H}{FF_H} \cdot R_{SET}\,(C_{EXT}+10pF).$$

In the AD9500, $t_{PD1} + t_{PD3} = 4ns$,
$V_{OS} = 45mV$
$V_{DACFS} = 256mV$.

$$\text{TOTAL DELAY} = t_{PD} + t_D$$

$$= 4ns + \frac{45}{256} \cdot R_{SET}\,(C_{EXT} + 10pF) + \frac{XX_H}{FF_H} \cdot R_{SET}\,(C_{EXT} + 10pF)$$

$$= 4ns + 0.18\,R_{SET}\,(C_{EXT} + 10pF) + \frac{XX_H}{FF_H} \cdot R_{SET}\,(C_{EXT} + 10pF).$$

$$\text{MINIMUM PROP. DELAY} = t_{PD}$$

$$t_{PD} = 4ns + 0.18\,R_{SET}\,(C_{EXT} + 10pF)$$

$$\text{PROGRAMMED DELAY} = t_D$$

$$t_D = \frac{XX_H}{FF_H} \cdot R_{SET}\,(C_{EXT}+10pF).$$

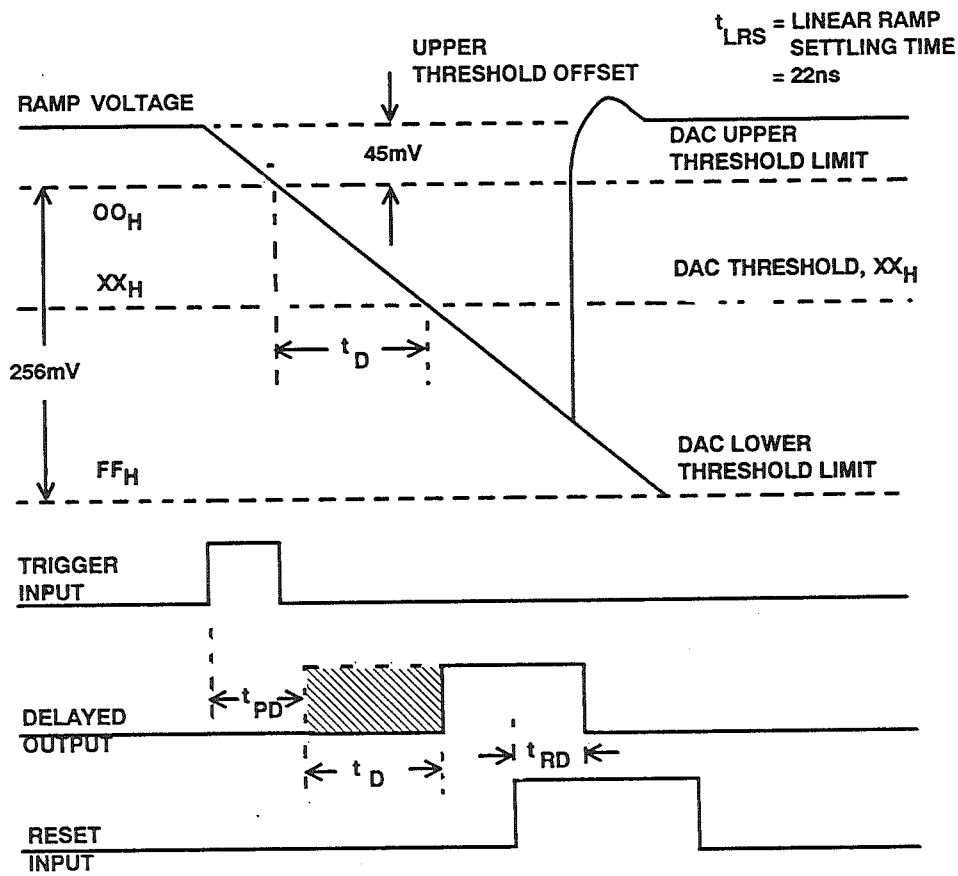
Another important AD9500 specification is the reset propagation delay t_{RD} which is the time from the leading edge of the RESET pulse input until the delayed output Q returns to a logic "0". This requires that the ramp voltage cross the upper threshold limit and thereby return the comparator to its initial state. The timing relationships are shown in Figure 7.8. Note that the time required for the linear ramp voltage to settle after reset t_{LRS} is typically 22ns.

The input latch is designed to accept an 8-bit TTL program delay input and has a TTL latch enable function. When the LATCH ENABLE is a logic "0" the input data is passed to the DAC. A logic "1" freezes the data in the latch.

Key specifications for the AD9500 are summarized in Figure 7.9 along with a simplified functional block diagram.

Further details of the operation of the circuits within the AD9500 can be found in the following United States Patent:

Patent #4742331
Date of patent: May 3, 1988
Inventors: Jeffrey G. Barrow
Adrian P. Brokaw
Assignee: Analog Devices, Inc.
Norwood, MA



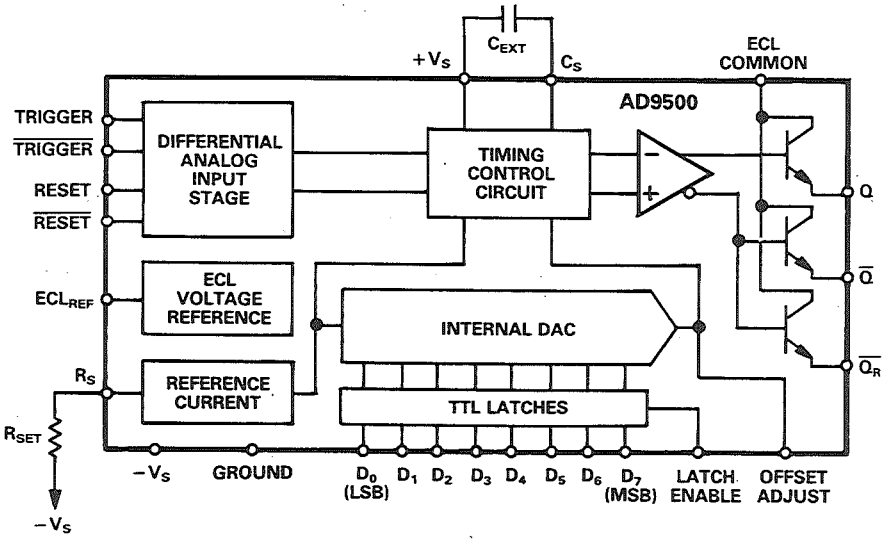
t_{PD} = MINIMUM PROPAGATION DELAY

t_D = PROGRAMMED DELAY

t_{RD} = RESET PROPAGATION DELAY

AD-9500 TIMING RELATIONSHIPS

Figure 7.8



- 2.5ns TO 100 μs^+FULLSCALE RANGE
- 10ps DELAY RESOLUTION
- 8-BIT TTL INTERNAL LATCH AND DAC
- LOW POWER DISSIPATION - 310mW

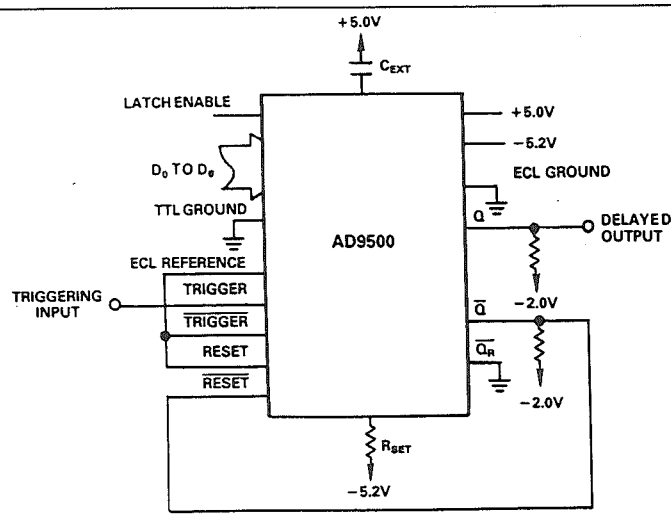
AD-9500 KEY SPECIFICATIONS

Figure 7.9

AD9500 MINIMUM OUTPUT PULSE WIDTH CONFIGURATION

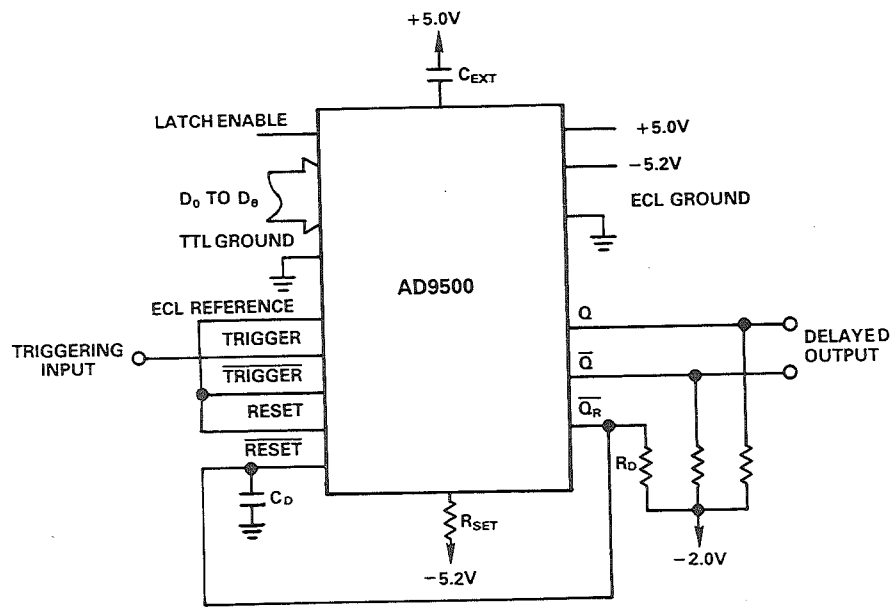
Figure 7.10 shows the AD9500 configured for minimum output pulse width. Only one of the TRIGGER inputs is used. The other is connected to the ECL reference midpoint, ECL_{REF}. This allows the AD9500 to be triggered with standard 10K or 10KH single-ended ECL signals. Improved noise margin, temperature tracking, and common mode noise rejection are obtained, however, if the TRIGGER and $\overline{\text{TRIGGER}}$ inputs are driven differentially.

Once the triggering event occurs, the Q output will go to a logic 1 state after the total delay interval has passed. The $\overline{Q}$ output is then used to drive the RESET input, causing the AD9500 to reset itself. The result is a delayed output pulse which is only as wide as the reset propagation delay ($t_{RD} \simeq 5$ns).



AD-9500 MINIMUM OUTPUT PULSE WIDTH CONFIGURATION

Figure 7.10



RESET TIME = t_{RD} + 0.54R_DC_D

$R_D \geq 300\Omega$

NOTE: IF R_D RETURNED TO -5.2V,
RESET TIME = t_{RD} + 0.12R_DC_D

$R_D \geq 1000\Omega$

AD-9500 EXTENDED OUTPUT PULSE WIDTH CONFIGURATION

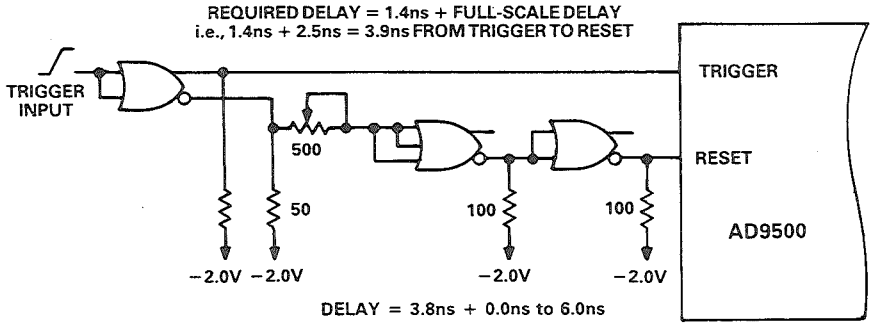
Figure 7.11

AD9500 CONFIGURED FOR EXTENDED OUTPUT PULSE WIDTHS

The extended output pulse configuration shown in Figure 7.11 is similar to the minimum configuration except that the output pulse width is extended. The Q_R output is used to drive the RESET input through a resistor/capacitor charging network. The charging network causes the signal at the RESET input to fall more slowly thereby extending the output pulse width. The appropriate values for R_D and C_D are determined using the equations in Figure 7.11.

AD9500 CONFIGURED FOR HIGH SPEED TRIGGERING

The AD9500 can be triggered at rates above 100 MHz. This is accomplished by resetting the AD9500 shortly after it is triggered, which also tends to generate an extremely narrow output pulse. The delay circuit shown in Figure 7.12 between the TRIGGER input and the RESET input provides the variable delay required for various configurations from 2.5ns fullscale to over 10ns fullscale (greater than 10ns total delay precludes 100 MHz triggering).



AD-9500 CONFIGURED FOR HIGH SPEED TRIGGERING

Figure 7.12

MULTIPLE PATH DESKEWING

High speed electronic systems with parallel signal paths require that close delay matching be maintained. If delay mismatch (or skew) occurs, errors can be made in transfer of data. Therefore, delays are matched, usually by carefully matching lead lengths.

High-speed, high-pin-count testers must maintain close matching under different circuit conditions to test different device types. In these cases, matching of lead length is not sufficient to maintain matching to the required subnanosecond tolerance. A calibration cycle is typically included in the changeover from one device to another. During the calibration cycle, a single stimulus pulse is applied to each input of the circuit shown in Figure 7.13.

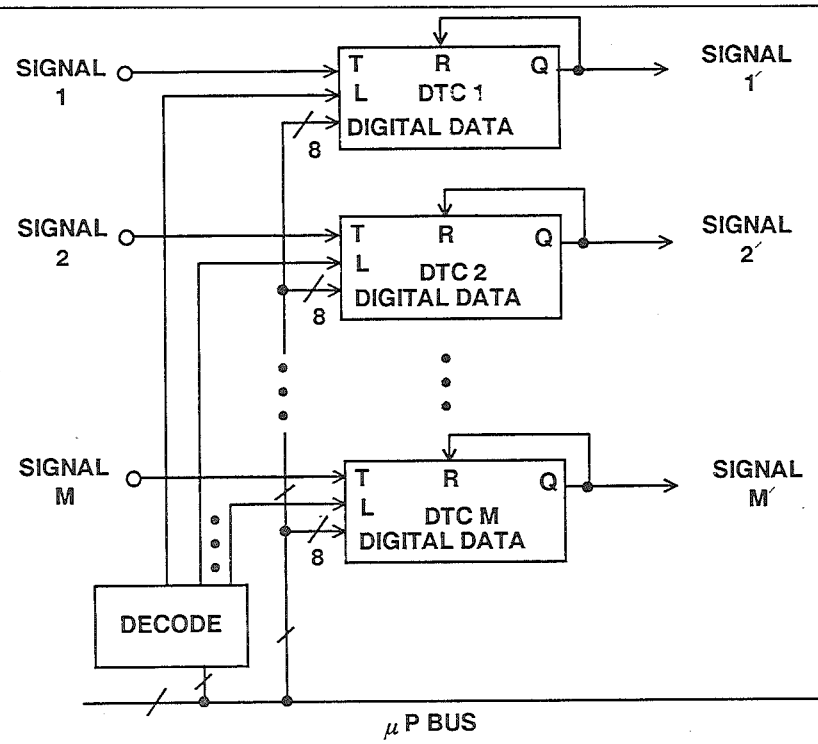
The delay of each signal path is then measured by the tester delay measurement circuitry. Using a closed-loop technique, each delay is equalized by changing the digital value held in the register of the DTC. Once the delays are matched to the desired tolerance, the calibration loop is opened, and the tester is ready to test.

Delay for each DTC can be calculated with the equations:

$$T_{DTC} = t_{DTC} + t_{pd}$$

when:

$$t_{DTC} = (XX_H/FF_H) * RC$$



MULTIPLE PATH DESKEWING
Figure 7.13

where:

T_{DTC} is total delay through the DTC.
t_{DTC} is the programmed delay.
t_{pd} is the prop delay with zero programmed delay.
XX_H is the 8-bit digital input.
FF_H is full-scale digital input.
R is in ohms.
C is in farads.

PROGRAMMABLE PULSE GENERATOR

In this application, (see Figure 7.14), two DTCs are triggered from a common clock signal. Their outputs go to the inputs of an RS flip-flop. A digital delay value is latched into each DTC with DTC #2 typically having a greater value than DTC #1.

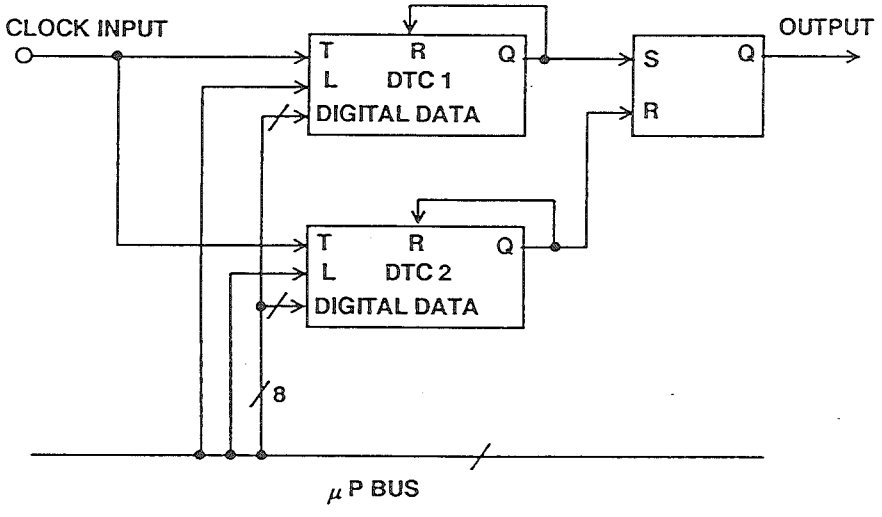
Changing the delay value from one clock cycle to the next generates a pseudo-random pulse whose leading and trailing edge delays are controlled relative to Clock In.

The frequency and pulse width of the pulse generator can be determined as follows:

$$f = f_{CLOCK\ IN}$$

and:

$$t_{pw} = t_{DTC2} - t_{DTC1}$$



PROGRAMMABLE PULSE GENERATOR

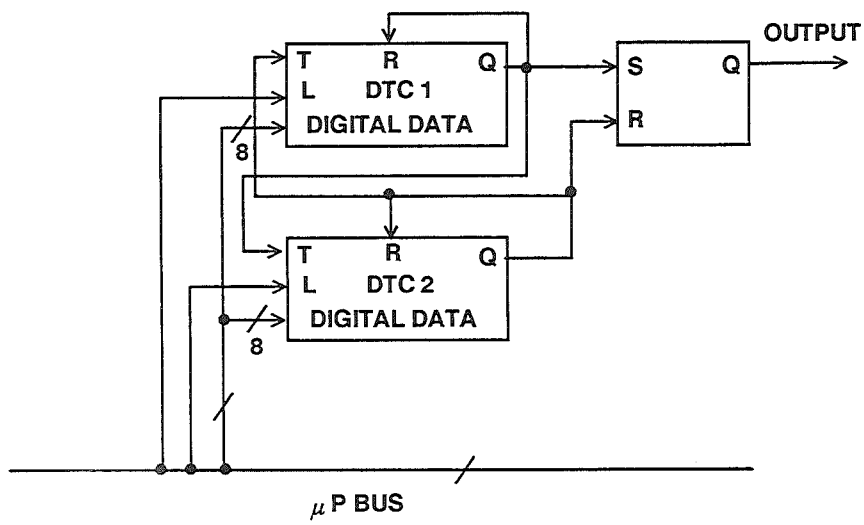
Figure 7.14

PROGRAMMABLE OSCILLATOR

Two DTCs are configured as an astable oscillator as shown in Figure 7.15. Delay through each side of the oscillator is determined by the value held in the DTCs register, plus the fixed propagation delay of each DTC. Increasing the digital value decreases frequency, just as increasing RC decreases frequency in a traditional oscillator. Frequency and duty cycle are both controllable.

Frequency can be found by the equation:

$$f = 1/(2t_{pd} + t_{DTC1} + t_{DTC2}).$$



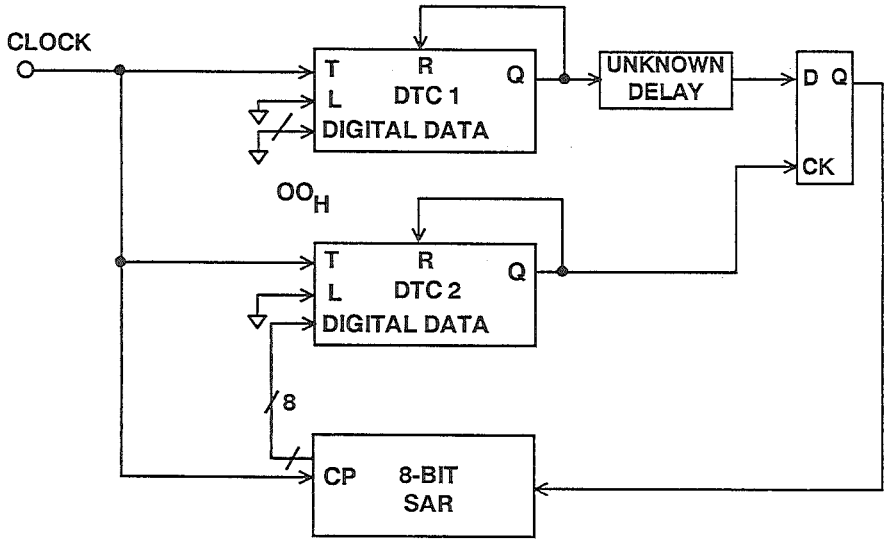
PROGRAMMABLE OSCILLATOR

Figure 7.15

DIGITAL DELAY DETECTOR

An unknown digital delay can be measured by applying a repetitive clock to the circuit shown in Figure 7.16. DTC #1 is set to zero delay. Like a successive approximation ADC, this delay detector requires 8 cycles of the clock to determine the value of the unknown delay.

Since, in reality, there are non-ideal characteristics in the circuits which are shown, the value of DTC #1 should be adjusted with zero delay substituted for the unknown delay; this will compensate for set-up time of the flip-flop, stray delays, etc.



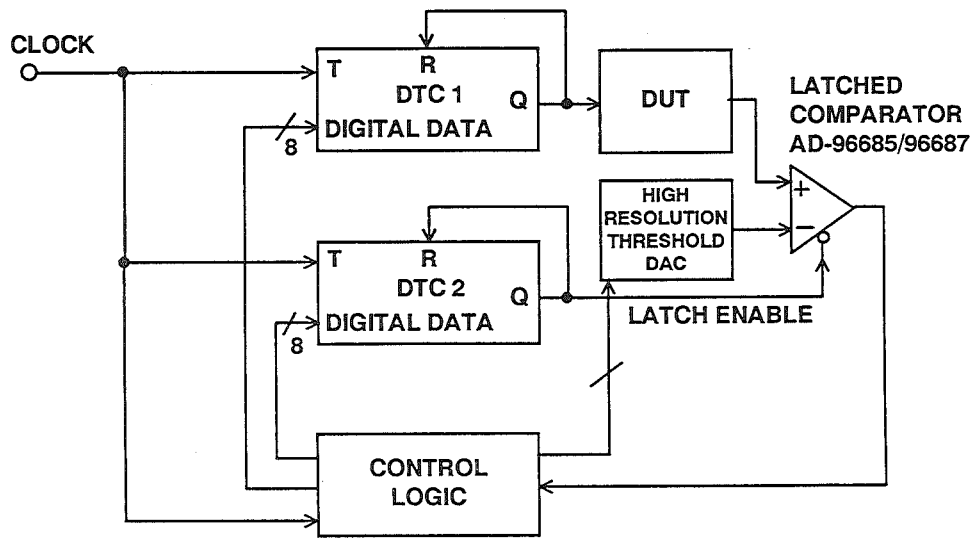
MEASURING UNKNOWN DELAYS

Figure 7.16

DIGITIZING AC WAVEFORMS

The circuit shown in Figure 7.17 can be used to measure the time profile of high-speed waveforms. The DAC sets a threshold level which drives one of the differential comparator inputs. The other comparator input is driven by the device under test (DUT). The output of the first AD9500 causes the DUT to produce an output. The second AD9500, which is also triggered along with the first AD9500, strobes the comparator latch enable.

If the DUT output is greater than the DAC threshold when the comparator is latched, the comparator output will be a logic 1. If the output is below the DAC threshold, the comparator will be a logic 0. The programmed delay setting of the second AD9500 is adjusted to the point where the DUT output equals the DAC threshold. By varying the DAC threshold level and adjusting the second AD9500 programmed delay, a point by point reconstruction of the AC waveform can be created.



MEASURING AC WAVEFORMS

Figure 7.17

MEASURING ANALOG SETTLING TIME

This circuit as shown in Figure 7.18 functions in a manner similar to the digital delay detector circuit of Figure 7.16. The clock must be repetitive; and DTC #1 is used to cancel prop delay of DTC #2, set-up time of the comparators, stray delays, etc. The difference is in the detection method. The register is replaced by a window comparator.

Timing for this circuit operates by starting at fullscale (after the DUT has settled) and decrementing the latch strobe delay. The output of the detector will be high as long as the signal is within the limits set by V_1 and V_2.

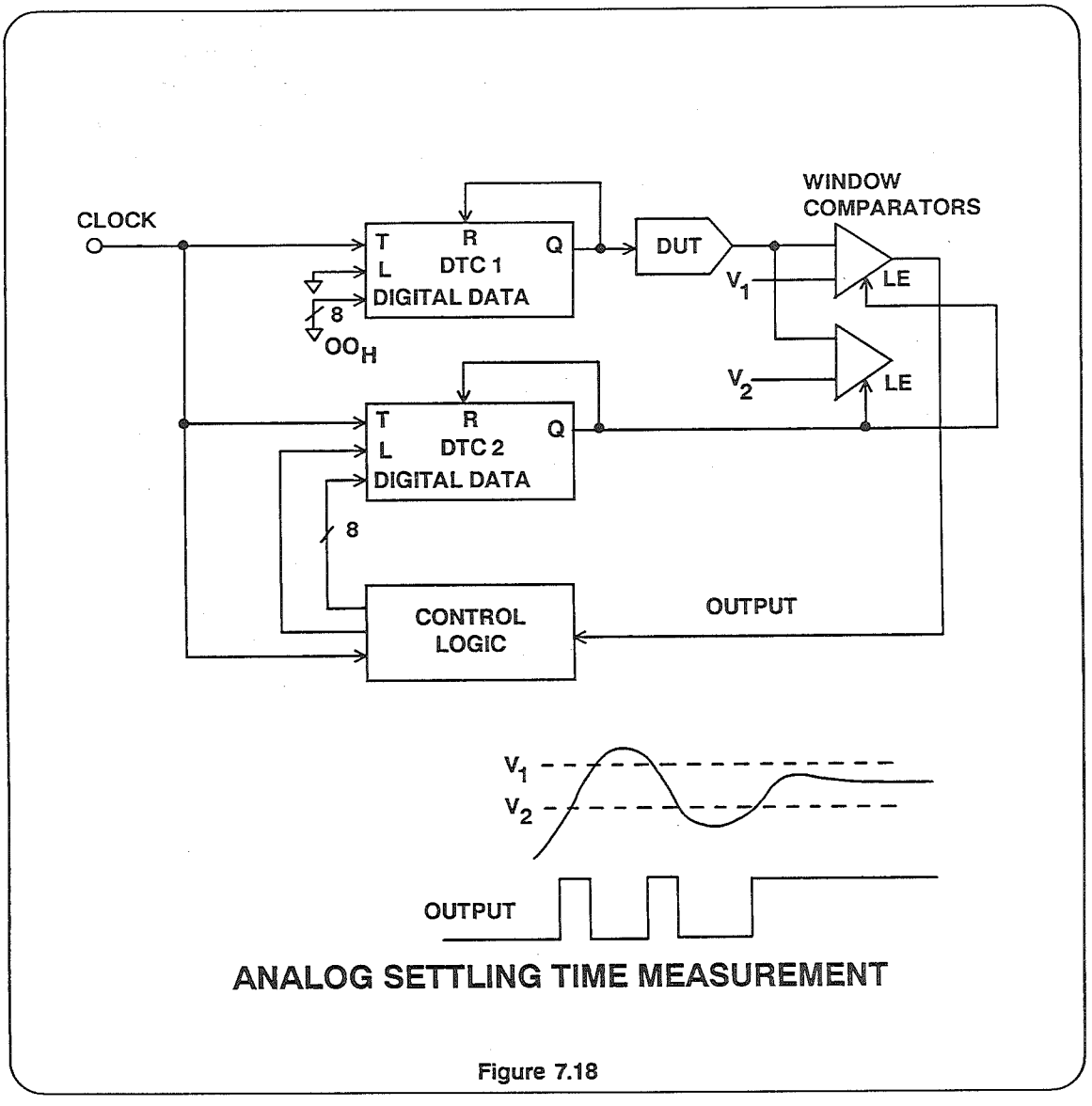
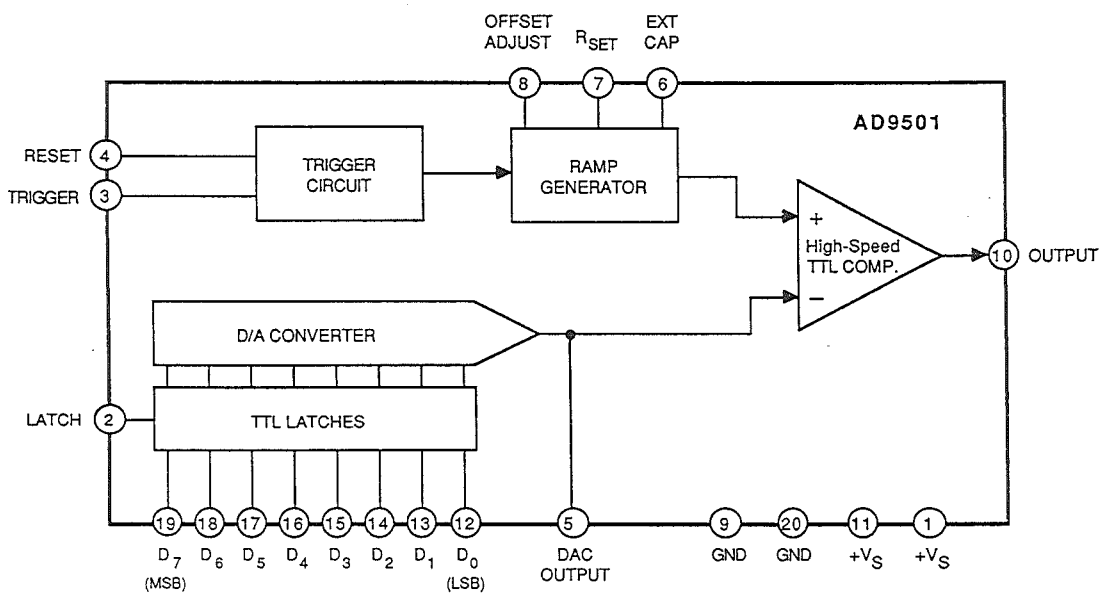

CLOCK
T
L
R
DTC 1
DIGITAL DATA
Q
8
OO_H
DUT
WINDOW
COMPARATORS
V_1
LE
V_2
LE
T
L
R
DTC 2
DIGITAL DATA
Q
8
CONTROL
LOGIC
OUTPUT
V_1
V_2
OUTPUT
ANALOG SETTLING TIME MEASUREMENT

Figure 7.18

AD-9501: TTL COMPATIBLE PROGRAMMABLE DELAY GENERATOR

The AD-9501 is a fully TTL compatible version of the AD-9500, operating off a single +5V power supply. The principles of operation are similar to the AD-9500.

A block diagram along with key specifications for the AD-9501 are shown in Figure 7.19



AD9501 Functional Block Diagram

- 2.5 ns TO 10μs FULLSCALE RANGE
- 10 ps DELAY RESOLUTION
- TTL AND CMOS COMPATIBLE
- SINGLE +5V SUPPLY
- LOW POWER DISTRIBUTION: 415 mW

AD-9501 KEY SPECIFICATIONS

Figure 7.19