SECTION VI

TIME DOMAIN FUNCTIONS: COMPARATORS AND PIN ELECTRONICS

TIME DOMAIN FUNCTIONS: COMPARATORS AND PIN ELECTRONICS

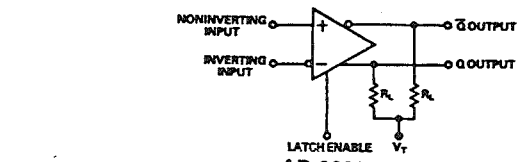
COMPARATOR OPERATION

High speed comparators have widespread applications in automatic test equipment, instrumentation, electronic warfare, radar, and telecommunications. In the field of data acquisition, high speed comparators form the basic building block for flash converters and successive approximation A/D converters.

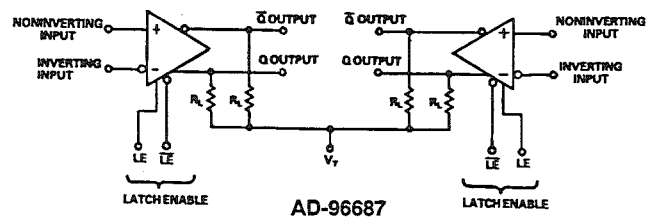
A block diagram, timing, and characteristic data for the AD96685 (single) and AD96687 (dual) ECL comparators is shown in Figure 6.1. In addition to performing the basic compare function, this comparator contains an integral latch. The AD96687 comparator "tracks" the input signal when the LE line is high and the LE line is low. The comparator data is latched when the LE line goes low and the LE line goes high. Differential inputs on the latch enable lines on the AD96687 insure a minimum amount of clock feedthrough which could alter the comparator's input threshold. If the latch function is not going to be used, the LE line should be grounded, and the LE left floating or tied to -2V, thereby disabling the latching function. Occasionally, one of the two comparator stages in the AD96687 will not be used. The inputs of the unused comparator should not be allowed to "float". The high internal gain may cause the output to oscillate (possibly affecting the other comparator which is being used) unless the output is forced into a fixed state. This is easily accomplished by insuring that the two inputs are at least one diode drop apart, while also grounding the LE input.

Best performance of high speed ECL comparators will be achieved with the proper use of ECL terminations. The open-emitter outputs of the AD96685/AD96687 are designed to be terminated in 50 ohms to -2V. If a -2V supply is not available, an 82 ohm resistor to ground and a 180 ohm resistor to -5.2V provides a suitable equivalent. If high speed ECL signals must be routed more than a few centimeters, microstrip techniques should be used to prevent ringing and possible oscillation or false triggering. The use of a low impedance ground plane and power supply decoupling (with 0.1μF ceramic capacitors) at the power pins is also essential. Sockets should be avoided due to stray capacitance and inductance. If proper high speed techniques are used, the AD96685/96687 should be free from oscillation when the comparator input signal passes through the switching threshold, and resolution approaching 1mV should be achievable.

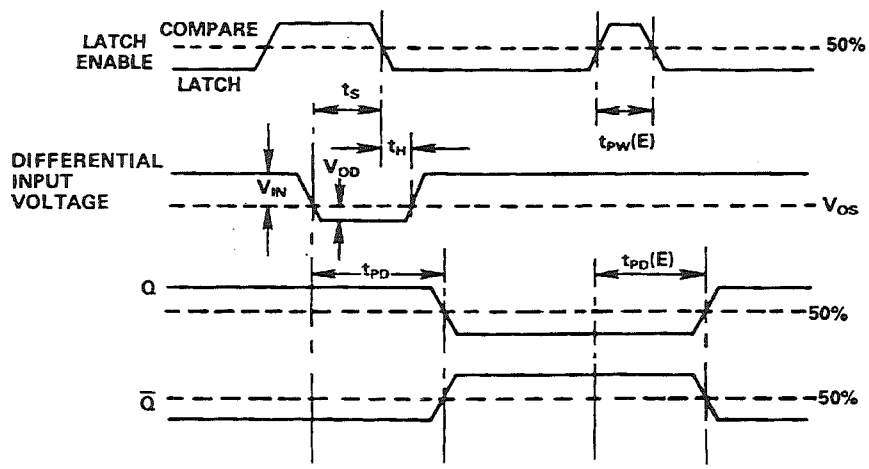
Another technique for reducing the possibility of oscillation when the input signal is near the switching threshold is the use of a narrow latch enable strobe. If the latch enable pulse width is made equal to or slightly less than the comparator propagation delay, the effects of positive feedback from the output to the input are greatly reduced. For the AD96685/96687, the minimum latch enable pulse width is 2ns compared to the propagation delay of 2.5ns. In this mode, the comparator is allowed to compare or "track" for only 2ns. The remainder of the time is spent in the "latch" mode until the next comparison is made.



AD-96685



AD-96687



t_S = 0.5ns - Minimum Setup Time
t_H = 0.5ns - Minimum Hold Time
t_{PD} = 2.5ns - Input to Output Delay
t_{PD} (E) = 2.5ns - LATCH ENABLE to Output Delay
t_{PW}(E) = 2.0ns - Minimum LATCH ENABLE Pulse Width
V_{OS} = 10mV - Input Offset Voltage
V_{OD} = 10mV - Overdrive Voltage

- DISPERSION: 50ps
- COMMON MODE REJECTION RATIO: 90dB
- ECL COMPATIBLE
- INPUT IMPEDANCE: 200k Ω||2pF
- INPUT VOLTAGE RANGE: -2.5V, +5V
- POWER DISSIPATION: AD-96685 (SINGLE) - 120mW
  AD-96687 (DUAL) - 240mW
- POWER SUPPLY REJECTION RATIO: 70dB

AD-96685/AD-96687 COMPARATOR SPECIFICATIONS

Figure 6.1

REDUCING COMPARATOR OSCILLATION

- Layout - Microstrip Techniques
- Ground Plane
- No Sockets
- Power Supply Decoupling at Pins Using Chip Capacitors
- Narrow Latch Strobe
- Hysteresis

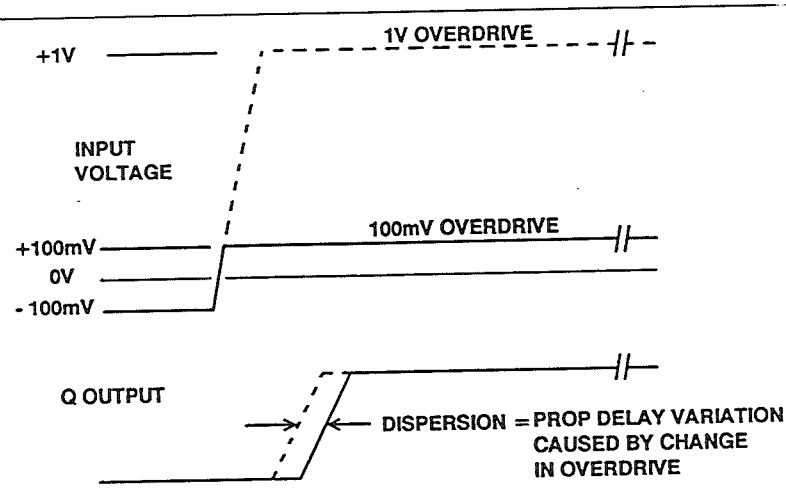
Figure 6.2

COMPARATOR PROPAGATION DELAY DISPERSION

Dispersion is a specification which is important in critical timing applications such as ATE, bench instruments, and nuclear instrumentation. Dispersion is defined as the variation in propagation delay as the input overdrive conditions are changed. For the AD96685/96687 comparators, dispersion is typically 50ps as the overdrive is changed from 100mV to 1V (see Figure 6.3). This specification applies for both positive and negative overdrives since the AD96685/96687 has equal delays for positive and negative going inputs.

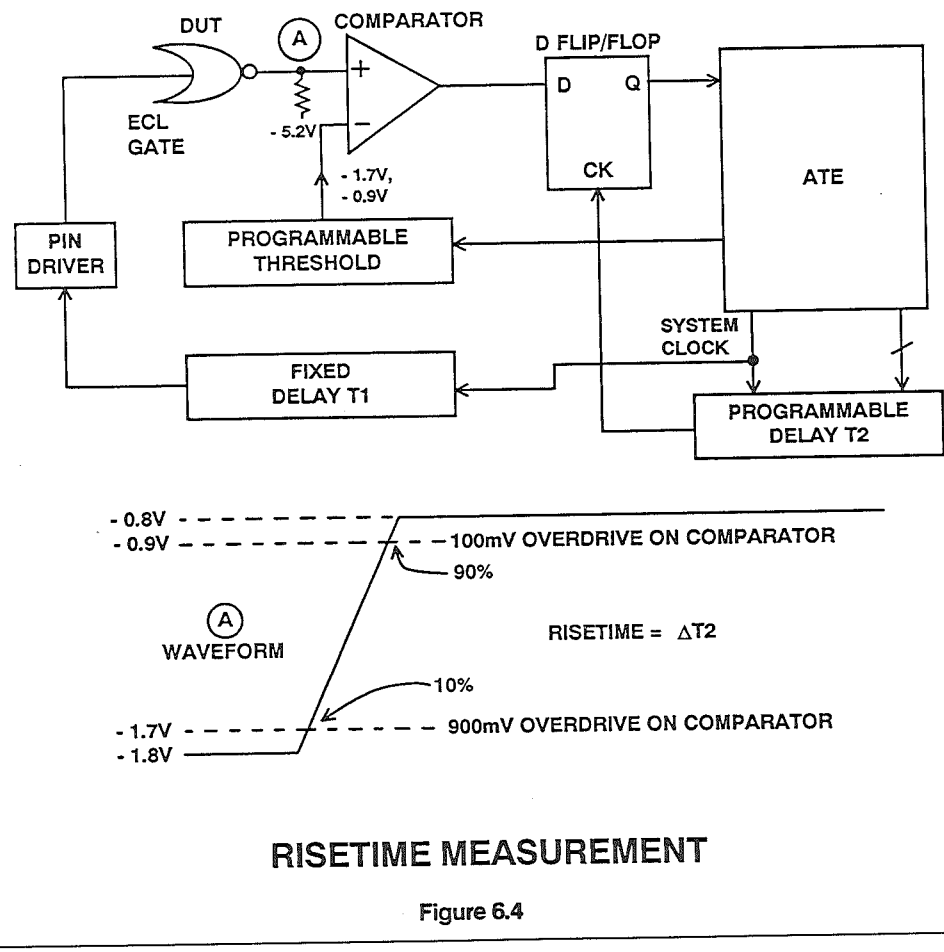
The 50ps propagation delay dispersion of the AD96685/96687 offers considerable improvement over the 200-300ps dispersion of the older 685/687 series comparators.

The effects of dispersion are illustrated in the ATE application shown in Figure 6.4, where the device under test (DUT) is being tested for output logic risetime. The comparator threshold is first set to -1.7V (10% point). The programmable delay T2 is set until the output of the D flip-flop is toggling equally between the 1 and 0 state. The comparator threshold is then set to -0.9V (90% point) and the programmable delay is changed until the D flip-flop is again toggling equally between the 1 and 0 state. The change in T2 between the two measurements corresponds to the DUT output logic risetime. Any propagation delay dispersion in the comparator will cause a corresponding risetime measurement error due to the two different overdrive conditions required to perform the 10% and 90% measurement.



COMPARATOR DISPERSION

Figure 6.3



RISETIME MEASUREMENT

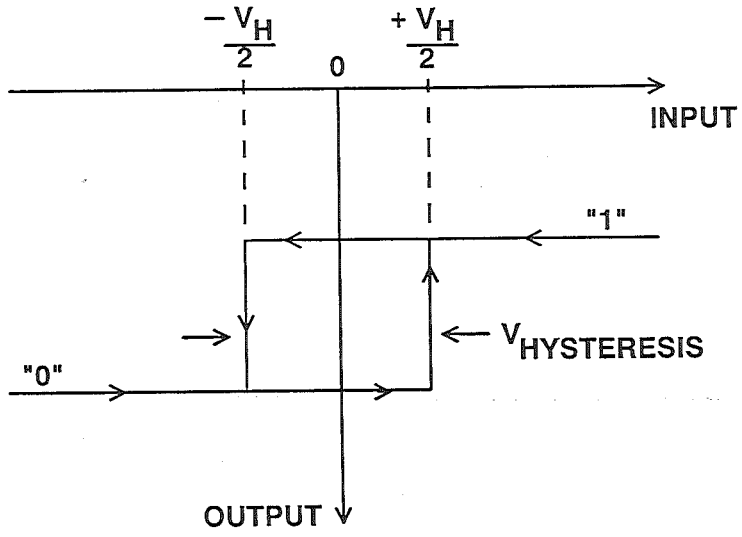
Figure 6.4

COMPARATOR HYSTERESIS

The addition of hysteresis to a comparator is often useful in a noisy environment or where it is not desirable for the comparator to toggle between states when the input signal is at the switching threshold. The transfer function for a comparator with hysteresis is shown in Figure 6.5. If the input voltage approaches the threshold from the negative direction, the comparator will switch from a "0" to a "1" when the input crosses $+V_H/2$. The "new" switching threshold now becomes $-V_H/2$. The comparator will remain in a "1" state until the threshold $-V_H/2$ is crossed coming from the positive direction. In this manner, noise centered around OV input will not cause the comparator to switch states unless it exceeds the region bounded by $\pm V_H/2$.

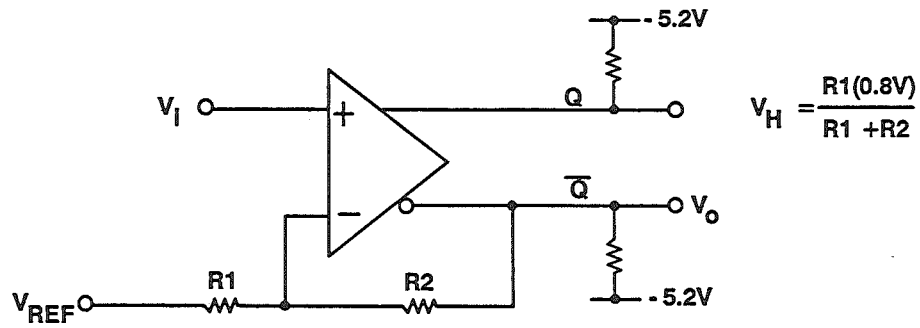
Positive feedback from the output to the input is often used to produce hysteresis in a comparator (see Figure 6.6).

The AD96685/96687 series comparators are designed so that the latch enable function can be used to produce hysteresis as shown in Figure 6.7.



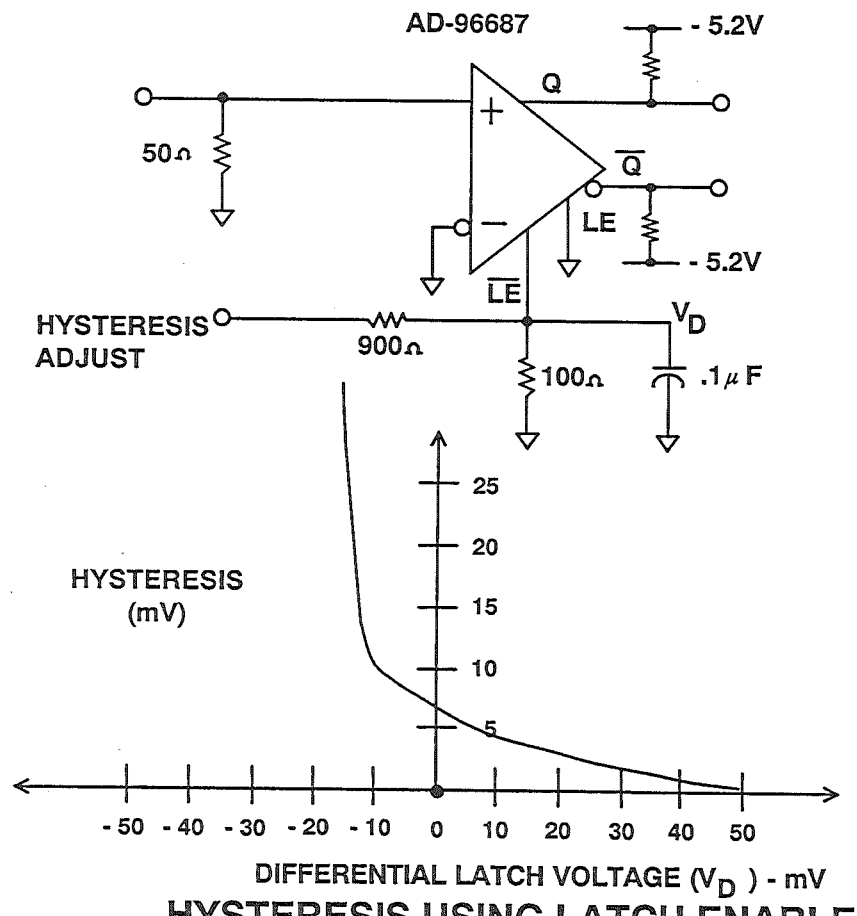
COMPARATOR HYSTERESIS

Figure 6.5



HYSTERESIS USING POSITIVE FEEDBACK

Figure 6.6



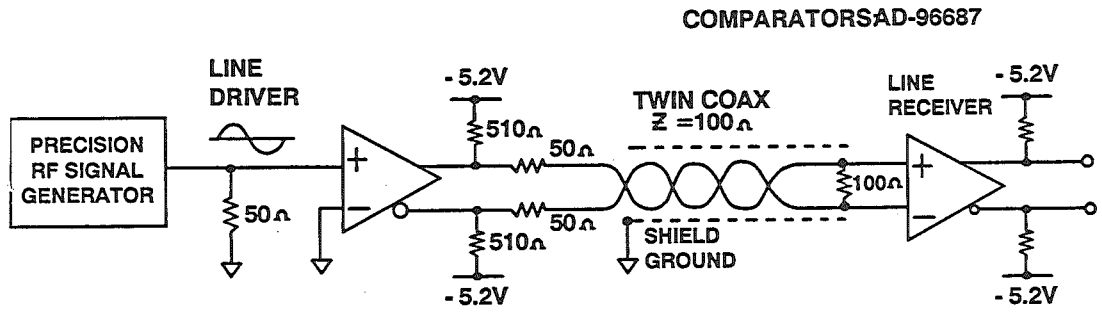
HYSTERESIS USING LATCH ENABLE

Figure 6.7

6

COMPARATOR LINE DRIVER AND RECEIVER

Figure 6.8 shows how high speed comparators can be used to transmit and receive high speed clock and logic signals across noisy interfaces with minimal degradation. The line driving comparator converts the sinewave output of the RF signal generator into balanced differential ECL logic signals. The driver is source terminated and the signal transmitted over shielded 100 ohm twin-conductor coaxial cable. The line receiving comparator input is terminated in 100 ohms line-to-line. This arrangement makes the output of the line receiver virtually immune to jitter caused by common mode noise on the twin conductors.

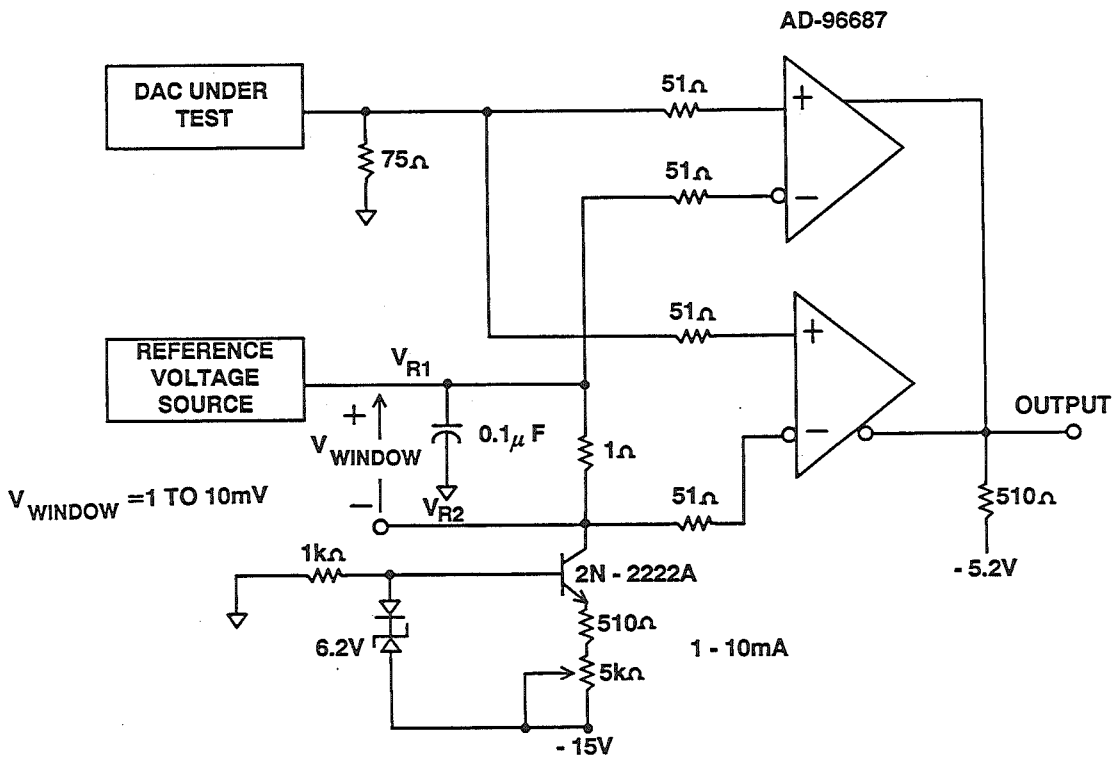


PRECISION CLOCK DISTRIBUTION: COMPARATOR LINE DRIVER AND RECEIVER

Figure 6.8

HIGH SPEED WINDOW COMPARATOR CIRCUIT FOR SETTLING TIME MEASUREMENTS

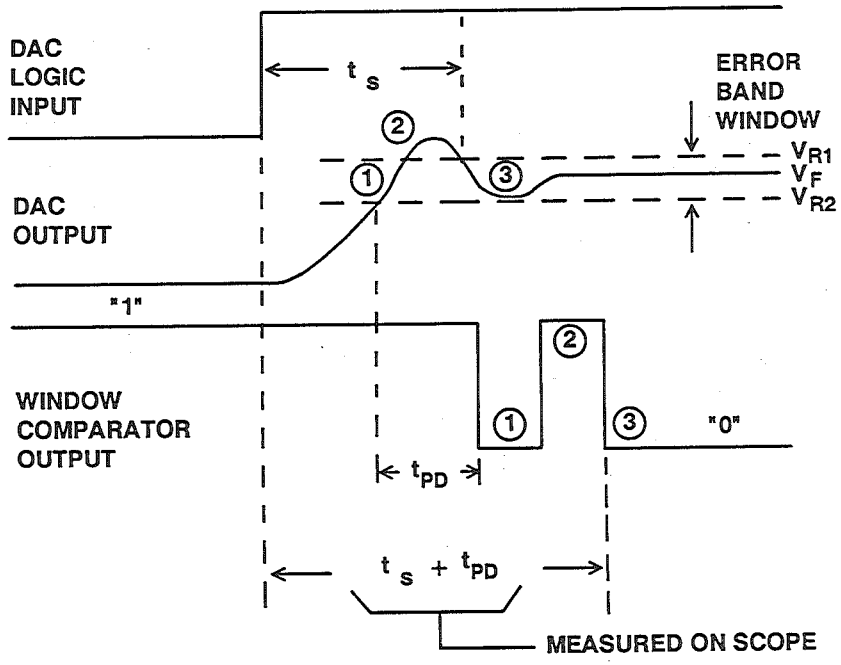
A dual AD96687 comparator can be used to make settling time measurements as shown in Figure 6.9. The wire-or feature of ECL logic is used so that the output of the window comparator circuit is a logic 0 whenever the common input signal lies between the window voltage set by V_{R1} and V_{R2}. The error band window is set by adjusting the current source which develops the window voltage across the 1 ohm resistor. The upper reference voltage V_{R1} is set by the reference voltage generator.



WINDOW COMPARATOR FOR MEASURING D/A CONVERTER SETTLING TIME

Figure 6.9

Figure 6.10 shows the resulting waveforms after proper setting of the reference voltages. The upper reference voltage V_{R1} is set to the final value of the DAC output (measured with a DVM) plus 1/2 the error band window. The current source is set so that V_{R2} is 1/2 the error band below the final value. The DAC is then switched from all zeros to all ones, and the settling time is measured as shown. The propagation delay of the comparator (t_{PD} = 2.5ns) must be subtracted in order to obtain the correct settling time measurement.



WINDOW COMPARATOR SETTLING TIME WAVEFORMS

Figure 6.10

HIGH SPEED COMPARATOR SELECTION GUIDE

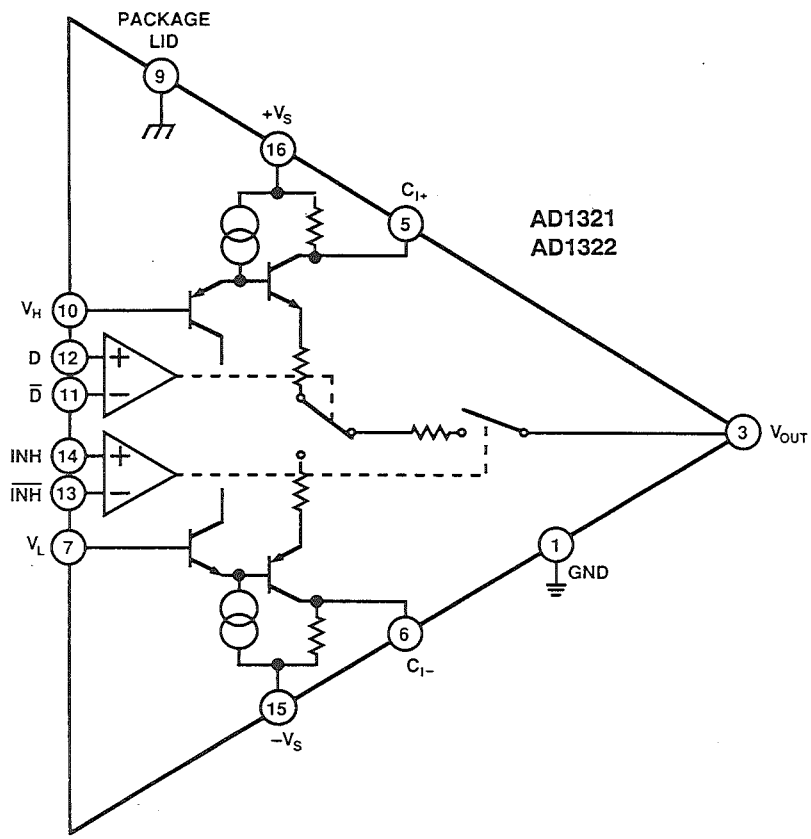
PART #	TYPE	TTL/ECL	PROP. DELAY	POWER DISSIPATION
[1] AD-96685	Single	ECL	3.5 ns MAX	135 mW MAX
[1] AD-96687	Dual	ECL	3.5 ns MAX	270 mW MAX
AD-9686	Single	TTL	7 ns MAX	306 mW MAX
[2] AD-9696	Single	TTL	6 ns MAX	351 mW MAX
[2] AD-9698	Dual	TTL	6 nx MAX	176 mW MAX
[3] AD-790	Single	TTL	40 ns MAX	60-240 mW

[1] DISPERSION = 50 ps TYP
[2] DISPERSION = 100 ps TYP
[3] WIDE COMMON MODE INPUT RANGE
SINGLE + 5 V OR ±15V SUPPLY OPERATION

Figure 6.11

AD1321 and AD1322 High Speed Pin Drivers

The AD1321 and AD1322 pin drivers are designed to be used in general purpose instrumentation and digital functional test equipment. The main difference between the AD1321 and AD1322 is rise and fall times. The AD1321 is best suited for operation at or below 100MHz, where the AD1322 is capable of greater than 200MHz operation. A block diagram of the AD1321 and AD1322 is shown in Figure 6.12. The purpose of the pin driver is to accept digital, analog and timing information from a system source known as the Formatter and combine these to drive the device under test. Simply stated, a pin driver performs the function of a precise, high speed level translator. Key features of the AD1321 and AD1322 are summarized in Figure 6.13.



HIGH SPEED PIN DRIVER BLOCK DIAGRAM

Figure 6.12

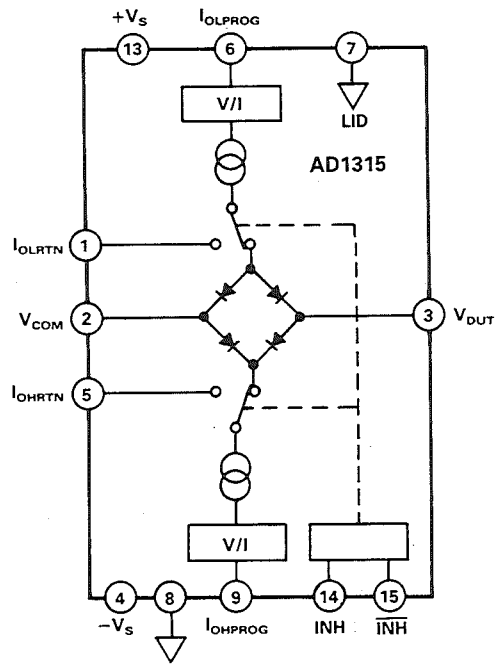
KEY FEATURES: AD1321/AD1322 PIN DRIVERS

- Driver Operation: 100MHz (AD1321), 200MHz (AD1322)
- Slew Rate: 1V/ns (AD1321), 2V/ns (AD1322)
- Edge Matching: 250 ps (AD1321), 200ps (AD1322)
- Variable Output Voltages for ECL, TTL, CMOS
- 50Ω Output Impedance
- Driver Inhibit Function
- High Speed Differential Inputs for Maximum Flexibility
- Hermetically Sealed Small Gull Wing Package

Figure 6.13

AD1315 High Speed Active Load

The AD1315 high speed active load is also used in the same tester application. The function of the active load is to provide independently variable source and sink currents for the device under test. The AD1315 block diagram is shown in Figure 6.14. An active load performs the function of loading the output of the device under test with a programmed I_{OH} and I_{OL}. These currents are independently programmed. V_{COM} is the commutation voltage point at which the load switches from a source to sink mode. The active load may also be inhibited, steering current to the IOLRTN and IOHRTN pins, effectively disconnecting it from the test pin. Key features of the AD1315 are summarized in Figure 6.15.



ACTIVE LOAD BLOCK DIAGRAM

Figure 6.14

6

KEY FEATURES: AD1315 ACTIVE LOAD

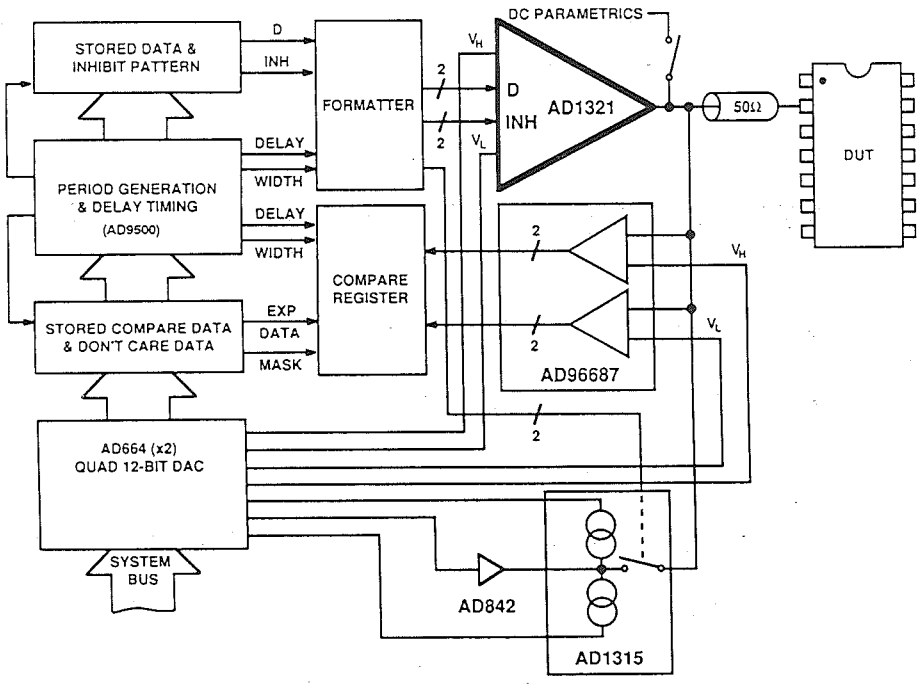
- ±50mA Voltage Programmable Current Range
- 1.5ns Propagation Delay
- Inhibit Mode Function
- High Speed Differential Inputs for Maximum Flexibility
- Hermetically Sealed Small Gull Wing Package
- Compatible with AD1321, AD1322 Pin Drivers

Figure 6.15

Tester Application

Figure 6.16 shows a block diagram illustrating the electronics behind a single pin of a high speed digital functional test system with the ability to test I/O pins on logic devices. As shown, the AD9500 programmable delay generator is used to define the shape, in time, of the digital waveform being constructed in the Formatter. It can also be used to correct each channel for timing deskews which may originate "downstream" from the Formatter (refer to Section VII). The Formatter waveforms, or vectors as they are called, are sent to the driver and active load.

The driver converts the ECL logic "1" to the programmed logic high level, V_H, and the ECL logic "0" to the programmed logic low level, V_L. Since these vectors have all been deskewed, any variation in propagation delay through the driver due to temperature and duty cycle will result in testing errors. The driver is required to swing the full TTL levels of +7V and down to the minimum ECL levels of -1.8V.



HIGH-SPEED DIGITAL TEST SYSTEM BLOCK DIAGRAM

Figure 6.16

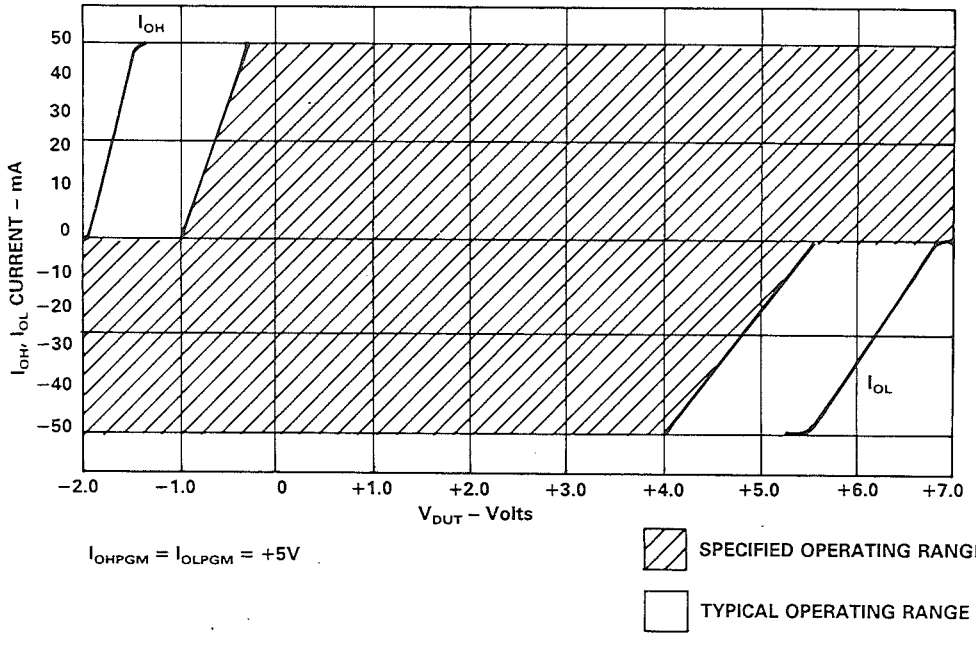
When the driver is stimulating the input of a device under test the output is normally being monitored to ensure that the output meets the data sheet logic "1" and "0" minimum and maximum logic voltage and current levels. As an example, for standard TTL logic, the driver will force a logic "1" of 2.4V at the output by driving the input to a logic low, or 0.8V. The output of the DUT must sustain a 2.4V level under a current load of -400μA. When the driver delivers a logic "1" to the DUT's input its output must sustain a 0.4V level while under a current load of 16mA. With a transfer function of 1V/10mA, the AD1315's logic high and low current program voltages are set at 1.6V and 0.4V, respectively (removing any gain and offset errors). The point at which the DUT changes from sink to source mode occurs when the DUT's output voltage passes through the programmed active load's commutation voltage, in this case 1.6V.

Similar to the driver, propagation changes through the active load due to variation in temperature and duty cycle will directly influence the overall accuracy of the tester. Recent advances in design and process technology allow the driver and active load functions to be developed in a single monolithic IC which greatly reduces these errors.

AD1315 V_{DUT} Voltage Range

In Figure 6.17, V_{DUT} range, I_{OH} and I_{OL} typical current maximums are plotted versus DUT voltage. In the I_{OH} mode (V_{DUT} higher than V_{COM}), the load will sink 50 mA, until its output starts to saturate at approximately -1.5V. In the I_{OL} mode (V_{DUT} lower than V_{COM}), the load will source 50 mA until its output starts to saturate at approximately +5.5V. At +7V, the source current will be close to zero.

Ideally, the commutation point set at V_{COM} would provide instantaneous current sink/source switching. Because of I/V characteristics of the internal bridge diodes, this is not the case. To guarantee full current switching at the DUT, at least a 1 volt difference between V_{COM} and V_{DUT} must be maintained in steady state conditions. Because of the relatively fast edge rates exhibited by typical logic device outputs, this should not be a problem in normal ATE applications.

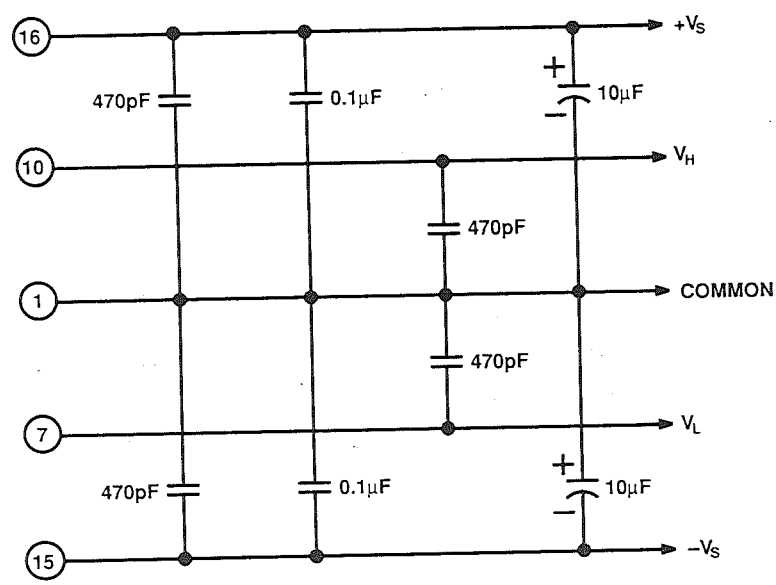


ALLOWABLE CURRENT RANGE FOR I_{OH}, I_{OL} vs. V_{DUT} FOR AD1315

Figure 6.17

Layout Considerations for AD1321/AD1322 Pin Drivers

Good engineering practice to capacitively decouple the power supplies is essential with high speed drivers where dynamic power supply current changes from -100mA to +100mA is required in only a few nanoseconds. A 470pF high frequency decoupling capacitor must be located within 0.25 inches of the +Vs and -Vs terminals to a low impedance ground. A 0.1μF capacitor in parallel with a 10μF tantalum capacitor should also be situated between the power supplies and ground; however, proximity to the device is less critical. Circuit performance will be similarly enhanced and noise minimized by locating a 470pF capacitor as close to V_H and V_L and connected to ground. Bypass considerations have been summarized in Figure 6.18.



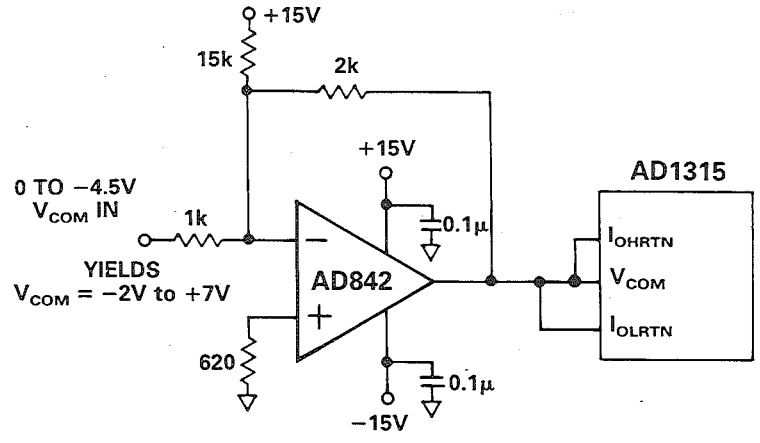
DECOUPLING CIRCUIT FOR AD1321/AD1322

Figure 6.18

Layout Considerations for AD1315 Active Load

I_{OHRTN} and I_{OLRTN} may be connected to any potential between -2V and +7V. These return points must be able to source or sink 50 mA, since the I_{OH} and I_{OL} programmed currents are diverted here in the inhibit mode. The RTNs may be connected to a suitable GND. However, to keep transient ground currents to a minimum, they are typically tied to the V_{COM} programming voltage point.

The V_{COM} input sets the commutation voltage of the active load. With DUT output voltage above V_{COM}, the load will sink current (I_{OH}). With DUT output voltage below V_{COM}, the load will source current (I_{OL}). Like the I_{OH} and I_{OL} return lines, the V_{COM} must be able to sink or source 50 mA; therefore a standard op amp will not suffice. An op amp with an external complementary output stage or a high power op amp such as the AD842 will work well here. A typical application is shown in Figure 6.19.



SUGGESTED I_{OHRTN}, I_{OLRTN}, V_{COM} HOOKUP

Figure 6.19