SECTION IV

HIGH SPEED OP AMPS

HIGH SPEED OP AMPS

HIGH SPEED OP AMP CHARACTERISTICS

Designers can choose from a variety of cost effective, high performance components. These include both voltage and current feedback (transimpedance) op amps in both hybrid and monolithic form. Depending on system requirements, the designer can also choose from bipolar or FET input op amps.

The trend in data acquisition is toward higher speed and accuracy. High performance amplifiers are required to drive cables, A/D converters, and also act as I to V converters on the outputs of fast D/A converters. Important specifications are wide bandwidth, DC accuracy, low harmonic distortion and fast settling with low overshoot.

KEY HIGH SPEED OP AMP SPECIFICATIONS

- Wide Bandwidth
- Low Harmonic Distortion
- Fast Settling Time
- Low Overshoot
- Low Noise
- High Output Current
- DC Accuracy

Figure 4.1

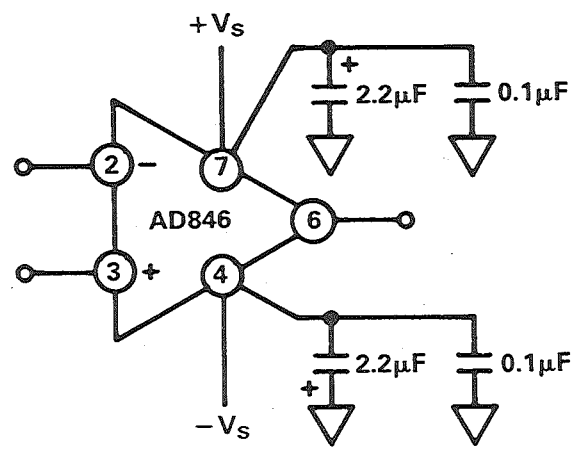
Each application has different requirements. For example, low bias current FET input op amps are useful in sample-and-hold (SHA) circuits and peak detectors. Current feedback op amps have low voltage noise, high bandwidths, and fast settling times while maintaining unity-gain stability. Voltage feedback op amps are cost effective, extremely versatile and are available in a wide range of bandwidths and precision.

Most of the circuits in this seminar are shown in simplified form in order to convey more clearly the principles involved. These circuits can successfully be used in actual applications by following the advice on precision high speed signal handling (grounding, decoupling, isolation, etc.) given in this section and Section X. The applications section of individual device data sheets will provide additional guidance in this respect.

GROUNDING AND BYPASSING

In designing practical high speed circuits some special precautions are needed. Circuits must be wired using short interconnect leads. Ground planes should be used on the component side of the P.C. board to provide both a low resistance, low inductance circuit path and to minimize the effects of high frequency coupling. IC sockets should be avoided, since their capacitance and inductance can degrade the bandwidth of the device.

Power supply leads should be bypassed to the ground plane as close as possible to the pins of the amplifier. Again, the component leads should be kept very short. As shown in Figure 4.2, a parallel combination of a 2.2 μF tantalum and a 0.1 μF ceramic disc capacitor is recommended for amplifiers with closed-loop bandwidths less than 50MHz. If the amplifier is driving a light resistive load (>1k Ω) and only 10pF - 20pF of capacitance, then the 2.2 μF capacitor may not be needed at each amplifier, but can be shared by amplifiers within 5cm power supply run of the capacitor.



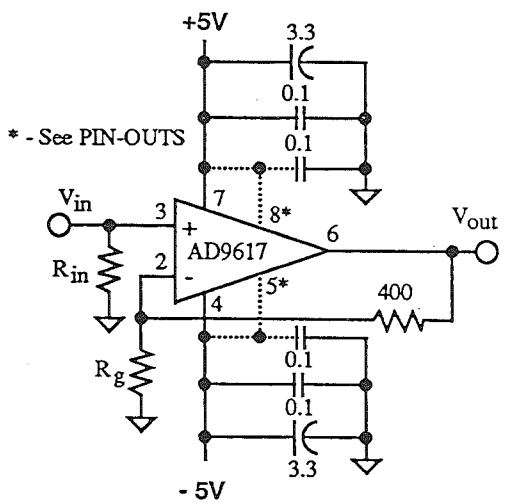
POWER SUPPLY BYPASSING FOR 50 MHz AMPLIFIERS

Figure 4.2

Amplifiers with 100MHz or higher bandwidths require additional bypassing and care in layout as illustrated in Figure 4.3. Note the use of parallel supply pins to reduce the lead inductance between the external bypass capacitors and the amplifier's internal circuitry. Using 0.1μF chip capacitors instead of 0.1μF discs further reduces lead inductance, and is highly recommended for amplifiers such as the AD9611, AD9617 and AD9618 with bandwidths of over 100MHz.

Temperature stable linear power supplies with low noise and ripple should be used for powering high speed circuits. Switching power supplies often seems to meet these criteria, including ripple specifications. However, ripple specs are generally expressed in volts rms which tends to obscure the peak amplitude of the output spikes generated by virtually all switching mode supplies. These spikes can produce virtually unfilterable noise peaks with amplitudes of several hundred millivolts.

If switching supplies are used, they should be carefully shielded, and their outputs should be well filtered right at the supply. They should also be located some distance from critical circuits to minimize electric field and magnetic field noise coupling.



POWER SUPPLY BYPASSING FOR 100+ MHz AMPLIFIERS

Figure 4.3

Special precautions should be taken in the selection of resistors, since many types of resistors have substantial parasitic capacitance. Bulk metal or carbon composition resistors have lower shunt capacitance than spirally wound types such as the RN55 series. Sockets should be avoided if possible because of their stray inductance and capacitance. If sockets are necessary, individual pin sockets (sometimes called "cage jacks") should be used. These contribute far less stray reactance than molded socket assemblies.

Evaluation boards are often available for ultra high-speed op amps. In some cases, suggested PC board layouts are shown on the individual op amp data sheets.

CLASSES OF HIGH SPEED DC COUPLED AMPLIFIERS

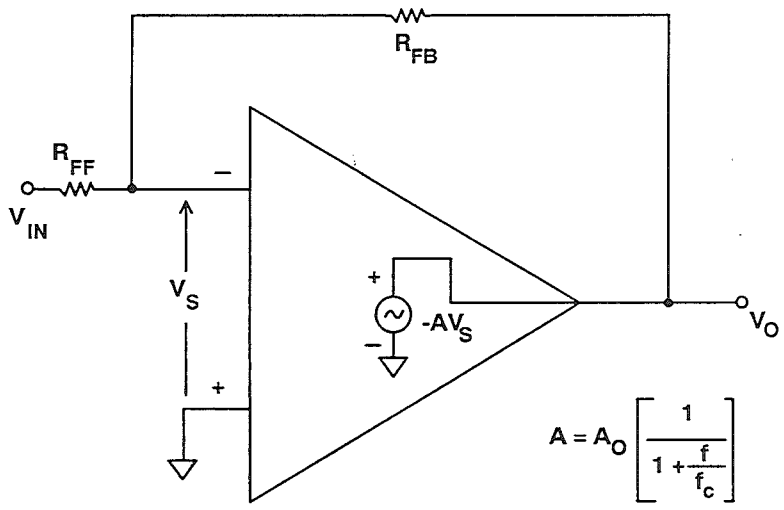
- Voltage Feedback Op-Amps
- Open-Loop Buffers
- Closed-Loop Buffers
- Current Feedback Op-Amps (Transimpedance Amplifiers)

Figure 4.4

HIGH SPEED VOLTAGE FEEDBACK OP AMPS

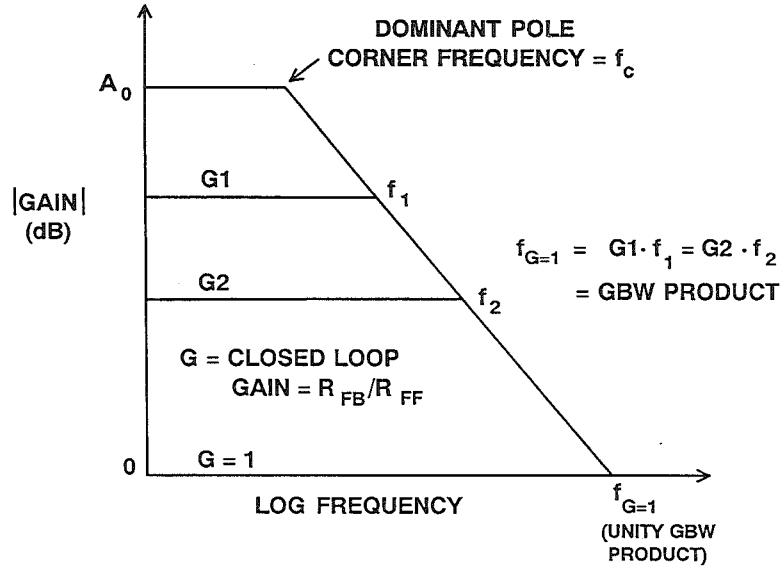
The equivalent circuit for a voltage feedback op amps is shown in Figure 4.5. Figure 4.6 shows the classic gain versus frequency response obtained with dominant pole compensation. The 6dB/octave rolloff is the optimum choice for best phase margin and fastest settling time. The product of the closed loop gain and the closed loop bandwidth (gain-bandwidth product) is constant for fixed compensation. The closed loop bandwidth therefore varies inversely with the closed loop gain.

A simplified schematic of a high speed voltage feedback is shown in Figure 4.7. For purposes of discussion the amplifier is shown in the inverting mode. The amplifier consists of a differentialinput stage (common emitter), a voltage amplification stage, and a Class AB (push-pull) output driver.



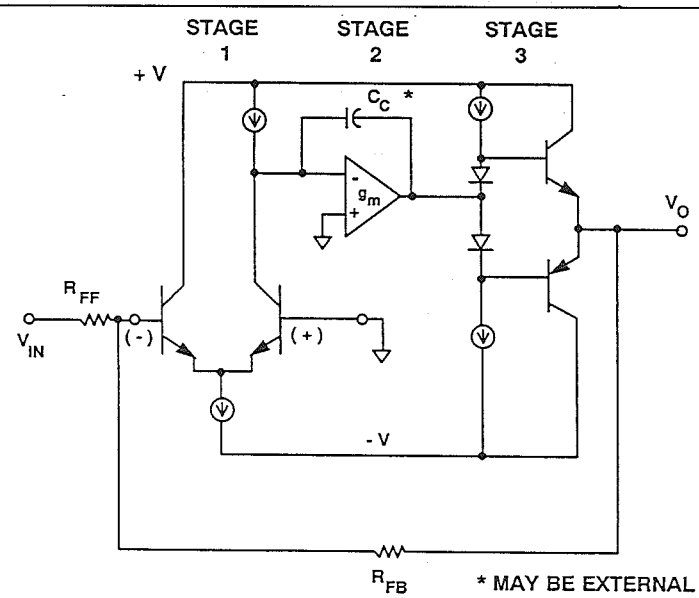
VOLTAGE FEEDBACK OP-AMP EQUIVALENT CIRCUIT

Figure 4.5



VOLTAGE FEEDBACK OP-AMP FREQUENCY RESPONSE

Figure 4.6

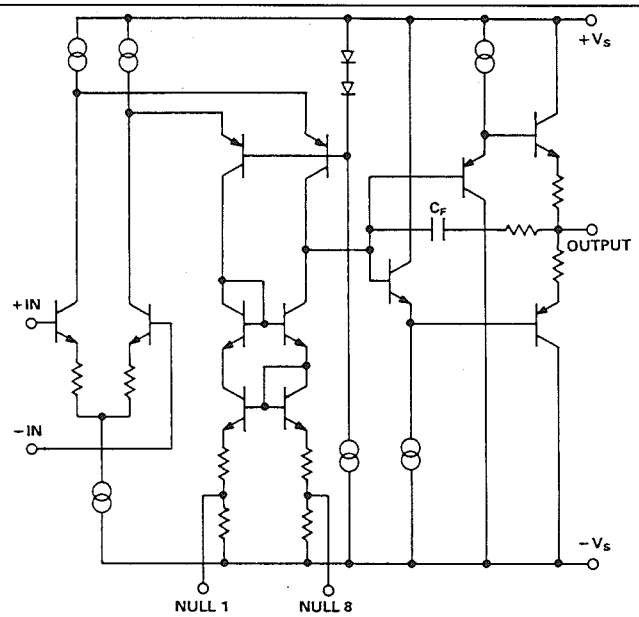


VOLTAGE FEEDBACK
OP-AMP CIRCUIT
Figure 4.7

A High Speed Voltage Feedback Op Amp: The AD847

The AD847 is fabricated on Analog Devices' proprietary complementary bipolar (CB) process which enables the construction of pnp and npn transistors with similar f_Ts in the 600MHz to 800MHz region. The AD847 circuit (Figure 4.8) includes an npn input stage followed by fast pnps in the folded cascade intermediate gain stage. The CB pnps are also used in the current amplifying output stage. The internal compensation capacitance that makes the AD847 unity gain stable is provided by the junction capacitances of transistors in the gain stage.

The capacitor, C_F, in the output stage mitigates the effect of capacitive loads. At low frequencies and with low capacitive loads, the gain from the compensation node to the output is very close to unity. In this case C_F is bootstrapped and does not contribute to the compensation capacitance of the part. As the capacitive load is increased, a pole is formed with the output impedance of the output stage. This reduces the gain, and therefore, C_F is completely bootstrapped. Some fraction of C_F contributes to the compensation capacitance, and the unity gain bandwidth falls. As the load capacitance is increased, the bandwidth continues to fall, and the amplifier remains stable.



AD847 SIMPLIFIED SCHEMATIC

Figure 4.8

VOLTAGE FEEDBACK OP AMP DYNAMIC CHARACTERISTICS

- Constant Gain-Bandwidth Product for Fixed Compensation
- External Compensation Allows High Gain Bandwidth Products
- Closed Loop Bandwidth (CLBW) Varies Inversely with Closed Loop Gain for Fixed Compensation

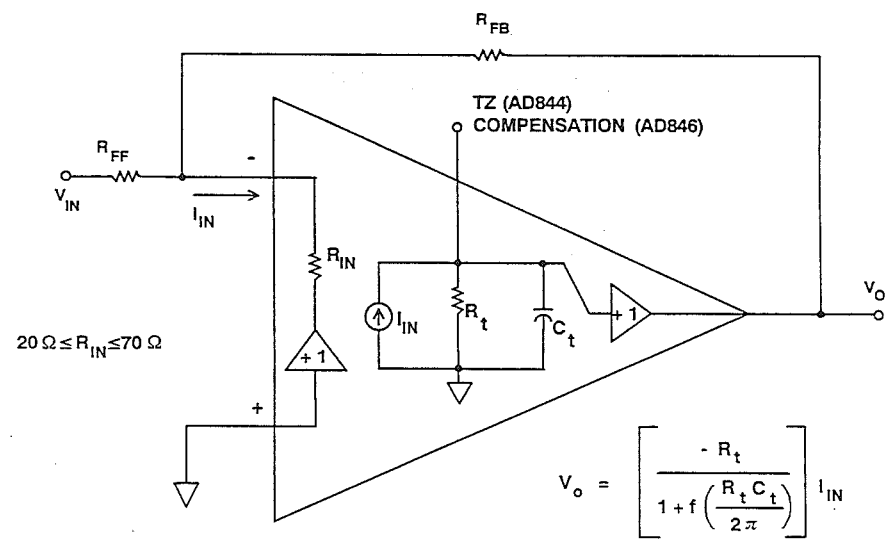
$$\frac{\text{CLBW (G = X)}}{\text{CLBW (G = 1)}} \approx \frac{1}{1 + \frac{R_{FB}}{R_{FF}}} = \frac{1}{1 - G}$$

- High Open Loop Input Impedance
- Parasitic Poles at Input Created at Summing Junction Can Compromise Bandwidth and Pulse Fidelity
- Symmetrical Inverting and Non-Inverting Inputs
- FET Input Transistors Reduce Input Bias Currents, Raise Input Impedance

Figure 4.9

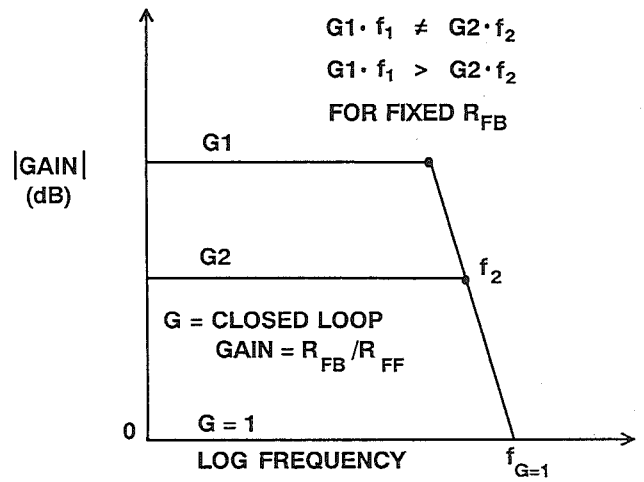
HIGH SPEED CURRENT FEEDBACK AMPLIFIERS

The equivalent circuit for a current feedback op amp is shown in Figure 4.10. An ideal current feedback amplifier has zero input impedance at its inverting input ($R_{IN} = 0$), infinite input impedance at its non-inverting input, and the voltage at the inverting input is held at that of the non-inverting by a unity gain buffer. The transfer function of this amplifier (V_O/I_{IN}) is a dimensional quantity (dimension R), not a ratio as in the case for voltage feedback op amps. Because of the very low (ideally zero) inverting input impedance, the current feedback op amp has a bandwidth which is more or less independent of closed loop gain for a fixed feedback resistor R_{FB}. This implies that the product of the closed loop gain and the closed loop bandwidth is not a constant, hence it is inappropriate to apply the term *gain bandwidth product* to current feedback amplifiers.



CURRENT FEEDBACK OP AMP EQUIVALENT CIRCUIT

Figure 4.10



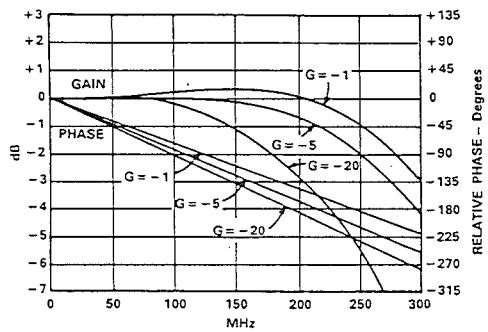
CURRENT FEEDBACK OP-AMP FREQUENCY RESPONSE

Figure 4.11

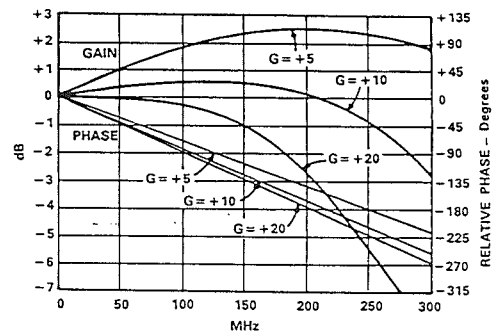
The closed loop bandwidth for the AD9611 high performance current feedback amplifier is shown in Figure 4.12. Note that the inverting 3dB bandwidth is approximately 300MHz for G = -1 and falls to only 200MHz for G = -20. A traditional voltage feedback amplifier's closed loop bandwidth would be reduced to 15MHz for G= -20 (assuming a unity gain bandwidth product of 300MHz). Note also that the phase linearity for this amplifier is excellent (typically better than 1° up to 120MHz).

The practical current feedback amplifier is based upon a common base input stage as shown in Figure 4.13. This configuration is characterized by a high impedance noninverting input which drives the inverting input via a unity gain buffer. The open loop inverting input impedance is approximately equal to any resistance in series with the emitter (R_E) plus the dynamic input impedance of the grounded base transistor (r_E). The output voltage is controlled by the input current and is related to it by the transimpedance gain expressed in ohms. Because of the low impedance inverting input common base stage, a stepped input voltage ΔV_{IN} will produce a stepped current in the emitter and collector of Q1. This will yield a slew rate of I_{IN}/C_C. Thus the rise and fall times of the output are essentially constant regardless of the output voltage swing. This attribute provides for exceptional fullpower bandwidth.

Bandwidth characteristics for several current feedback op amps are shown in Figure 4.14.



INVERTING

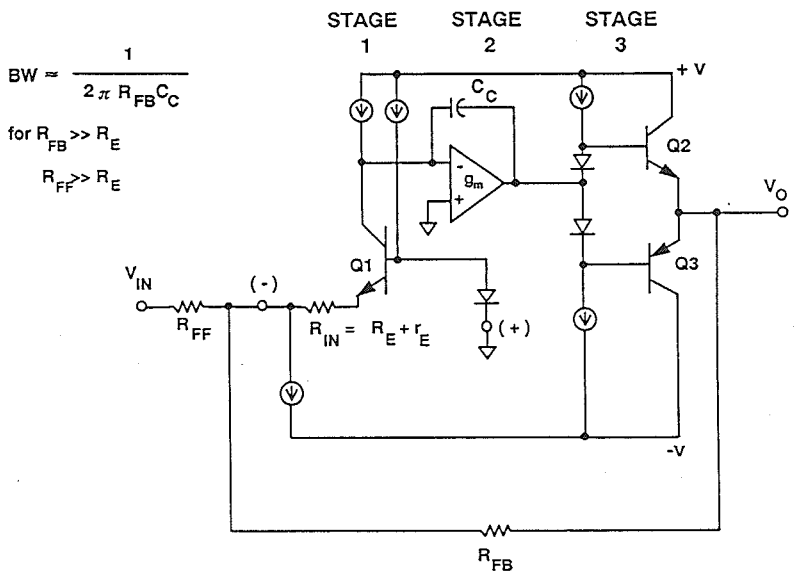


NON-INVERTING

GAIN AND PHASE VS. FREQUENCY FOR AD-9611

Figure 4.12

4



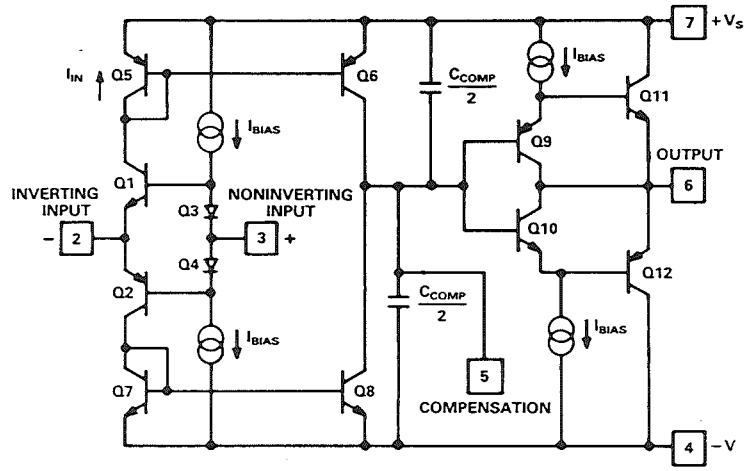
SIMPLIFIED CURRENT FEEDBACK OP-AMP CIRCUIT

Figure 4.13

CURRENT FEEDBACK OP AMP BANDWIDTH COMPARISONS

		AD846:		
R_{FB}	R_{FF}	GAIN	CLBW	"GBW"
1000Ω	1000Ω	-1	46 MHz	46 MHz
1000Ω	100Ω	-10	20 MHz	200 MHz
		AD844:		
R_{FB}	R_{FF}	GAIN	CLBW	"GBW"
500Ω	500Ω	-1	60 MHz	60 MHz
500Ω	50Ω	-10	33 MHz	330 MHz
		AD9617:		
R_{FB}	R_{FF}	GAIN	CLBW	"GBW"
400Ω	400Ω	±1	185 MHz	185 MHz
400Ω	27Ω	±15	105 MHz	1575 MHz
		AD9611:		
R_{FB}	R_{FF}	GAIN	CLBW	"GBW"
1000Ω	1000Ω	-1	300 MHz	300 MHz
1000Ω	50Ω	-20	200 MHz	4000 MHz

Figure 4.14



AD846 SIMPLIFIED SCHEMATIC

Figure 4.15

Figure 4.15 shows a simplified schematic of the AD846 current feedback amplifier which is implemented on a high speed complementary bipolar process.

Effects of Feedback Resistor on Bandwidth of Current Feedback Amplifiers

High speed current feedback amplifiers are usually optimized for a fixed value of feedback resistor. In the case of the AD9610, AD9611 and AD9615, the feedback resistor is included in the hybrid itself. One side of the resistor is connected internally to the inverting input and the other side is brought to a pin. For the AD844, AD846, AD9617 and AD9618, the feedback resistor is supplied by the user. In a current feedback amplifier, the value of the feedback resistor determines the location of the closed-loop dominant pole. As the feedback resistor is increased, the bandwidth for a given closed loop gain decreases as shown in Figure 4.16. If the feedback resistor is decreased, the bandwidth increases and phase margin decreases, possibly resulting in instability.

For high closed loop gains, it may be desirable to increase the feedback resistor so that the feed forward resistor can be made a reasonable value. If the feedback resistor is internal to the hybrid (AD9610,

EFFECT OF FEEDBACK RESISTOR VALUE ON CURRENT FEEDBACK AMPLIFIER BANDWIDTH

AD9611:

R_{FF}	R_{FB}	GAIN	CLBW
200Ω	1000Ω	- 5	280 MHz
300Ω	1500Ω	- 5	175 MHz
400Ω	2000Ω	- 5	135 MHz
500Ω	2500Ω	- 5	125 MHz

AD844:

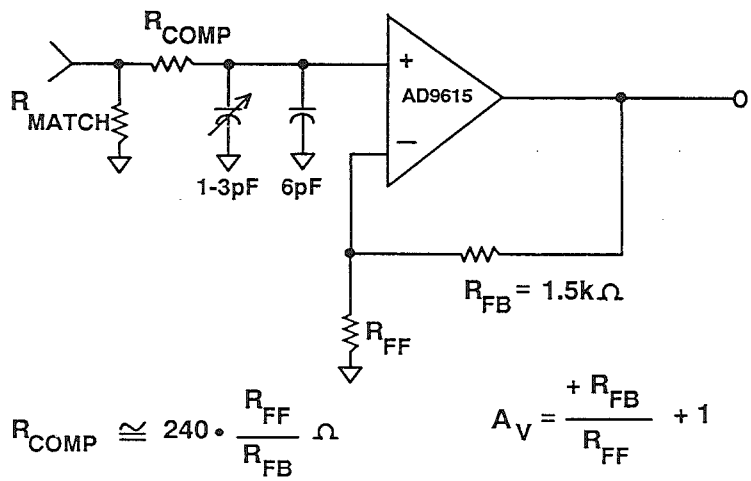
100Ω	500Ω	- 5	49 MHz
500Ω	1000Ω	- 2	30 MHz
1000Ω	2000Ω	- 2	15 MHz
1000Ω	5000Ω	- 5	5.2 MHz

Figure 4.16

AD9611, AD9615), the value of the feedback resistor should be increased by the addition of an external resistor of the appropriate value in series with the internal resistor. This will minimize the effect of the additional shunt capacitance in the feedback loop. The external resistor should be a low inductance, low capacitance type.

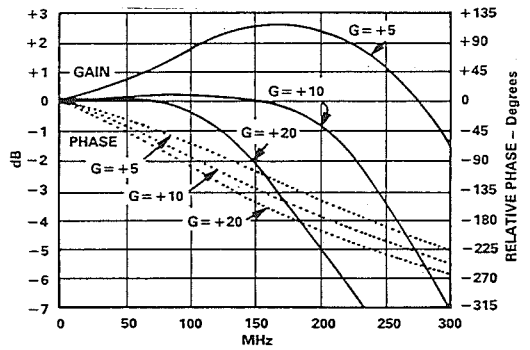
Compensating for Peaking in the Non-Inverting Mode (Current Feedback Op Amps)

Current feedback op amps which are optimized for best performance in the inverting mode may exhibit peaking for low closed loop gains when operated in the non-inverting mode. This peaking is made worse by adding additional stray capacitance to the inverting input. The peaking at low non-inverting gains can be reduced by the addition of a low-pass network to the non-inverting as shown in Figure 4.17. The results of this compensation are shown in Figure 4.18 for the AD9615 op amp.

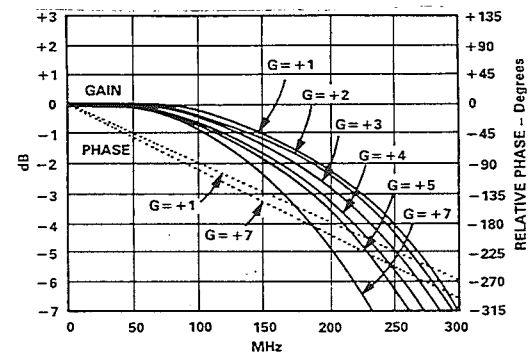


GAIN/FREQUENCY COMPENSATION FOR AD9615, NON-INVERTING MODE, LOW GAINS ($A_V \leq +8$)

Figure 4.17



NON-COMPENSATED



COMPENSATED

EFFECTS OF COMPENSATION ON GAIN/FREQUENCY PERFORMANCE OF AD9615 IN NON-INVERTING MODE

Figure 4.18

CURRENT FEEDBACK OP AMP DYNAMIC CHARACTERISTICS

- Bandwidth Less Sensitive to Closed Loop Gain Than Voltage Feedback Op Amps

$$\frac{\text{CLBW (G = X)}}{\text{CLBW (G = 1)}} \approx \frac{1}{1 + \frac{R_{IN}}{R_{FF}}} = 1,$$

For $R_{FF} >> R_{IN}$

- Wide Bandwidth
- Fast Settling
- Low Distortion (AD9617, AD9618)
- Low Inverting Input Impedance (Approx. 20Ω to 70Ω)
- Optimized and Compensated for Fixed Feedback Resistor R_{FB}

Figure 4.19

4

SETTLING TIME CHARACTERISTICS OF HIGH SPEED AMPLIFIERS

Settling time is defined as:

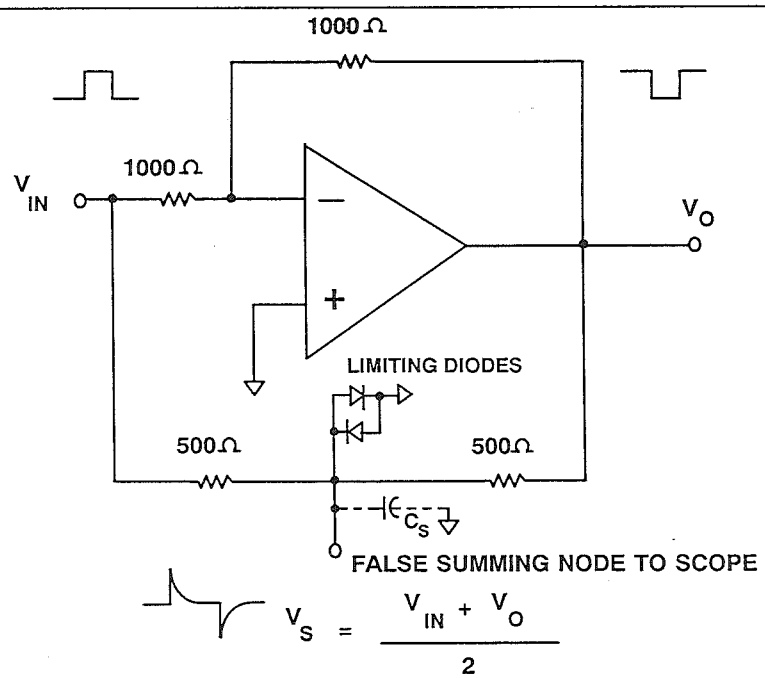
> The interval of time from the application of an ideal step function input until the closed-loop amplifier output has entered and remains within a specified error band.

This definition encompasses the major components which comprise settling time. They include (1) propagation delay through the amplifier; (2) slewing time to approach the final output value; (3) the time of recovery from the overload associated with slewing and (4) linear settling to within a specified error band.

Expressed in these terms, the measurement of settling time is obviously a challenge and needs to be done accurately to assure the user that the amplifier is worth consideration for the application.

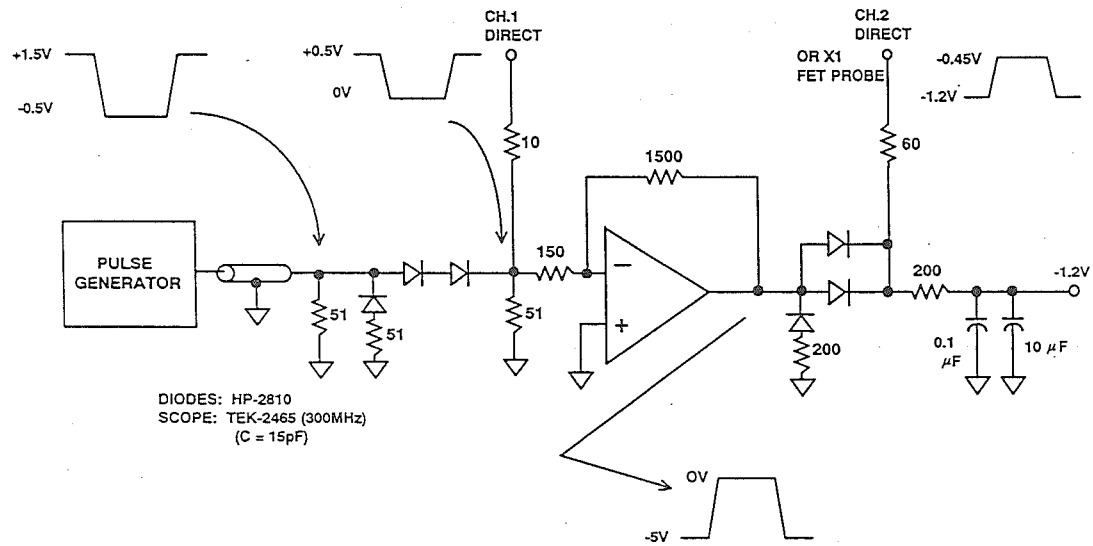
Settling times of high speed op amps are extremely fast. For example, the AD9617 op amp has a 3dB bandwidth of 180MHz and a settling time of only 14ns to 0.02%. The AD840, AD841, AD842 and AD846 all feature settling times of 100ns to 0.01%. Measuring settling times of less than 100ns in the inverting mode is usually accomplished by creating a false summing node with a resistive divider connected between the amplifier output and the input as shown in Figure 4.20. Care should be taken to insure that the time constant at the false summing junction created by the scope capacitance is less than that of the amplifier being tested. The back-to-back diodes help prevent oscilloscope overdrive. An alternative method for measuring settling time is shown in Figure 4.21. The diode network on the amplifier output limits the swing of the 5V output step to 0.75V. This step can be observed directly by the scope with approximately25mV/division vertical sensitivity without overdriving the input (see Figure 4.22). The diode network on the input of the amplifier insures that the pulse at the input of the feedforward resistor is flat.

The Data Precision 6100 Waveform Digitizer with the 640 Sampling Plug-In can be used to measure fullscale settling time directly without overdrive.



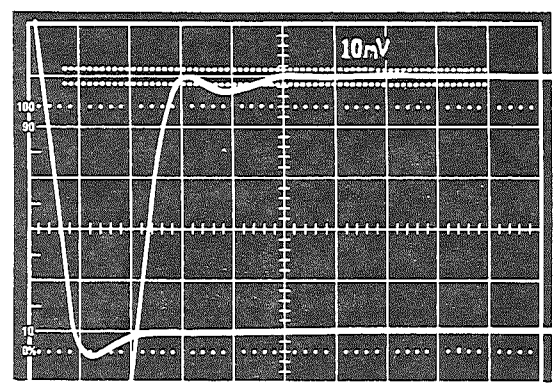
LESS THAN 100ns SETTLING TIME MEASUREMENT USING FALSE SUMMING NODE

Figure 4.20



SETTLING TIME TEST CIRCUIT

Figure 4.21



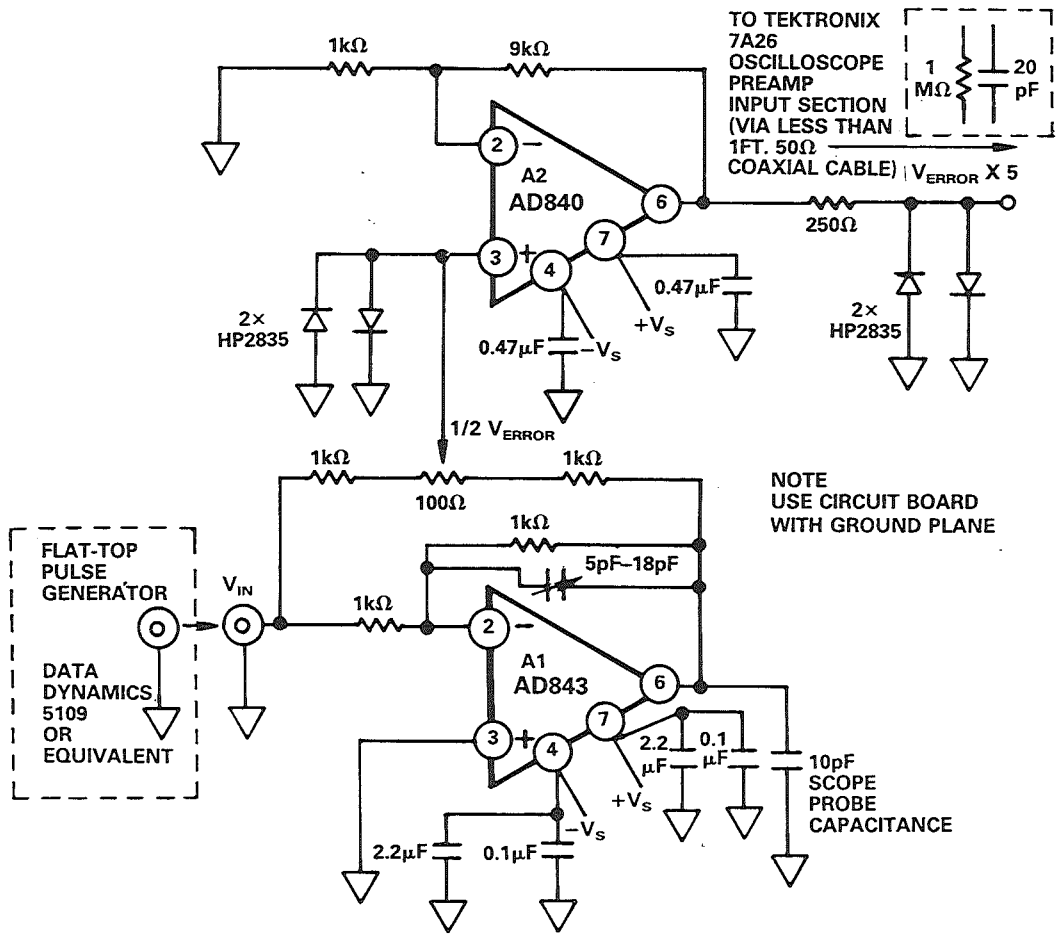
GAIN = −10; 5V OUTPUT; ERROR WINDOW (±5mV) = 0.1%; 5ns/DIV

AD9610 SETTLING TIME

Figure 4.22

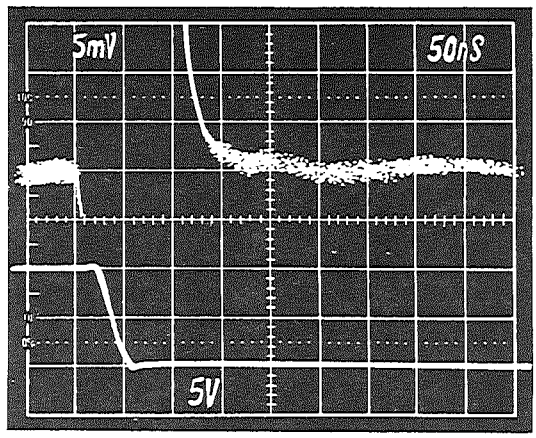
In order to duplicate results like these, excellent high speed layout techniques must be used. Attention must be given to insure a massive ground plane, compact layout, appropriate decoupling, and the use of pin sockets for the amplifier (if sockets must be used at all).

Another test configuration especially useful for measuring settling times of over 80ns to 12-bit accuracy (0.01%) is shown in Figure 4.23. This shows the test setup for the AD843 high speed FET input op amp which settles to 0.01% in less than 135ns. The actual settling time characteristics are shown in Figure 4.24.



GREATER THAN 80ns SETTLING TIME TEST CIRCUIT

Figure 4.23



UPPER TRACE: AMPLIFIED ERROR VOLTAGE (0.01%/DIV)

LOWER TRACE: OUTPUT OF AD843 (5V/DIV)

AD843 FET INPUT OP AMP SETTLING CHARACTERISTIC FOR +10V TO 0V STEP

Figure 4.24

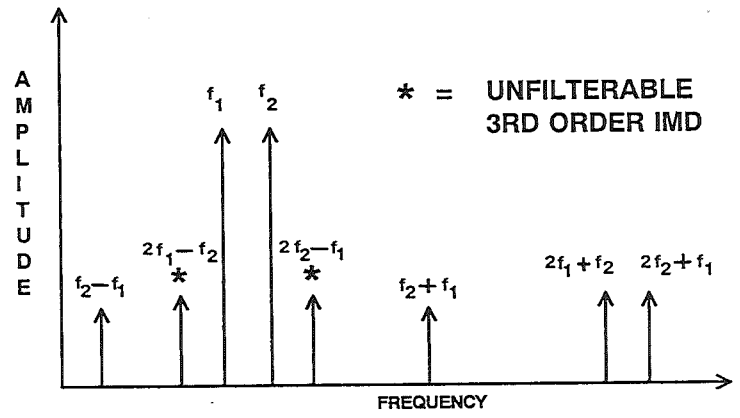
INTERMODULATION DISTORTION (IMD)

Intermodulation distortion occurs at frequencies that are the sam and/or different of integer multiples of the fundamental frequencies. Consider a non-linear amplifier with two large input signals at f_1 and f_2 (See Figure 4.25). The non-linearity gives rise to additional output components at $f_2 + f_1$ and $f_2 - f_1$: these are known as "second order intermodulation products". These second order products mix with the original signals and produce "third order intermodulation products" at frequencies of:

$2f_1 + f_2$ $\quad$ $2f_2 + f_1$

$2f_1 - f_2$ $\quad$ $2f_2 - f_1$

The third order products ($2f_1 - f_2$ and $2f_2 - f_1$) are a major nuisance in radio reception, especially in channelized systems, because they fall close to the signals causing them. Further discussion of IMD is given in the technical article at the end of this section as well as in Section V.



3RD ORDER INTERMODULATION DISTORTION

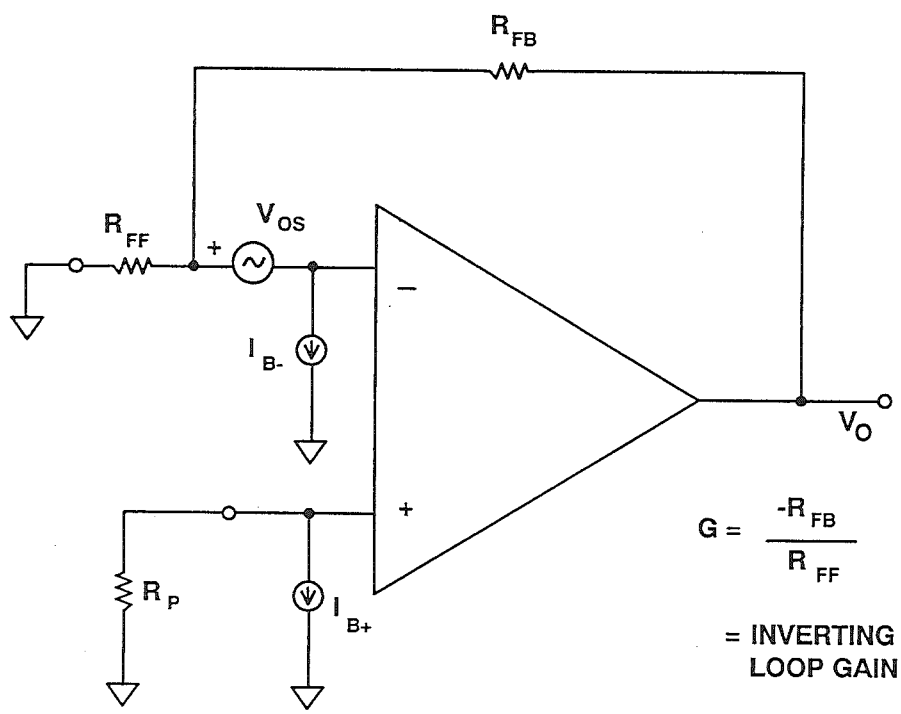
Figure 4.25

OP AMP BIAS CURRENT AND OFFSET VOLTAGE MODEL

Current feedback amplifiers must be treated somewhat differently from voltage feedback amplifiers when making output offset voltage calculations. The inverting and non-inverting inputs of standard voltage feedback op amps have similar characteristics, therefore the input bias currents are usually similar. In a current feedback amplifier, however, the inverting input is a low impedance emitter, while the non-inverting input is a high impedance. It is therefore quite likely that the respective input bias current characteristics will be different. The data sheet should always be consulted before making any assumptions.

A generalized bias current and offset voltage model for an op amp is shown in Figure 4.26. The equation for calculating the output offset voltage due to the input offset voltage and input bias currents is

easily derived by inspection. For op amps with well matched input bias currents, it is common to cancel the input bias currents by making $R_p = R_{FF} \parallel R_{FB}$. This is much less likely to be the case in current feedback op amps. Input offset voltages and bias currents are given in Figure 4.27 for several current feedback amplifiers. Due to differences in the inverting and non-inverting inputs, the input bias current temperature coefficients for current feedback amplifiers are likely to be different also. The data sheets should always be consulted.



OUTPUT OFFSET VOLTAGE =

$$V = (I_{B-})(R_{FB}) - (I_{B+})(R_P)(1 - G) + V_{OS}(1 - G)$$

V_{OS} = INPUT OFFSET VOLTAGE
I_{B-} = INVERTING INPUT BIAS CURRENT
I_{B+} = NONINVERTING INPUT BIAS CURRENT

OP-AMP OFFSET VOLTAGE/CURRENT MODEL

Figure 4.26

INPUT OFFSET VOLTAGE AND BIAS CURRENTS AT 25°C

	AD844	AD846	AD9610	AD9611	AD9615	AD9617/ 9618*
I_{B+}	0.15μA	0.003μA	15μA	5μA	2μA	12μA
I_{B-}	0.20μA	0.15μA	50μA	5μA	2μA	12μA
V_{OS}	50μA	25μA	1mV	3mV	1mV	0.5mV

*Typical Specs

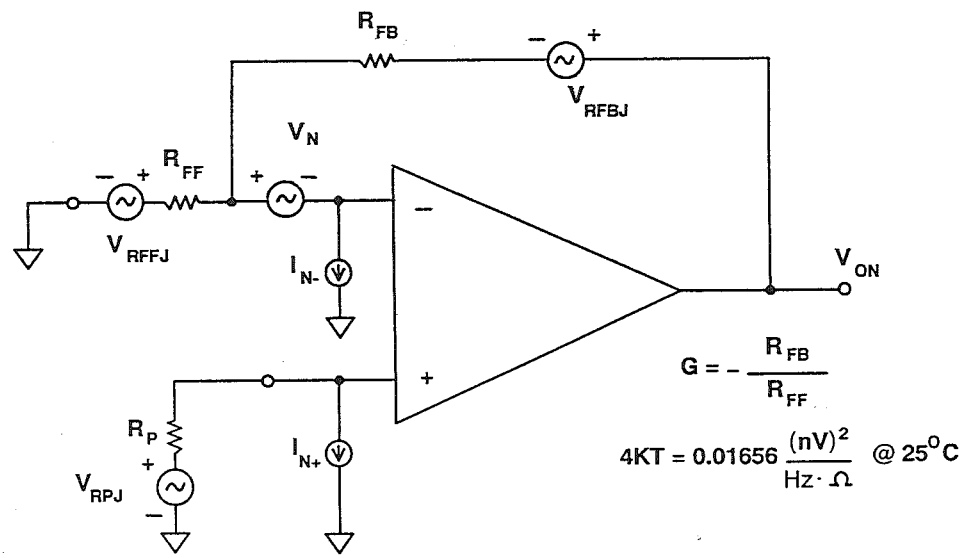
Figure 4.27

OP AMP NOISE MODEL

Current feedback amplifiers in general tend to be noisier than voltage feedback types when operating at low gains. The inverting and non-inverting input noise currents are also usually different. Figure 4.28 shows a generalized noise model which is applicable to all op amps including the current feedback variety. In addition to the input noise currents and voltages, the Johnson thermal noise voltages associated with the three resistors are also included. The equation is given for calculating the effective integrated output noise voltage in a given bandwidth. The appropriate values for I_{N-}, I_{N+}, and V_N are taken from the current and voltage noise spectral densities which are given on the data sheet. Usually the non-inverting input noise current I_{N+} is neglected because the non-inverting input is almost always grounded, bypassed, or driven from a low impedance source. In making noise performance comparisons between op amps, it is often useful to convert the output noise voltage to an effective integrated input noise voltage. This is easily accomplished by dividing the integrated output noise voltage by the noise gain, i.e., $1 + R_{FB}/R_{FF}$.

A noise current and voltage spectral density plot for the AD9611 is shown in Figure 4.29. The current noise is for the non-inverting and inverting input. Both the noise current and noise voltage are a function of frequency but flatten out above 10kHz where the 1/f current noise is no longer significant. In order to determine the effective noise over a bandwidth where the curves are not flat, the user must determine the areas under the respective curves for the bandwidth of interest.

Figure 4.30 shows a plot of the effective integrated output noise for the AD844 current feedback op amp. Note that at low closed loop gains the predominant noise source is the input current noise which flows through the feedback resistor (1000 Ω). For closed loop gains greater than 15, however, the effects of the "gained-up" input voltage noise begin to dominate the output noise.



EFFECTIVE INTEGRATED OUTPUT NOISE =

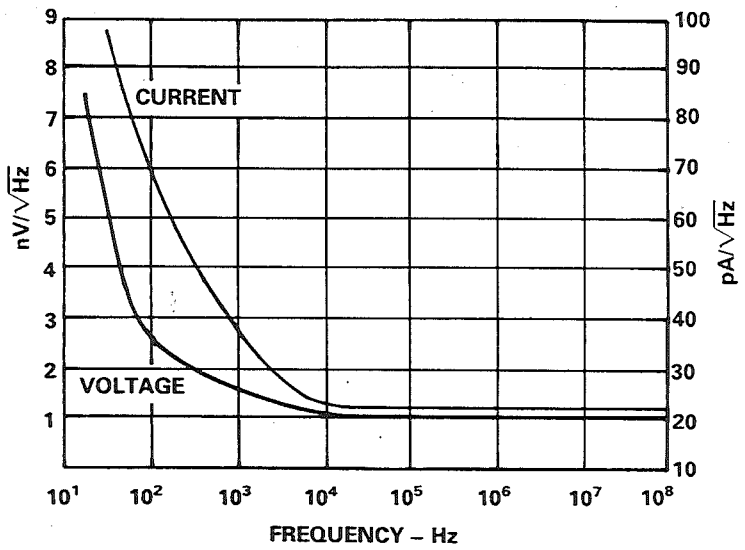
$$V_{ON} = \sqrt{BW}\left[I_{N-}^2 R_{FB}^2 + I_{N+}^2 R_P^2 (I-G)^2 + V_N^2 (I-G)^2 + 4KTR_{FB} + 4KTR_{FF} G^2 + 4KTR_P (I-G)^2\right]^{\frac{1}{2}}$$

EFFECTIVE INTEGRATED INPUT NOISE =

$$V_{IN} = \frac{V_{ON}}{I - G}$$

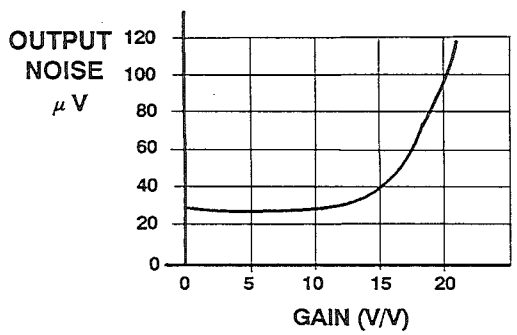
OP-AMP NOISE MODEL

Figure 4.28



INPUT NOISE VS. FREQUENCY FOR AD9611

Figure 4.29



BW = 10MHz

R_{FB} = 1000 Ω

R_P = 0

EQUIVALENT INTEGRATED OUTPUT NOISE VS. GAIN FOR AD844

Figure 4.30

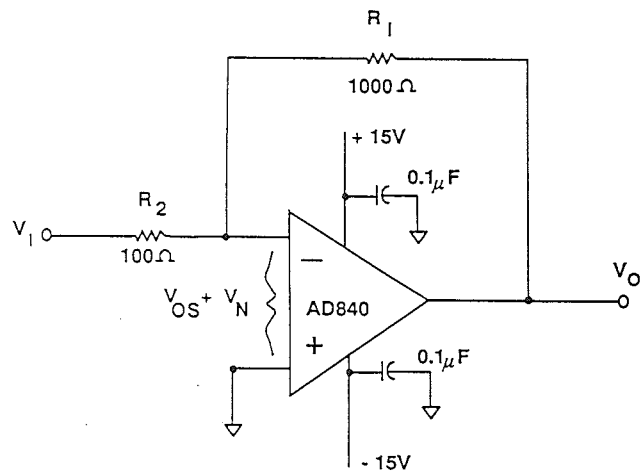
Stabilizing High Gain Op Amps at Lower Gain

In some cases, it is convenient to use an op amp that is internally compensated to be stable at a high closed loop gain at a lower gain. For example, this may minimize the number of amplifier types that are required to fill the sockets in an instrument.

The way to accomplish this is to operate the amplifier at a higher noise gain than signal gain, as illustrated in Figure 4.31 and 4.32, for a G = 10 stable amplifier in the inverting configuration. This technique can be applied to followers, but it is much trickier since the circuits' stability will depend on the input signal's source impedance.

The AD840 is stable in the inverted circuit Figure 4.31 because it is operating at a noise gain of 11 which is greater than its minimum stable noise gain of 10. In this case, the magnitude of the noise and signal gains are almost equal.

Figure 4.32 illustrates the extension of the Figure 4.31 circuit to stable operation at a gain of -1, which implies a noise gain of 2,



$G = -\frac{R_1}{R_2}$ = SIGNAL GAIN = -10

$1 - G = 1 + \frac{R_1}{R_2}$ = NOISE GAIN = 11

$V_O = -\frac{R_1}{R_2} \cdot V_1 + \left(1 + \frac{R_1}{R_2}\right)\left(V_{OS} + V_N\right)$

$V_O = -10\,V_1 + 11\,(V_{OS} + V_N)$

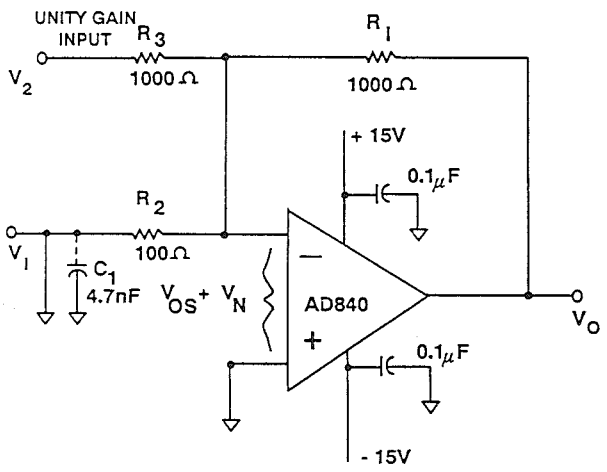
SIGNAL GAIN NOISE GAIN

V_{OS} = INPUT OFFSET VOLTAGE

V_N = INPUT NOISE VOLTAGE

NORMAL INVERTING MODE CONFIGURATION FOR MINIMUM GAIN (G = 10) OPERATION: AD840

Figure 4.31



$$V_O = -\frac{R_1}{R_2} \cdot V_1 - \frac{R_1}{R_3} \cdot V_2 + \left(1 + \frac{R_1}{R_2 \| R_3}\right)(V_{OS} + V_N)$$

$$= -10V_1 - V_2 + 12\,(V_{OS} + V_N)$$

FOR $V_1 = 0$

$$V_O = -1\,V_2 + 12\,(V_{OS} + V_N)$$

SIGNAL GAIN — NOISE GAIN

FOR V_1 GROUNDED THROUGH C_1:

$$V_O = -V_2 + 2V_{OS} + 12V_N$$

LOW GAIN OPERATION FOR OP AMP WITH G_{MIN} = 10, THE AD840

Figure 4.32

far lower than the factor of 10 the AD840 requires for stability. A 1kΩ resistor is connected to the inverting terminal to provide a unity gain input for V_2. The G = -10 input, V_1, is grounded to maintain the high noise gain required for stability. Alternatively, a signal can be applied to the V_1 input from a source with an impedance much less than the 100Ω value of R_2. In this case, the output voltage will be:

$$V_0 = -10V_1 - V_2 + 12 \text{ (offset + noise)}$$

Note that the amplifiers input offset and noise "see" the noise gain of 12 so essentially this circuit trades off increased output noise and drift to achieve stability at G = -1. The output offset error can be substantially reduced by AC coupling the V_1 input (through C_1). The R_2C_1 time constant should be about 500ns (or about 100 times the circuit closed loop time constant of 5ns) to minimize distortion of the pulse response.

The small signal -3dB bandwidth will be the same for either the V_1 or V_2 inputs and in this case will be approximately 40MHz, the AD840's closed loop bandwidth at G = 10.

If the V_1 input is left open or is driven from high (>>100Ω) source impedance, the noise gain will be 2 and the circuit will oscillate. This technique can be extended to a larger number of arbitrarily weighted inputs or to other minimum stabile noise gains by insuring that this condition is met:

$$1 + \frac{R_1}{R_2 \| R_3 \| \cdots R_N} \geq G_{MIN},$$

Where G_{MIN} is the specified minimum stable (noise) gain of the amplifier.

Driving Capacitive Loads with Wideband Op Amps

Most wideband amplifiers are sensitive to capacitive loading. In general, the higher the closed loop operating bandwidth, the greater the sensitivity.

A wideband amplifier will usually tolerate a small amount of capacitive loading and still maintain rated performance specifications. As the capacitive loading is increased, the performance is degraded (longer settling time, ringing and overshoot, etc.). Unless the amplifier has been designed to be unconditionally stable for all capacitive loads (AD847, AD848, AD849), as the capacitive loading is further increased, a point will be reached where the amplifier becomes unstable and oscillates. In order to prevent this instability, external compensation circuits are required which will reduce the overall closed loop bandwidth.

A list of wideband amplifiers and their relative tolerance to capacitive loads is given in Figure 4.33 and Figure 4.34.

VOLTAGE FEEDBACK OP AMP CAPACITIVE LOADING

MODEL	BW AT MIN CLOSED LOOP GAIN	C_L MAX FOR RATED PERFORMANCE	C_L MAX FOR STABILITY
AD840	40 MHz	20 pF	100 pF
AD841	40 MHz	20 pF	100 pF
AD842	40 MHz	20 pF	100 pF
AD843	35 MHz	20 pF	100 pF
AD845	16 MHz	20 pF	100 pF
AD847	50 MHz	10 pF	NO LIMIT
AD848	35 MHz	10 pF	NO LIMIT
AD849	30 MHz	10 pF	NO LIMIT

Figure 4.33

CURRENT FEEDBACK OP AMP CAPACITIVE LOADING

MODEL	BW AT MAIN CLOSED LOOP GAIN	C_L MAX FOR RATED PERFORMANCE	C_L MAX FOR STABILITY
AD844	67 MHz	10 pF	100 pF
AD846	46 MHz	20 pF	100 pF
AD9610	100 MHz	10 pF	10 pF
AD9611	300 MHz	5 pF	5 pF
AD9615	250 MHz	5 pF	5 pF
AD9617	185 MHz	10 pF	10 pF
AD9618	160 MHz	10 pF	10 pF

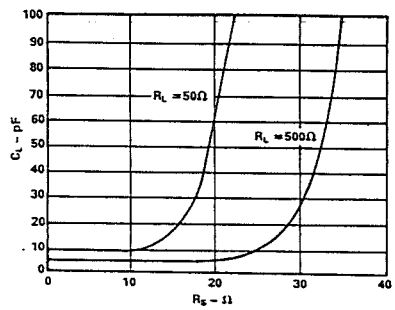
Figure 4.34

Various circuits can be used to compensate for excessive ringing, peaking and instability when driving capacitive loads. A series resistor between the op amp output and the capacitive load is often used. The graph is Figure 4.35 shows how to select the appropriate series isolation resistor R_S as a function of the capacitive and resistive load for the AD9611 and AD9615 current feedback op amps.

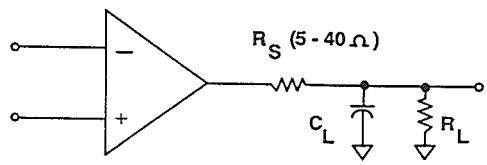
Figure 4.36 shows a typical circuit for driving a large capacitive load with the AD841 voltage feedback op amp. The 51Ω output resistor isolates the high frequency feedback from the load and stabilizes the circuit. Low frequency feedback is returned to the summing junction via the low pass filter formed by the 51Ω resistor and the load capacitance C_L.

Figure 4.37 shows a similar circuit using the AD843 BiFET op amp to drive a 110pF load. Pulse response is shown in Figure 4.38. The AD843 is configured as a unity gain non-inverting buffer. In Figure 4.39, the AD843 is configured as a unity gain inverter, and its response is shown driving a 410pF load in Figure 4.40.

A circuit for driving a 1000pF load using the AD844 current feedback amplifier is shown in Figure 4.41. The feed forward-network is connected between the TZ pin (pin 5) and the output pin (pin 6). By using this external network capacitive drive capability can be extended to over 10,000pF, limited only by the internal power dissipation.

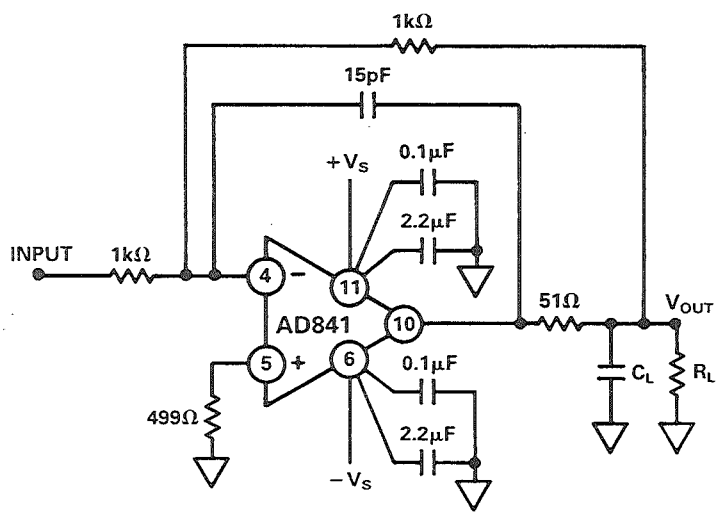


AD9611 CURRENT FEEDBACK
AD9615 OP AMPS



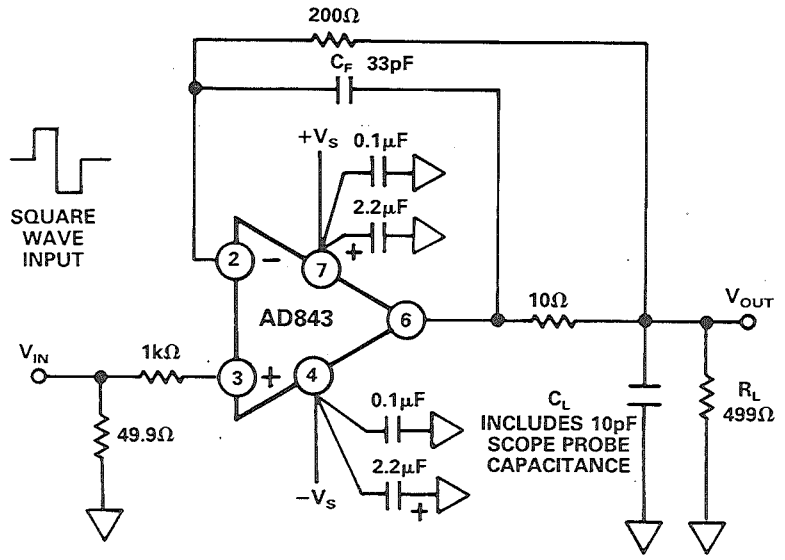
COMPENSATION WHEN DRIVING CAPACITIVE LOADS

Figure 4.35



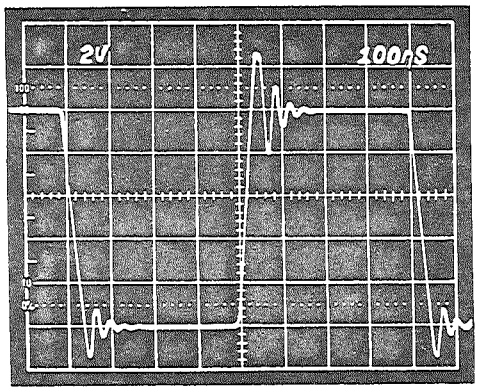
CIRCUIT FOR DRIVING A LARGE CAPACITIVE LOAD WITH THE AD841

Figure 4.36

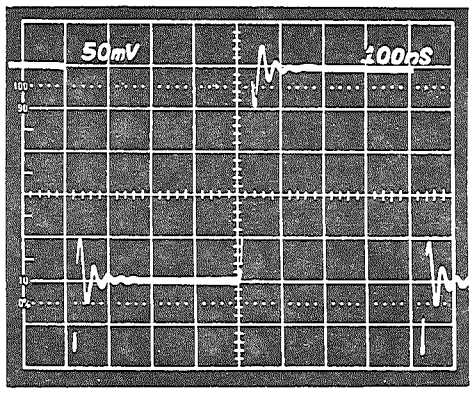


UNITY GAIN BUFFER CIRCUIT FOR DRIVING CAPACITIVE LOADS WITH THE AD843

Figure 4.37



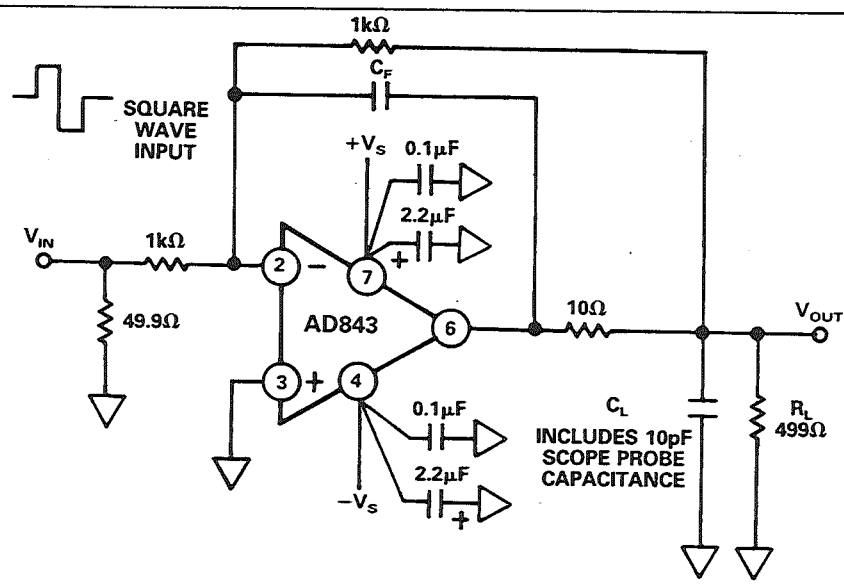
LARGE SIGNAL



SMALL SIGNAL

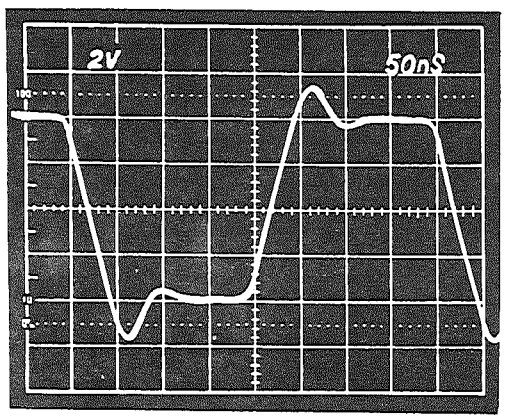
AD843 BUFFER RESPONSE, C_L = 110pF, C_F = 33pF

Figure 4.38

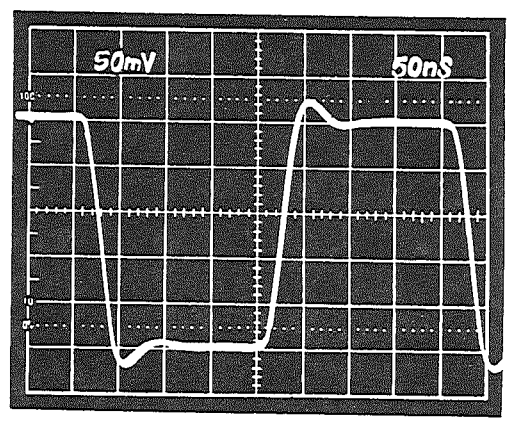


UNITY GAIN INVERTER CIRCUIT FOR DRIVING CAPACITIVE LOADS WITH AD843

Figure 4.39



LARGE SIGNAL

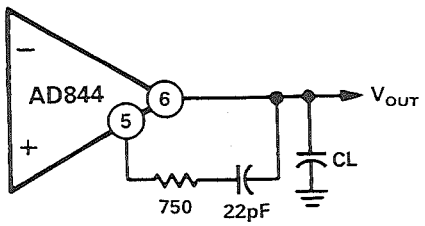


SMALL SIGNAL

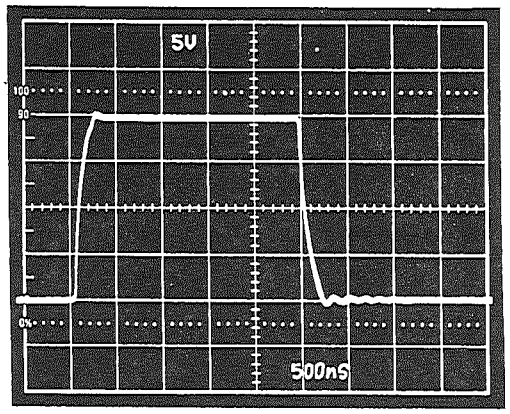
AD843 INVERTER RESPONSE, C_L = 410pF, C_F = 15pF

Figure 4.40

The AD847, AD848 and AD849 voltage feedback op amps are internally compensated to remain stable driving any value of capacitive load. The photographs in Figure 4.42 show the large signal pulse response of the AD847 driving a 100pF and a 1000pF load.



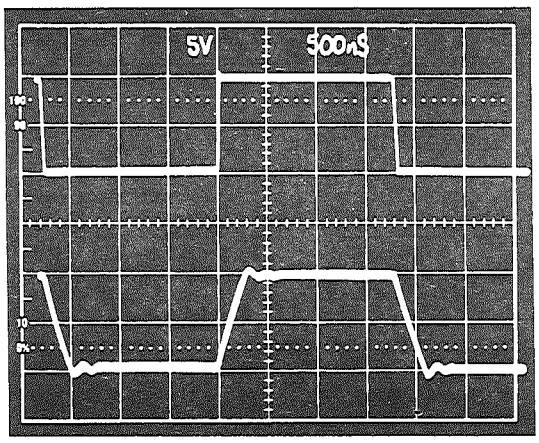
FEED FORWARD NETWORK
FOR LARGE CAPACITIVE LOADS



PULSE RESPONSE
FOR C_L = 1000pF

DRIVING LARGE CAPACITIVE LOADS WITH THE AD844

Figure 4.41

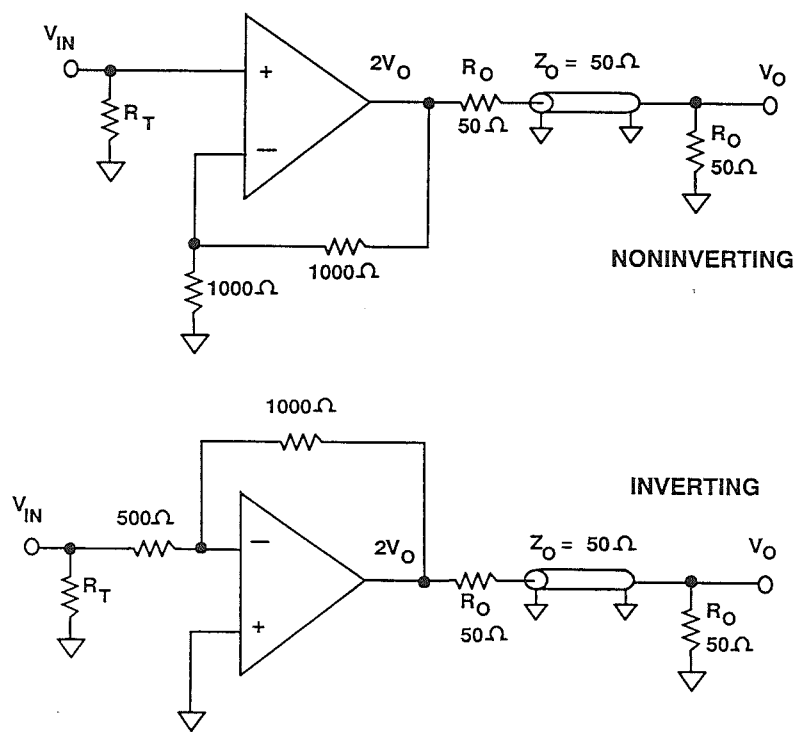


AD847 DRIVING A CAPACITIVE LOAD - NO EXTERNAL COMPENSATION

Figure 4.42

High Speed Cable Drivers and Receivers

High speed amplifiers are ideally suited for driving coaxial cables. The preferred methods are shown in Figure 4.43. Best performance is obtained by both series and load terminating the cables in order to prevent unwanted reflections. This requires that the amplifier be configured for a gain of 2 in order to maintain the original signal amplitude. If the cable is neither series or load terminated it appears as a capacitive load to the amplifier, and the suggestions in the previous section should be followed.

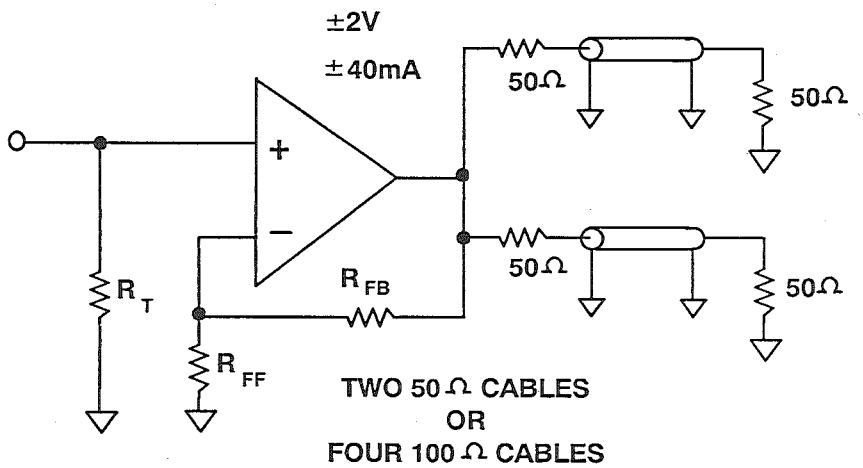


NONINVERTING AND INVERTING CABLE DRIVERS

Figure 4.43

Multiple cables can be driven by a single op amp as shown in Figure 4.44 provided the output current capability of the amplifier is not exceeded.

Appropriate values for the feedback and feedforward resistors are given in Figure 4.45 for a variety of wideband amplifiers.



DRIVING MULTIPLE CABLES

Figure 4.44

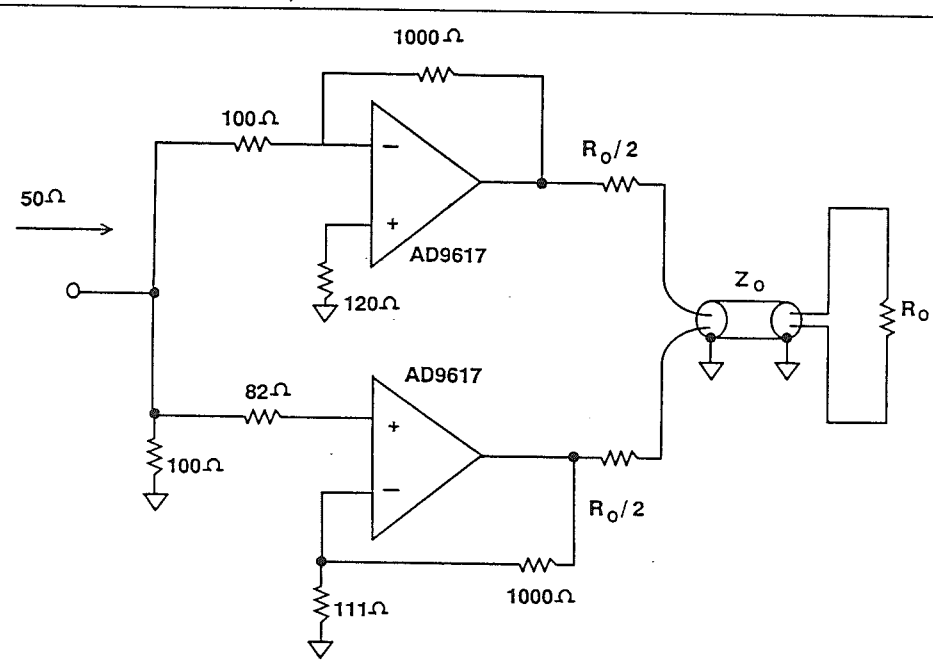
HIGH SPEED CABLE DRIVERS

MODEL	R_{FF}	R_{FB}	I_{OUT}	BW
AD841	402Ω	402Ω	50 mA	20 MHz
AD842	402Ω	402Ω	100 mA	40 MHz
AD847	402Ω	402Ω	25 mA	25 MHz
AD9610	1500Ω	1500Ω	50 mA	100 MHz
AD9611	1000Ω	1000Ω	40 mA	300 MHz
AD9615	1500Ω	1500Ω	40 mA	250 MHz
AD9617	402Ω	402Ω	50 mA	180 MHz

Figure 4.45

A circuit using two amplifiers to convert a single ended signal to a differential signal is shown in Figure 4.46. By using this circuit, a signal can be transmitted over a cable having high common mode noise.

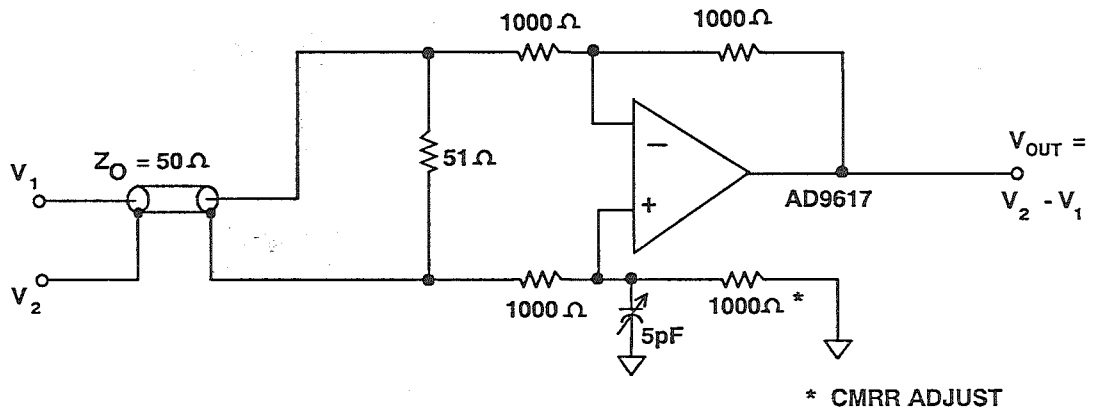
By receiving the signal with a wideband instrumentation amplifier, the common mode noise can be rejected, and the differential signal recovered at the output of the instrumentation amplifier.



SINGLE-ENDED TO DIFFERENTIAL CONVERSION

Figure 4.46

If the common mode rejection ratio at high frequencies is high enough, an op amp can effectively be used as a differential-to-single ended converter as shown in Figure 4.47. The circuit can be used to receive true differential signals or signals from coaxial cables with floating shields. Common mode noise is attenuated by the op amps CMRR.

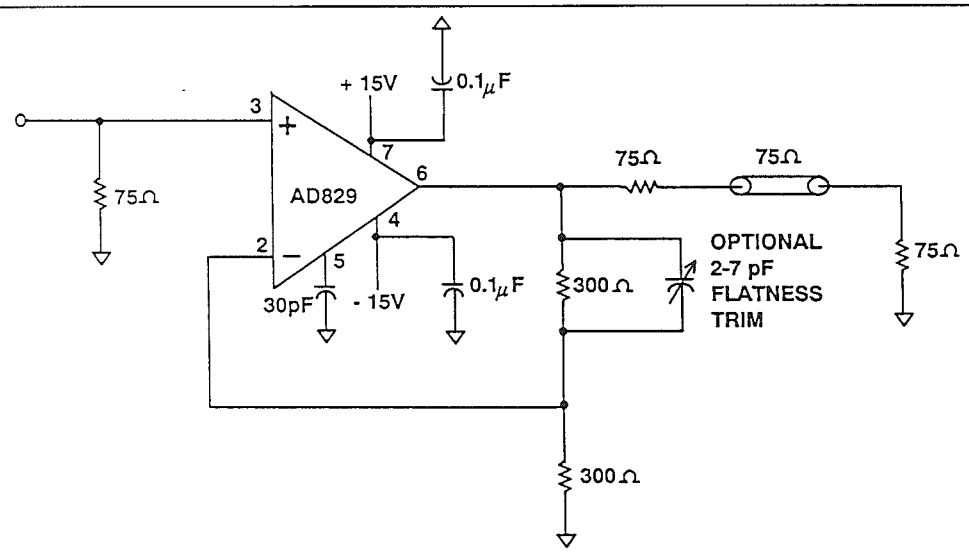


COAXIAL CABLE DIFFERENTIAL RECEIVER

Figure 4.47

Low Differential Gain and Phase Video Line Driver

The buffer circuit shown in Figure 4.48 will drive a back-terminated 75Ω video line to standard video levels (1V p-p) with 0.1 dB gain flatness to 30 MHz with only 0.02^0 and 0.02% differential phase and gain at the 4.43 MHz PAL color subcarrier frequency. This level of performance, which meets the requirements for high-definition video displays and test equipment, is achieved at just 6 mA quiescent current.



LOW DIFFERENTIAL GAIN AND PHASE
VIDEO LINE DRIVER: AD829

Figure 4.48

Precision Measurement of Differential Gain and Phase

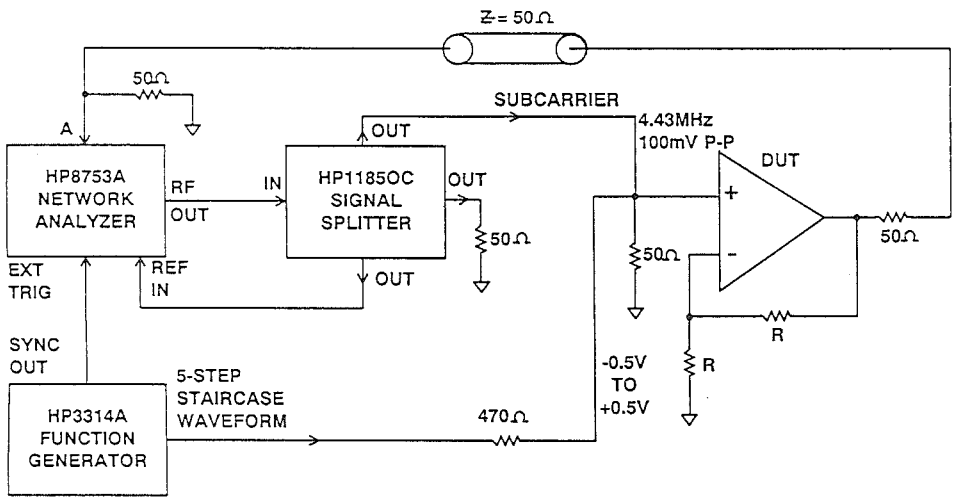
In a television transmission system, a phase- and amplitude-modulated subcarrier carries color (chrominance) information. In the National Television Standards Committed (NTSC) system used in the U.S. and Japan, the color subcarrier is at 3.58 MHz. The PAL (used in the U.K. and West Germany) and SECAM (used in France) systems use a 4.43 MHz color subcarrier. Any amplitude or phase modulation introduced on the subcarrier by the video transmission system can result in a color change for the viewer. Thus, video systems have stringent requirements for differential phase and gain, usually limiting changes to less than 0.1^0 and 0.1%.

These systems specifications mandate even more stringent standards for individual components, with the differential phase and differential gain requirements for the op amps used in video systems ideally approaching 0.01^0 and 0.01%. Measuring these levels exceeds the resolution of normal video test equipment, which is about the same as system-level specifications at 0.1^0 differential phase and 0.1% differential gain.

Figure 4.49 shows a high resolution setup that uses a HP3314A arbitrary waveform generator and a HP8753A network analyzer to measure differential phase and gain to 0.01^0 and 0.01% accuracy. The

arbitrary waveform generator generates a staircase that simulates the luminance (picture level) portion of a video waveform. The network analyzer supplies the color subcarrier waveform, in this case a 4.43 MHz color subcarrier. The network analyzer also measures the differences in the color subcarrier's phase and gain by comparing the output of the DUT and the reference signal returned by the HP11850 signal splitter.

Note that the 4.43 MHz color subcarrier and the staircase signal are summed at the input to the op amp. This summing action superimposes the color subcarrier on the staircase, thus generating the standard video test waveform. The differential phase and gain is defined as the maximum difference in the phase or gain between any of the steps in the staircase waveform. The differential phase and gain measurements are made and plotted separately. In each case, the horizontal scale shows the modulating staircase and the vertical scale shows the relative differences in phase and gain.

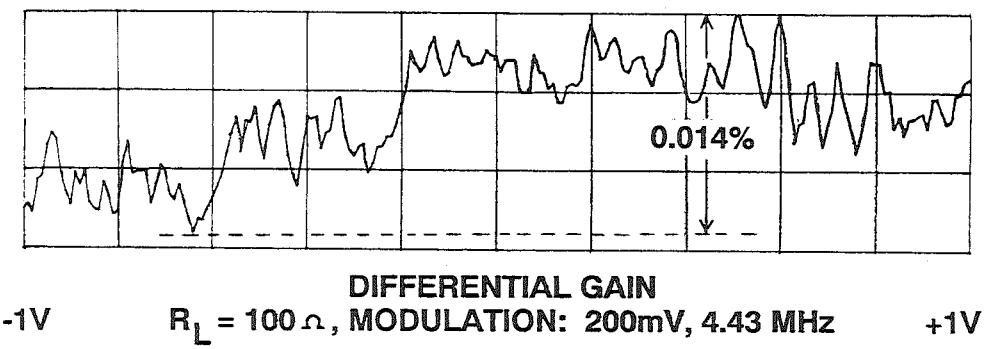


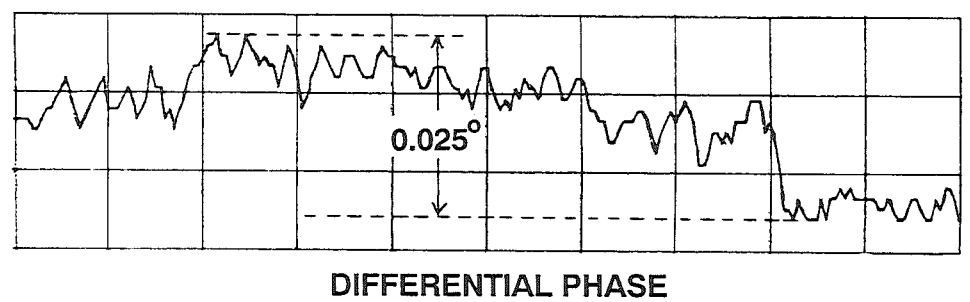
PRECISION MEASUREMENT
OF DIFFERENTIAL GAIN

Figure 4.49

Figure 4.50 shows the differential gain of the AD829 plotted at a scale of 0.005% per vertical division for a -1V to +1V staircase. Note that the total differential gain is 2.6 divisions, or 0.013%. Figure 4.50 also shows the AD829's differential phase plotted on a vertical scale of 0.01^0 per vertical division. Note that the total differential phase is 2.7 divisions, or 0.027^0.

The circuit in Figure 4.49 also shows an op amp connected as a gain-of-2 amplifier driving a 50Ω reverse-terminated line. The 50Ω termination resistor both absorbs reflections from the line and isolates the op amp from the capacitive load presented by the line. The 50Ω termination resistor and the 50Ω load form a voltage divider, so the net gain from the input to the DUT circuit to the load is unity. It should be noted that this represents a more stringent condition than conventional video systems where 75Ω is the standard impedance level.





AD829 DIFFERENTIAL GAIN AND PHASE

Figure 4.50

Driving A/D Converters

Wideband low distortion op amps are required to drive high performance A/D converters. Each A/D architecture (flash, successive approximation, and subranging) places unique requirements on the drive amplifier.

Flash ADCs require amplifiers of wide bandwidth and low distortion. Since a flash converter's input is capacitive, a small isolation resistor is often required between the op amp output and the flash converter input to maintain op amp stability. The input capacitance of the flash converter is usually signal-dependent, therefore the series resistor should be kept as small as possible to minimize non-linearities.

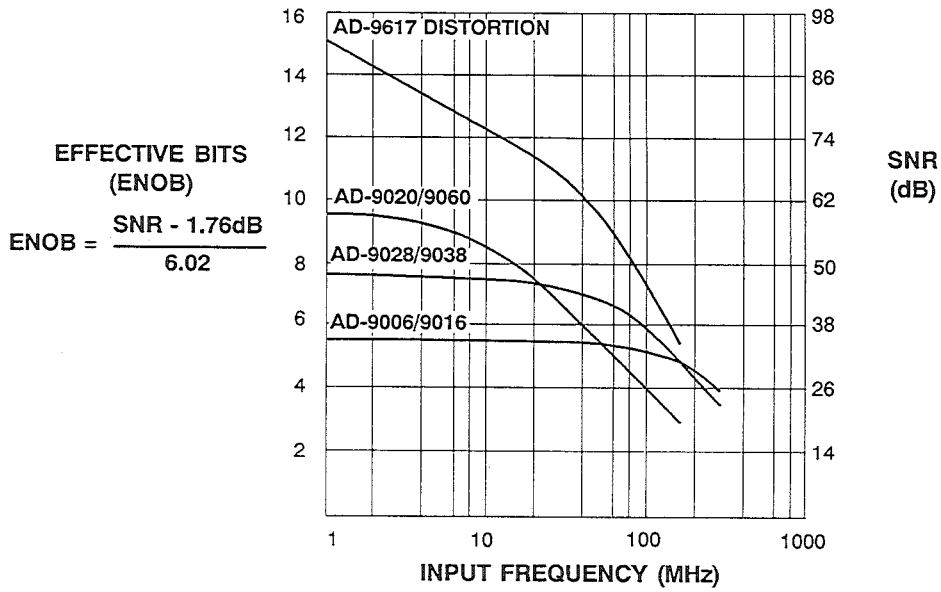
It is also important that the signal-to-noise ratio and harmonic distortion performance of the drive amplifier not degrade basic performance of the flash converter. Curves such as those shown in Figure 4.51 are useful in selecting the appropriate drive amplifier.

For successive approximation ADCs, the input current is modulated at the summing point of the comparator during each bit comparison. The amplifier must re-establish the proper input voltage within 1/2 LSB before the comparator output is latched, or an error will be induced. This requires that the op amp driving a successive approximation ADC must have a low output impedance at DC, at the signal frequency, and at the frequency of the conversion clock of the ADC.

The AD846 op amp meets this requirement for most successive approximation ADCs. It is also suitable for driving subranging ADCs such as the AD671. Its output impedance at an inverting gain of 10 is 10Ω at 10 MHz. Furthermore, the AD846 is easily configured as a clamped amplifier to protect the ADC input.

If dynamic signals are to be digitized by a successive approximation ADC, a suitable SHA will be required to drive the ADC. In this case, the same requirements discussed above apply to the SHA output.

In the case of "sampling" ADCs (with internal SHAs) the drive amplifier should be selected to exceed the performance of the ADC -- especially in terms of bandwidth, distortion and noise.



FLASH ADC	RESOLUTION	SAMPLING RATE
AD9020	10 BITS	40 MSPS
AD9060	10 BITS	60 MSPS
AD9028/9038	8 BITS	250 MSPS
AD770	8 BITS	200 MSPS
AD9002	8 BITS	125 MSPS
AD9012	8 BITS	75 MSPS
AD-9048	8 BITS	35 MSPS
AD9006/9016	6 BITS	400 MSPS

FLASH ADC AND OP AMP DYNAMIC PERFORMANCE

Figure 4.51

A/D CONVERTERS AND RECOMMENDED DRIVE AMPLIFIERS

MODEL	RESOLUTION	MAX. SAMPLING RATE	INPUT C	DRIVE AMPLIFIER
AD9688	4-Bits	175 MSPS	10pF	AD5539
AD9000	6-Bits	75 MSPS	35pF	AD844
AD9006/16	6-Bits	500 MSPS	8.5pF	AD9617, AD9611
AD9048	8-Bits	35 MSPS	16pF	AD847, AD844
AD9012	8-Bits	75 MSPS	16pF	AD9617, AD846
AD9002	8-Bits	125 MSPS	16pF	AD9617
AD770	8-Bits	200 MSPS	19pF	AD9617
AD9028/38	8-Bits	300 MSPS	17pF	AD9617
AD9020/60	10-Bits	60 MSPS	45pF	AD9617
AD9003	12-Bits	1 MSPS	5pF	AD846
AD9005	12-Bits	10 MSPS	5pF	AD9617

Figure 4.52

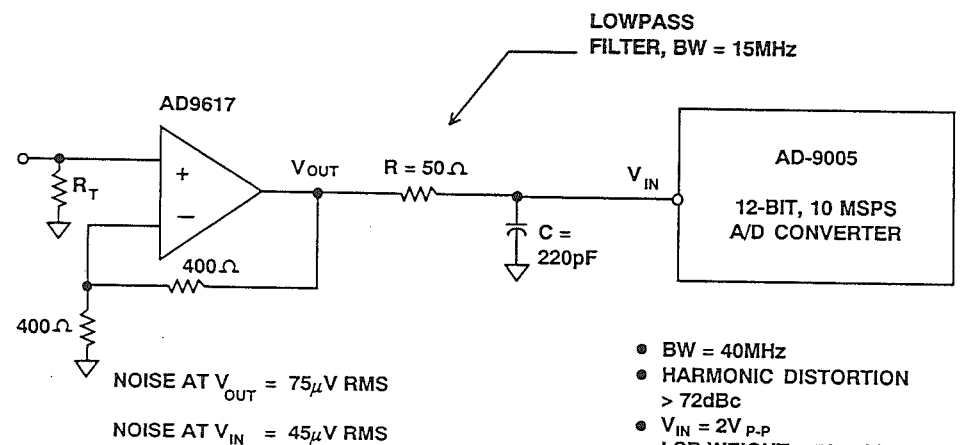
Driving High Performance 12-Bit A/D Converters

In order for the whole system to match the dynamic characteristics of the ADC itself, it is necessary to exercise great care in selecting amplifiers to drive such high speed, high performance converters as the AD9005 (a 12-bit 10MSPS ADC). For instance, the AD9005 front end bandwidth is 40MHz, and the harmonic distortion is 72dB down for a full-scale 4MHz input signal. The AD9617 current feedback amplifier harmonic distortion is approximately 80dB down under the same conditions, and will therefore not degrade the A/D converter distortion performance.

However, the effective integrated output noise voltage of the AD9617 in a 40MHz bandwidth is approximately 75 μV RMS, compared to the AD9005 LSB weight of 500 μV. A single pole lowpass filter having a 3dB bandwidth of 15MHz can be inserted between the amplifier and the A/D converter as shown in Figure 4.53.

This filter effectively reduces the RMS noise voltage to approximately 45 μV thereby improving the signal to noise ratio of the system without degrading the harmonic distortion.

The theoretical quantization noise for a 12-bit A/D converter with a 2-volt input range is $q/\sqrt{12}$, or 144 μV where q is the weight of the LSB. Combining the theoretical quantization noise of 144 μV and the integrated noise of 45 μV yields a theoretical value of 150 μV for the effective input noise to the A/D converter.



DRIVING A HIGH PERFORMANCE 12-BIT A/D CONVERTER

Figure 4.53

Use of High Speed Op Amps as D/A Converter Output Buffers

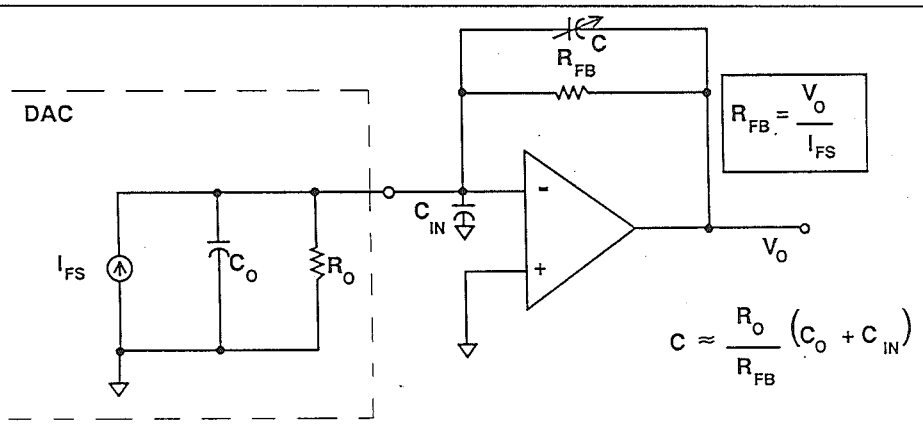
A D/A converter I to V conversion circuit using a voltage feedback op amp is shown in Figure 4.54. The value of the feedback resistor is chosen based on the fullscale D/A output current and the desired output voltage. The value of the feedback capacitor C is chosen to compensate for the pole formed by R_O, C_O, and C_{IN} in parallel with the amplifiers input resistance.

Using a current feedback amplifier with its low impedance inverting input eliminates the effects of the pole formed by R_O, C_O, and C_{IN}. It also eliminates the reduced slew rates caused by this pole. When using a current feedback amplifier with a feedback resistor value that has been optimized for best settling time and bandwidth, the D/A output current may be divided as shown in Figure 4.55 in order to provide the correct output voltage.

The series resistor R_{FF} also isolates the D/A output capacitance from the amplifier's inverting input. This capacitance could cause excessive peaking and possible instability if connected directly to the inverting input.

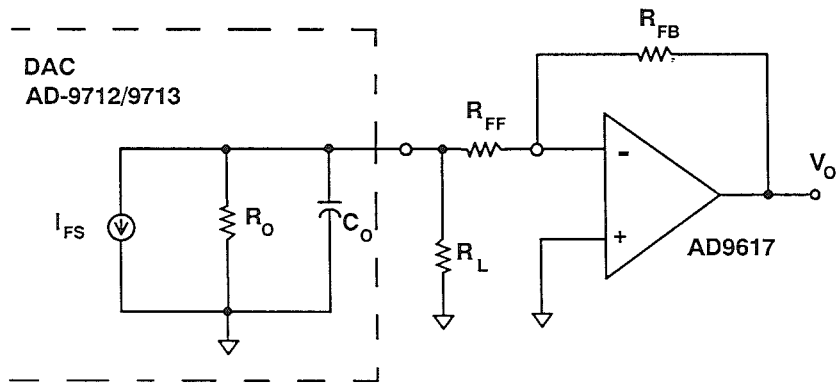
If the D/A output current matches the optimum feedback resistor and the desired output voltage, then the D/A output is connected directly to the inverting input as shown in Figure 4.56. The compensation capacitor is adjusted for optimum output pulse response and compensates for the D/A output capacitance.

Current feedback amplifiers can also be used in the non-inverting mode to buffer and amplify the D/A output. The circuit in Figure 4.57 amplifies the D/A output voltage I_{FS} R_O and provides a positive unipolar output.



D/A I TO V CONVERSION USING A VOLTAGE FEEDBACK OP AMP

Figure 4.54



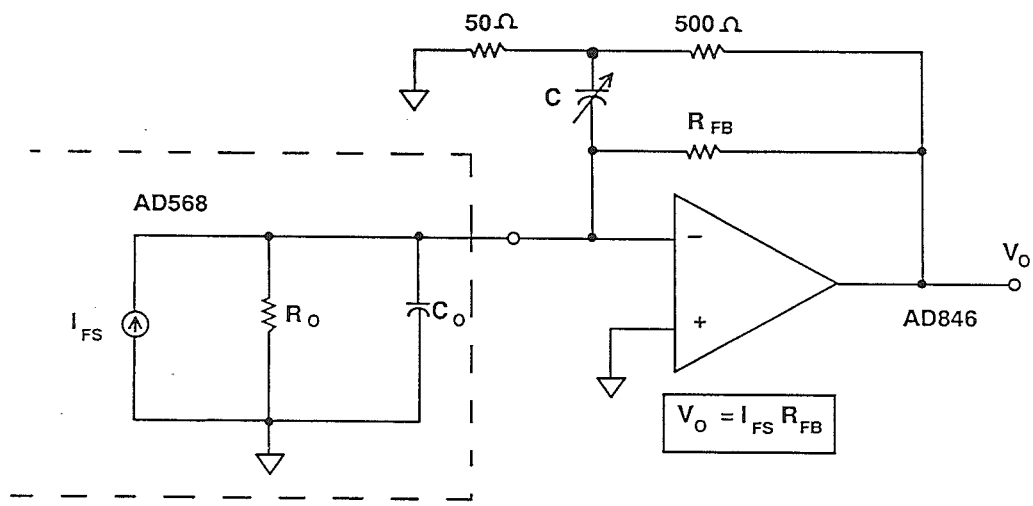
$$R_{FF} = \frac{R_O R_L}{R_O + R_L}\left[R_{FB} \cdot \frac{I_{FS}}{V_O} - 1\right]$$

I_{FS}= 20mA, R_O = 2500Ω, R_L = 50Ω, V_O = 2V

R_{FB}= 400Ω, R_{FF}= 147Ω, C_O = 30pF

I TO V CONVERSION USING CURRENT FEEDBACK AMPLIFIERS

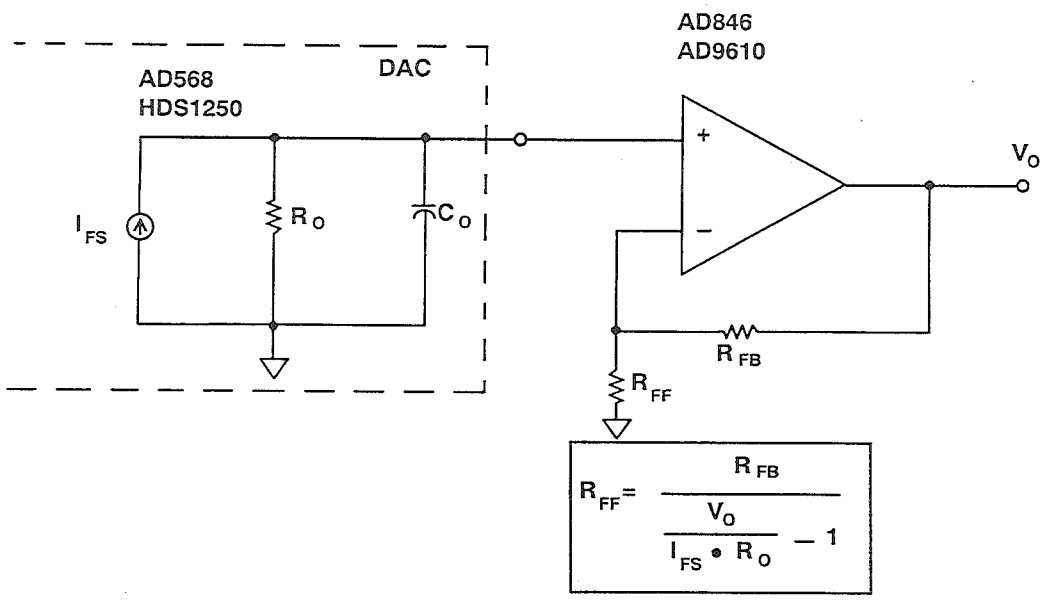
Figure 4.55



FOR D/A = AD568, OP-AMP = AD846
I_{FS} = 10mA, R_O = 100Ω, R_{FB} = 1000Ω, V_O = -10V
C_O = 15pF, C ≈ 5pF

I TO V CONVERSION USING CURRENT FEEDBACK AMPLIFIERS

Figure 4.56



FOR D/A = AD568, OP-AMP = AD846/AD9610
I_{FS} = 10mA, R_O = 100Ω, R_{FB} = 1000Ω, V_O = + 10V
R_{FF} = 111Ω

NONINVERTING D/A OUTPUT BUFFER

Figure 4.57

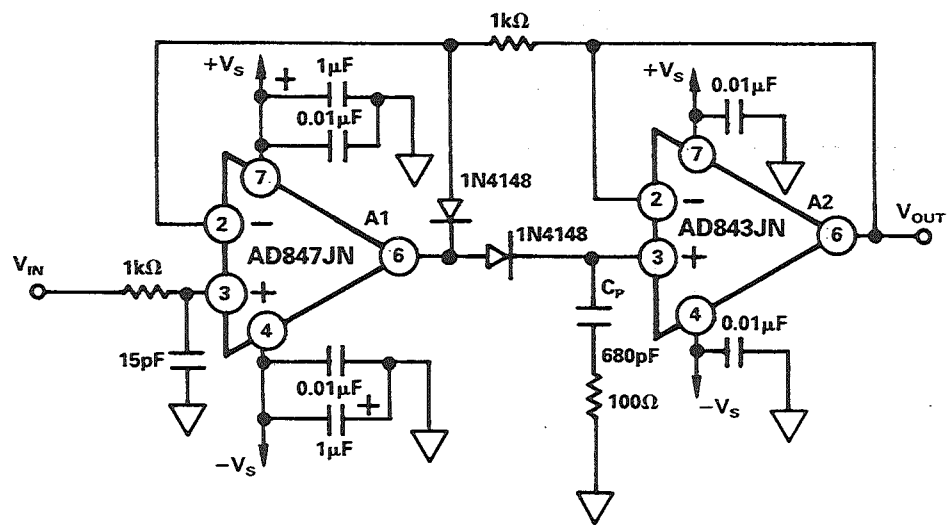
A Fast Peak Detector Circuit

The peak detector circuit of Figure 4.58 can accurately capture the amplitude of input pulses as narrow as 200 ns and can hold their value with a droop rate of less than 20 μV/μs. This circuit will capture the peak value of positive polarity waveforms; to detect negative peaks, simply reverse the polarity of the two diodes.

The high bandwidth and 200V/μ s slew rate of amplifier A2, an AD843, allows the detector's output to "keep up" with its input thus minimizing overshoot. The low (<1 nA) input current of the AD843 ensures that the droop rate is limited only by the reverse leakage of diode D2, which is typically <10 nA for the type shown.

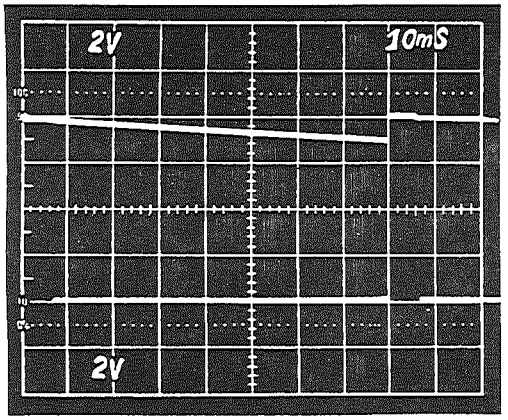
The low droop rate is apparent in Figure 4.59. The detector's output (top trace) loses slightly over a volt in the 8 volt peak input value (bottom trace) in 72 ms, or a rate of approximately 16 μV/μs.

Amplifier A1, an AD847, can drive 680pF hold capacitor, C_p, fast enough to "catch-up" with the next peak in 100 ns and still settle to the new value in 250 ns, as illustrated in Figure 4.59. Reducing the value of capacitor C_p to 100pF will maximize the speed of this circuit at the expense of increased overshoot and droop. Since the AD847 can drive an arbitrarily large value of capacitance, C_p can be increased to reduce droop, at the expense of response time.



A FAST PEAK DETECTOR CIRCUIT

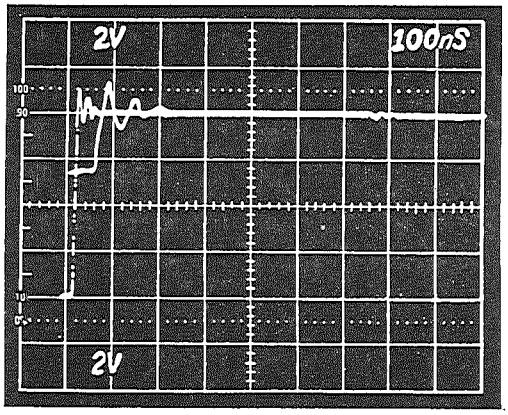
Figure 4.58



TOP TRACE: PEAK DETECTOR OUTPUT

BOTTOM TRACE: INPUT, 8V PEAK @ 125Hz

PEAK DETECTOR RESPONSE
TO 125 Hz PULSE TRAIN



TOP TRACE: PEAK DETECTOR OUTPUT, 8V

BOTTOM TRACE: INPUT VOLTAGE, 8V PEAK,
650ns PULSE WIDTH

PEAK CAPTURE TIME

PEAK DETECTOR WAVEFORMS

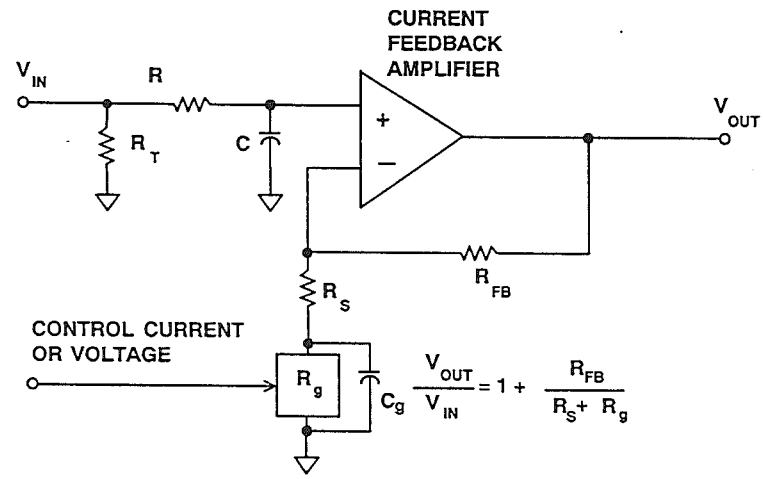
Figure 4.59

Variable Gain Current Feedback Amplifiers

Because their closed loop bandwidth is relatively independent of closed loop gain, current feedback amplifiers are excellent choices for variable gain applications. Figure 4.60 shows a simple circuit where the gain is changed by varying the control voltage or current to a variable resistance element, R_g, such as a FET or photoresistor. The series resistor R_S isolates the parasitic capacitance associated with the variable resistance and prevents peaking and instability. Peaking can also be eliminated at low gains by the addition of a simple RC network in series with the non-inverting input.

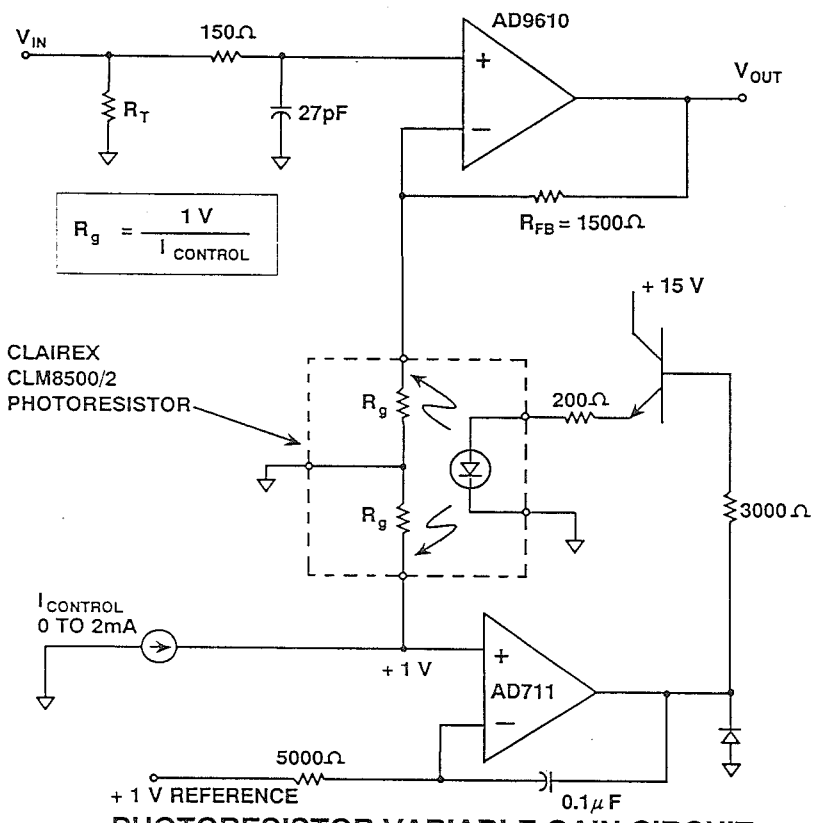
The circuit shown in Figure 4.61 used a photoresistor as the variable resistance element and provides a 12dB gain adjustment range. The gain remains flat within 1dB up to about 20MHz.

FETS can also be used as variable resistance elements, however, their on resistance varies with the drain-to-source voltage. This makes them virtually unusable if good harmonic distortion is required from the variable gain amplifier. The gain setting element resistance is signal dependent, thereby introducing undesirable non-linearities.



VARIABLE GAIN AMPLIFIER

Figure 4.60



PHOTORESISTOR VARIABLE GAIN CIRCUIT

Figure 4.61

20MHz Variable Gain Amplifier

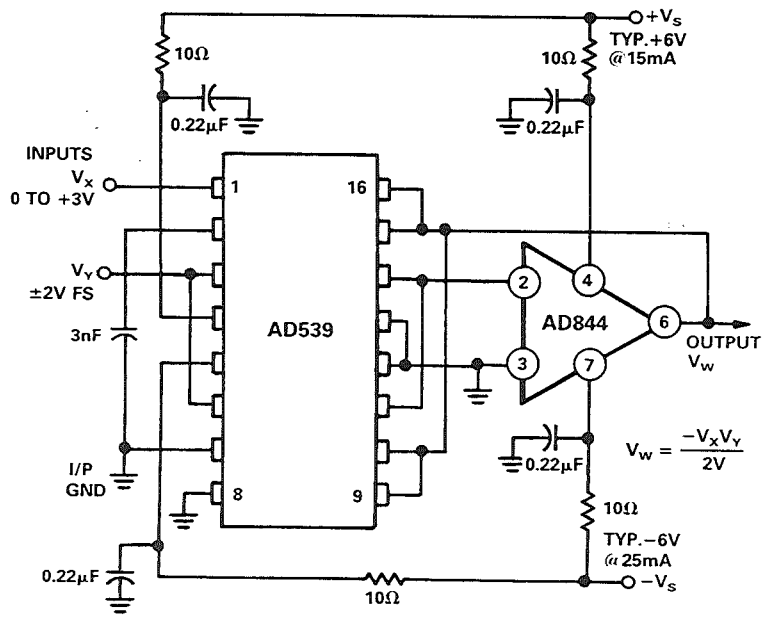
The AD844 is an excellent choice as an output amplifier for the AD539 multiplier, in all of its modes of operation. (See AD539 data sheet for full details.) Figure 4.62 shows a simple multiplier providing the output:

$$V_W = - \frac{V_X V_Y}{2V}$$

where V_X is the "gain control" input, a positive voltage of from 0 to +3.2V (max) and V_Y is the "signal voltage" nominally ±2V FS but capable of operation up to ±4.2V. The peak output in this configuration is thus ±6.7V. Using all four of the internal application resistors provided on the AD539 in parallel results in a feedback resistance of 1.5k Ω , at which value the bandwidth of the AD844 is about 22MHz, and is essentially independent of V_X. The gain at V_X = 3.16V is +4dB.

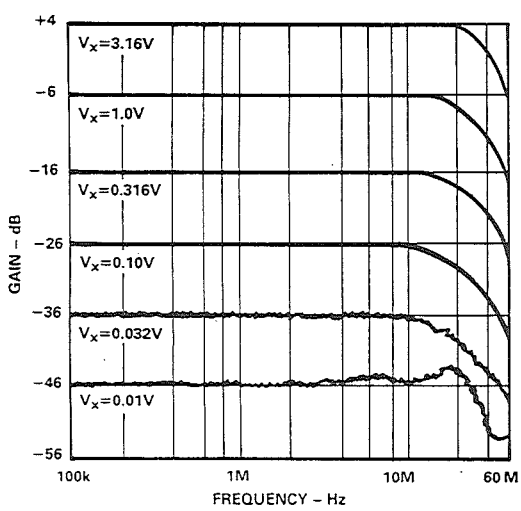
Figure 4.63 shows the small signal response for a 50dB gain control range (V_X = +10mV to +3.16V). At small values for V_X, capacitive feedthrough on the PC board becomes troublesome, and very careful layout techniques are needed to minimize this problem. A ground strip between the pins of the AD539 will be helpful in this regard. Figure 4.58 shows the response to a 2V pulse on V_Y for V_X = +1V, +2V and +3V. For these results, a load resistor of 500Ω was used and the supplies were ±9V. The multiplier will operate from supplies between ±4.5V and ±16.5V.

Disconnecting Pins 9 and 16 on the AD539 alters the denominator in the above expression to 1V, and the bandwidth will be approximately 10MHz, with a maximum gain of 10dB. Using only Pin 9 or Pin 16 results in a denominator of 0.5V, a bandwidth of 5MHz and a maximum gain of 16dB.

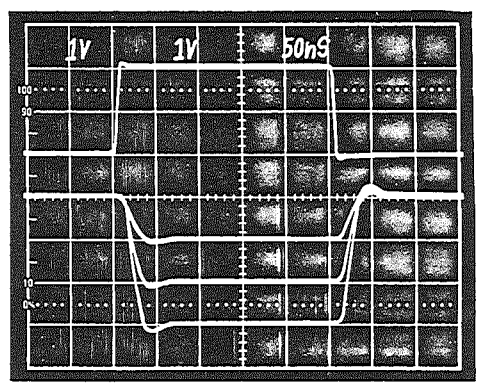


20MHz VARIABLE GAIN AMPLIFIER USING THE AD539

Figure 4.62



VGA ac Response



VGA Transient Response with V_X = 1V, 2V, and 3V

VGA AC AND TRANSIENT RESPONSE

Figure 4.63

High Speed Instrumentation Amplifier

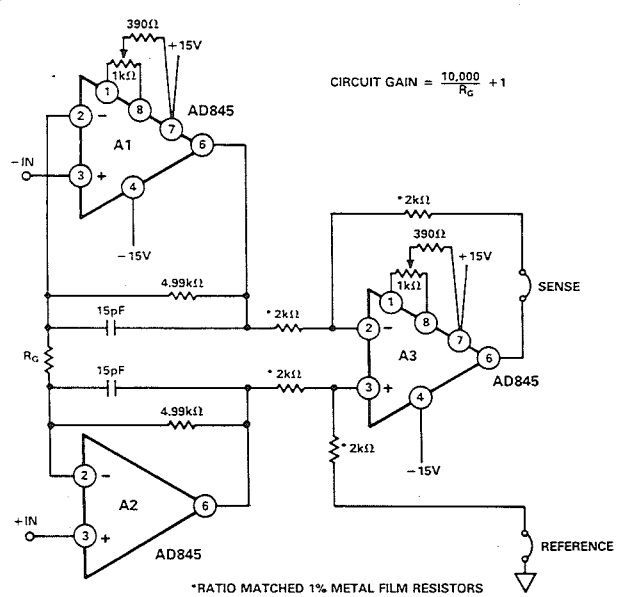
Instrumentation amplifiers are used when high input impedance balanced differential inputs are required. Instrumentation amplifiers offer performance advantages over standard op amps by offering wider common mode input ranges, high common mode rejection ratios, and stable, fixed gains.

In Figure 4.64, three AD845 FET input op amps are used to achieve these characteristics and gain ranges from unity to 1000. Low input bias currents and fast settling times are achieved with the AD845. The AD843 FET input op amp may also be used for improved performance due to its higher bandwidth, faster settling time, and higher slew rate.

Most monolithic instrumentation amplifiers do not have the high-frequency performance of the circuit in Figure 4.64. The circuit bandwidth is 4.9MHz at a gain of 1 and 1.1MHz at a gain of 10; settling time for the entire circuit is 800ns to 0.01% for a 10V step (Gain = 10).

The capacitors employed in this circuit greatly improve the amplifier's settling time and phase margin.

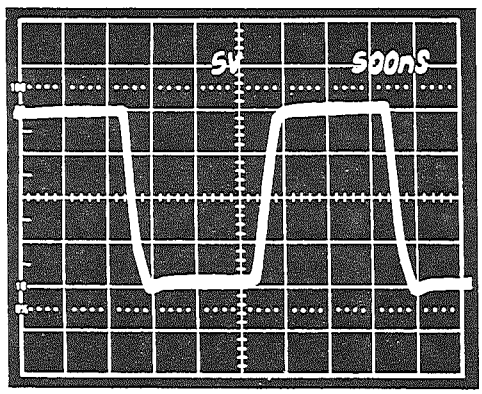
Pulse response and settling time of the three AD845 instrumentation amplifier are shown in Figure 4.65.



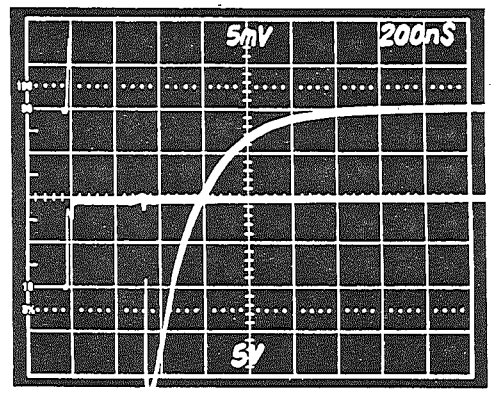
Gain	R_G	Bandwidth	Settling Time to 0.01%
1	NC	4.9MHz	700ns
2	10kΩ	4.2MHz	720ns
10	1.11kΩ	1.1MHz	800ns
100	101Ω	130kHz	3.5μs

HIGH PERFORMANCE, HIGH-SPEED INSTRUMENTATION AMPLIFIER

Figure 4.64



The Pulse Response of the Three Op Amp Instrumentation Amplifier: Gain = 1, Horizontal Scale:0.5μ s/Div, Vertical Scale: 5V/Div



Settling Time of the Three Op Amp Instrumentation Amplifier: Horizontal Scale: 200ns/Div,Vertical Scale, Pulse Input: 5V/Div; Output Settling:1mV/Div

HIGH SPEED INSTRUMENTATION AMP PULSE RESPONSE AND SETTLING TIME

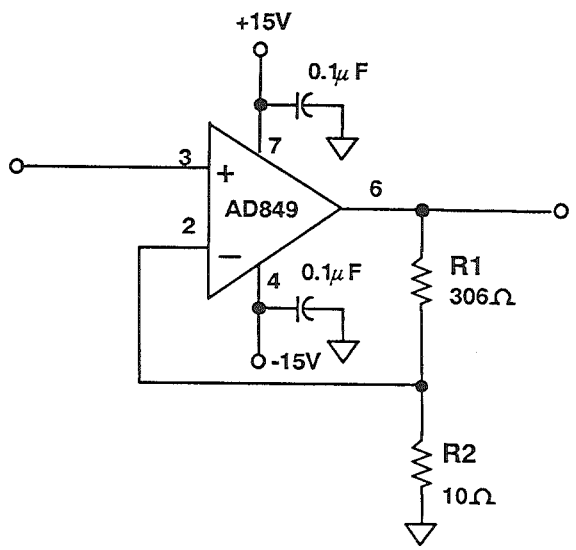
Figure 4.65

Low Noise Preamp Using the AD849

The circuit shown in Figure 4.66 has a gain of 30dB and uses the AD849 op amp which is stable for gains greater than 25 and has a 725MHz gain-bandwidth product. The low input noise voltage of the AD849 (3nV/$\sqrt{Hz}$ at 10kHz) and high gain bandwidth makes it well suited as a preamp in a high frequency system.

It should be noted that the current noise of the AD849 is approximately 1pA/$\sqrt{Hz}$.

This implies that with source resistances of less than 550Ω , the voltage noise will dominate. For source resistances greater than 500Ω , the Johnson noise in the source resistance is dominant until 15.5kΩ source resistance, after which the current noise flowing in the source resistance wins. It is obvious, however, that with impedances as high as this, the main problem will be reduced bandwidth due to shunt capacitance.



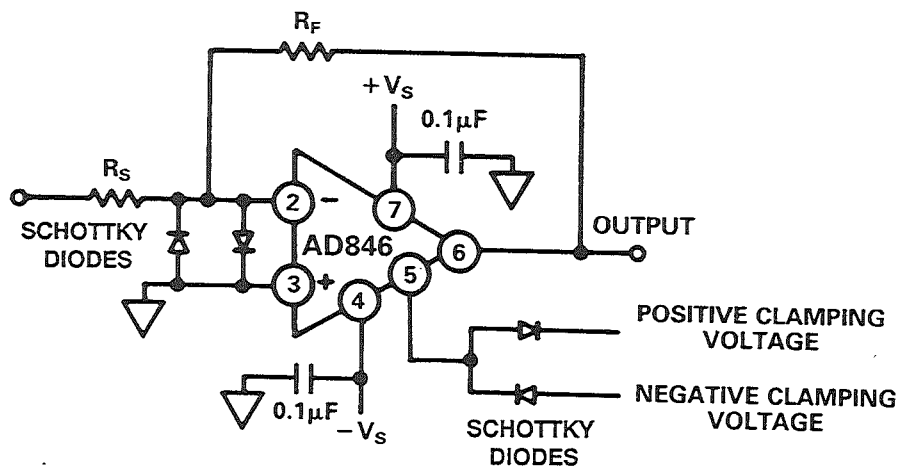
$$G_{dB} = 20\log\left[1 + \frac{R1}{R2}\right]$$

LOW NOISE PREAMP

Figure 4.66

Clamped Amplifier

The AD844 and AD846 precision current feedback op amps are well suited to act as clamped amplifiers able to protect delicate circuitry following the amplifier. Figure 4.67 shows the AD846 set up in the clamped amp configuration. By connecting schottky diodes to the compensation pin, the output is restricted to the range dictated by the diodes. The input of the amp should be clamped as well to avoid damaging the input transistors. This circuit exhibits excellent overvoltage recovery times.

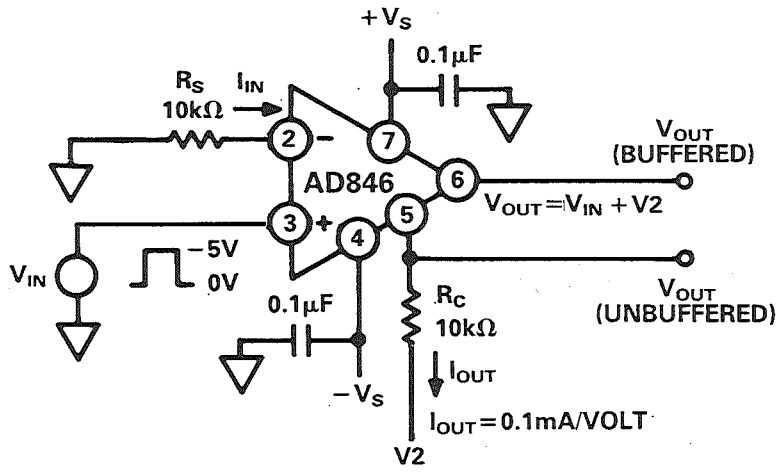


AD846 USED AS A CLAMPED AMPLIFIER

Figure 4.67

Level Shifting

Many applications require signals to be DC shifted. An extremely easy and straight forward means to accomplish this task is shown in Figure 4.68. The AD846 (or AD844) is set up with the input voltage signal connected to the non-inverting input. That voltage is mirrored to the inverting input by placing a resistor R_S in series to ground. The current developed is proportional to V_{IN}. This current flows from the compensation node (Pin 5) developing a voltage across resistor R_C (note $R_C = R_S$) which is connected to the level shifting voltage V2. The voltage developed at the compensation node is, therefore, V_{IN} + V2, and directly follows changes in V_{IN}. By scaling R_C, a level shift with voltage gain is produced. The normal output voltage developed at Pin 6 is nearly equal to the voltage seen at the compensation pin, and can provide a low output impedance, buffered, level shifted output.



AD846 CONNECTED AS A LEVEL SHIFT AMPLIFIER

Figure 4.68

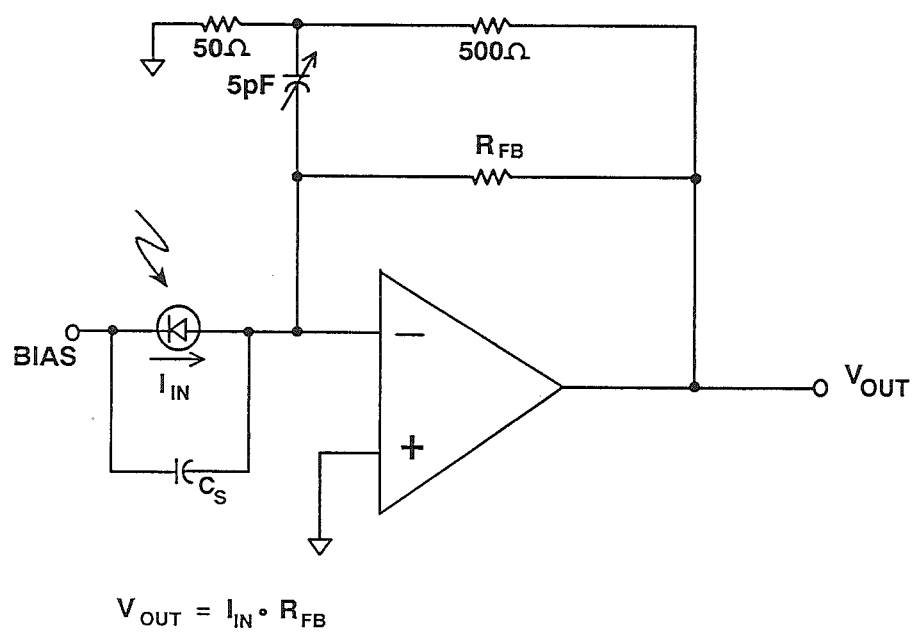
Photodiode Detectors

Current feedback amplifiers can be used to amplify the current from a wideband fiberoptic photodiode receiver as shown in Figure 4.69. The compensation circuit is required to prevent peaking and instability caused by the diode capacitance.

In photodiode applications, the effective input current noise should be calculated for the circuit conditions to verify that the diode current is not swamped out by the op amp noise.

The current noise of bipolar input voltage feedback op amps of the AD840-series (AD840, 841, 842, 847, 848, 849) is basically the schottky (shot) noise in the input junction. This is given by the formula:

$I_{IN} = 5.7 \times 10^{-10} \sqrt{BI_J}$, where
I_{IN} = rms noise current (AMPS)
I_J = junction bias current (AMPS)
B = bandwidth (Hz)



PHOTODIODE DETECTOR

Figure 4.69

Active Filters: A Wideband Sallen Key Filter

Figure 4.70 shows an AD843 FET input op amp used in a 1MHz Sallen-Key filter. This circuit also works well with the AD841, AD845 or the AD847. The circuit is designed to be a maximum-flatness Butterworth filter with a Q of 0.575, and a DC gain of 1.26. The frequency response of the filter of a 0dBm input signal is shown in Figure 4.71. (Measured with an HP8753A Network Analyzer).
In this design if R1 = R2, and C1 = C2, the circuits sensitivity to variations in component values is minimized. The cutoff frequency f_c is given by

$$f_c = \frac{1}{2\pi\sqrt{R1 \cdot R2 \cdot C1 \cdot C2}} = \frac{1}{2\pi R1 \cdot C1}$$

and the circuit Q is given by

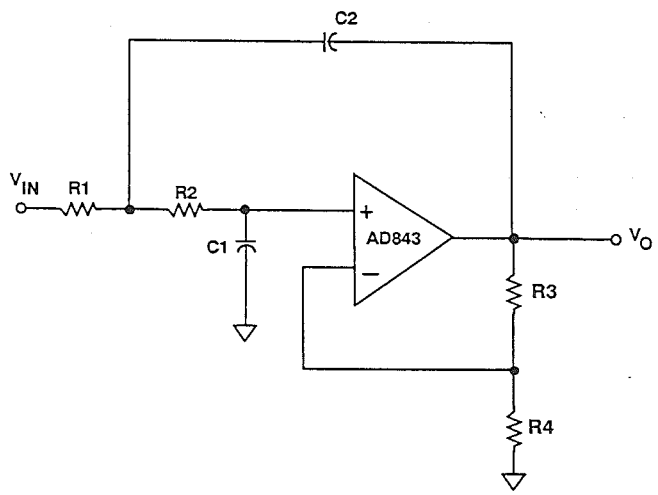
$$Q = \frac{1}{3 - K},$$

$$\text{where } K = 1 + \frac{R3}{R4}.$$

The complete transfer function is given by

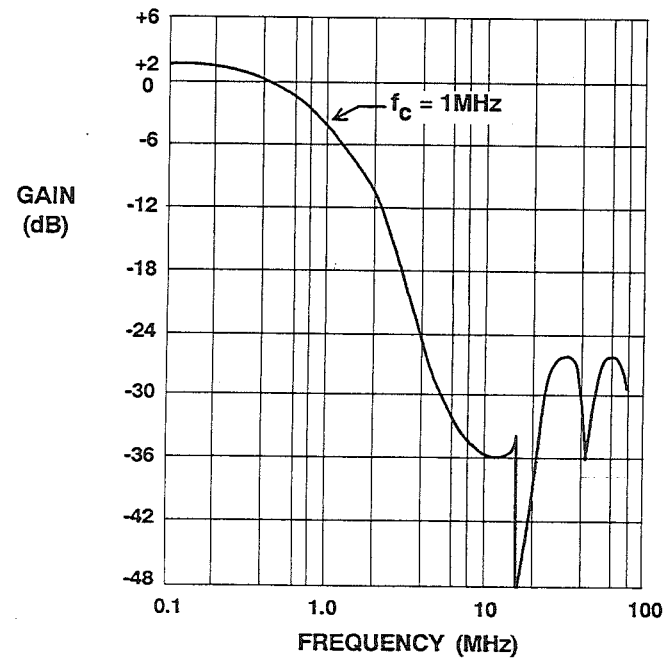
$$\frac{V_O}{V_{IN}} = \frac{K/R^2C^2}{s^2 + \left(\frac{3 - K}{RC}\right)s + \frac{1}{R^2C^2}}$$

where R = R1 = R2 and C = C1 = C2.



1 MHz SALLEN KEY FILTER

Figure 4.70



ACTIVE FILTER SMALL SIGNAL FREQUENCY RESPONSE

Figure 4.71

OP AMP SELECTION GUIDE

VOLTAGE FEEDBACK OP AMPS

MODEL	GBW (MHz)	MINIMUM STABLE GAIN	SLEW RATE (V/μs)	SETTLING TIME (ns)	POWER SUPPLY (V)	COMMENTS
AD5539	1400	+5, -4	600	12(1%)	±8	____
AD840	400	10	400	100(.01%)	±15	____
AD841	40	1	300	110(.01%)	±15	±50mA Output
AD842	80	+2, -1	375	100(.01%)	±15	±100mA Output
AD843	35	1	250	110(.01%)	±15	FET Input
AD845	16	1	100	350(.01%)	±15	FET Input
AD847	50	1	300	120(.1%)	±15, ±5	Stable With Capacitive Load
AD848	175	5	300	100(.1%)	±15, ±5	Stable With Capacitive Load
AD849	725	25	300	80(.1%)	±15, ±5	Low Noise Pre-amp
AD711	3	1	16	1000(.01%)	±15	FET Input
AD712	3	1	16	1000(.01%)	±15	Dual AD711
AD713	3	1	16	1000(.01%)	±15	Quad AD711
AD744	13	+2, -1	75	500(.01%)	±15	FET Input
AD746	13	+2, -1	75	500(.01%)	±15	Dual AD744
AD827	50	1	300	120(.1%)	±15	Dual AD847
AD829	800	1 → 25	10→300	120(.1%)	±15	Externally Compensated AD849

Figure 4.72

OP AMP SELECTION GUIDE

CURRENT FEEDBACK OP AMPS

MODEL	BW* (MHz)	MINIMUM STABLE GAIN	SLEW RATE (V/μs)	SETTLING TIME (ns)	POWER SUPPLY (V)	COMMENTS
AD844	67	1	2000	90(.1%)	±15, ±5	High Slew-Rate
AD846	46	1	450	100(.01%)	±15	Precision
** AD9610	100	1	3500	18(.1%)	±15	Large Output Swing
** AD9611	300	1	1900	13(.1%)	±5	Ultra-Fast
** AD9615	250	1	1400	13(.1%)	±5	Precision
AD9617	185	+1	1600	16(.02%)	±5	Low Distortion
AD9618	160	+5, -1	1500	16(.02%)	±5	Low Distortion

* Bandwidth stated for minimum stable gain with recommended feedback resistor

**Hybrid Op Amps

Figure 4.73

INTERMODULATION DISTORTION IN THE AD9610 and AD9611

by Tom Gratzek & Robert Kim – Analog Devices: Computer Labs Division

January 1988

Operational amplifiers and their applications have been extensively described in sources ranging from elementary textbooks to data sheets to dedicated in-depth specialty monographs (often available from established "off-the- shelf" merchant suppliers.) As vendors attempt to improve on "the state of the art", two general areas are often targeted: ac and dc performance. DC performance often includes enhancing parameters such as offset voltage, bias currents, and open loop gain. AC performance includes wider bandwidth, faster settling time, lower noise (over frequency), and less distortion (harmonic and intermodulation). The user must decide which amplifier is "best" for each application. In most cases, the "best" amplifier is the one that wins the design-in struggle.

Manufacturers have tried to improve both ac and dc specifications with novel designs and by utilizing better transistors. Another trend that has benefitted amplifier users is enhanced testing. For example, the industry-standard 741 is typically available from manufacturers with dc testing only. Parameters tested include open loop gain, output voltage swing, input offset voltage and bias current, PSRR, and supply currents.
As competition intensified and market segments increased, additional tests have been added over the years. Some of the parameters that are now tested by various manufacturers include - dc testing over temperature, rise/fall times, slew rates, -3dB bandwidth at a given gain, and harmonic distortion. Competition has moved amplifier suppliers to test their parts more thoroughly in search of an advantage in the market place.

This article centers on new ultra high-speed operational amplifiers available from Analog Devices, notably the AD9610 and AD9611. While dc specifications are important and are fully tested, the targeted market segments for these parts clearly called for superior ac performance guaranteed by the manufacturer. Enhanced testing for these parts includes detecting the -3dB bandwidth, amplitude of peaking over frequency, and distortion measurements. For the AD9610, total harmonic distortion (with a 20 MHz fundamental) is measured. The testing of the AD9611 goes even further; both second and third harmonic tones are measured separately (with a *60 MHz* fundamental).

One of the applications for which the AD9610 and AD9611 are particularly suited is driving the newest generation of flash A/D converters (such as the AD9002; 8 bits, 150MHz). Users of these premium converters are interested in obtaining the highest dynamic performance from their *Op-Amp :A/D system.* As an example, an 8-bit converter with perfect linearity will deliver a 49dB signal-to-noise ratio (SNR). This implies that distortion from the amplifier should be better than -55 dB (relative to the signal) at the required frequency to avoid affecting the system SNR.

When flash A/D users talk about distortion, they are generally concerned with the spurs introduced into the spectrum of interest. In laboratory conditions (as simulated by most production test beds), harmonic distortion is a major area of concern and is usually measured by inserting a single-tone fundamental into the device under test (DUT), then looking at the relevant frequency (2x fundamental for 2nd harmonic; and 3x fundamental for the third harmonic) to determine the magnitude of the harmonic tones.

While this testing is useful to many customers, it does not always appease everyone. Manufacturers who claim to have amplifiers with -3dB bandwidths in the tens of MHz region often test distortion with only a 10kHz input tone. The results of this testing are undoubtedly favorable (to the manufacturer) but somewhat unsatisfying to the informed customer, who usually wants to know the level of performance that can be expected at higher operational frequencies, and the magnitude of the spurs from other sources (notably intermod distortion).

After the amplifier leaves the factory and is installed in the equipment for which it was selected, there is no guarantee that it will be exposed to such a pure spectrum (implicit to harmonic distortion testing). In many cases the amplifier is asked to operate in *spectrally-rich environments* where the intermodulation distortion properties of the amplifier are of keen interest.

Examples of applications demanding good intermodulation distortion performance include: **Radar**, where interference from other radars and jammers often pollute the RF spectrum; **Satellite Communications**, where the usable bandwidth for each transponder is limited and multiple signals are frequency multiplexed onto one carrier; **Digital Radio Receivers**, where a segment of the RF spectrum is digitized and scanned by high-speed data signal processors (DSPs), often in classified national security (snooping) applications.

The **intermodulation distortion (IMD)** performance of wideband, dc-coupled amplifiers is a relatively new area for operational amplifier suppliers. Methods to measure and communicate the extent of this distortion to users have been borrowed from traditional "RF" companies which have historically supplied the radar and radio communications industries where the importance of it was first highlighted.

In the remaining sections of this article, which will be published in RF Design magazine in April, the authors describe IMD, its mathematical derivation, how to test for it, and present results for two ADI amplifiers (AD9610 and AD9611).

Mathematical Derivation of Intermodulation Distortion

Harmonic distortion is caused by nonlinearities in the amplitude transfer characteristics. The typical output contains not only the fundamental frequency, but integer multiples of it. IMD results from mixing of two or more signals of different frequencies. The spurious output occurs at the sum and/or difference of integer multiples of the input frequencies. The non-ideal characteristics of an amplifier can be described using the Power Series Expansion:

$$V_{out} = K0 + K1(Vin) + K2\,(Vin)^2 + K3(Vin)^3 + \ldots\ldots\ldots \qquad \text{(Eqn. 1)}$$

A one-tone input signal (V_{in} = Esinwt) produces harmonic distortion. A two-tone input signal produces harmonic distortion and intermodulation distortion.

$$V_{in} = E1\sin w_1 t + E2\sin w_2 t \qquad \text{(Eqn. 2)}$$

Combining Equations 1 and 2 results in the following identity:

$$V_{out} = K0 + K1(\,E1\sin w_1 t + E2\sin w_2 t\,) +$$

$$K2\,(\,E1\sin w_1 t + E2\sin w_2 t\,)^2 +$$

$$K3(\,E1\sin w_1 t + E2\sin w_2 t\,)^3 + \ldots\ldots \qquad \text{(Eqn. 3)}$$

The first term (K0) represents the dc offset of the amplifier; the second term is the fundamental signal(s). The subsequent terms represent the distortion of the amplifier. The second IMD can be found by analyzing the third term of Eqn. 3.

$$K2\,(Vin)^2 = K2\,(\,E1^2\sin^2 w_1 t + E2^2\sin^2 w_2 t + 2E1E2\sin w_1 t(\sin w_2 t))$$

(Eqn. 4)

Remembering that [$\sin^2 x = (1 - \cos 2x)/2$]

and[$\sin(x)\sin(y)=(\cos(x-y)-\cos(x+y))/2$] and substituting into Eqn 4 provides:

$$K_2 (V_{in})^2 = K_2 (E_1^2 + E_2^2)/2 - \quad (1)$$

$$(K_2/2) (E_1^2 \cos 2w_1 t + E_2^2 \cos 2w_2 t) + \quad (2)$$

$$2 K_2 E_1 E_2 (\cos(w_1 t - w_2 t) - \cos(w_1 t + w_2 t)) \quad (3)$$

(Eqn. 5)

The first and second terms in Equation 5 represent dc offset and second-order harmonics. The third term is the second-order IMD. This excercise can be repeated with the fourth term of Equation 3 to study third-order effects.

$$K_3 (V_{in})^3 = K_3(E_1^3 \sin^3 w_1 t + E_2^3 \sin^3 w_2 t + 3E_1^2 E_2 \sin^2 w_1 t (\sin w_2 t) + 3E_1 E_2^2 \sin w_1 t (\sin^2 w_2 t))$$

(Eqn. 6)

Utilizing the identities, $\sin^3 x = 1/4(3\sin x - \sin 3x)$ and
$\sin^2 x \sin y = 1/2(\sin y - 1/2(\sin(2x+y) - \sin(2x-y)))$, Equation 6 reduces to:

$$K_3 (V_{in})^3 = (3K_3/4)(E_1^3 \sin w_1 t + E_2^3 \sin w_2 t + 2E_1^2 E_2 \sin w_2 t + 2E_2^2 E_1 \sin w_1 t)$$

(1)

$$(K_3 E_2^3/4)(E_1^3 \sin 3w_1 t + E_2^3 \sin 3w_2 t) +$$

(2)

$$(3K_3 E_1^2 E_2/2)(\sin(2w_1 t - w_2 t) - 1/2\sin(2w_1 t + w_2 t)) +$$

(3)

$$(3K_3 E_2^2 E_1/2)(\sin(2w_2 t - w_1 t) - 1/2(\sin(2w_2 t + w_1 t))$$

(4)

(Eqn. 7)

Term 1 from Equation 7 represents amplitude offset at the fundamental frequencies. Term 2 signifies the third-order harmonics. Terms 3 and 4 represent third-order IMD.

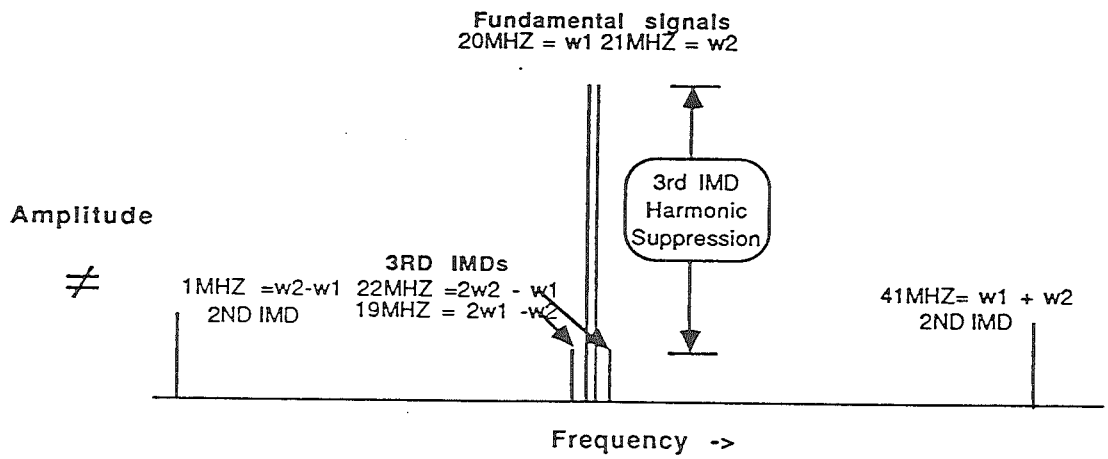
Some Simple Relationships

Intermodulation distortion occurs at frequencies that are the sum and/or difference of integer multiples of the fundamental frequencies. For example, assume a composite input signal has fundamental frequencies w1 and w2. Distortion products will occur at frequencies aw1±bw2 where a and b = 0,1,2,3... Intermodulation Distortion terms of order a+b occur when either a or b is not equal to zero. The following table illustrates this relationship.

2nd Order IMD Frequencies	3rd Order IMD Frequencies	
w1-w2	2w1+w2	2w2+w1
w1+w2	2w1-w2	2w2-w1

Most IMD can be filtered out. However, if the two input tones are of similar frequencies, the third-order IMD (2w1-w2, 2w2-w1) will be very close to the fundamental frequencies and cannot be easily filtered. Third-order IMD is of most concern in narrow bandwidth applications. Second-order IMD is of greater concern in broad bandwidth applications. Figure 1 below illustrates the 2nd and 3rd IMDs for the condition in which the fundamental tones (w1 & w2) are 20 and 21MHz sinewaves.

Figure 1: Relationship Between Fundamentals and IMDs



AMPLITUDE OF IMD vs. the FUNDAMENTAL

The location of the IMDs relative to the fundamental tones has now been defined. The relationship of the amplitudes of the IMD tones to the amplitude of the fundamental tones depends on the order of the IMD. The coefficients of the third-order IMD term in Equation 7 can be used as a starting point in the analysis.

$$\textit{Amplitude of 3rd IMD tones} = 3K3E1^2\,E2/2.$$

Converting to dB provides:

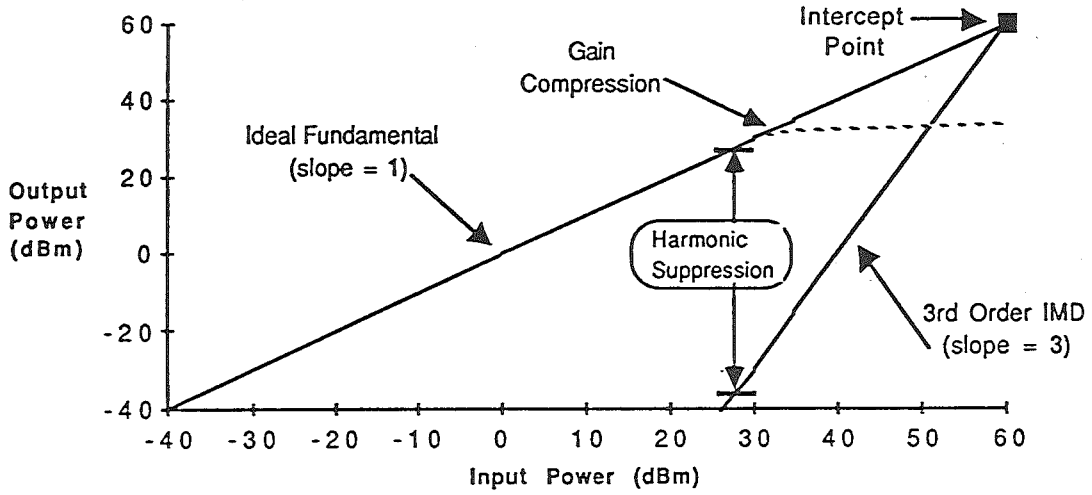
$$\textit{Amplitude of 3rd IMD tone} = 20\log(3K3/2) + 20\log(E1^{2)} + 20\log(E2).$$

$$\textit{Amplitude of 3rd IMD tone}\ (\text{dB}) = \text{Constant} + 2E1 + E2 \qquad \text{(Eqn. 8)}$$

where E1 & E2 are expressed in dB.

Equation 8 shows that if the two inputs are changed by 1dB, the third-order IMD amplitude will change by 3dB. The desired output of the amplifier and any IMD can be represented by two straight lines of different slopes. The desired output line has a slope of 1; any IMD has a slope of n, where n is the order of the IMD. The third-order IMD has a slope of 3. (See Figure 2.)

Figure 2: Relationship Between Fundamental and 3rd IMD



Ideally, the output of an amplifier will track the input. *Gain Compression* occurs at the point where the actual output power drops below the ideal. The *Intercept Point* is at the intersection of the ideal output signal and the extension of the IMD. The intercept point can be determined from the value of the harmonic suppression which must be determined experimentally. Equation 9 illustrates this relationship.

Intercept Point = (Harmonic Suppression)/(N-1) + (Power of One Fundamental at Output of Amplifier)

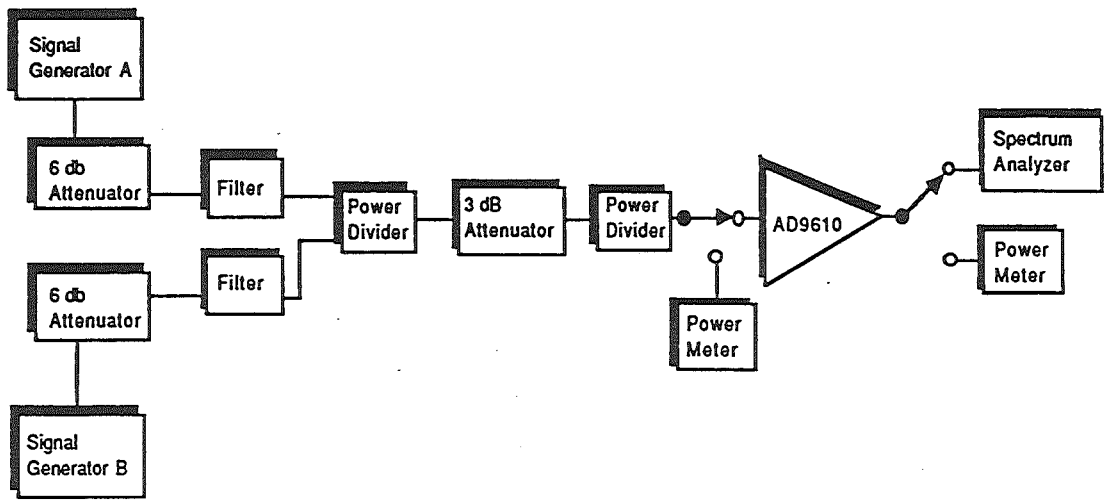
(Eqn. 9)

Harmonic suppression must be measured where the amplifier exhibits a linear output/input (i.e., below the gain compression point.) "N" is the order of the IMD of interest.

Determining Harmonic Suppression

The test system used to measure harmonic suppression for the AD9610 wide-bandwidth transimpedance amplifier is diagrammed below.

Figure 3: Test Setup to Measure Harmonic Suppression



(Attenuators are used to limit the IMD of the signal generator setup; for every 1 dB attenuation of the fundamental signals, the nth order IMD is reduced by n dB.)

4

Test Procedure to Determine Harmonic Suppression

1) Set the amplitude of the two inputs equal with the power meter.

2) Check for gain compression by reducing the signal power of both fundamentals by 1dB, then checking to make sure that the 3rd IMD tone is reduced by 3dB. If past the compression point (see Figure 2), then the amplitude of the input to the amplifier should be reduced (REPEAT STEP 1).

3) Measure the harmonic suppression of the 3rd IMD tone on the spectrum analyzer. This is the difference between the magnitude of the fundamental and the 3rd IMD. (See Figure 1.)

4) Measure the amplitude of a fundamental signal at the output of the AD9610 by disconnecting one of the signal generators.

5) Calculate the intercept point using Equation 9.

THIRD-ORDER IMD RESULTS FOR THE AD9610 and AD9611

The 3rd IMD intercept points were measured for the AD9610 and AD9611 using fundamental input frequencies from 2MHz to 200MHz with 500kHz separation between tones. All parts were set up in a gain of -5 and were driven into a 50Ω load.

Figure 4 is the plot of the 3rd IMD intercept points at different frequencies. The IMD Interept data are valid at different gain settings as long as the measurements are made below the gain compression point. The AD9610 is a very good performer, and becomes better than the AD9611 below 8 MHz. The AD9611 is the best dc-coupled wide band amplifier in the world in terms of IMD.

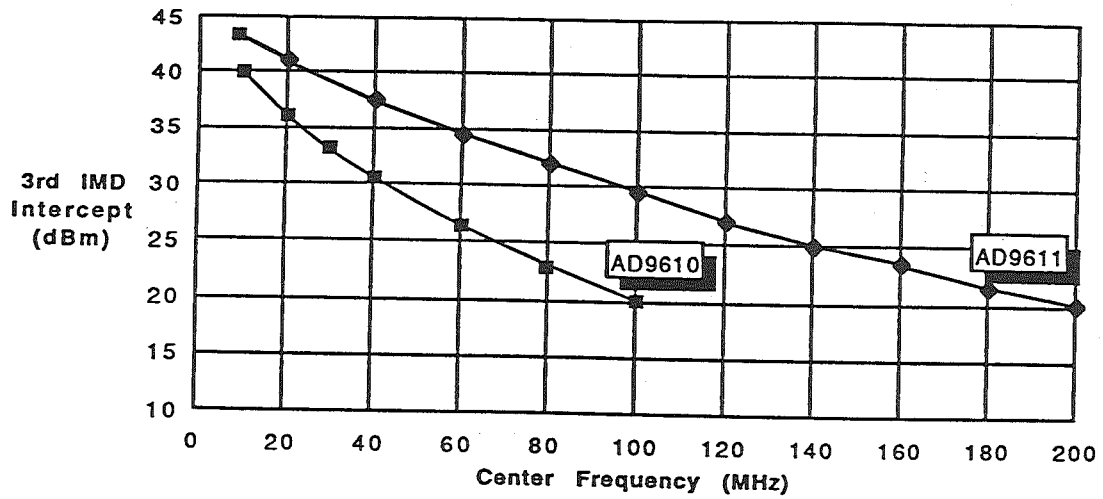


Figure 4.

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