SECTION II

DIGITAL VIDEO APPLICATIONS

DIGITAL VIDEO APPLICATIONS

2

BROADCAST VIDEO DIGITIZATION

HIGH DEFINITION TV

MULTIPLEXING AND SWITCHING VIDEO SIGNALS

ELECTRONIC IMAGE PROCESSING

BROADCAST VIDEO DIGITIZATION

In recent years digital techniques have gained widespread popularity in professional video applications such as time base correctors, frame stores and synchronizers, standards converters, special effects generators, etc. These digital "black boxes" take advantage of developments in data conversion, data storage, and DSP to perform functions previously performed by analog technology.

The term "codec" describes the A/D and D/A portion of a typical digital device as shown in Figure 2.2. Certain standards have evolved with respect to television codecs relating to sampling rates and resolution.

In order to discuss these standards, it is first necessary to understand the basics of a color television signal.

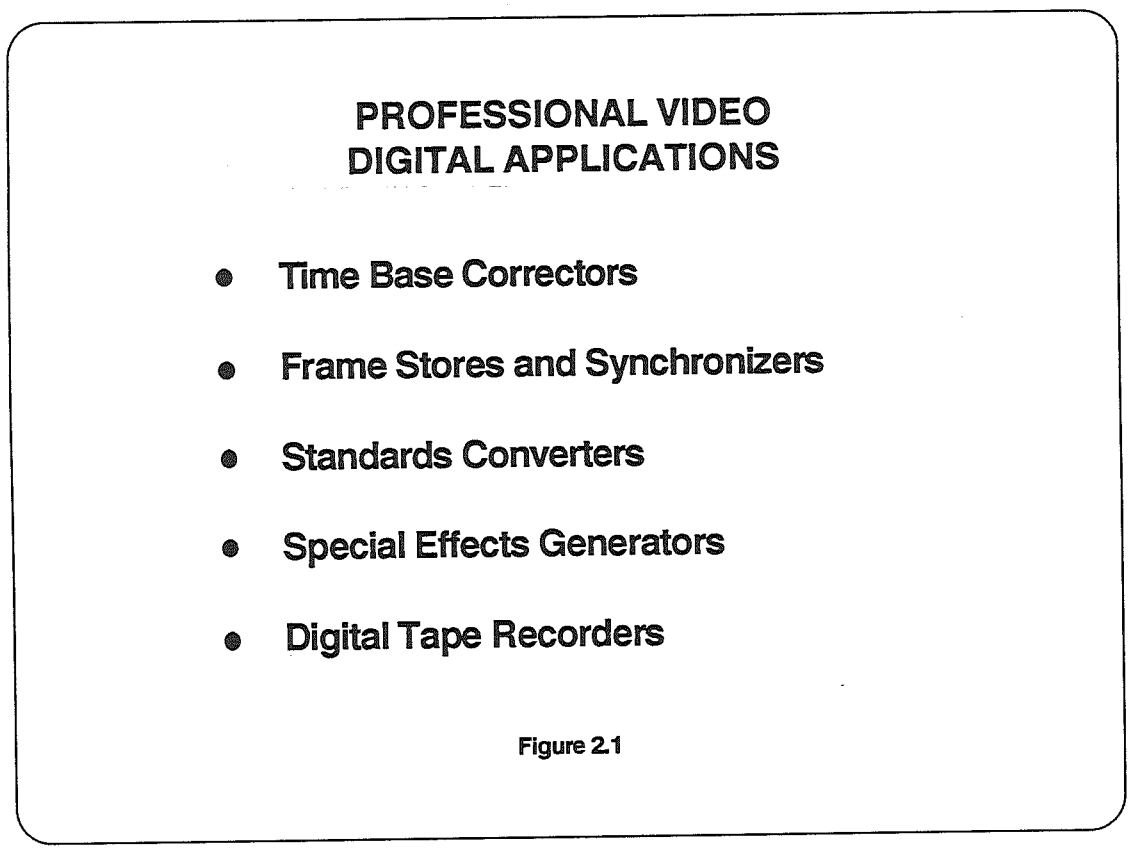
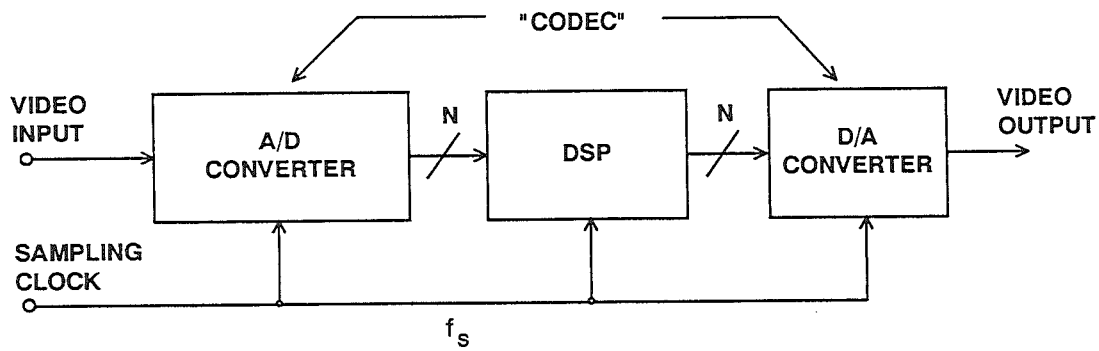


Figure 2.1



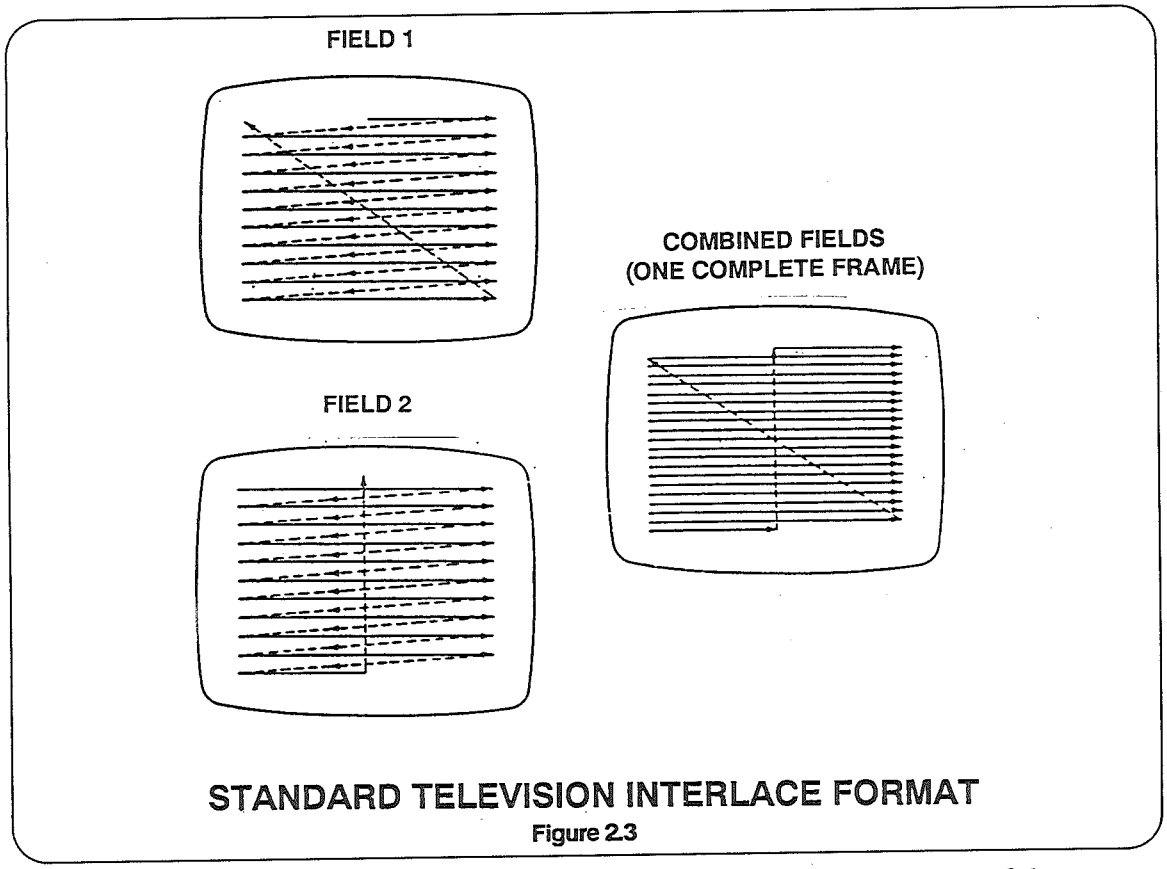
TYPICAL DIGITAL TV DEVICE

Figure 2.2

NTSC Characteristics

The *standard video format* is the specification of how the video signal looks from an electrical point of view. Light strikes the surface of an image sensing device within the camera and produces a voltage level corresponding to the amount of light hitting a particular spatial region of the surface. This information is then placed into the standard format and sequenced out of the camera. Along with the actual light intensity information, synchronization pulses are added to allow the receiving device - a television monitor, for instance - to identify where the sequence is in the frame data.

A standard video format image is read out on a line-by-line basis from left to right, top to bottom. A technique called *interlacing* refers to the reading of all even-numbered lines, top to bottom followed by all odd lines (see Figure 2.3). The television picture *frame* is thus divided into even and odd *fields*. Interlacing is used to produce an apparent update of the entire frame in half the time that a full update actually occurs. This results in a television image with less apparent flicker.



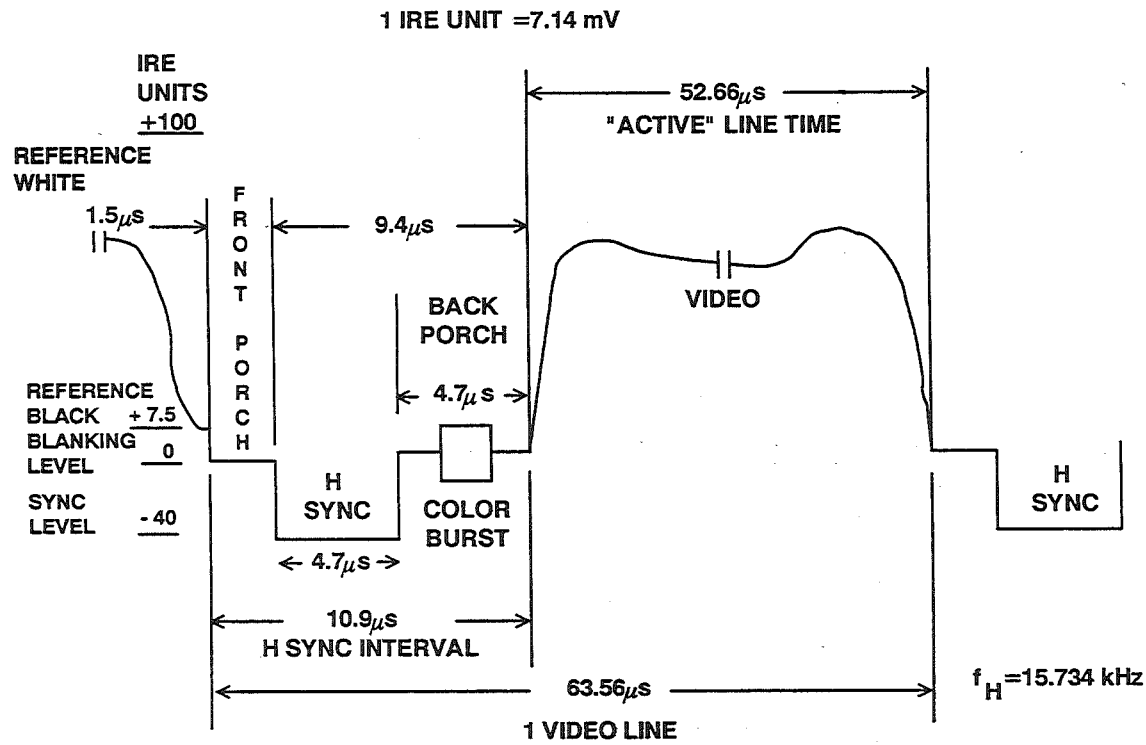
STANDARD TELEVISION INTERLACE FORMAT

Figure 2.3

The original black and white, or *monochrome*, television format specification is the EIA RS-170 specification which prescribes all timing and voltage level requirements for standard commercial broadcast video signals. The standard specification for color signals, NTSC, modifies RS-170 to work with color signals by adding color information to the signal which otherwise contains only brightness information.

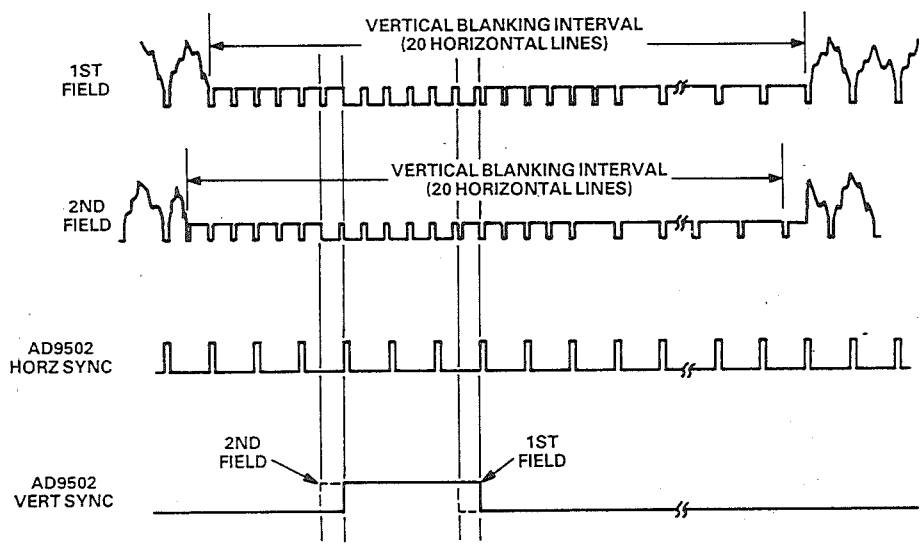
A video signal comprises a series of analog television lines. Each line is separated from the next by a synchronization pulse called the *horizontal sync*. The fields of the picture are separated by a longer synchronization pulse called the *vertical sync*. In the case of a monitor receiving the signal, its electron beam scans the face of the display tube with the brightness of the beam controlled by the amplitude of the video signal. Whenever a horizontal sync pulse is detected, the beam is reset to the left side of the screen and moved down to the next line position. A vertical sync pulse, indicated by a horizontal sync pulse of longer duration, resets the beam to the top left point of the screen to a line centered between the first two lines of the previous scan. This allows the current field to be displayed between the previous one. A single line for the NTSC color video signal is shown in Figure 2.4, and a field timing diagram is shown in Figure 2.5.

Figure 2.6 is a simplified block diagram of the NTSC color processing system. The three color signals (R, G, B) from the color camera are combined in a MATRIX unit to produce what is called the "luminance" signal (Y) and two color difference signals (I and Q). These "components" are further combined to produce what is called the "composite" color signal.



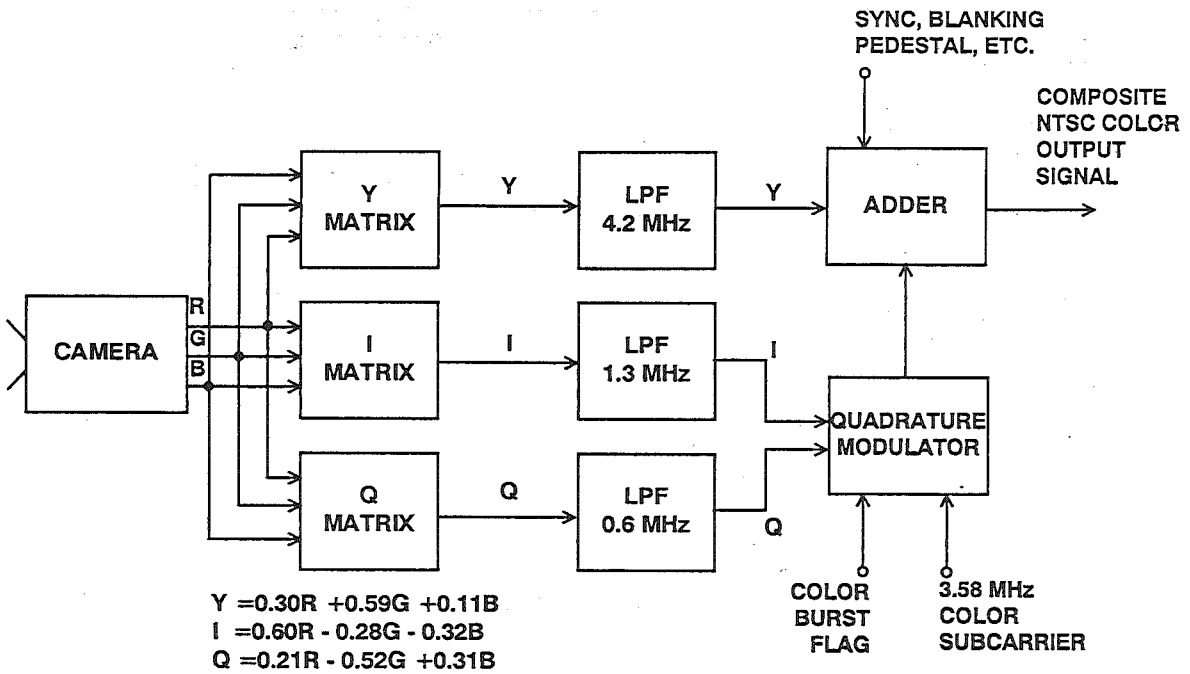
NTSC COLOR VIDEO LINE

Figure 2.4



NTSC FIELD TIMING DIAGRAM

Figure 2.5



GENERATING THE COMPOSITE NTSC COLOR SIGNAL

Figure 2.6

The A/D converter requirements in a digital application depend upon the point at which the video signal is digitized. For digital tape recorders, it is common to digitize the signal at the component level (Y, I Q) using three A/D converters. The sampling rate for the Y channel is typically twice that of the I and Q channel due to the larger bandwidth. Sampling rates of 13.5 MHz are typically used for the Y channel, and 6.75 MHz for the I and Q channel. A resolution requirement of 8 bits is quite common for component digitization. Flash converters such as the AD9048 fulfill these requirements in a cost effective manner.

In many digital television applications it is more desirable to digitize the entire composite NTSC signal. A sampling rate of 14.32 MHz (4 times the color subcarrier frequency of 3.58 MHz) is the accepted standard. The A/D converter resolution requirement is typically 8 bits, although 9 or 10 bits is more desirable if the signal must pass through multiple codecs before leaving the studio environment.

The PAL system is standard for Europe and is similar but not compatible with the NTSC system. The PAL system utilizes 625 horizontal lines (rather than 525 lines for NTSC) and a color subcarrier frequency of 4.43 MHz. The sampling rate requirement is therefore 17.73 MHz for 4x sampling of the composite signal.

Television signals are usually AC coupled, and therefore DC restoration is required ahead of the A/D converter. A track and hold can be used to sample the "back porch" portion of the video line and the DC offset reinserted using an op amp as shown in Figure 2.8. In addition to DC restoration, an anti-aliasing filter is required before applying the signal to the A/D converter input.

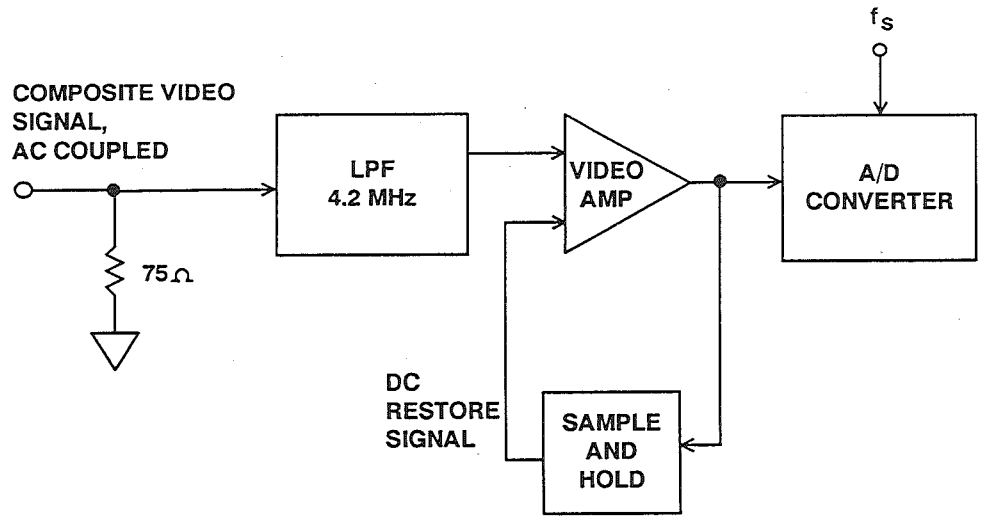
	NTSC	PAL
Horizontal Lines	525	625
Color Subcarrier Frequency	3.58 MHz	4.43 MHz
Composite Signal Sampling Rate	14.32 MHz	17.73 MHz
Frame Frequency	30 Hz	25 Hz
Field Frequency	60 Hz	50 Hz
Horizontal Sync Frequency	15.734 kHz	15.625 kHz

NTSC AND PAL CHARACTERISTICS

Figure 2. 7

Broadcast Video References

- IEEE Standard for Performance Measurements of A/D and D/A Converters for PCM Television Circuits, IEEE Standard 746-1984
- W.A. Kester, "PCM Signal Codecs for Video Applications", SMPTE Journal, Vol. 88, Nov. 1979, pp. 770-778.



CONDITIONING THE COMPOSITE VIDEO SIGNAL FOR DIGITIZATION

Figure 2.8

HIGH DEFINITION TV (HDTV)

Recent developments in the evolving field of High Definition TV (HDTV) require higher sampling rates and more resolution than is currently needed for NTSC, PAL, or SECAM. HDTV is touted as offering 35mm film quality video with CD quality audio. The generic requirements of HDTV that have been agreed upon internationally are the following: twice the vertical resolution of current systems, wide-screen aspect ratio, and digital audio. The similarities between systems stops there.

Different HDTV systems have been proposed in Japan, Europe, and the US. The HDTV standards in Japan and Europe are fairly well characterized, while a US standard has yet to be selected. US companies are currently participating in a series of FCC qualifications to select the US standard. It is expected that a final US standard will be established during 1991 or 1992.

Figure 2.9 shows the differences between the Japanese MUSE system (Multiple Subnyquist Sampling Encoding) and the European standard, which was developed by the Eureka-95 committee, and is known as HD-MAC (High Definition Multiplexed Analog Component). Both

MUSE and HD-MAC are designed to be delivered via DBS (Direct Broadcast Satellite) which will be received by small dishes attached to the roofs or windows of Japanese and European homes. This differs from the main means of US delivery, which are cable and terrestrial (i.e., through the air).

Because of the increased resolution of these HDTV systems (twice the vertical resolution and twice the horizontal resolution) there is four times as much data as for conventional TV systems. This increased bandwidth, even after compression, requires A/D converters with faster speeds and wider bandwidths than are needed for NTSC, PAL, or SECAM.

A major reason that HDTV is possible is the growing ability to manipulate TV images once they have been received by TV sets. IDTV (Improved Definition TV) sets are now becoming available with line and frame stores which process NTSC to improve transmission and display quality. Digital storage capability will be used not only for reception processing like ghost cancellation (the elimination of phase-shifted images received due to interference from large objects, see Figure 2.10), but also for advanced services like interactive shopping. In order to facilitate this image manipulation, the received signal must be digitized. Because of the loss of resolution due to ghost cancellation, gamma correction and a host of other

	MUSE	HD-MAC
COUNTRY/REGION	Japan	Western Europe
DELIVERY SYSTEM	DBS	DBS
VERTICAL RESOLUTION	1125 Lines	1250 Lines
FIELD RATE	60 Hz	50 Hz
INTERLACED	2:1	2:1
CHANNEL FREQUENCY	12 MHz	10.5 MHz
AUDIO	Digital	Digital
ADC CLOCK RATE	16.2 MSPS	20.25 MSPS
ADC RESOLUTION	10 Bits	10 Bits

MUSE AND HD-MAC CHARACTERISTICS

Figure 2.9

advanced image processing algorithms that may be implemented, it is generally acknowledged that more than 8-bits of resolution will be required.

NTSC, PAL, and SECAM are transmitted as composite video. Composite video modulates the image information about a number of carrier frequencies. These frequencies are typically confined to a narrow baseband frequency. A major artifact of composite video is crosstalk between the individual color and luminance information. Many HDTV systems use component video. Component video time multiplexes the image information, thereby reducing crosstalk as well as minimizing a number of other transmission related artifacts.

Figure 2.11 shows a block diagram of a typical HDTV system.

Analog Devices is currently working on a number of components for use in HDTV systems. The ADV7121 and ADV7122 are triple 10-bit, 80MSPS DACs which will be used to drive the CRTs of large-screen HDTV sets. Currently under development is the AD773. This 10-bit 20MSPS ADC will be suitable for use in HDTV receiver decoders for MUSE, HD-MAC, and eventually for a US standard. Also available are the AD9020 (10-BITS, 60 MSPS, TTL) and the AD9060 (10-BITS, 75 MSPS, ECL) ADCs for even higher sampling rates. The AD829 op amp is a good choice for HDTV applications due to its exellent differential gain and differential phase performance.

Further reading in HDTV:

Y. Ninomiya, et al., "NHK Proposes High-Definition TV Using MUSE Bandwidth Compression," **Journal of Electrical Engineering**, March 1985, pp. 40-44.

T. Ivall, "Eureka 95 - A World Standard?", **Electronics & Wireless World**, August 1988, pp. 845-850.

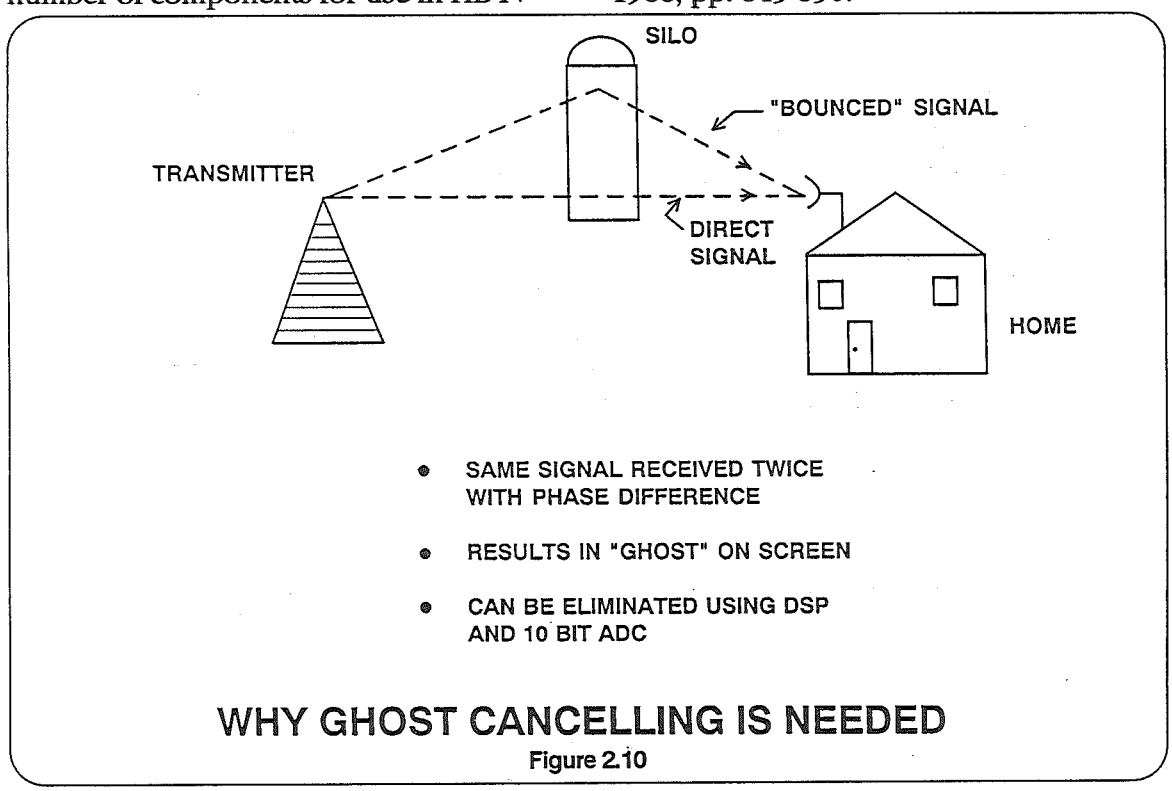
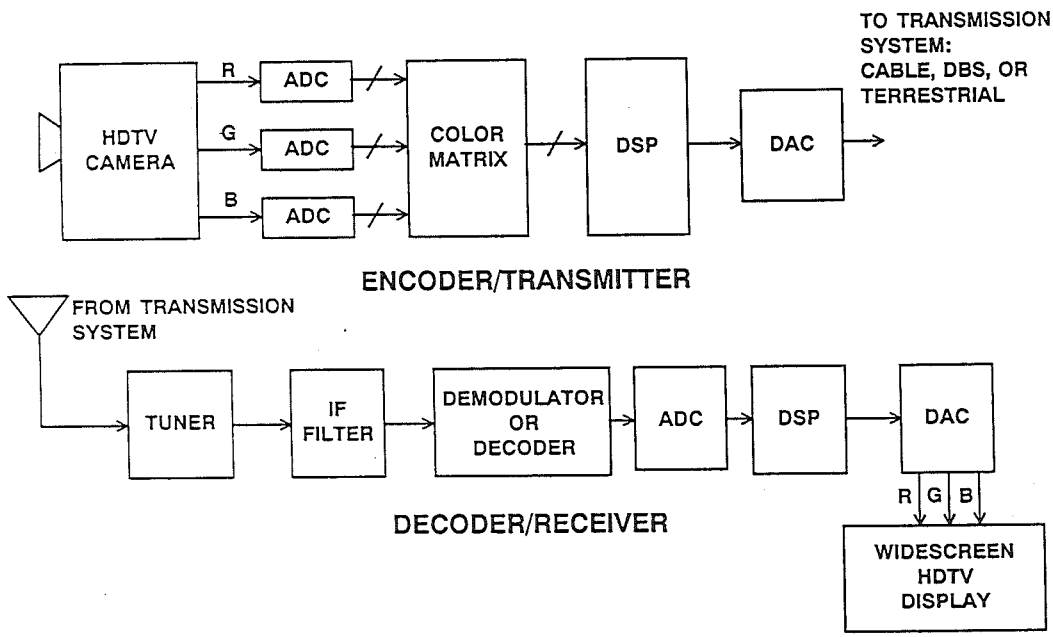


Figure 2.10



TYPICAL HDTV SYSTEM

Figure 2.11

HDTV COMPONENTS

ADC: AD773 - 10 BITS, 20 MSPS
AD9020 - 10 BITS, 60 MSPS (TTL)
AD9060 - 10 BITS, 75 MSPS (ECL)

DAC: ADV7121, ADV7122 } TRIPLE 10-BIT 30, 50, 80 MSPS

AMP: AD829

Figure 2.12

MULTIPLEXING AND SWITCHING VIDEO SIGNALS

There are many applications which require multiple video signals to be routed between several points or switched at high rates into a single output line. The largest application for video multiplexers is professional video signal routing and mixing. Other applications include radar, medical imaging, ECM, instrumentation and electro optics.

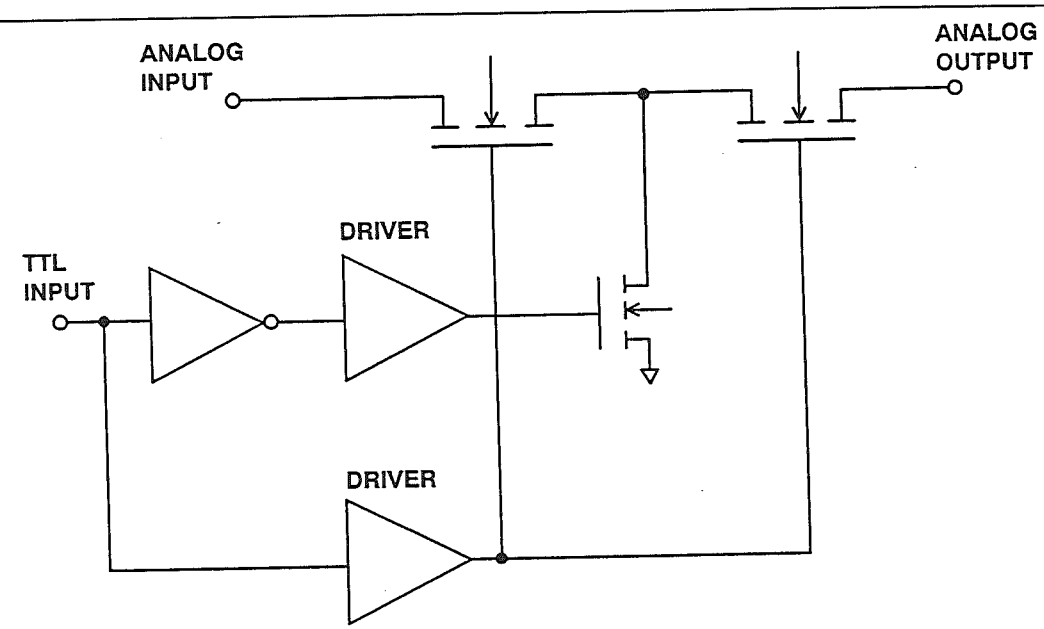
Key specifications for video multiplexers include gain tolerance, bandwidth, switching speed and settling time, channel to channel isolation, differential gain and phase and low power consumption. Individual switches are usually cascaded in a routing switch with a 64 x 16 router being a common configuration in professional video applications. The heart of a video multiplexer is the switch element. Discrete transistors and diodes are often combined in hybrid or modular packages to perform this switching function. DMOS (double diffused MOS) switches can be used in a "T" arrangement as shown in Figure 2.14 to provide the required signal isolation. Switching times of less than 100ns are achievable, but "ON" resistances are limited to about 50 ohms minimum.

The AD9300 4 x 1 wideband video multiplexer offers a totally monolithic bipolar solution with the key specifications shown in Figure 2.15.

VIDEO MULTIPLEXER KEY SPECIFICATIONS

- "On" Resistance
- Bandwidth
- Gain flatness and tolerance
- Crosstalk rejection
- Power consumption
- Cascadable
- Low input capacitance
- Low output impedance

Figure 2.13



DMOS "T" SWITCH

Figure 2.14

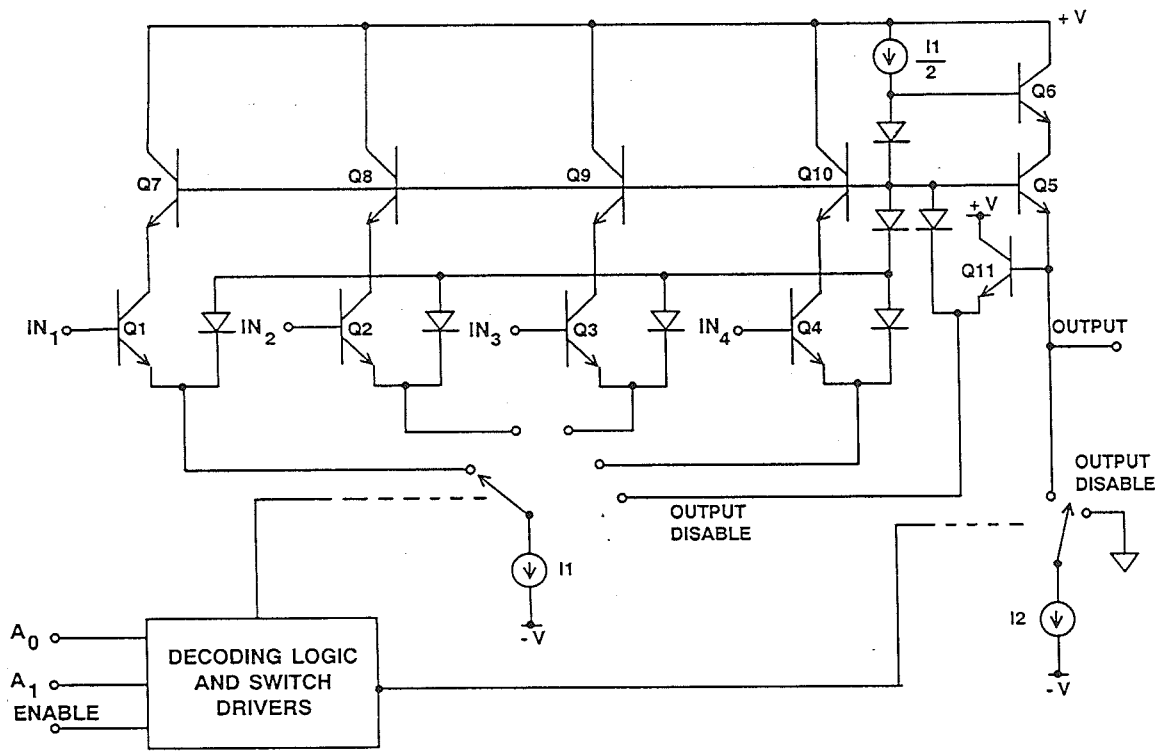
AD9300 4 x 1 Video Multiplexer Key Specifications

- 3 M Ω || 2 pF input impedance
- 34 MHz full power bandwidth, 2V p-p input
- ±0.1dB gain flatness to 8 MHz
- 75 dB crosstalk rejection at 10 MHz
- 0.05%/0.05° differential gain/phase
- 50ns switching time between channels
- 300mW power dissipation (±12V supplies)
- Outputs can be paralleled for switch matrixes
- No "On" Resistance

Figure2.15

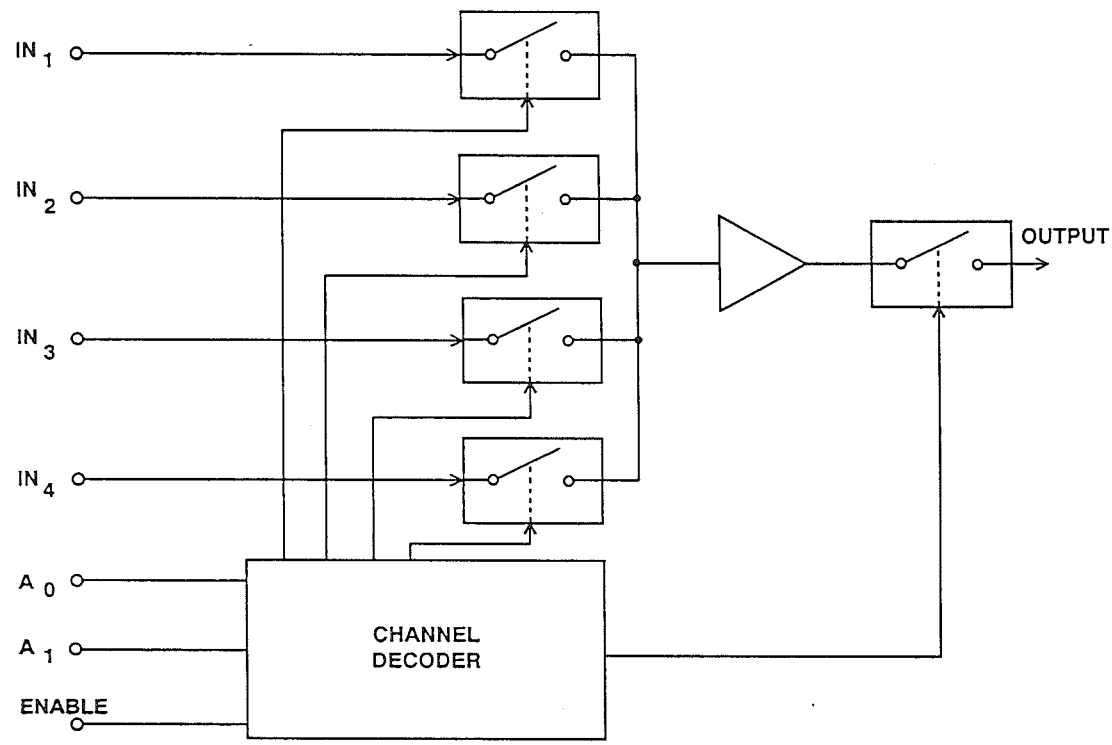
A block diagram of the AD9300 is shown in Figure 2.16. The input channel which is to be connected to the output is determined by a 2-bit TTL digital code applies to A_0 and A_1. The selected input will not appear at the output unless a digital "1" is also applied to the ENABLE input. The output is a high impedance (to allow cascading) if the ENABLE input is a logic "0".

A simplified schematic of the AD9300 is shown in Figure 2.17. Channel switching is achieved by routing the current I_1 to the appropriate cell as determined by the decoding logic. The output is disabled by turning off the current I_2 and routing the current I_1 as shown. The AD9300 achieves its high degree of linearity by utilizing bootstrapped emitter followers in the signal path which are biased at a constant V_{CB} of OV.



AD-9300 SIMPLIFIED SCHEMATIC

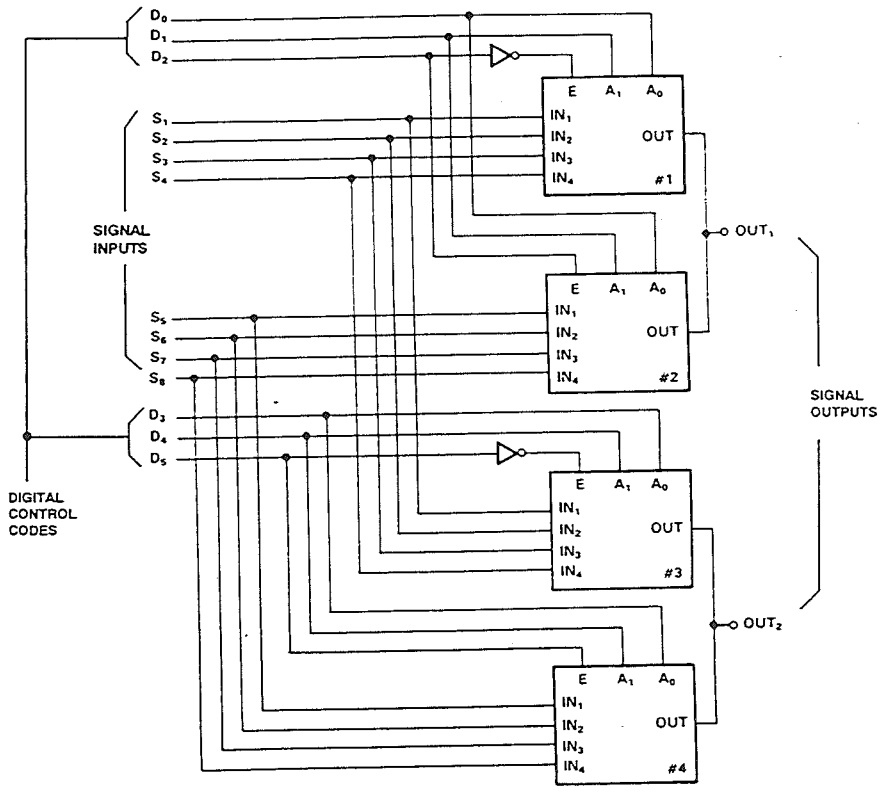
Figure 2.16



AD-9300 BLOCK DIAGRAM

Figure 2.17

Four AD9300 multiplexers can be used to implement an 8 x 2 crosspoint switch as shown in Figure 2.18. The truth table describes the relationships among the digital inputs (D_0 - D_5) and the analog input signals (S_1 - S_8); and which signal input is selected at the outputs (OUT_1 and OUT_2). The number of crosspoint modules that can be connected in parallel is limited by the drive capabilities of the input signal sources. High input impedance (3MΩ) and low input capacitance (2pF) of the AD9300 help minimize this limitation. Adding to the number of inputs applied to each crosspoint module is simply a matter of adding AD9300 multiplexers in parallel to the module. Eight devices connected in parallel result in a 32 x 1 crosspoint which can be used with input signals having 30MHz bandwidth and 1V p-p amplitude.



8 X 2 SIGNAL CROSSPOINT USING FOUR AD9300 MULTIPLEXERS

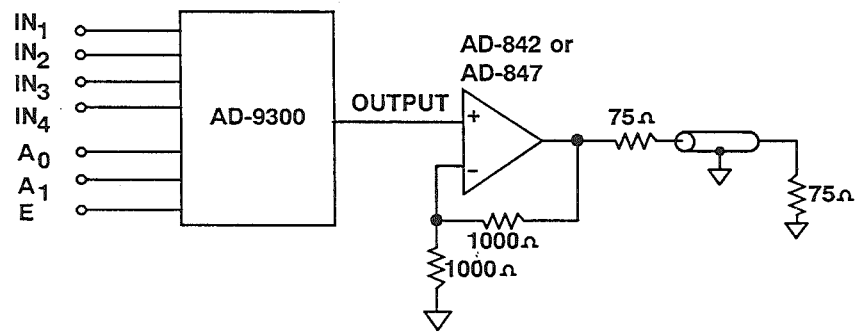
D_2 or D_5	D_1 or D_4	D_0 or D_3	OUT_1 or OUT_2
0	0	0	S_1
0	0	1	S_2
0	1	0	S_3
0	1	1	S_4
1	0	0	S_5
1	0	1	S_6
1	1	0	S_7
1	1	1	S_8

8 x 2 Crosspoint Truth Table

Figure 2.18

The output stage of the AD9300 has an impedance of approximately 10 ohms and is capable of driving a 2kΩ || 10pF load.

For applications such as cable driving, output buffers are recommended as shown in Figure 2.19.



AD-9300 MULTIPLEXER WITH BUFFERED OUTPUT DRIVING 75Ω COAXIAL CABLE

Figure 2.19

ELECTRONIC IMAGE PROCESSING SYSTEM DESCRIPTION AND APPLICATIONS

Computer processing of video images has found wide application in machine vision, pattern recognition, assembly operations, inspection, and graphic arts to name but a few. There are several important differences between an image processing system and the digital systems for broadcast television which were discussed in the previous section.

The first major difference is the lack of standardization in the image processing field. Broadcast television is regulated by the FCC, which rigidly enforces standards and performance requirements at key points in the transmission link. Since an image processing system is entirely self contained, there is no external requirement to conform to any particular standard other than the self-imposed restrictions of the camera itself. The manufacturer is thus entirely free to optimize the system design to achieve the particular performance requirements of the selected markets being addressed.

IMAGE PROCESSOR APPLICATIONS

- Machine Vision
- Pattern Recognition
- Automatic Assembly
- Inspection
- Graphic Arts

Figure 2.20

A second major difference between image processing systems and broadcast television lies in the methods used to synchronize the video signal. In broadcast applications, all cameras and other equipment inside the studio are synchronized to the studio horizontal sync, vertical sync, and color subcarrier signals. In an image processor, however, the synchronization signals are usually derived from the camera itself which serves as the master reference.

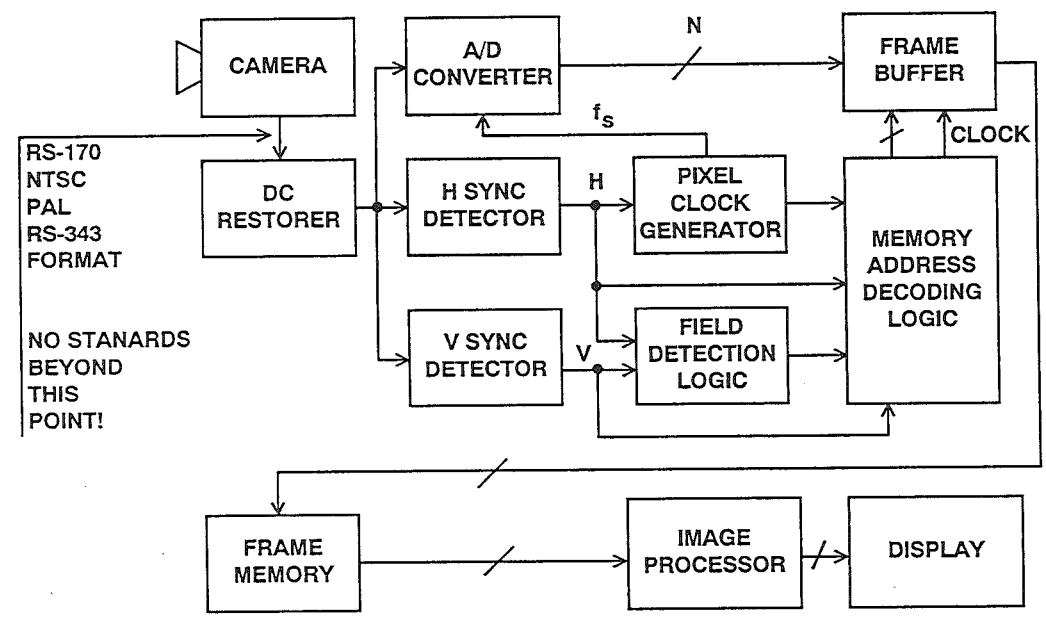
Figure 2.21 shows a block diagram of a typical image processing system. The video signal from the camera is usually AC coupled, therefore a DC restorer is required prior to further signal processing. After DC restoration, horizontal and vertical sync detectors extract the required synchronization signals from the camera video. Some high quality cameras such as CCD cameras provide the H and V sync outputs in addition to the video output. If H and V sync outputs are available from the camera, then the need for the two sync detector circuits is eliminated.

The A/D converter must then digitize the video signal for storage in the frame buffer. Typically 6- to 8-bit flash converters are used for this purpose. A number of factors enter into the process of determining the sampling rate (or pixel clock frequency) which are discussed in detail in the application note: "The AD9502 Video Signal Digitizer and Its Application". The following is a brief summary of the process.

The first step is to determine the vertical and horizontal resolution requirements. The standard RS-170 signal has an aspect ratio of 4:3, i.e., the image is wider than it is tall. The RS-170 frame consists of 525

horizontal lines of which 485 lines contain active video. The remaining 40 lines are allocated to what is called the "vertical interval" which distinguishes between the two interlaced fields of 242 1/2 active lines each.

It is important to determine what the "active" vertical and horizontal video resolution is going to be, since only the "active" video pixels need to be stored in the frame memory. Memory conservation is extremely important in image processors due to cost, power, size, and software complexity.

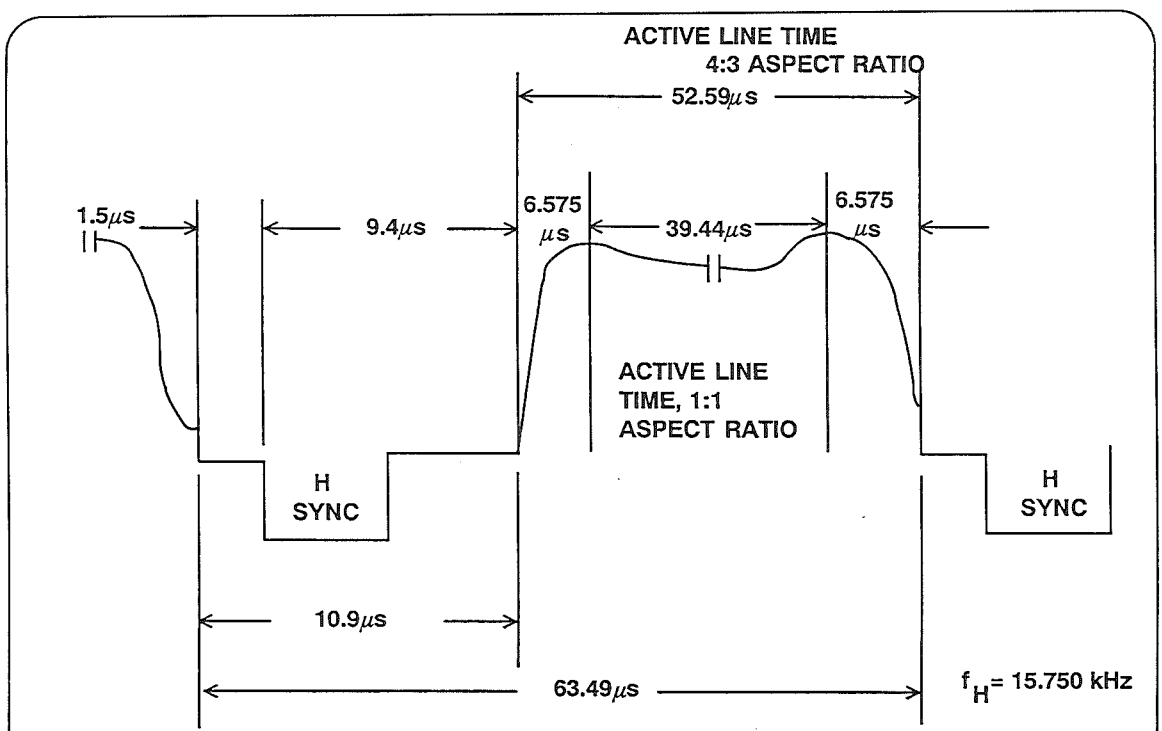


BASIC IMAGE PROCESSING SYSTEM

Figure 2.21

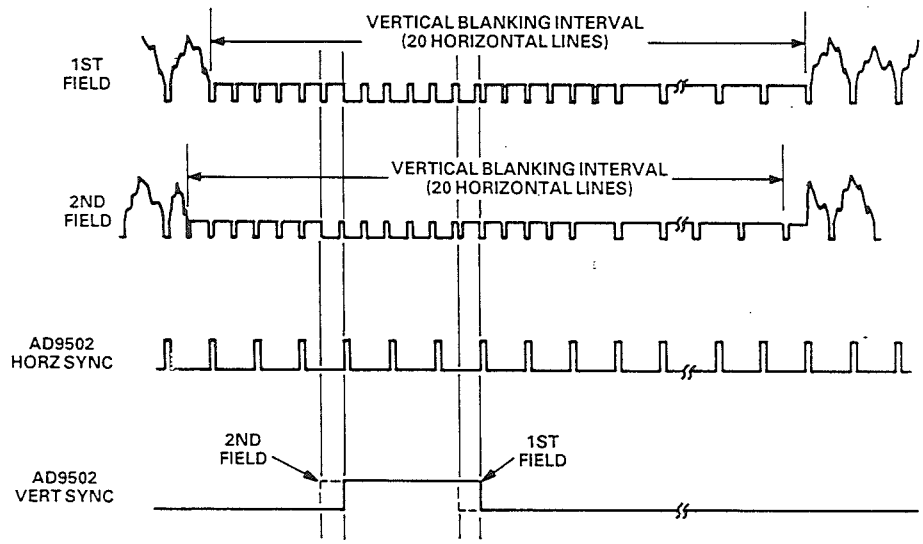
The active video portion of a horizontal line is 52.59 μs for a 4:3 aspect ratio in RS-170. (This is shown in Figure 2.22.) Many image processing algorithms are designed for a 1:1 aspect ratio, in which case the active line time is 3/4 x 52.59 μs= 39.44 μs. This new active line time of 39.44 μs is centered within the 4:3 aspect ratio line of 52.59 μs allowing an "inactive" time of 6.575 μs on either side. The ultimate image will have an aspect ratio of 1:1 appearing with black on either side to fill the entire 4:3 screen.

The active portion of the horizontal line must now be divided into a finite number of picture elements, or pixels. Each pixel on the horizontal line will represent one sample out of the A/D converter, therefore the pixel clock rate is determined by the active line time and the number of desired pixels. For instance, a resolution of 512 pixels per line is common for image processing systems. In an RS-170 system where the aspect ratio is 1:1, the active line time has been shown to be 39.44 μs. The pixel clock frequency can now be calculated by dividing the number of desired pixels (512) by the active line time (39.44 μs) resulting in a pixel clock rate of 12.98 MHz. If the pixel clock frequency is determined by a gated oscillator, the oscillator frequency is simply set to 12.98 MHz. It is often desirable, however, to have the oscillator frequency generated by a phase locked loop (PLL) which is locked to the horizontal frequency of 15.750 kHz. The nearest frequency to 12.98 MHz which is an integer multiple of 15.750 kHz is 12.978 MHz which is 824 times 15.750 kHz. The divide-by-N circuit in the PLL would therefore require N = 824.



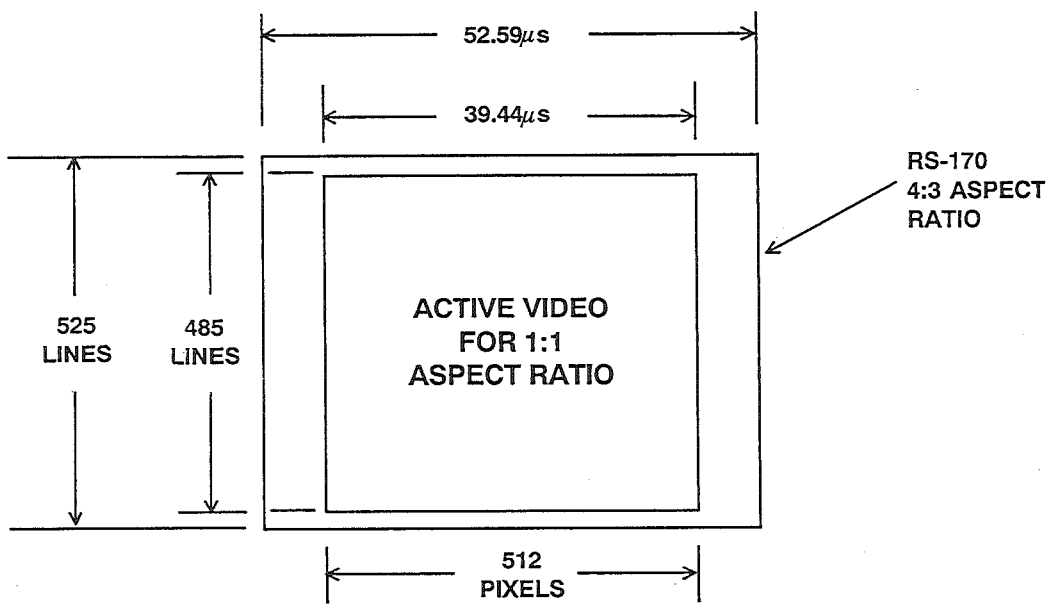
RS-170 ACTIVE LINE TIME

Figure 2.22



RS-170 FIELD TIMING

Figure 2.23



RS-170 ACTIVE VIDEO

Figure 2.24

Referring to Figure 2.21, the purpose of the memory address decoding logic is to gate the A/D converter data to the appropriate memory location in the frame buffer. The field detection logic examines the H and V sync signals and identifies which of the two fields is being processed. Pixel data from the A/D converter is only clocked into the frame buffer during the active line time of the active video lines. Field timing is shown in Figure 2.23, and the active picture area in Figure 2.24.

Image Processing Memory Management

To understand the flow of the digitization process, we start at the vertical sync time. This sync signal indicates that a field is beginning. The field detection logic determines if it is an even or odd field. Assuming it is an even field, a video line counter is set to zero. Digitization starts following the eleven blank video lines and the detection of the successive horizontal sync pulse. Horizontal sync indicates the start of a line. Once detected, the video pixel counter is set to zero and a delay timer times or counts pixels for 9.4 μs (width of remaining horizontal sync interval) plus 6.575 μs (the inactive line time for a 1:1 aspect ratio). At the end of the 15.975 μs delay interval, the sampling process begins occurring repetitively at the interval prescribed by the number of pixels in the line. Once the correct number of pixels have been sampled, sampling stops and the next horizontal sync is awaited. The arrival of the next vertical sync indicates the start of the odd field. The sampling process continues for the odd field as has been previously described for the even field.

If the pixel clock is phased locked to the H sync it will run continuously. The memory address decoding logic contains a number of counters which perform the delay function and clock the A/D converter pixel data into the appropriate address of the frame buffer at the appropriate time.

If the pixel clock is generated using a gated oscillator, the oscillator is started at the detection of the leading edge of the sync pulse. Delay counters are used in a similar manner until the last pixel of the active line time is digitized. The oscillator is then stopped until the next horizontal sync pulse is detected.

MEMORY MANAGEMENT/SYNCHRONIZATION FLOWCHART

- Detect Vertical Sync
- Detect Even or Odd Field
- Count 11 No-Video Lines
- Detect H Sync Pulse for First Active Line
- Count Out 9.4 μs to End of H Sync Interval
- Count Out Inactive Line Time 6.575 μs (For 1:1 Aspect Ratio)
- Count Out and Digitize Active Video Pixels
- Stop Pixel Counter
- Detect H Sync Pulse for Second Active Line
    -
    -
    -
- Stop Active Line Counter After Last Active Line Sync Pulse
- Detect Vertical Sync
- Detect Even or Odd Field
    -
    -
    -

Figure 2. 25

The purpose of this somewhat tedious process of memory management where only active pixels are stored in the frame buffer is illustrated in Figure 2.26. If all pixels are stored in memory and the pixel data sorted in software, a total of 432,600 pixels per frame is required. If a 1:1 aspect ratio is chosen and only the active pixels are stored, a total of only 248,320 pixels per frame are required. The 43% savings in memory is well worth the additional logic required for memory management.

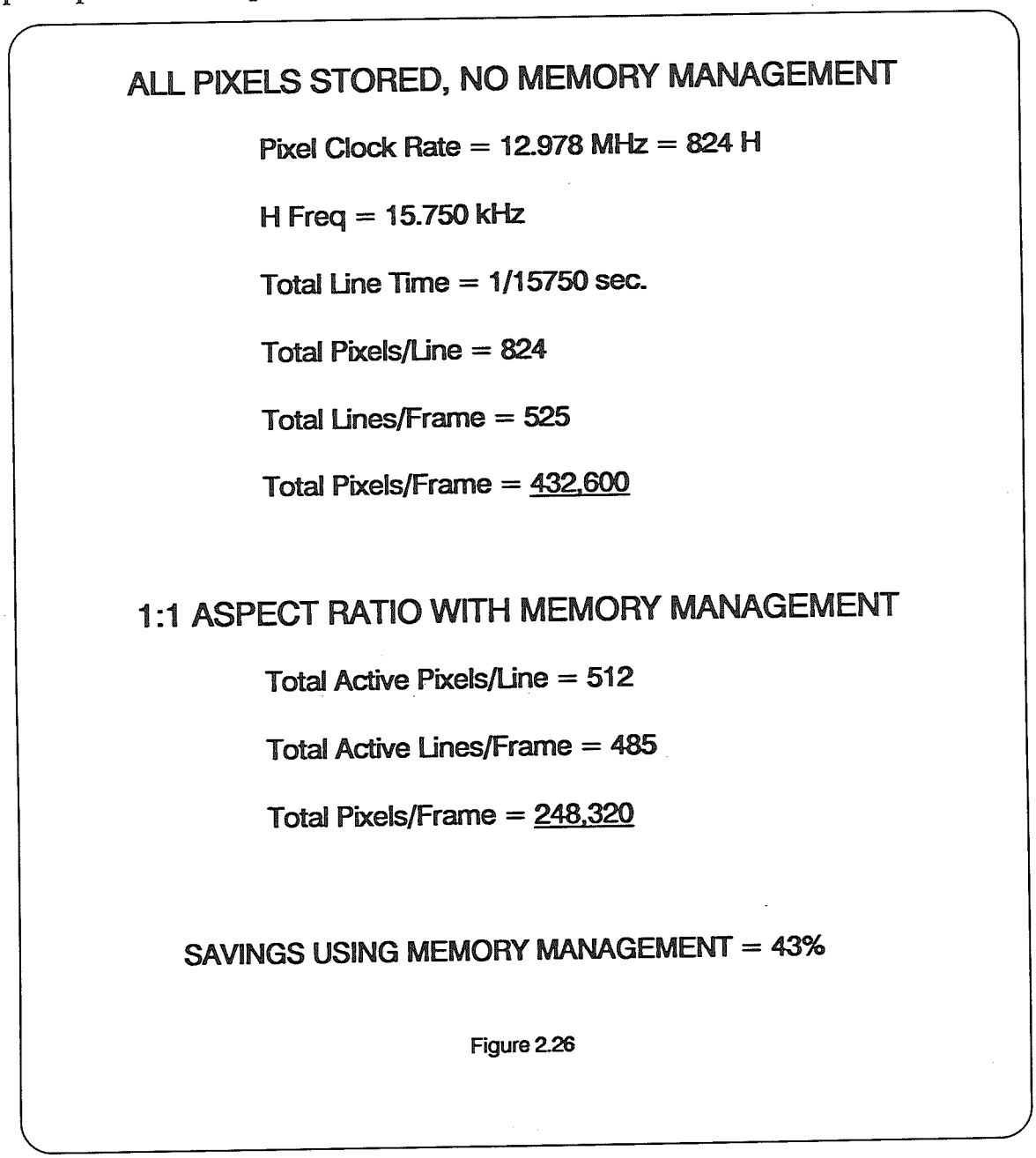


Figure 2.26

AD-9502 RS-170 DIGITIZER DESCRIPTION

The AD9502 hybrid RS-170 digitizer offers a convenient approach to signal conditioning and data acquisition for an image processor. A block diagram is shown in Figure 2.27. The AD9502 consists of four major parts: the phase locked loop (PLL), DC restoration, sync detector, timing circuits, and an 8-bit flash A/D converter.

The PLL comprises a phase detector, loop filter/amplifier, voltage controlled oscillator (VCO), and a digital divider. The frequency of the pixel clock (F_{pc}) is related to the horizontal line frequency (F_H) by the following equation:

$F_{pc} = F_H \bullet 16 \bullet N$, where $28 < N < 62$, N an Integer.

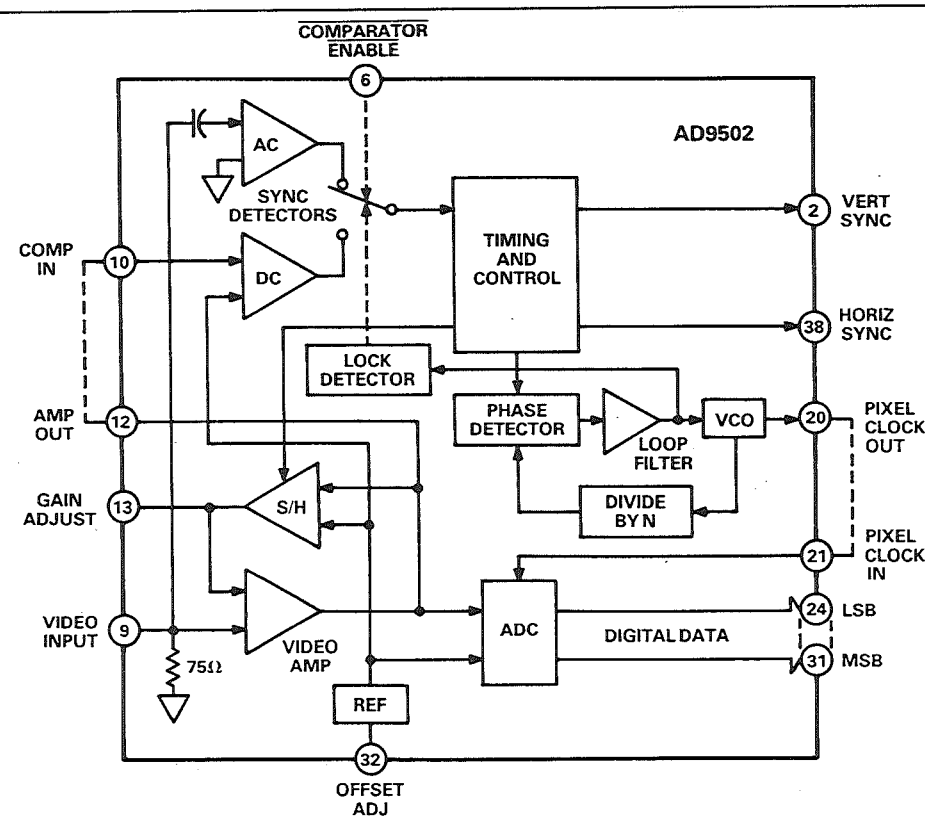
Three values of N are offered as options:

AD9502AM, N = 29, $F_{pc} = 464\ F_H$

AD9502BM, N = 39, $F_{pc} = 624\ F_H$

AD9502CM, N = 51, $F_{pc} = 816\ F_H$

For other values of N, consult the factory.



AD-9502 FUNCTIONAL BLOCK DIAGRAM

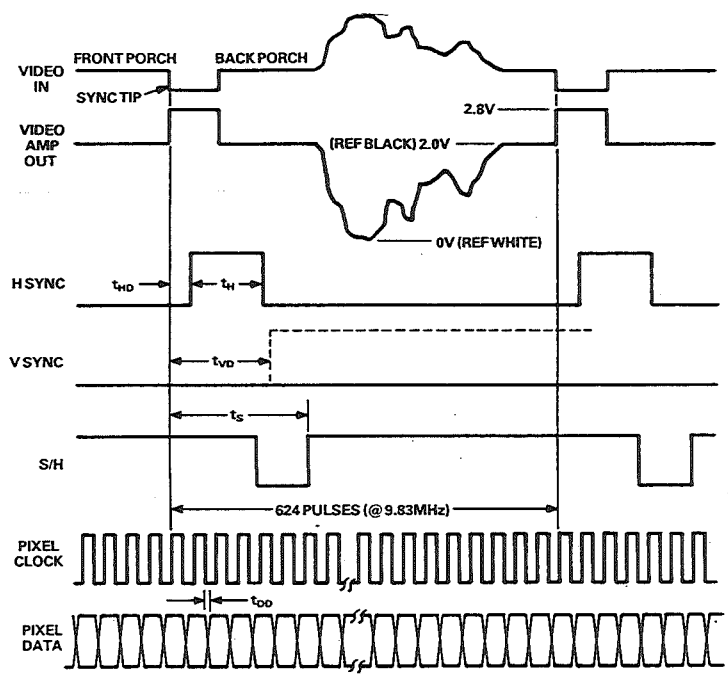
Figure 2.27

The sample and hold video amplifier establishes a feedback loop for DC restoration. Figure 2.28 depicts system timing. The sample pulse for the monolithic S/H amplifier occurs during the back porch of the video signal. When S/H is placed in the hold mode, the output of the S/H produces the proper amount of offset to DC restore the video signal into the range of the flash A/D converter.

During normal operation, sync pulses from the video amplifier drive the PLL after pulse detection and conditioning.

During power up or loss of signal the PLL will be unlocked. The comparator and all pulses are disabled during this time and the AC coupled signal path is enabled, allowing the PLL to synchronize.

The vertical sync pulse is generated whenever the duration of the incoming horizontal sync pulse is longer than 6.6 μs. This pulse is shown with a dashed line in Figure 2.28 to indicate it is present only after the correct number of horizontal lines have occurred.



		MIN	MAX
		μs	
t_{HD}	H SYNC DELAY	−0.4	+0.7
t_H	H SYNC WIDTH	+4.5	+5.4
t_{VD}	V SYNC DELAY	+5.5	+6.7
t_S	SAMPLE DELAY	+7.9	+9.4
t_{DD}	DATA DELAY	+0.02	+0.05

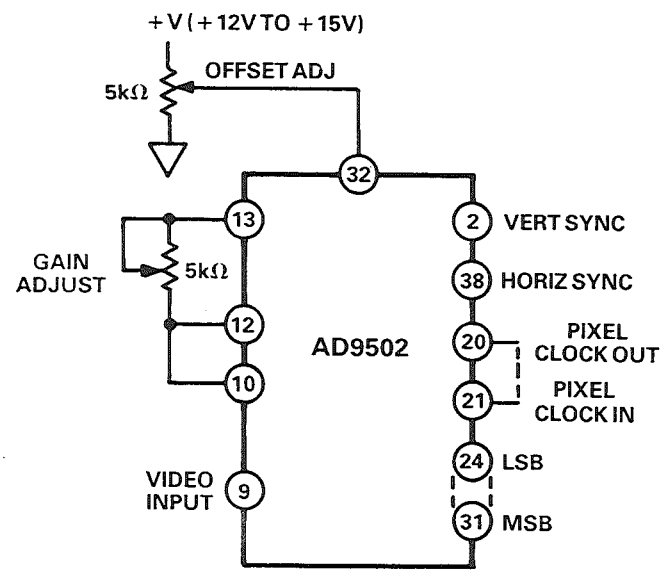
AD-9502 TIMING DIAGRAM

Figure 2.28

Since the RS-170 standard allows for differences in the amplitude and setup (difference between reference black and the blanking level) of the video signals, the AD9502 includes a capability of changing gain 3 dB and varying the offset by 200mV as shown in Figure 2.29.

The internal flash converter provides 8 bits of resolution and digitizes the range from reference white to reference black (sometimes called the "gray scale").

The application of the AD9502 to RS-170, NTSC, and PAL signals is shown in Figure 2.30.



AD-9502 GAIN AND OFFSET ADJUSTMENT

Figure 2.29

AD9502 APPLICATIONS

	RS-170		NTSC		PAL		
F_H (HORIZ. FREQ.)	15.750 kHz		15.734 kHz		15.625 kHz		
ACTIVE LINE WIDTH	52.59 μs		52.66 μs		51.95 μs		
PART NUMBER	PIXEL RATE (MHz)	PIXELS PER LINE	PIXEL RATE (MHz)	PIXELS PER LINE	PIXEL RATE (MHz)	PIXELS PER LINE	PIXEL* RATE
AD9502AM	7.308	384	7.300	384	7.250	377	464 F_H
AD9502BM	9.828	517	9.818	517	9.750	507	624 F_H
AD9502CM	12.852	676	12.839	676	12.750	663	816 F_H

*CONTACT FACTORY FOR PIXEL CLOCK FREQ = F_H • 16 • N, WHERE 28 ≤ N ≤ 50.

Figure 2.30