SECTION XI

HIGH SPEED TECHNIQUES

HIGH SPEED TECHNIQUES

INTRODUCTION

IMPEDANCE
Resistance, Inductance, Capacitance

GROUNDS AND GROUNDING
Kirchoff's Law, Ground Systems

NOISE
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CONSTRUCTION
IC Sockets

PROTOTYPING HIGH SPEED CIRCUITS

HIGH SPEED PROBING TECHNIQUES

INTRODUCTION

Low speed digital circuits can be fabricated using the "node" approach. That is to say, the components are wired together according to the circuit diagram, and any two points in the circuit which are connected by conductors, either wire or PC track, are assumed to be at the same potential. This approach does not work with high speed or high precision circuits and most especially does not work with high speed high precision circuits. This is because the conductors making connections between the components are not pure short circuits, as the "node" approach assumes, but have resistance, inductance and capacitance and therefore modify the original circuit.

One of the most important mistakes arising from the "node" approach is the assumption that all points in a circuit which are connected to "ground" on the circuit diagram will be at the same potential. As we shall see, this is a major source of errors.

Low speed digital circuits are also highly resistant to noise problems - whether from internally or externally generated noise. High speed and high precision analog circuits are not resistant to noise, and again we must consider all possible noise effects when designing the physical layout of such systems.

It is quite difficult to formulate rules for the efficient layout of high speed and high precision circuits, which is why effective CAD software for such a task is largely unavailable. This section of our seminar is devoted to discussion of the problems involved in such layouts. While it contains considerable detail of potential problems, it contains few specific rules for precision high speed layout, since almost all such "rules" tend to be more misleading than useful.

The rules that it does offer, as absolutes, are some Laws of Physics: Ohm's Law, Kirchoff's Law, Faraday's Laws and Lenz's Law, together with a basic law of life: Murphy's Law (sometimes known as Klipstein's Law in German-speaking countries) - this states that if anything can go wrong, it will!

BASIC LAWS INVOLVED IN PCB LAYOUT.

(MURPHY'S LAW IS THE MOST IMPORTANT.)

- OHM'S LAW
- KIRCHOFF'S LAW
- FARADAY'S LAWS
- LENZ'S LAW
- MURPHY'S LAW

Figure 11.1

Consideration of these laws reminds us that, since room temperature superconductors are not yet available (at the time of writing this section of the seminar, at any rate), any conductor, whether wire or PC track, will have resistance. It will also have self-inductance, and self-capacitance, and mutual inductance and capacitance to any adjacent conductors. All these properties will affect circuit performance and must be considered when designing the physical layout of high-performance analog systems. Murphy's law tells us that when designing such systems it is extremely ill-advised to disregard any physical effect known to be present without doing a calculation (or an experiment) to prove that such neglect is justified.[1]

IMPEDANCE - Resistance

At 25°C the resistivity of pure copper is 1.724E-6 ohm cm. The thickness of standard weight (1 ounce) PCB foil is 0.038 mm (0.0015"). The sheet resistance of standard PCB copper is therefore 0.45 milliohms/square, which implies a resistance for the 0.25 mm track frequently used in computer designed digital circuitry of 18 milliohms/cm, which is quite large. Moreover, the temperature coefficient of resistance for copper is about 0.4% /degree C around room temperature, which can be a further inconvenience.

As an illustration of the effect of PCB track resistance, consider a 16-bit ADC with a 5K input resistance which has 5 cm of 0.25 mm PCB track between it and its signal source. This track has a resistance of approximately 0.09 ohms and introduces a gain error of well over 1 LSB into the ADC.

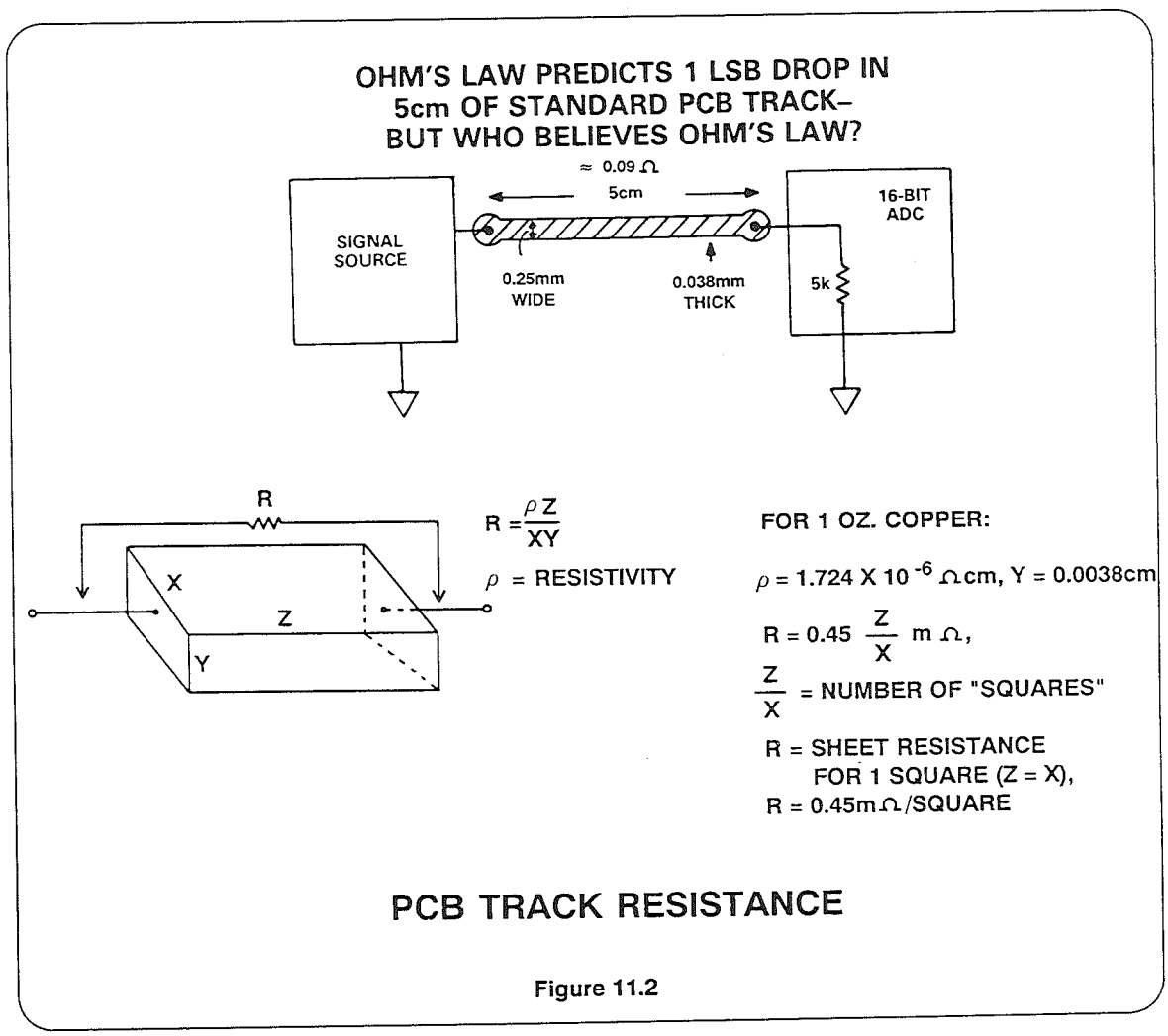


Figure 11.2

This, of course, is a DC effect. At high frequencies we must also consider the "skin effect" where inductive effects cause currents to flow only in the surface of conductors. This has the effect of increasing the resistance of a conductor at high frequencies (note that this effect is separate from the increase in impedance due to the effects of the self-inductance of conductors as frequency is increased - that will be dealt with later). Skin effect is quite a complex phenomenon and detailed calculations are beyond the scope of this seminar. However a good approximation for copper is that the skin depth is

$6.61/\sqrt{f}$ cm, where f is the frequency in Hz.

Assuming that skin effects become important when the skin depth is less than 50% of the thickness of the PC foil this tells us that for normal 0.038 mm PC foil we must be concerned about skin effects at frequencies above approximately 12 MHz.

Where skin effect is important, the resistance in ohms per square for the surface area of copper is

$$2.6 \times 10^{-7} \sqrt{f} \text{ ohms per square.}$$

When calculating skin effects in PCBs it is important to remember that current flows in both sides of the PC foil (this is not necessarily the case in microstrip lines), so the resistance per square of PC foil is half the above value.

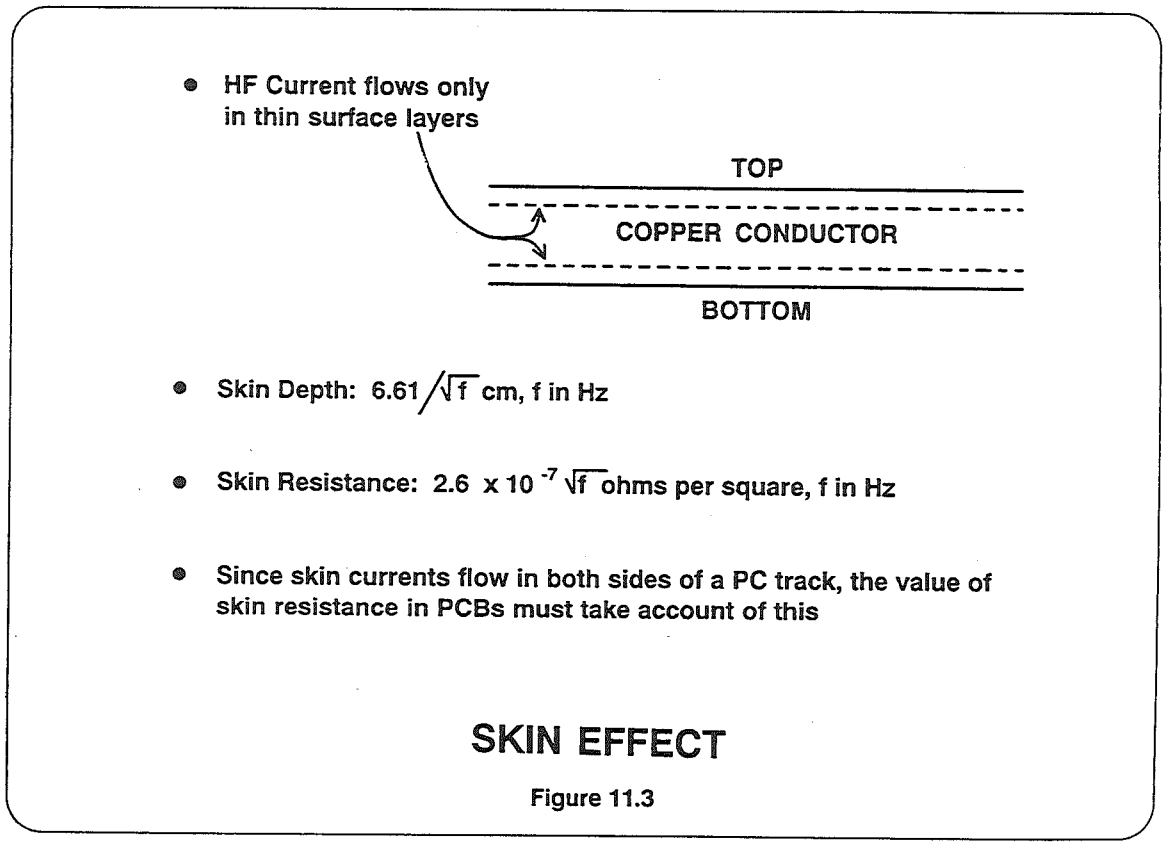


Figure 11.3

IMPEDANCE - Inductance

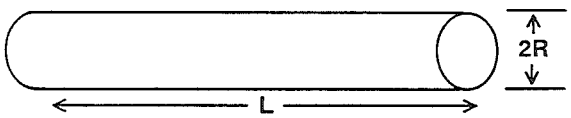
The inductance of conductors is also important. The inductance of a wire of length L mm and circular cross-section with radius R mm in free space is

$$0.0002L\left[\ln\left(\frac{2L}{R}\right) - 0.75\right]\mu H.$$

The inductance of a strip conductor (an approximation to a PC track) of width W mm and thickness H mm in free space is

$$0.0002L\left[\ln\left(\frac{2\text{-}L}{W+H}\right) + 0.2235\left(\frac{W+H}{L}\right) + 0.5\right]\mu H.$$

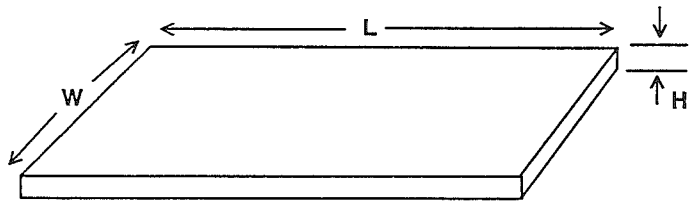
In real systems these formulae both turn out to be very approximate but they do give some idea of the order of magnitude of inductance involved. They tell us that 1 cm of 0.5 mm outside diameter wire has an inductance of 7.26 nH and 1 cm of 0.25 mm PC track has an inductance of 9.59 nH - these figures are reasonably close to measured results.



L, R in mm

WIRE INDUCTANCE = $0.0002L\left[\ln\left(\frac{2L}{R}\right) - 0.75\right]\mu H$

EXAMPLE: 1cm of 0.5mm o.d. wire has an inductance of 7.26nH
(2R = 0.5mm, L = 1cm)



STRIP INDUCTANCE = $0.0002L\left[\ln\left(\frac{2L}{W+H}\right) + 0.2235\left(\frac{W+H}{L}\right) + 0.5\right]\mu H$

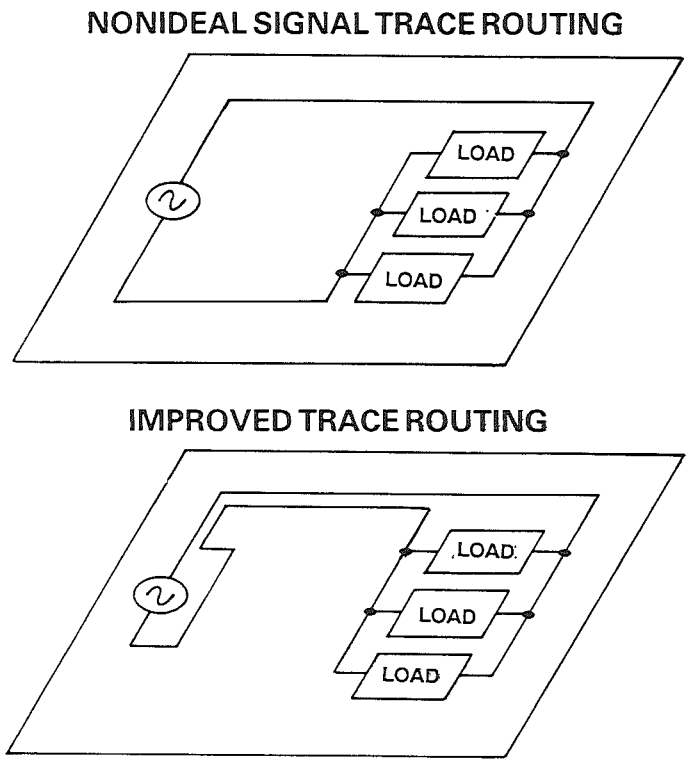
EXAMPLE: 1cm of 0.25 mm PC track has an inductance of 9.59 nH
(H = 0.038mm, W = 0.25mm, L = 1cm)

INDUCTANCE

Figure 11.4

Another consideration with respect to inductance is the separation of outward and return currents. As we shall discuss in more detail later, Kirchoff's Law tells us that current flows in circles - there is always an outward and return path. The whole path forms a single-turn inductor.

If the area enclosed by the turn is large, the inductance, and hence the AC impedance, will also be large, whereas if the outward and return paths are close together the inductance will be much smaller. The principle is illustrated in Figure 11.5.



NONIDEAL AND IMPROVED SIGNAL ROUTING

Figure 11.5

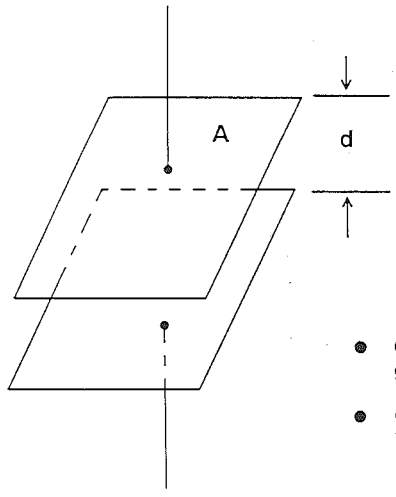
The nonideal routing in Figure 11.5 has another drawback - the large area enclosed by the conductor produces extensive external magnetic fields, which may interact with other circuits and cause unwanted coupling. Similarly the large area is more vulnerable to interaction with external magnetic fields, which can induce unwanted signals in the loop. The small area routing is far less liable to these mutual inductance effects.

IMPEDANCE - Capacitance

Like inductance calculations, capacitance calculations on PCBs are somewhat approximate, being affected by edge effects. The commonest calculation, that of a PC track above a ground plane, uses the simple parallel plate capacitor formula

$$C = 0.00885\ E_r\ A/d\ pF$$

where A is the area of plates in square mm, d is their separation (the board thickness) in mm, and E_r is the dielectric constant (relative to air). Given that one of the commonest types of PCB uses glass-fibre/epoxy material with E_r of approximately 4.7 and that the most often used thickness is 1.5 mm (approximately equal to 1/16 inch), the capacity of PC track over a ground plane may be roughly estimated at 0.28 pF/sq.cm. Such capacitors do not have particularly good Q (unless expensive low-loss board materials such as teflon are used) and so are not generally used in place of discrete capacitors in critical applications. However, their effect on circuit performance must always be considered.



$$C = \frac{0.00885\ E_r\ A}{d}\ pF$$

A = plate area in mm

d = plate separation in mm^2

E_r = dielectric constant relative to air

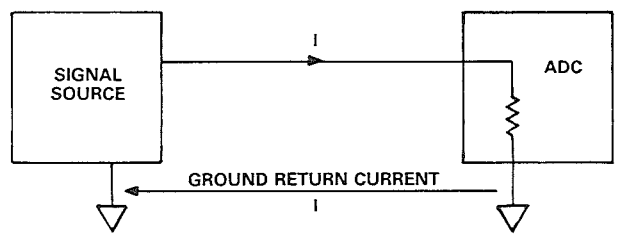
- Commonest type of PCB uses 1.5mm glass-fiber epoxy material with $E_r = 4.7$
- Capacity of PC track over ground plane is roughly $0.28pF/cm^2$

CAPACITANCE

Figure 11.6

GROUNDS & GROUNDING - Kirchoff's Law

Kirchoff's Law tells us that at any point in a circuit, the algebraic sum of the currents is zero. This means that all currents flow in circles and, particularly, the return current must always be considered when analyzing a high-speed or high precision circuit.[2]

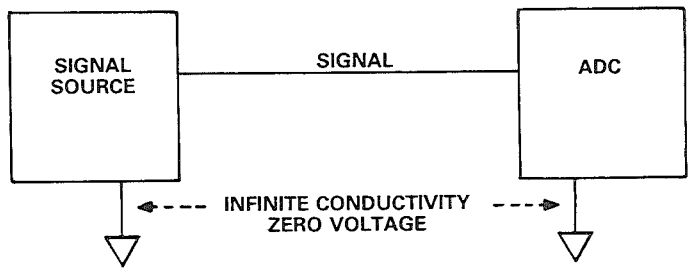


AT ANY POINT IN A CIRCUIT
THE ALGEBRAIC SUM OF THE CURRENTS IS ZERO
OR
WHAT GOES OUT MUST COME BACK
WHICH LEADS TO THE CONCLUSION THAT
ALL VOLTAGES ARE DIFFERENTIAL
(EVEN IF THEY'RE GROUNDED)

KIRCHOFF'S LAW

Figure 11.7

Most people consider the return current when considering a fully differential circuit, but when considering the more usual circuit where a signal is referred to "ground" it is far too common for engineers to assume that all the points on the circuit diagram where the ground symbol is to be found are at the same potential.

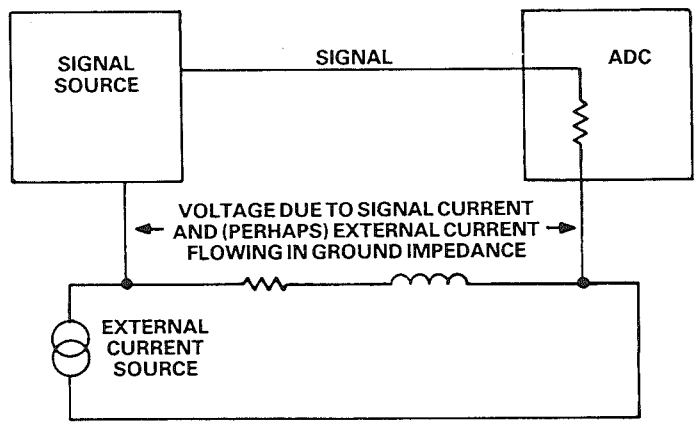


THE IDEAL GROUND

Figure 11.8

A more realistic model of ground is shown in Figure 11.9. Not only does the return current flow in the complex impedance which exists between the two "ground" points shown in Figure 11.8, giving rise to a voltage drop in the total signal path, but also external currents may flow in the same path, generating uncorrelated noise voltages which are seen by the ADC.

Once we have defined the problem, the nature of the solution becomes obvious: minimize ground impedances so that the ground of a system really is unipotential and also attempt to minimize externally-generated noise currents in sensitive ground impedances. Unfortunately, this is more easily said than done, and many diferent ground arrangements have been adopted at various times to try to solve the basic problem.



A MORE REALISTIC GROUND

Figure 11.9

GROUNDS & GROUNDING - Ground Systems

The most common techniques are the star ground, separate analog and digital grounds, the ground plane, and the elimination of the need for an accurate ground by the use of differential signal transmission. All have their advantages and disadvantages but, as it is rare for one approach to solve all problems, hybrid solutions are frequently chosen.

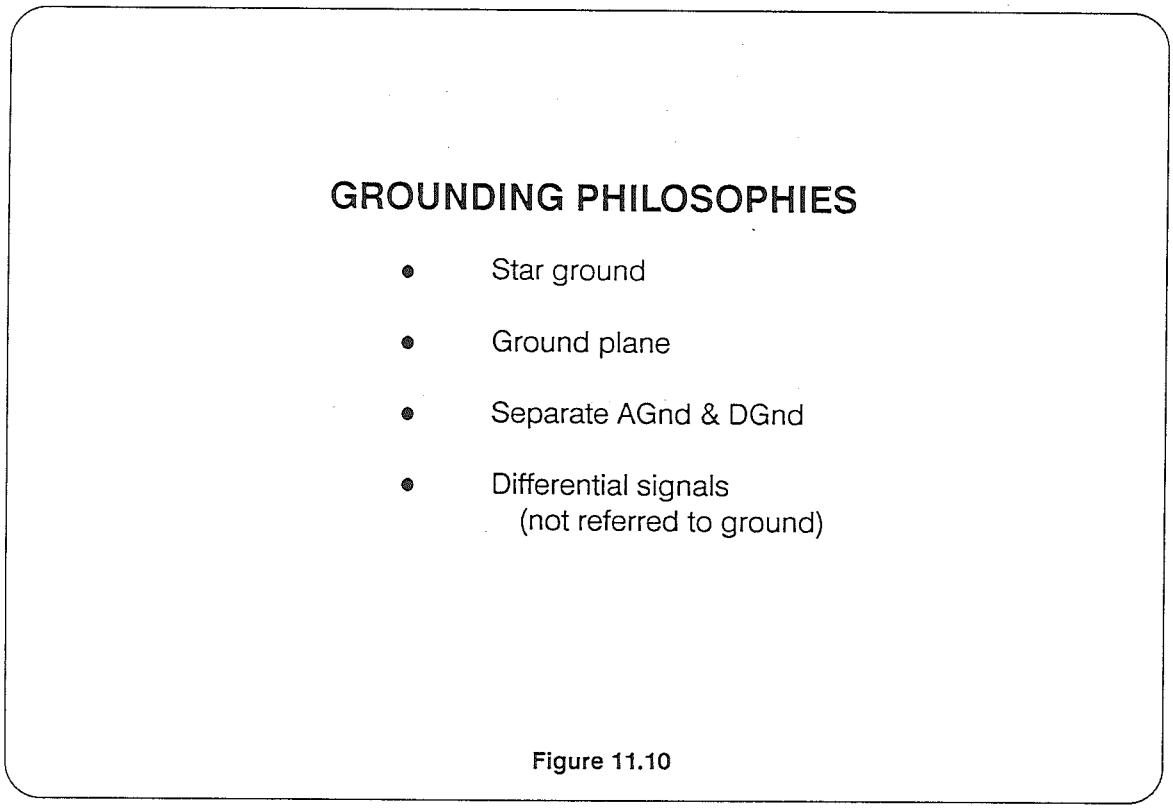


Figure 11.10

The "star" or "Mecca" ground philosophy is based on the theory that there is a single point in a circuit to which all voltages are referred. This is known as the "star" or "Mecca" point.

This philosophy is reasonable but encounters practical difficulties. For example, if we design a system with a star ground, we first draw all the signal paths to minimize signal interaction and the effects of high impedance signal or ground paths. We frequently find, however, when the power supplies are added to the circuit diagram, that the power supplies either add unwanted ground paths, or that supply currents, flowing in existing ground paths, are sufficiently large, or noisy, or both, as to corrupt the signal transmission. This problem is often avoided by having separate analog and digital power supplies and separate

analog and digital grounds, joined at the star point.

There is often a practical problem with analog-digital converters (ADCs). For reasons concerned with practical interfacing techniques and available integrated circuit architectures, it is common for monolithic and hybrid ADCs to have separate analog ground (AGnd) and digital ground (DGnd) pins. Nevertheless, they must not see a potential difference of more than a few mV, and must therefore be connected close to the ADC package. How do we accomplish this? We can, of course, make this point the star point of the whole system but it is rarely convenient to do so - and impossible if there are several such ADCs in a system.

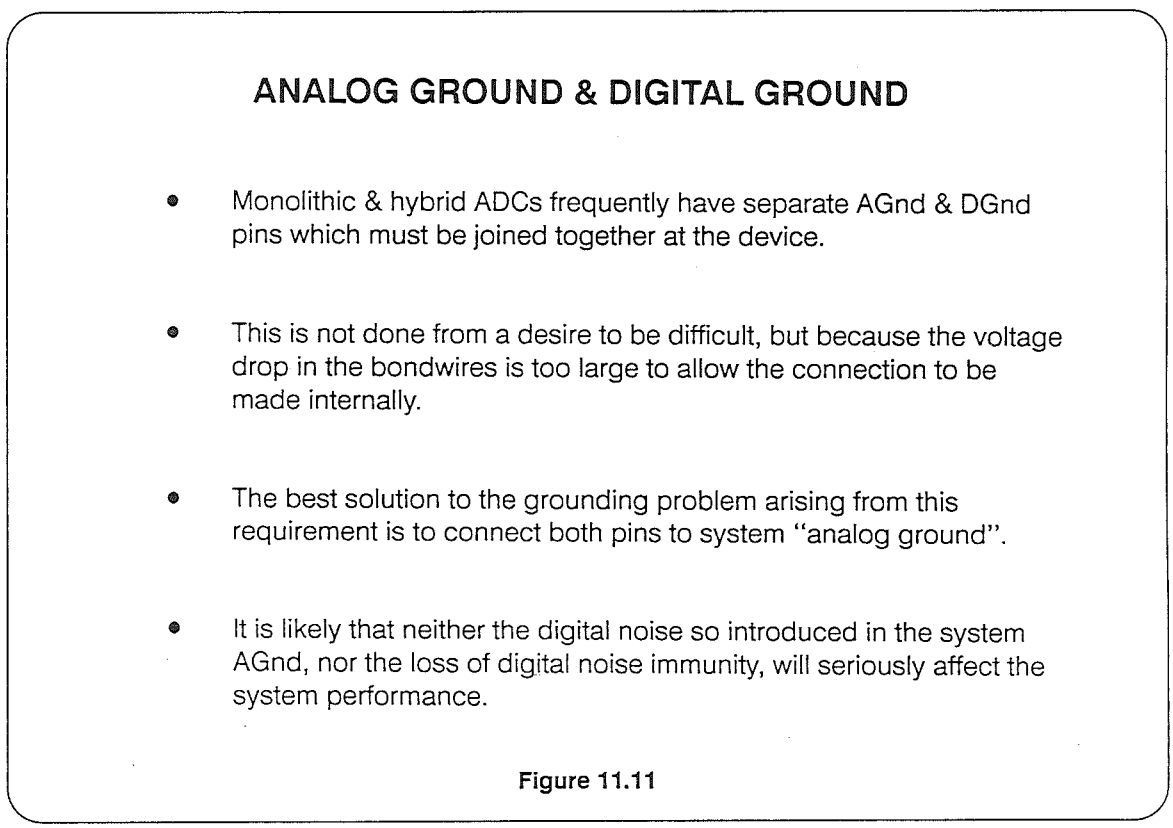


Figure 11.11

In most cases the correct way to connect such an ADC is to join AGnd and DGnd at the device as instructed, and then join the node to the system AGnd. If the system AGnd has suitably low impedance, the digital currents flowing in it should not seriously affect the ground noise. The degradation of digital noise immunity caused by noise voltages between system AGnd and DGnd is most unlikely to have any effect at all (most logic families have at least hundreds of millivolts of noise immunity - a few have volts).

Related to the star ground system is the use of a ground plane. One side of a double-sided PCB, or one layer of a multi-layer board, is made of continuous metal, which is used as ground. The theory behind this is that the large amount of metal will have low resistance and as low inductance as is possible.

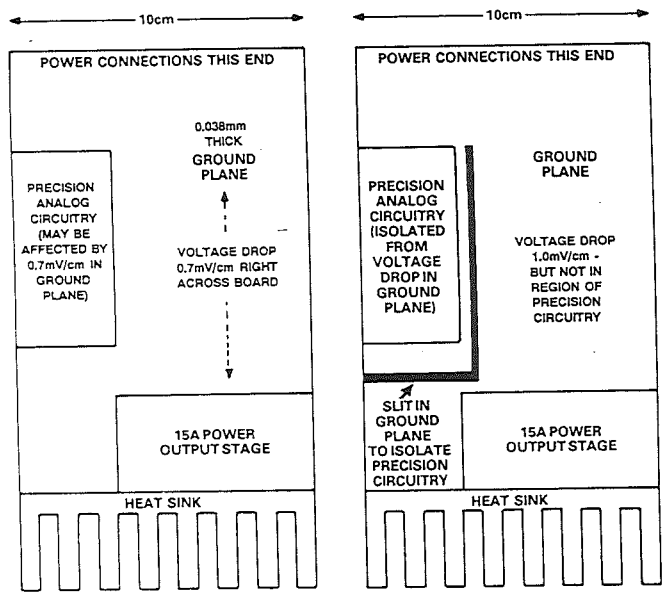
GROUND PLANES

- One entire side or layer of a PCB is continuous grounded conductor.
- This gives minimum ground resistance and inductance but is not always sufficient to solve all grounding problems.
- Breaks in ground planes can improve or degrade circuit performance - there is no general rule.
- Twenty years ago ground planes were difficult to fabricate. Today they are not.
- If your PCB facility objects to fabricating ground planes - GET A NEW PCB FACILITY!

Figure 11.12

It is sometimes argued that ground planes should not be used because they are liable to introduce problems in manufacture and assembly. Such an argument may have had limited validity twenty years ago when PCB physics were less understood, wave-soldering less reliable, and solder resist techniques less well understood, but today it should not be tolerated.

Ground planes solve many ground impedance problems, but not all. Even a continuous sheet of copper foil has residual resistance and inductance, and in some circumstances they can be enough to prevent proper circuit function. Figure 11.13 shows such a problem - and a possible solution.



A SLIT IN A GROUND PLANE CAN
RECONFIGURE CURRENT FLOW FOR BETTER ACCURACY

Figure 11.13

Consider a ground-plane PCB 100 mm wide with a ground connection at one end and a power amplifier at the other drawing 15A. If the ground plane is 0.038 mm thick and 15A flows in it, there will be a voltage drop of 68 μV/mm. This voltage drop would cause quite serious problems to any ground-referenced precision circuitry sharing the PCB. However, if we slit the ground plane so that high current does not flow in the region of the precision circuitry, we can probably solve the problem - even though the voltage gradient will increase in those parts of the ground plane where the current does flow.

A break in a ground plane is not always a good thing. We earlier considered the benefits of outward and return signal paths being close together so that inductance is minimized. When an HF signal flows in a PC track running over a ground plane, the arrangement functions as a microstrip transmission line, and the majority of the return current flows in the ground plane underneath the line. Suppose that there is a break in the ground plane (in Figure 11.14 the break is to allow another conductor to cross the first): the return current must flow around the break and both the inductance, and the vulnerability of the circuit to external fields are increased.

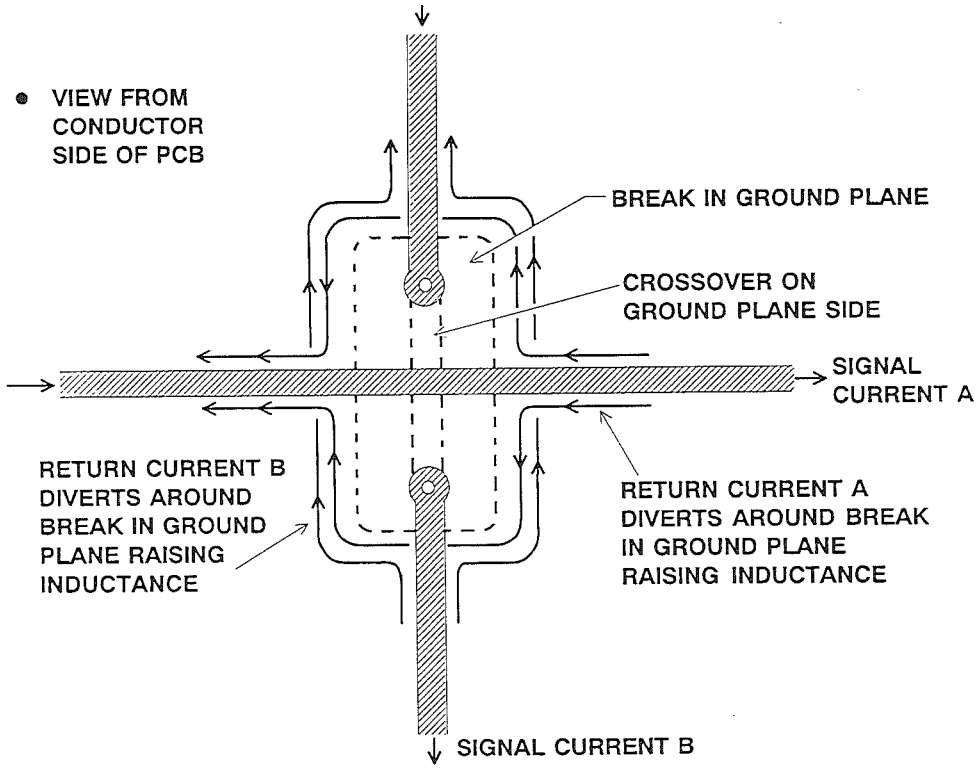

• VIEW FROM CONDUCTOR SIDE OF PCB
BREAK IN GROUND PLANE
CROSSOVER ON GROUND PLANE SIDE
SIGNAL CURRENT A
RETURN CURRENT B DIVERTS AROUND BREAK IN GROUND PLANE RAISING INDUCTANCE
RETURN CURRENT A DIVERTS AROUND BREAK IN GROUND PLANE RAISING INDUCTANCE
SIGNAL CURRENT B
• RETURN CURRENTS A AND B MAY INTERACT
BREAKS IN GROUND PLANE RAISE INDUCTANCE

Figure 11.14

It would be far better if the second signal were carried across both the first signal and the ground plane by means of a piece of wire. The ground plane then acts as a Faraday shield between the two signal conductors, and the two ground return currents, flowing in opposite sides of the ground plane as a result of skin effects, do not interact.

With a multilayer board both the cross-over and the continuous ground plane can be accomodated without the need for a wire link. Multilayer PCBs are expensive and harder to troubleshoot than simple double-sided boards but do offer even better shielding and signal routing. The principles involved remain unchanged, but the range of layout options is increased.

Use of double-sided or multilayer board with at least one continuous ground plane is undoubtedly one of the most successful approaches to the design of high performance, high frequency analog and converter PC cards.

NOISE

We have discussed elsewhere the problems of noise intrinsic to electronic circuitry: Johnson noise, Schottky noise, 1/f noise, etc. In this section we shall consider noise which is the result of external signals finding their way into a system and degrading its performance.

NOISE SOURCES

- Conducted noise
- Capacitively coupled noise
- Inductively coupled noise
- Electromagnetically coupled noise

Figure 11.15

NOISE - Conducted

Rather obviously, conducted noise is noise which enters the circuit on conductors. We have already seen how currents flowing in a ground impedance produce voltages which may corrupt circuit performance. The other common source of conducted noise is power supplies.

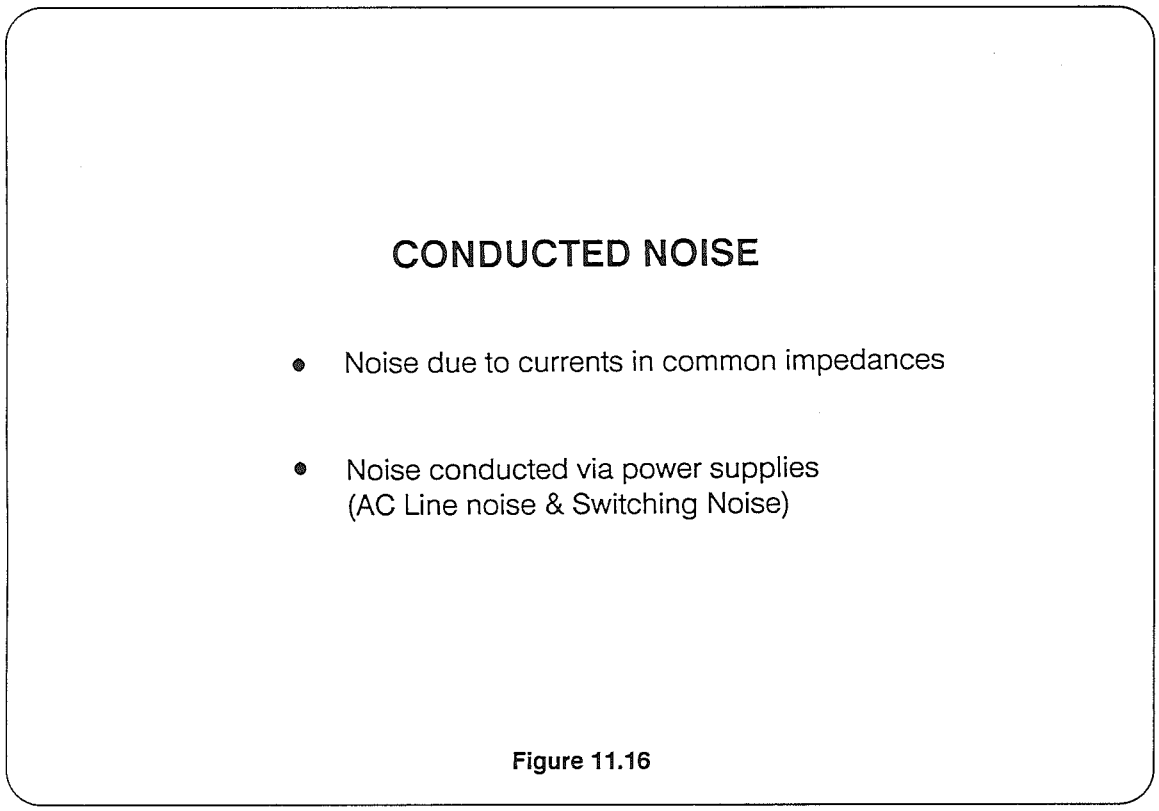


Figure 11.16

When we design an electronic circuit we generally assume that our power supplies are noise-free voltages, of exactly the nominal voltage, with zero source impedance at all frequencies. This is not the case.

We also assume that the published power supply rejection figures (PSRR) for the devices which we use are valid at all frequencies from DC to light. This is not the case either.

POWER SUPPLY NOISE

- Long-term voltage variation
  (Long-term variations in voltage or AC line voltage)
- AC Line noise
  (Both 100/120 Hz ripple on rectifier output and transient noise on the AC line which passes to the DC output)
- Switching noise
  (Digital noise from switching- mode power supplies)
- Power line noise transfer
  (Unwanted signals which pass from one part of a circuit to another via the common power supply)

Figure 11.17

All power supplies have noisy outputs. This noise may consist of long-term voltage drift, line ripple at 100 or 120 Hz, or high frequency spikes from switching regulators. All power supplies also have finite output impedance, so that if a circuit draws a varying current, the supply voltage will vary with the current. If two circuits are supplied from a common supply, this provides a mechanism whereby one circuit may affect the other. Once we appreciate all these effects, we can attempt to quantify them, and take steps to minimize their adverse effects on our systems.

Long-term supply voltage changes, whether due to battery voltage drop during life, or line voltage variations, are rarely a problem. Where such variations might cause difficulties, the system will incorporate a supply voltage regulator to keep variations within acceptable limits. Similarly, ripple at twice the AC line frequency, and any spikes or HF noise which may enter the system via the AC supply, should not cause degradation of performance in a well-designed system. If the decoupling capacitors in the rectifier do not adequately minimize the effect, the series regulator almost certainly will. It is, however, always worthwhile to have a surge eliminator on the AC line input to any system. While such a circuit is unlikely to be needed in preventing normal line noise from currupting system performance, it is essential to prevent occasional large surges (from lightning or

similar causes) from causing actual damage to the power supply or the system that it is powering.

The commonest type of power supply noise is switching noise. Switching power supplies are small, cheap, efficient and, in too many cases, extremely noisy! Not only do they generate conducted noise, they are also efficient producers of capacitively coupled noise, magnetically coupled noise, and electromagnetically coupled noise. The *best* possible advice is to not use them.

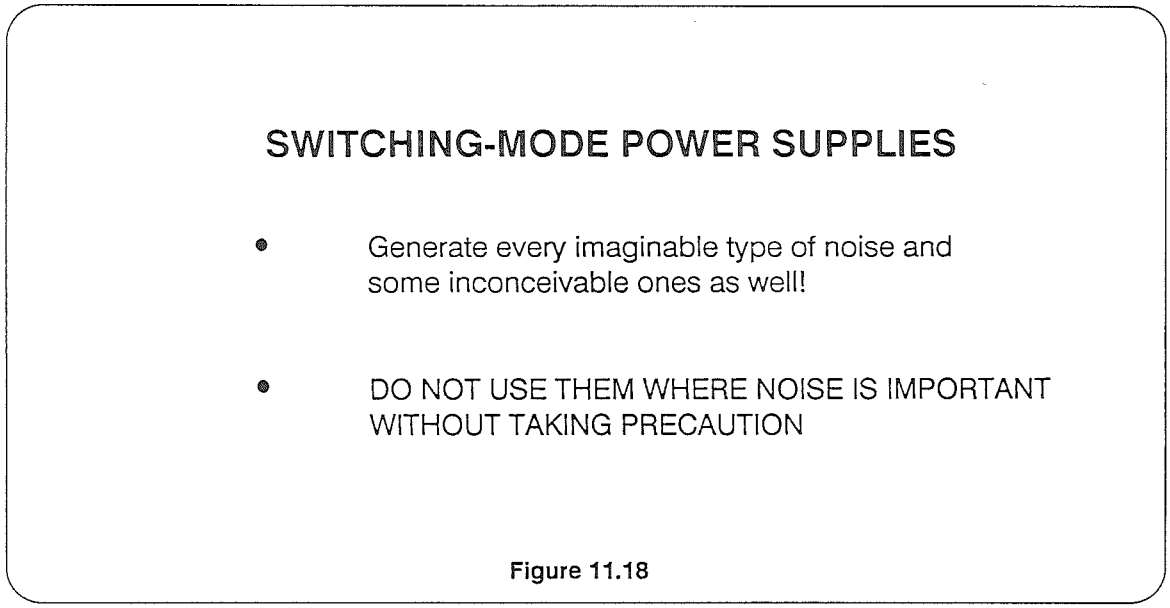


Figure 11.18

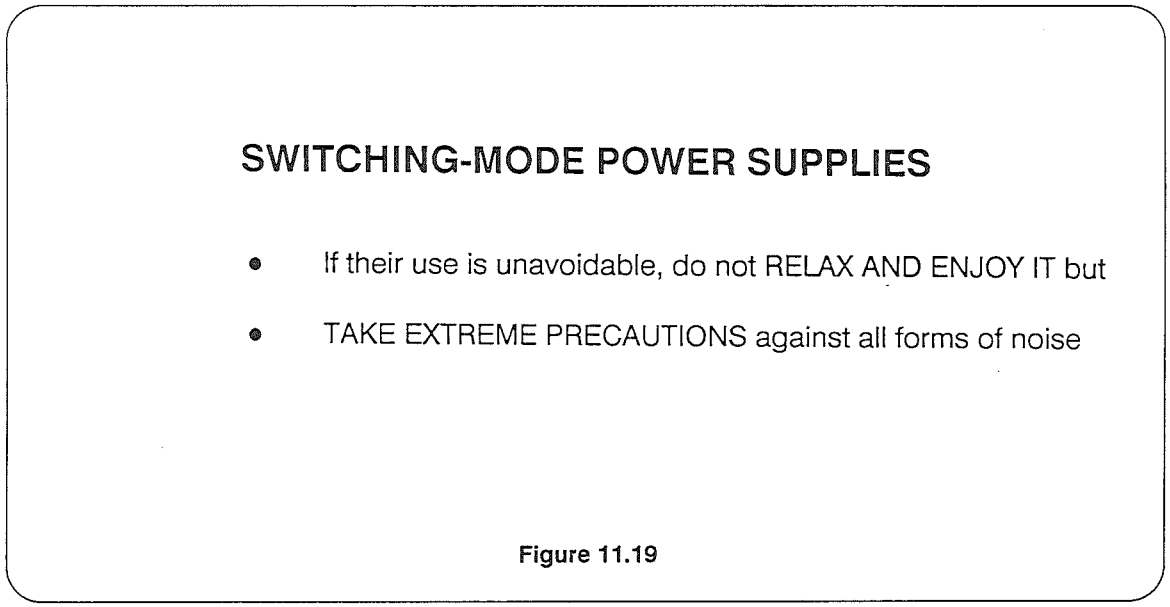
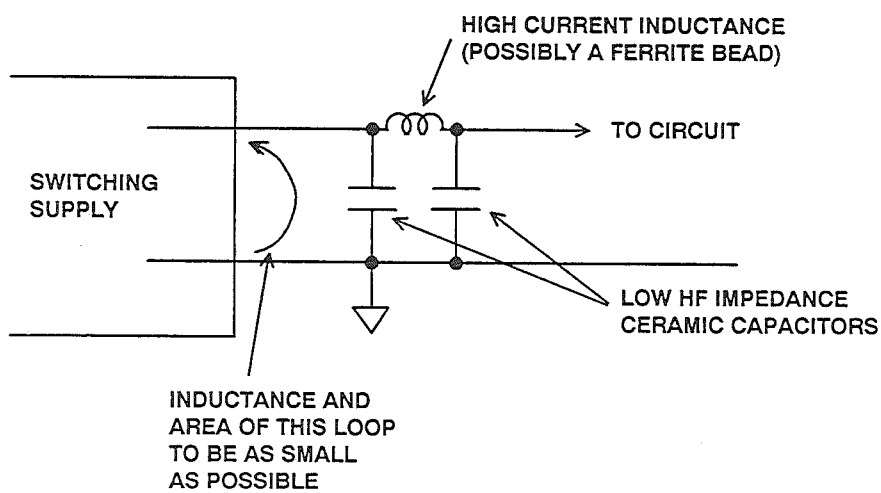


Figure 11.19

It is, unfortunately, not always possible to avoid the use of switching power supplies. Where they must be used, they must be treated with the gravest suspicion, and all possible precautions should be taken to prevent their noise from corrupting the analog circuits that they power. Their input and output lines should be decoupled at all frequencies, they should be shielded to prevent external electric and magnetic fields from causing interference, and they should be sited as far as possible from sensitive circuits so that residual electric and magnetic fields are prevented by distance from causing serious damage.

Where switching supplies are used, it is always worthwhile to remove them temporarily and supply the system with batteries or a low noise bench supply in order to determine if the system performance is being compromised by the switching supply. It often is.

The noise transients on the output lines of switching supplies consist of voltage spikes of very short duration. Large capacitors, such as electrolytic or plastic film types, have considerable inductance and too high an impedance at HF to decouple such spikes satisfactorily. The best output filter for a switching supply will have high value capacitors to remove the low frequency noise which will also be present. In addition, a pi filter using ceramic capacitors, with short leads, having low impedance at HF plus a series inductor (which may be a ferrite bead on the output line) can provide inductive blocking of the spikes. It is possible to buy such a pi filter as a single bulkhead mounted feedthrough component.

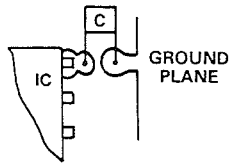


PI - FILTER ON SWITCHING SUPPLY OUTPUT
(SOMETIMES AVAILABLE AS A SINGLE CERAMIC COMPONENT)

Figure 11.20

Power lines in electronic circuitry have decoupling capacitors for two reasons: to remove ripple and noise originating in the power supply, and to remove ripple and noise resulting from modulation of the supply current by the circuitry it feeds. We have discussed the former, but the latter needs more consideration.

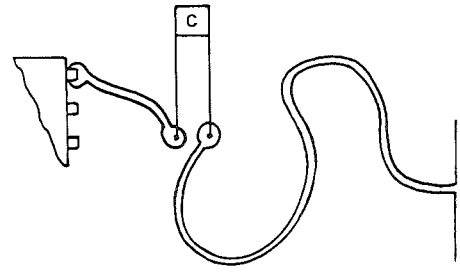
Even low frequency integrated circuits contain transistors having f_t of hundreds of MHz. If the power supply to a circuit behaves as a resonant circuit at a few hundred MHz, it may be possible for the circuit to oscillate. Such oscillation will seriously degrade the performance of the circuit and yet will be too high in frequency to be detected by a standard oscilloscope (indeed, the capacity of the oscilloscope probe may be enough to stop the oscillation). To prevent such parasitic oscillation, and also to restrict high frequency supply currents to the region of the device, all integrated circuit supply pins should be decoupled with a capacitor having low HF reactance and short leads, placed very close to the device (if there are two pins for one supply, both should be decoupled). Ideally, surface-mount capacitors should be used for this purpose, because of their very low inductance, but in most cases monolithic ceramic capacitors with lead lengths of under 2 mm will be satisfactory. Where very low impedance decoupling may be needed, two or more capacitors in parallel should be used.



IDEAL HF DECOUPLING HAS

1. LOW INDUCTANCE CAPACITOR (MONOLITHIC CERAMIC)
2. MOUNTED VERY CLOSE TO THE IC
3. WITH SHORT LEADS
4. AND SHORT, WIDE PC TRACKS

IT MAY BE SHUNTED WITH A TANTALUM BEAD ELECTROLYTIC TO PROVIDE GOOD LF DECOUPLING AS WELL.

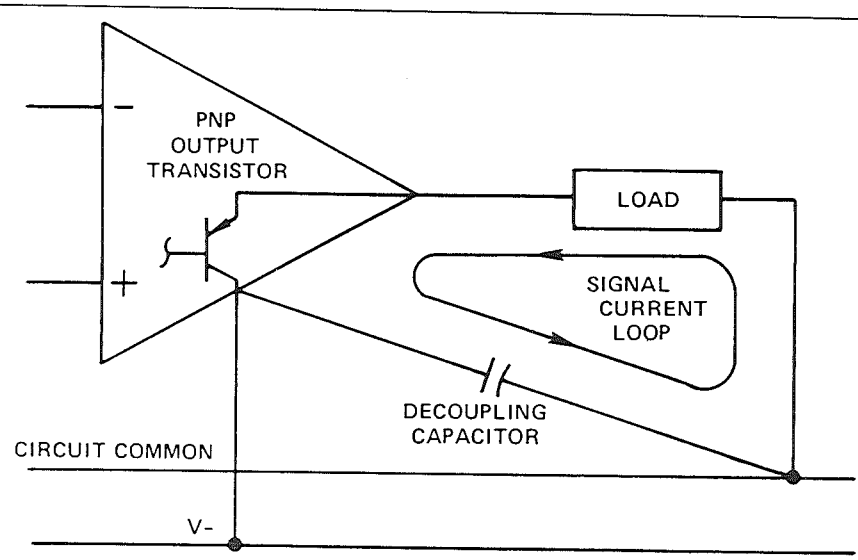


THIS SORT OF THING IS USELESS!

HIGH FREQUENCY DECOUPING
(REQUIRED EVEN BY LF ANALOG CIRCUITS)

Figure 11.21

If the integrated circuit so decoupled is driving a load at HF, Kirchoff's Law tells us that there should be a low impedance between the ground connection to the load and the ground connection of the decoupling capacitor. This topic is more fully covered in an Application Note.[3]

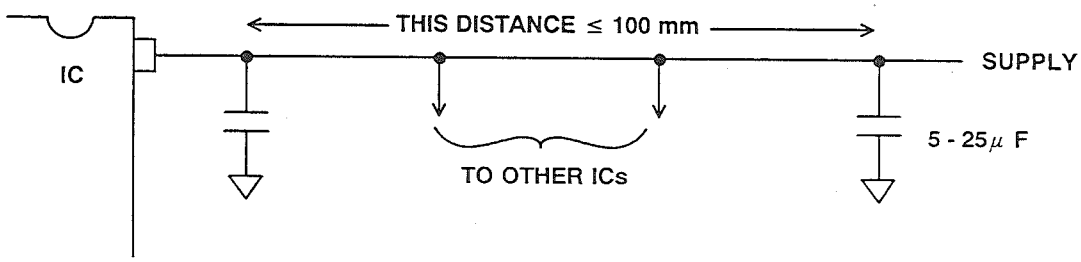


DECOUPLING OF NEGATIVE SUPPLY FOR A GROUNDED LOAD

Figure 11.22

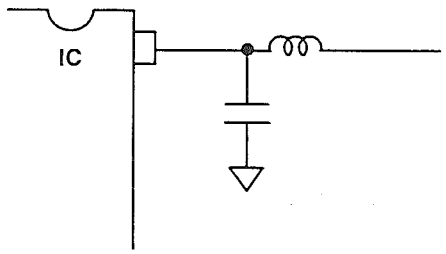
In addition to HF decoupling at every device, it is good practice in high precision circuits to have LF decoupling capacitors of 5-25 μF on all supplies where LF noise could be a problem (in effect this generally means analog circuit supplies, but not necessarily logic supplies). A good rule of thumb is that no IC should be more than 100 mm of circuit track away from such a capacitor, but circumstances will change this. Power supply tracks should be as wide as possible, not just to prevent them from melting from the currents that they carry but to minimize their impedance.

Sometimes low impedance supply lines can be a disadvantage. We have pointed out that any conductor has inductance. The inductance of a power line, combined with a decoupling capacitor, can form an LC resonant circuit which may ring at its resonant frequency when excited by transient currents. In some cases a small series resistance in the power line can be useful in lowering the Q of such a resonant circuit and preventing such effects.



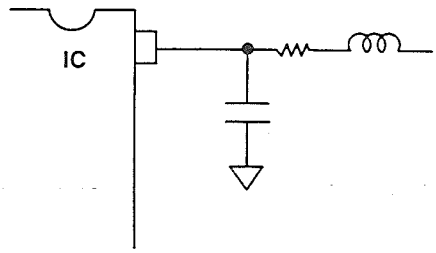
ON-BOARD LF DECOUPLING

Figure 11.23



EQUIVALENT CIRCUIT
OF DECOUPLED POWER
LINE - RESONANT AT

$$f = \frac{1}{2\pi\sqrt{LC}}$$



SMALL SERIES RESISTANCE
CLOSE TO THE IC REDUCES THE Q

RESONANT CIRCUITS FORMED BY DECOUPLED POWER LINES

Figure 11.24

Even with ample decoupling, noise from one part of a circuit can sometimes interfere with another part by coupling through the power supplies. Where such a problem occurs, it is often best to have separate power supplies. In many cases a separate series regulator will be an effective solution, but sometimes a separate transformer winding and rectifier is necessary. The latter expedient offers the further advantage that it may often be connected so as to remove common ground coupling problems as well.

SEPARATE POWER SUPPLIES

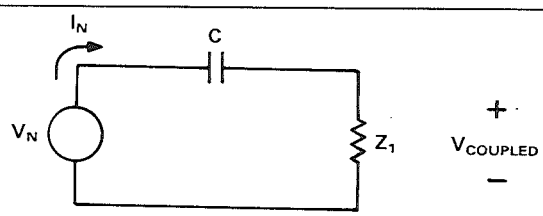
- Separate power supplies help minimize coupling of signals from one part of a system to another.
- Often separate series regulators will provide adequate isolation at low cost.
- In extreme cases completely separate transformer windings, rectifiers and regulators may be necessary to isolate both "supply" and "ground" lines.
- Where supply coupling of noise is suspected replace the supply to one part of the circuit with a battery - and see if the problem is resolved.

Figure 11.25

NOISE - Capacitive coupling

There is a capacitance between any two conductors separated by a dielectric (air or vacuum is a dielectric). If there is a change of voltage on one there will be a movement of charge on the other. The basic model is shown in Figure 11.26.

It is evident that the voltage coupled into Z1 may be reduced by reducing V_n, the frequency involved, the capacitance, or Z1, but frequently none of these can be changed. The best solution is to insert a grounded conductor (known as a Faraday shield) between the noise source and the circuit which it affects.



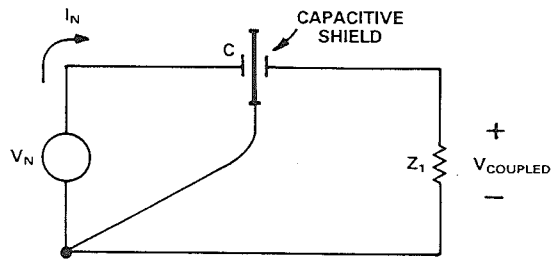
Z_1 = CIRCUIT IMPEDANCE
$Z_2 = 1/j\omega C$

$$V_{COUPLED} = V_N \left(\frac{Z_1}{Z_1 + Z_2} \right)$$

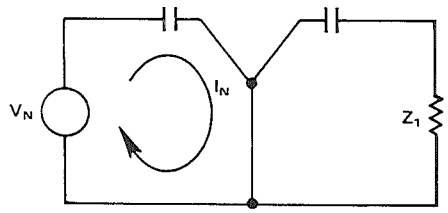
CAPACITIVE COUPLING EQUIVALENT CIRCUIT

Figure 11.26

CAPACITIVE SHIELD INTERRUPTS THE COUPLING ELECTRIC FIELD



EQUIVALENT CIRCUIT ILLUSTRATES HOW A CAPACITIVE SHIELD CAUSES THE NOISE CURRENTS TO RETURN TO THEIR SOURCE WITHOUT FLOWING THROUGH Z_1

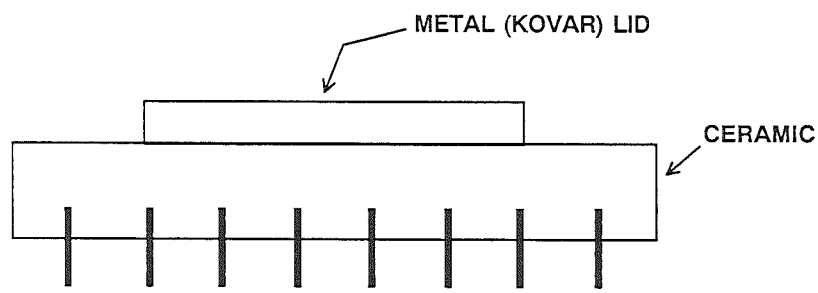


CAPACITIVE SHIELDING

Figure 11.27

The Faraday shield is easily implemented and almost invariably successful. For this reason, capacitively coupled noise is rarely an intractable problem. However, to be effective, the shield must completely block the electric field between the noise source and the shielded circuit and must be connected so that the noise current returns to its source without flowing in any part of the circuit where it might introduce conducted noise. A Faraday shield must never be left unconnected, as this almost always makes capacitively coupled noise worse.

An example of this problem is seen in sidebrazed ceramic IC packages. These D.I.L. packages have a small square conducting kovar lid soldered onto a metallized rim on the ceramic package top. Package manufacturers offer only two options: the metallized rim may be connected to one of the corner pins of the package or it may be left unconnected. Most logic circuits have a ground pin at one of the package corners, and therefore the lid is grounded. Many analog circuits do not have a ground pin at a package corner and the lid is left floating. Such circuits turn out to be far more vulnerable to electric field noise than the same chip in a plastic D.I.L. package where the chip is completely unshielded.



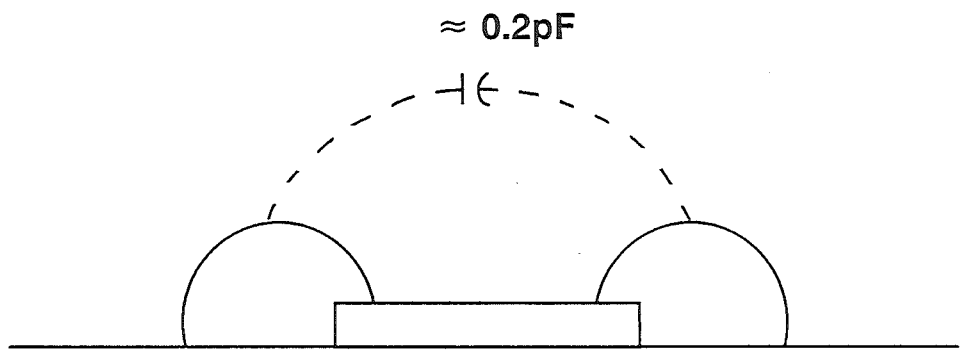
- SIDEBRAZE CERAMIC D.I.L. PACKAGES SOMETIMES HAVE ISOLATED METAL LIDS
- THESE ARE VULNERABLE TO CAPACITIVE INTERFERENCE AND SHOULD BE GROUNDED (IF POSSIBLE)

CAPACITIVE EFFECTS DUE TO METAL LIDS

Figure 11.28

In fact, it is good practice for the user to ground the lid of any sidebrazed ceramic IC where the lid is not grounded by the manufacturer. This can be done with conductive paint from the lid to the ground pin, with a wire soldered to the lid (this will not damage the device if the joint is made reasonably quickly with standard 60:40 solder), or with a phosphor-bronze clip with a tag which is soldered to ground. Never attempt to ground such a lid without verifying that it is, in fact, unconnected, as occasionally device types will be found with the lid connected to a power supply rather than to ground!

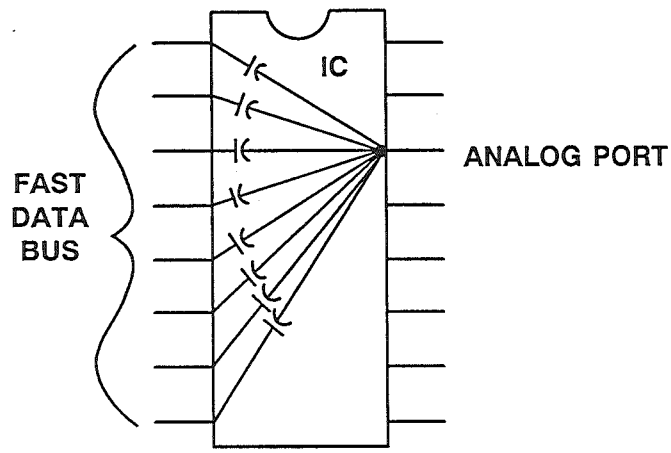
One case where a Faraday shield is impracticable is between the bondwires of an integrated circuit chip. This has important consequences.



STRAY CAPACITY BETWEEN CHIP BONDWIRES

Figure 11.29

The stray capacitance between two chip bondwires is of the order of 0.2 pF. If we have a high resolution converter (ADC or DAC) which is connected to a high speed data bus, then each line of the data bus, which will be carrying noise with 2-5 V/ns dV/dt, is connected to the converter analog port by 0.2 pF. Whenever the bus is active, this will couple intolerable amounts of noise to the analog port and will seriously degrade the performance of the converter.

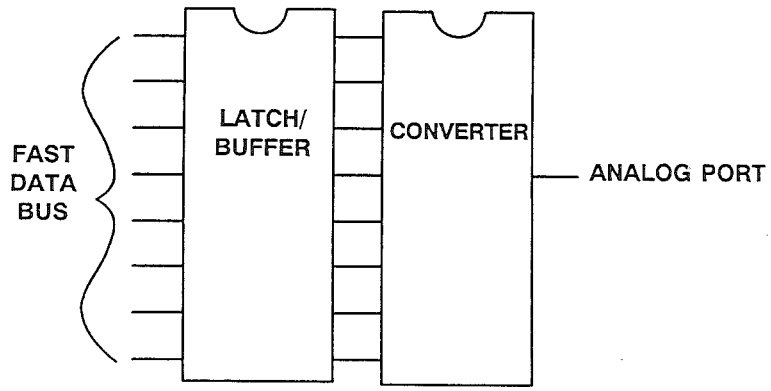


WITH A HIGH PERFORMANCE CONVERTER ON A HIGH SPEED DATA BUS, IT IS NOT POSSIBLE TO SHIELD THE ANALOG PORT FROM THE DIGITAL NOISE

Figure 11.30

Present technology offers no cure for this problem, which also sets serious limits on the performance possible from "mixed signal" ICs having analog and digital circuitry on a single chip. However, it may avoided quite simply by not connecting the databus directly to the converter, but by using a latched buffer as an interface.

This solution costs money, occupies board area, reduces reliability (very slightly), consumes power and complicates design - but it does improve the signal-to-noise ratio of the converter. The designer must decide whether it is worthwhile in individual cases.



- A BUFFER/LATCH CAN ACT AS A FARADAY SHIELD BETWEEN A FAST DATA BUS AND A HIGH PERFORMANCE CONVERTER
- IT ADDS COST, BOARD AREA, POWER CONSUMPTION, RELIABILITY REDUCTION, DESIGN COMPLEXITY AND IMPROVED PERFORMANCE

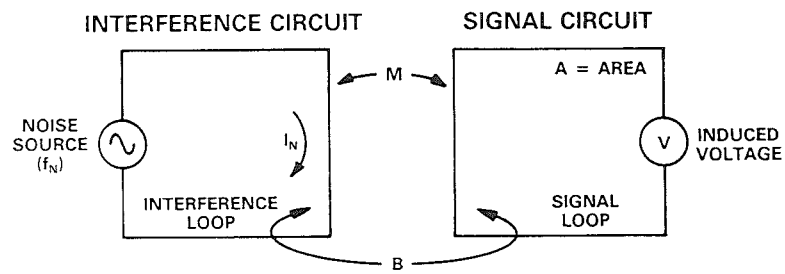
BUFFER LATCH USED AS FARADAY SHIELD

Figure 11.31

NOISE - Inductive Coupling

The mutual inductance of two conductors couples AC signals between them. The basic principle is illustrated in Figure 11.32 and is a common mechanism for the transfer of unwanted signals (noise) between circuits.

As with all other sources of noise, as soon as we define the principle at work, we can see ways of reducing the effect. In this case, reducing any or all of the terms in the equations in Figure 11.32 will reduce the coupling. Reducing the frequency or amplitude of the current causing the interference may be impracticable, but it is frequently possible to reduce the mutual inductance between the interfering and interfered with circuits by reducing loop areas on both sides and, possibly, increasing the distance between them.

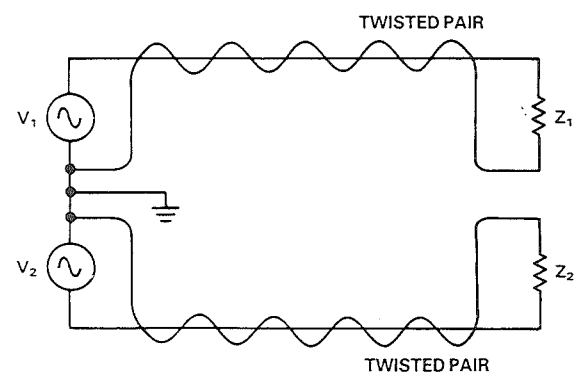


M = MUTUAL INDUCTANCE
B = MAGNETIC FLUX DENSITY
A = AREA OF SIGNAL LOOP
$\omega_N = 2\pi f_N$ = FREQUENCY OF NOISE SOURCE

V = INDUCED VOLTAGE = $\omega_N M I_N = \omega AB$

BASIC PRINCIPLES OF INDUCTIVE COUPLING

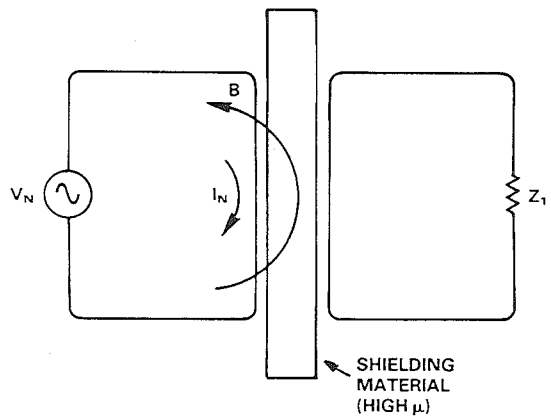
Figure 11.32



PROPER SIGNAL ROUTING REDUCES LOOP AREA

Figure 11.33

Shielding magnetic fields to reduce mutual inductance is sometimes possible ,but is by no means as easy as shielding electric fields with a Faraday shield. HF magnetic fields are blocked by conductive material, while LF and DC fields may be screened by a shield made of mu-metal sheet. Mu-metal is an alloy having very high permiability, but it is expensive, its magnetic properties are damaged by mechanical stress, and it will saturate if exposed to too high fields. Its use, therefore, should be avoided where possible.



- Magnetic shielding is not as easily accomplished as electrostatic shielding, but may be done at HF with a simple conducting screen, and at LF and DC with a screen of high permeability material such as Mu-metal.

MAGNETIC SHIELDING

Figure 11.34

NOISE - Electromagnetic Coupling

Noise can enter a circuit as electromagnetic radiation. Circuits can also generate electromagnetic radiation which can interfere with electronic devices at quite considerable distances away. Recent legisation in both the United States and the European Community sets limits on the amount of interference generated and the vulnerability of circuits to such interference.[4] This legislation, and the techniques needed to comply with it, are the subjects of many seminars and training courses, and an Analog Devices Application Note. It is not proposed to cover the topics in detail in this seminar.[5]

ELECTROMAGNETIC NOISE GENERATION

- Circuits must be designed so that external E/M fields are minimized.
- This is done by shielding, decoupling, minimising the area of HF current loops and designing circuits which generate as little EMI as possible.
- IT'S NOT JUST A GOOD IDEA
- IT'S THE LAW!

Figure 11.35

However, the principles of minimizing external radiation are closely related to the principles of low noise design which we have already discussed: high frequency and high dV/dt signals should be screened with Faraday shields, the area of current loops should be minimized, conductors should be decoupled at HF wherever unnecesary HF signals might otherwise occur, and external wires should be isolated with inductors or ferrite beads.

It is still too common at seminars like this to encounter skepticism about the need to protect circuitry from external electromagnetic fields. Even twenty years ago such skepticism was unjustified but today, when transmitters are ubiquitous, it is folly. Besides the more obvious broadcast, emergency and mobile radio services there are cellular and cordless telephones, radar, garage door openers and other remote controls, telemetry, and amateur and CB radio. For any designer to imagine that his circuit will never encounter a radio transmitter during its lifetime is folly on a grand scale.

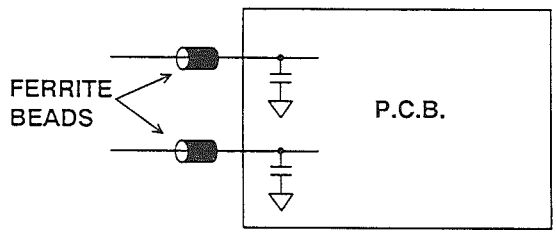
This is particularly so because the design of circuits which are immune to electromagnetic radiation of reasonable levels is not particularly difficult. If every conductor which leaves a PCB is decoupled with a ceramic capacitor and a ferrite bead, it is probable that no further precaution is necessary.

ELECTROMAGNETIC NOISE INTERFERENCE

- The World is full of radio transmitters.
- Police, taxis, broadcast, amateur, CB, cellular and cordless telephones, telemetry and garage door openers.
- Do not imagine that your circuit will never encounter one.

Figure 11.36

A few ports may be more vulnerable and require a pi filter rather than an L filter, and, of course, ports where an HF signal must actually enter or leave the board must be filtered to suppress other EMI but allow the signal to pass unaffected.



IN MANY CASES, ALL THAT IS REQUIRED
IS AN L FILTER, CONSISTING OF A FERRITE BEAD
AND A CAPACITOR, ON EACH EXTERNAL
CONNECTION TO THE BOARD

EMI PREVENTION

Figure 11.37

NOISE - Overall Layout

We have considered sources of noise in circuit design. Having assessed some of the causes of noise and how to minimize them individually, it is worthwhile to consider noise reduction on a complete PCB.

It is evident that we can minimize noise by paying attention to the layout of the whole board and preventing diferent signals from interfering with each other.

High level analog signals should be separated from low level analog signals, and both should be kept away from digital signals. We have seen elsewhere that in waveform sampling and reconstruction systems, the sampling clock (which is a digital signal) is as vulnerable to noise as any analog signal, but is as liable to cause noise as any digital signal, and so must be kept isolated from both analog and digital systems.

HIGH SPEED PC BOARD SIGNAL ROUTING

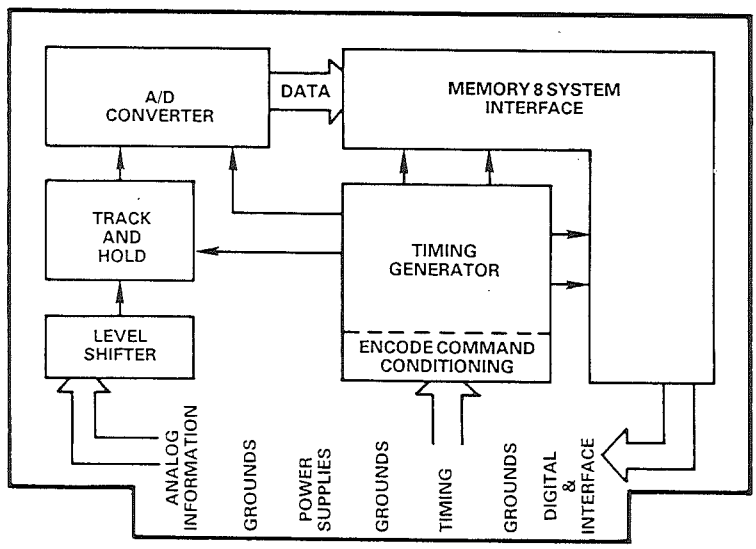
- Physically Separate Analog and Digital Signals
- Avoid Crossovers Between Analog and Digital Signals
- Be Careful with Sampling Clock and A/D Converter Analog Input Runs
- Be Careful with High Impedance Points
- Use Lots of Ground Plane
- Use Microstrip Techniques for Controlled Impedances

Figure 11.38

If a ground plane is used (and it should be in almost all cases) it can be used as a shield where sensitive signals cross. Figure 11.39 shows a good layout for a data acquisition system where all sensitive areas are isolated from each other, and signal paths are kept as short as possible. While real life is frequently not as tidy as this, the principle still applies.

There are several important considerations to the connectors at the edge of the board. First of all, this is the one place in the system where all signal conductors run parallel. It is therefore a good idea to separate them with ground pins to reduce coupling.

Multiple ground pins are important for another reason: to keep down the ground impedance at the junction between the board and the backplane. The contact resistance of a single pin of a PCB connector is quite low (of the order of 10



PCB "FLOW CHART" LAYOUT

Figure 11.39

EDGE CONNECTIONS

- Separate sensitive signals by ground pins
- Keep down ground impedance with multiple (20-30% of total) ground pins
- Have several pins for each power line
- Critical signals may require a separate connector (possibly co-ax)

Figure 11.40

mOhms) when the board is new. As the board gets older, the contact resistance is likely to rise, and the board's performance may be compromised. It is therefore well worthwhile to afford extra PCB connector pins so that there are many ground connections (perhaps 20-30% of all the pins on the PCB connector should be ground pins). For similar reasons there should be several pins for each power connection, although there is no need to have as many as there are ground pins.

NOISE - Multiple Card Systems

In systems where there are several PCBs, noise may be more of a problem. At first sight it would appear that the problem is similar to that of a single PCB where particular subsystems must be positioned so that harmful interactions are minimized. In a multicard system individual PCBs must be interconnected so that harmful interactions are minimized. There are three problems with this. First of all, there is far less opportunity for rearranging the physical layout of a system consisting of a few cards connected to a common backplane. Secondly, many multicard systems are designed to be reconfigured in a "mix 'n' match" arrangement to allow large numbers of system options. It can be impossible to predict what systems are going to be required and to ensure that all of them are noise free. Finally, multicard systems are likely to have higher ground currents than those occuring on single, relatively simple, PCBs. These currents must flow in the higher impedances which are associated with the intercard connectors, even when multiple ground pins are used.

The basic principles still apply: ground impedance must be as low as possible, high level and low level signals must be separated so that they do not interfere with each other, and capacitance and mutual inductance coupling must be avoided. Nevertheless, it must be accepted that situations can arise where it is not possible to transfer a high speed, high accuracy signal from one PCB to another without unacceptable signal degradation.

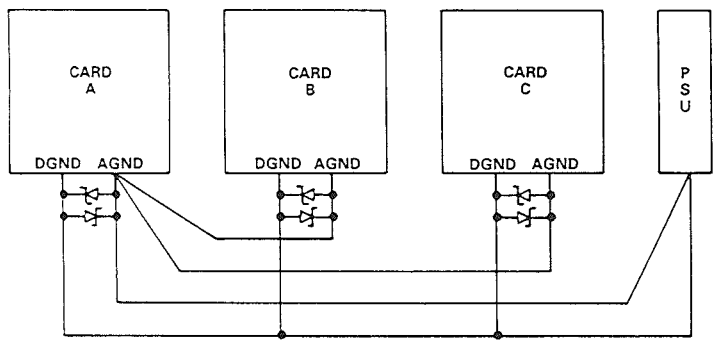
MULTIPLE CARD SYSTEMS

- Multiple card systems are likely to have higher ground currents and higher ground impedances than are found on a single PCB.
- It is therefore more difficult to transfer ground-referenced signals accurately between cards than across a PCB.
- In some cases it will be IMPOSSIBLE to transfer ground-referenced signals between PCBs without unacceptable loss of quality.

Figure 11.41

The best way of minimizing ground impedance in a multicard system is to use another PCB as a backplane and have a ground plane (or even two - one analog, one digital) on that mother card. If the earlier advice about multiple ground pins has been observed, this arangement is capable of excellent performance. Where there are several card cages (racks for PCBs) the ground planes of the several mother boards must be tied together and, probably, to the metal chassis holding the card cages. The exact layout of the inter-connections will depend on the overall system architecture.

If a mother board with a ground plane is not possible, then the ground pins of the PCB sockets must be wired together, with due attention to probable current flows and common ground impedances, with heavy, multi-strand wire, having as low resistance as possible. In many cases the resulting ground screen will be tied to chassis ground at a number of points, but it will sometimes be better to join them at a single star point.

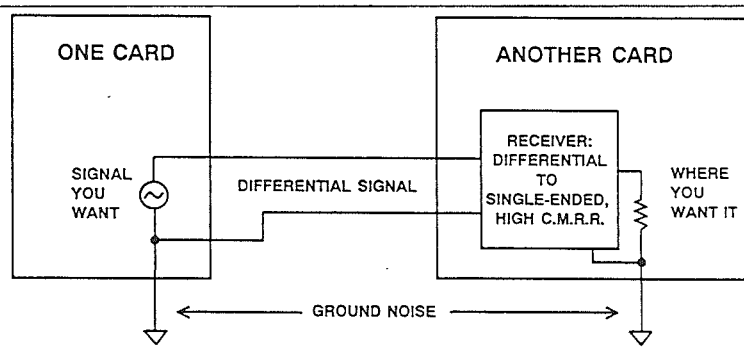


- Schottky diodes protect cards in the event of loss of analog ground
- This grounding system may be inadequate at high resolution or where large ground currents flow
- This MAY permit accurate intercard transmission of ground referenced signals

STAR ANALOG GROUND IN A MULTICARD SYSTEM

Figure 11.42

Modern high performance analog systems handle signals with resolutions of 8 bits at sampling rates of over 500 MHz and resolutions of 14 bits sampled at more than 10 MHz. Preserving signal integrity between cards is extremely difficult and may be impossible.



- At DC and LF the receiver will be an instrumentation amplifier
- At HF the receiver will be a transformer
- There is no ideal receiver for video signals which have components from DC to HF

DIFFERENTIAL TRANSMISSION MINIMIZES GROUND ERRORS

Figure 11.43

The use of balanced transmission lines can help, but if the signal bandwidth extends to DC, there will be a need for a very high performance instrumentation amplifier at the receiving end to restore a ground referenced signal.

The best solution to problems of this sort, and in many cases the only solution, is to partition the system so that the highest quality signals are not required to be transferred to another board.

VIDEO SIGNAL TRANSMISSION

- It is often IMPOSSIBLE to transmit very broadband high accuracy signals between the PCBs of a multicard system without unacceptable loss of quality.
- In such cases the system must be reconfigured to allow all the analog processing to take place on a single PCB.
- It may be inconvenient, but it's the only way you'll get it to work!

Figure 11.44

NOISE - Logic Types

It is well-known that TTL is noisy. This is partly because the "totem pole" output stage structure acts as a short-circuit on the supply for a nanosecond or so during switching. This gives rise to a large current spike, partly because the current flowing in the input changes, and changes quickly, between logic 0 and logic 1, and partly because the output swing, which takes place in a few nanoseconds, is several volts.

High speed CMOS does not have the change in input current (although there is a capacitance charging current pulse during switching, this is smaller) but may draw a supply current pulse during switching, and certainly has a large output swing with a large dV/dt.

ECL, on the other hand, draws almost constant current during switching (unless it is driving asymmetrical loads) and has much smaller output voltage swings. Thus, although ECL is faster than TTL and CMOS, it tends to generate less noise.[6]

In high speed systems where noise is important, therefore, ECL should be used rather than TTL or CMOS where this is possible.

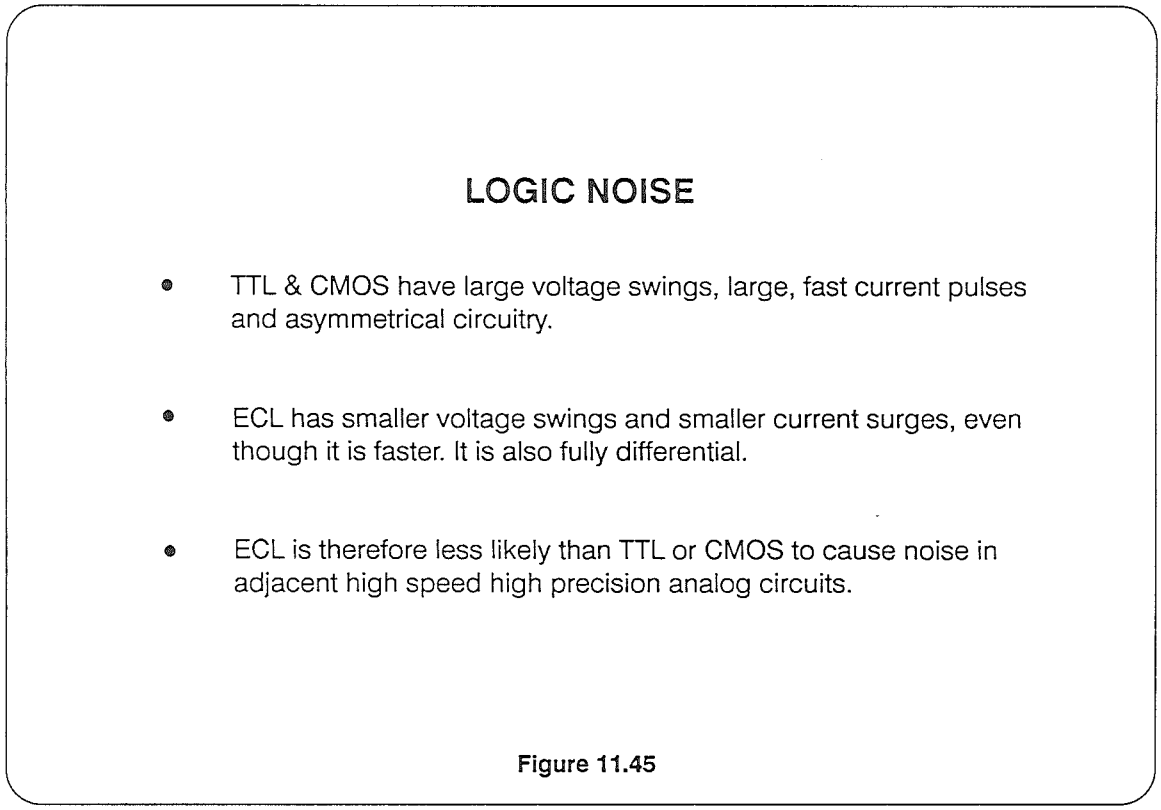


Figure 11.45

CONSTRUCTION - IC Sockets

It is tempting to mount expensive high speed components in sockets rather than soldering them in circuit - especially during circuit development.

Sockets add resistance, inductance and capacitance to the circuit and may degrade performance to unacceptable levels. When this occurs, though, it is always the IC manufacturer who is blamed - not the use of a socket. Even low profile, low insertion force sockets cannot be relied upon not to degrade the performance of high speed devices (and as the socket ages, and the board suffers vibration, the contact resistance of low insertion force sockets is very likely to rise).

With skillful use of a "solder sucker" or solder absorbtion wick, it is generally possible to remove and replace a D.I.L. package on a board several times without damage to the device and only minimal damage to the board (it is helpful to use copper loaded "Savebit" solder to do this to prevent the copper PC pads from being dissolved by the repeated soldering operations). If this is completely unacceptable, then individual pin sockets (sometimes called "cage jacks") may be used to make up a multi-pin socket in the PCB itself.

This approach still adds some resistance, inductance and capacitance to the circuit - but less than would be added by any multi-pin socket. Once the circuit is working, and it is obvious that the IC will not need to be removed, it may be soldered into the pin sockets to reduce resistance and the risk of increased resistance with age.

USE OF IC SOCKETS

- Don't!
- Use Individual "Pin Sockets" or "Cage Jacks" for Each Component Pin Such as AMP Part No. 5-330808-3 (Capped) and 5-330808-6 (Uncapped)

Figure 11.46

PROTOTYPING HIGH SPEED CIRCUITS

As we have seen, the circuit board layout is part of the circuit design of all high speed and high precision analog circuits. The primitive prototyping techniques derived from the "node" theory are quite unsuitable for circuits of this type: vector board and wire wrap prototyping will tell the engineer nothing about the behavior of a properly laid out version of the circuit.

The best technique for prototyping is to use a prototype of the final PCB. Certainly no design is complete until the final PCB layout has been proved to give the required performance. Nevertheless this approach may be a little limiting where a number of different possibilities are to be evaluated.

HIGH-SPEED PROTOTYPING

- Do not use vector board or wire-wrap.
- Do not use IC sockets (use pin sockets if you must).
- Use a prototype of your final PCB if you can. (Go to CAD layout as early as possible.)
- Use manufacturers' evaluation boards if possible.
- Pay as much attention to signal routing, component placing and supply decoupling on the prototype as on the final board.
- For "freehand" prototyping use a double-sided copper-clad board, mount components to it by their ground pins and wire the remaining connections point-to-point (use Wainwright Instruments' Minimount/Solder Mount adhesive PC pads if aerial point-to-point wiring seems too fraught with peril).

Figure 11.47

In this case, components should be mounted on a board having double-sided continuous copper ground plane, with ground connections made to the plane and short point to point wiring made above and below it. The overall component placing and signal routing should be as close as possible to the planned final layout. In fact, it is a good idea to wire point-to-point in a manner similar to how the traces on the PC board will ultimately be arranged (e.g., no more crossovers than allowed by the number of layers). That is, treat the prototyping phase almost as a PC layout phase.

As we have already indicated, IC sockets can destroy the performance of analog ICs, even in prototype equipments. Again, directly soldered components are best,

pin sockets mounted in the ground plane board may be acceptable (clear the copper, on both sides of the board, for about 0.5 mm around each ungrounded pin socket - solder the grounded ones to ground on both sides of the board). Allowing wiring to float in the air can be a little tricky. There is a breadboarding system which is conceptually very similar to that described above but which provides adhesive PC pads which stick to the ground plane and allow more rigid component mounting and wiring. This system is manufactured by Wainwright Instruments and is known as "Minimount" in Europe and "Solder Mounts" in the USA. The manufacturer's and distributer's addresses are given in the references at the end of this section.[7]

Manufacturer's evaluation boards are also useful in system prototyping since they have already been optimized for best performance. In fact, PCB layouts of many high speed evaluation boards are available from Analog Devices in the form of artwork which the users may incorporate into their own PCBs.

When the prototype layout is transferred to a CAD system for PCB layout, it is important to disable, or at any rate override where necessary, any automatic routing or component placing software. The criteria used by such software are more closely related to "node" theory and aesthetically pleasing rows of components (which, admittedly, are also easier on automatic component placing machinery) than to optimizing stray inductance and capacitance and minimizing common ground impedances.

HIGH SPEED PROBING TECHNIQUES

A problem often encountered in dealing with high speed circuits is the proper selection and use of high speed oscilloscopes and especially of their associated probes.[8]

In microwave systems, most impedance levels are 50 ohms and signals are transmitted over high quality transmission lines (stripline or co-ax) directly to the 50 ohm input of the oscilloscope. No probes are necessary, and the oscilloscope bandwidth is chosen to be two or three times greater than the maximum signal of interest. Bandwidth (BW) can be calculated from rise time using the approximations:

$$BW = \frac{0.35}{t_R}$$

$t_R = 2.2\ \tau$ where
t_R = Rise time (10% to 90%)
τ = Time constant
(= RC for a single-pole network)

In high speed analog circuits, however, not all high speed signals are necessarily

at 50 ohm levels, and it is often desirable to use a probe with higher impedance to minimize loading effects. If the probe bandwidth is BW_p and the oscilloscope bandwidth is BW_s, then then the approximate overall bandwidth of the measuring system is given by

$$BW_M = \left[\frac{1}{\left(\frac{1}{BW_P}\right)^2 + \left(\frac{1}{BW_S}\right)^2}\right]^{\frac{1}{2}}.$$

For instance, a 400 MHz oscilloscope (Tektronix 2465B) combined with a 400 MHz probe (Tektronix P6137) will yield an overall measurement bandwidth of approximately 280 MHz. The corresponding measurement rise time is 1.2 ns.

In addition to bandwidth, the probe input impedance (both real and imaginary parts) must be considered. There are four basic types of probes: low impedance passive probes, high impedance passive probes, active FET probes and sampling probes.

HIGH SPEED PROBE CONSIDERATIONS

- Grounding - Probe Tip Shield tc PC Board Connection < 1 Inch!
- Bandwidth of Measuring System, BW_M:

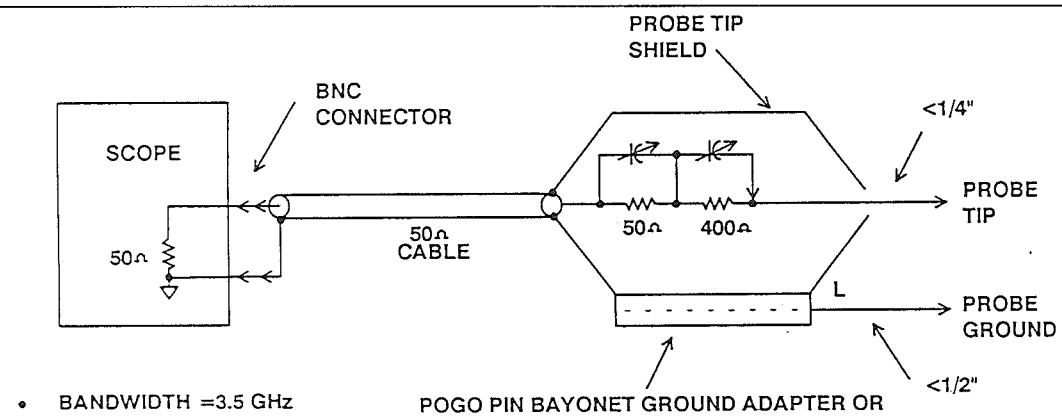
$$BW_M = \left[\frac{1}{\left(\frac{1}{BW_p}\right)^2 + \left(\frac{1}{BW_s}\right)^2}\right]^{\frac{1}{2}}.$$

BW_p = Probe Bandwidth
BW_s = Scope Bandwidth

- $BW = 0.35/t_R$, t_R = Rise Time (10% to 90%)
  $t_R = 2.2\,\tau$, τ = Time Constant (RC)
- Capacitance (Loading Effects)
- Resistance (Loading Effects)
- Attentuation
- Overdrive Characteristics

Figure 11.48

A low impedance passive probe and its typical characteristics are shown in Figure 11.49. Successful use of such a probe requires that the ground inductance be kept extremely low. This implies that the ground connection to the PCB ground plane be extremely short. This may be accomplished by using a "bayonet" ground probe sleeve equipped with a short sharpened "pogo pin" ground which connects directly to the probe tip shield ground. These fittings may or may not be part of the standard fittings supplied with the probe - if they are not they will generally be available from the probe manufacturer, whose catalogue should be consulted. In many cases special PCB mounted test jacks are available to provide suitable low impedance plug-in connection of the probe to a PCB.



- BANDWIDTH =3.5 GHz
- CAPACITANCE =1 pF
- RESISTANCE =500Ω
- ATTENUATION =10X
- TEKTRONIX P-6156
- MAKE YOUR OWN!

LOW IMPEDANCE PASSIVE PROBE

Figure 11.49

The use of long "alligator clip" probe ground leads is pointless at high frequencies, as they hopelessly corrupt the probe performance. To minimize ringing and other perturbations associated with probe ground inductance, the probe tip shield to system ground length should be kept to about 12 mm or less.

It is possible to construct a 500 ohm passive probe. Mount a PCB mounted oscilloscope probe test jack as close as possible to the point in the circuit to be monitored - the shield of the jack being soldered directly to the PCB ground plane. Connect the point in the circuit to be measured to the center conductor of the test jack with a 450 ohm high quality metal film resistor (ideally the jack should be placed so that the resistor leads are just long enough to solder to and not one tenth of a mm longer). The test jack is

connected to the oscilloscope with 50 ohm coaxial cable.

When using this, or any, low impedance probe it is important to consider the effect of the 500 ohm resistive loading on the circuit being measured.

The characteristics of a typical high impedance passive probe are listed in Figure 11.50. This type of probe is standard equipment with wideband analog oscilloscopes. Despite the higher resistance the 10.8 pF capacitance means that the impedance at HF is still quite low (approximately 40 ohms at 400 MHz), and the same precautions must be taken about probe tip shield grounding.

HIGH IMPEDANCE PASSIVE PROBE CHARACTERISTICS

Bandwidth: 400 MHz

Capacitance: 10.8pF

Resistance: 10MΩ

Attentuation: 10X

Example: Tektronix P6137 (Standard with 2465B Portable Scope)

Figure 11.50

HIGH IMPEDANCE ACTIVE FET PROBE CHARACTERISTICS

Bandwidth: 1 GHz

Capacitance: 3pF

Resistance: 100kΩ

Attenuation: 1X

Example: Tektronix P6201

Limited Dynamic Range (±0.6V)

Figure 11.51

The active FET probe, whose characteristics are shown in Figure 11.51, uses an FET amplifier in the probe itself to improve bandwidth and input impedance.

Although active FET probes have high sensitivity and wide bandwidth, their dynamic range is usually limited, and their overdrive recovery may be very slow. If they are overdriven very much, they may never recover at all - a painful and expensive experience. Because of these difficulties, measurements made with FET probes should be viewed with some suspicion - particularly intermodulation measurements.

Figure 11.52 shows the characteristics of two sampling probes, designed to be used with sampling oscilloscopes. They both allow very accurate measurements to be made of repetitive waveforms (sampling oscilloscopes take time-varying samples of successive cycles of a repetitive waveform to build up a picture of the complete wave shape - they cannot be used with single events).

The Data Precision probe is used with the Data Precision 640 digitizing plug-in, and the comparator of the digitizing ADC is located in the probe tip. This allows a vertical resolution of approximately 1 mV/division to be achieved while observing a 5 V step function - with practically no overshoot. Systems of this type are ideal for measuring the settling time, after large steps, of high accuracy, high speed op-amps and DACs.

HIGH SPEED SAMPLING PROBE CHARACTERISTICS

EXAMPLE 1: TEKTRONIX S3A

- Bandwidth: 1 GHz
- Capacitance: 2pF
- Resistance: 100k Ω
- Sensitivity: 2mV/division

EXAMPLE 2: DATA PRECISION 640

- Bandwidth: 1 GHz
- Capacitance: 4pF
- Resistance: 50k Ω
- Sensitivity: < 1mV/division to 5V Step Input
- Settling Time: < 10ns to 0.01% for 5V Step Input

Figure 11.52

REFERENCES

1. "Ohm's Law and Other Novelties of Analog Design" James M. Bryant (In preparation: Pub. Analog Devices).

   "Das Ohmsche Gesetz . . . und weitere *neue* Erkanntnisse bei der Entwicklung analoger Schaltungen" James M. Bryant (Design & Elektronik [Germany] 11 July 1989).

2. "Avoiding Ground Problems in High Speed Circuits" Jeff Barrow (R.F. Design, July 1989).

   "Grounding for Low- and High-Frequency Circuits" Paul Brokaw & Jeff Barrow (Analog Dialogue 23-3 1989 - Free from Analog Devices).

3. "An IC Amplifier User's Guide to Decoupling, Grounding and Making Things Go Right for a Change" by Paul Brokaw. Available free of charge on request to Analog Devices.

4. International EMI Emission Regulations

Canada	CSA C108.8-M1983	FDR	VDE 0871/VDE 0875
Japan	CISPR (VCCI)/PUB 22	USA	FCC-15 Part J

5. "Design and Layout of a Video Graphics System for Reduced EMI" by Bill Slattery & John Wynne (E1309-15-10/89) Free from Analog Devices (Also included in Section X of this Seminar).

6. "MECL System Design Handbook" Fourth Edition, Motorola, 1983.

7. Wainwright Instruments Inc., P. O. Box 2203, Capistrano Beach, CA 92624. Tel: 714-248-2490.

   Wainwright Instruments GmbH, Widdersberger Strasse 14, D-8138 Andechs-Frieding, Federal German Republic. Tel: +49-8152-2245.

8. "Probing Techniques Become Crucial Above 500 MHz" Eldon Walters & Stan Kaveckis (EDN, 15 October 1987).