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HIGH SPEED A/D CONVERSION

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HIGH SPEED A/D CONVERTER ARCHITECTURES

- Flash
- Successive Approximation
- Subranging
- Digitally Corrected Subranging

FLASH CONVERTERS - Basic Operation

Recent advances in VLSI process technology and design techniques have made 4-10 bit flash A/D converters practical. This type of converter is characterized by high sampling rates and the ability to convert fast video input signals, usually without requiring a separate track-and-hold amplifier. The latter characteristic is limited, however, as we will discuss later.

A block diagram of a typical flash converter is shown in Figure 1.1. The analog input signal to be digitized is applied simultaneously to 2^N-1 latched comparators, where N is the number of bits. The reference voltage input for each comparator is derived from a resistive voltage divider. The reference voltage for each comparator is one least significant bit (LSB) higher than the comparator immediately below it.

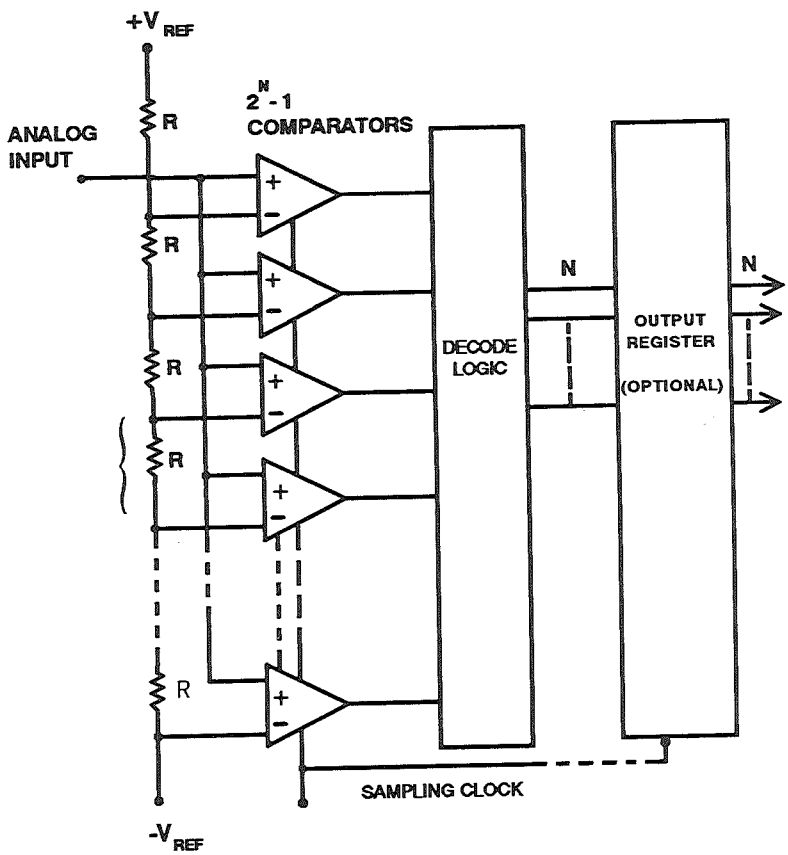


Figure 1.1

When an analog signal is present at the input of the comparator bank, all comparators which have a reference voltage below the level of the input signal will assume a logic "1" output. The comparators which have their reference voltage above the input signal will assume a logic "0" output. The result is often referred to as a "thermometer code" and is applied to a stage of decoding logic (See Figure 1.2). This decoding can be accomplished in a variety of ways (such as a simple priority encoder) and ultimately results in a binary digital output. The binary output of the decoding logic often drives an on-chip output latch.

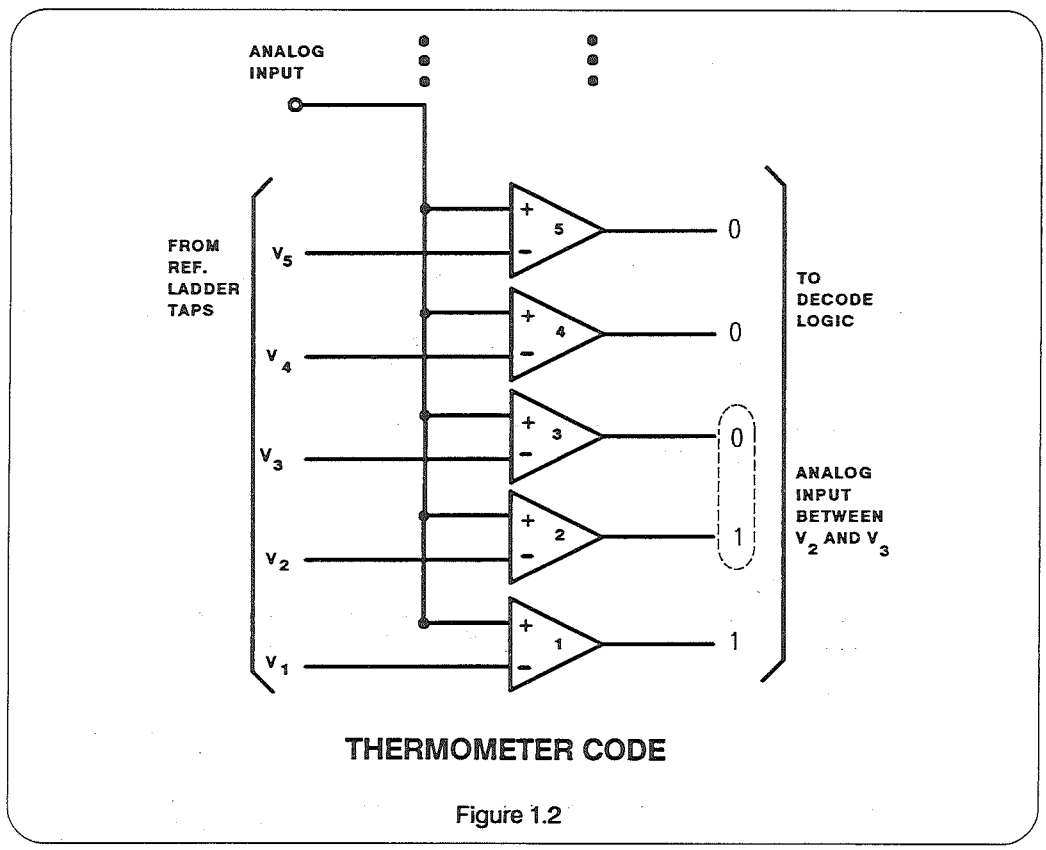
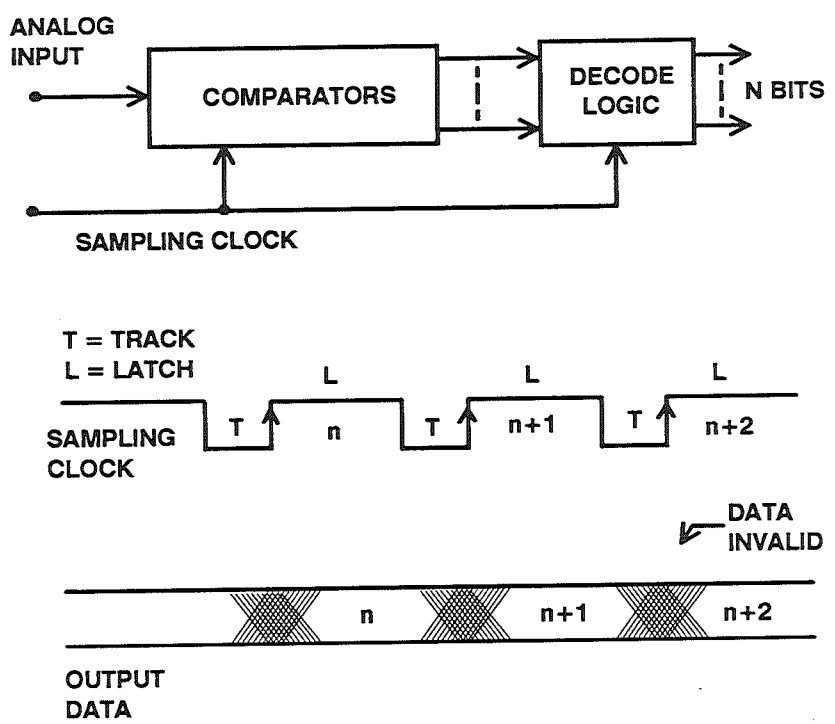


Figure 1.2

Flash Converters - Timing Considerations

The comparator bank in a flash converter has two states. In the first state (controlled by the sampling clock), the comparators essentially "track" the analog input signal. In this state, the comparator outputs are changing, and the binary decoding logic output is invalid. When the sampling clock changes to the opposite logic level, the comparators are latched or "held", much the same as in a track-and-hold amplifier.

In a flash converter which has no output data latch (such as the AD-9688 or the AD-9000), the timing of the sampling clock with respect to the output binary data is shown in Figure 1.3. Note that the output data is invalid for a period roughly equal to the sampling clock pulse width. Since this pulse width must exceed some specified minimum value for proper operation of the comparators, it follows that at high sampling rates, the time during which the output data is invalid reduces the "data valid" time, thereby making it more difficult to strobe the flash converter output into an external register. For instance, if the flash converter is operated at a 100MHz sampling rate and the sampling clock is 5ns wide (50% duty cycle), the output data will be valid for only 5ns (neglecting the rise and fall time of the output binary bits).



FLASH CONVERTER TIMING
NO PIPELINE DELAY

Figure 1.3

The addition of an internal latch after the decoding logic (such as the AD-9002, AD-9012, AD-9006, and the AD-9048) results in a timing diagram such as that shown in Figure 1.4. Note that the output data is now valid for approximately the entire clock cycle, and the flash converter can be viewed as an edge-triggered device with an inherent one-cycle "pipeline" delay. The additional pipeline delay is not usually a problem in most systems applications, and the task of clocking the output data at the proper time is simplified.

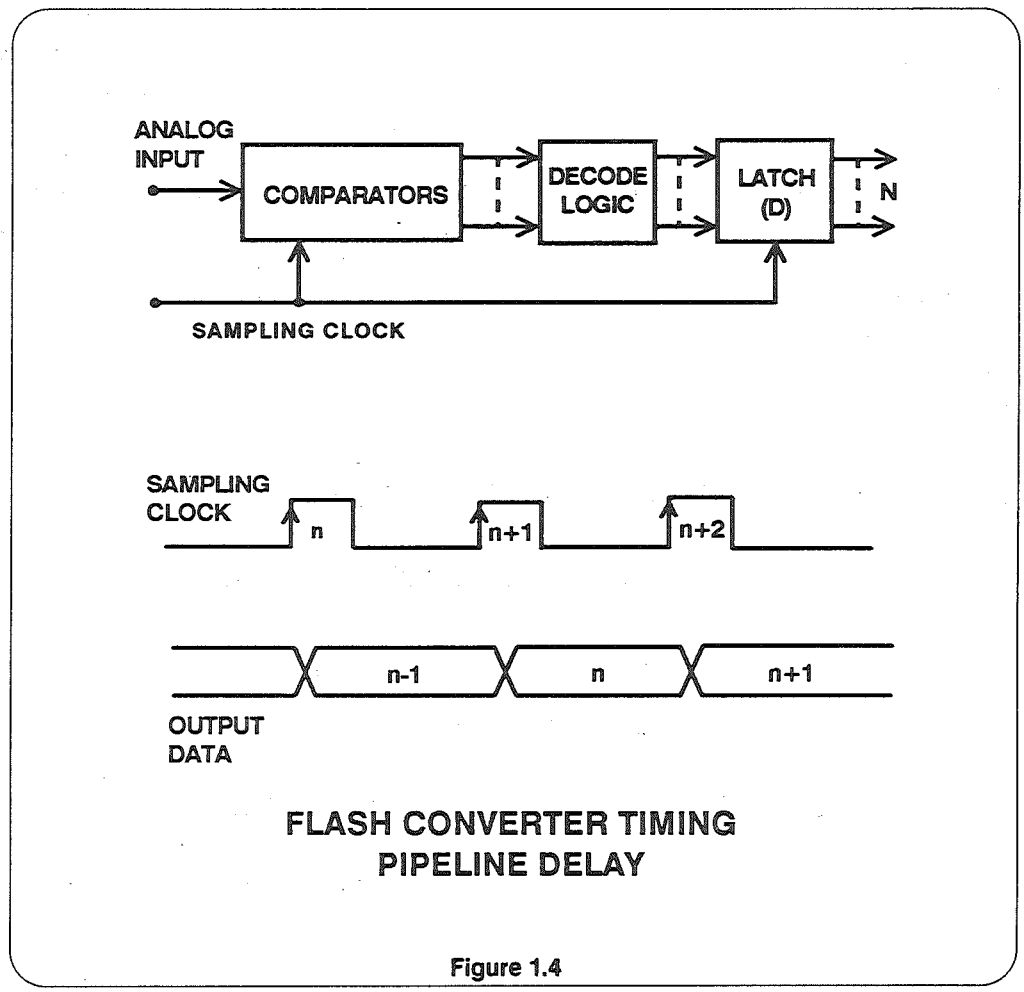


Figure 1.4

FLASH CONVERTER STATIC ERROR SOURCES

When a flash converter is digitizing a slowly changing or DC input voltage, the primary sources of integral and differential non-linearity are due to the matching of the reference ladder resistors, and the comparator input offset voltages and

currents. Although not usually specified on the data sheet, most flash converters are somewhat sensitive to the duty cycle and frequency of the encode command pulse. This problem is manifested as a shift in differential and integral non-linearity which is a function of clock duty cycle and frequency, especially when operating at or near the maximum specified sampling rate for the particular flash converter under consideration.

Another source of static flash converter errors, sometimes called "metastable state" errors, results from the finite probability that a comparator which is toggling between two logic levels (the analog input is equal to the comparator's reference voltage input) may produce an erroneous binary code at the flash converter's final output. This metastable condition can result in a fullscale error if it occurs at the flash converter's mid-scale code (i.e., bits changing from 0111...1 to 1000...0). These erroneous error codes may show up as white dots or "sparkles" when digitizing television waveforms, hence the term "sparkle codes".Proper design of the comparators and/or use of additional logic algorithms in the decoding function can minimize these errors to an acceptable level for most applications. (See section on Dynamic Testing of A/D Converters for further discussion and how to measure this error.)

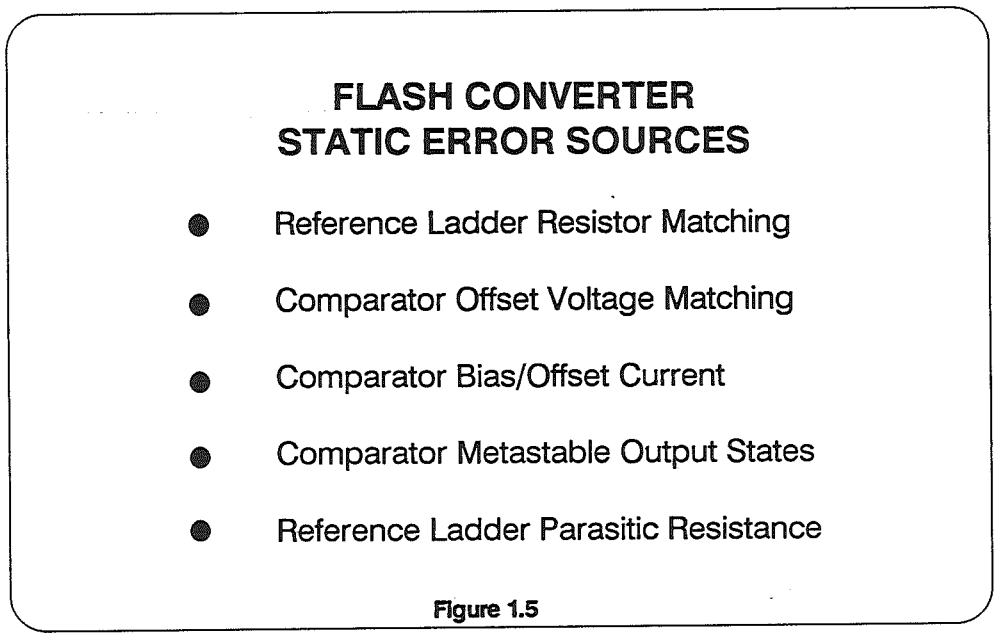


Figure 1.5

Flash Converter Dynamic Error Sources

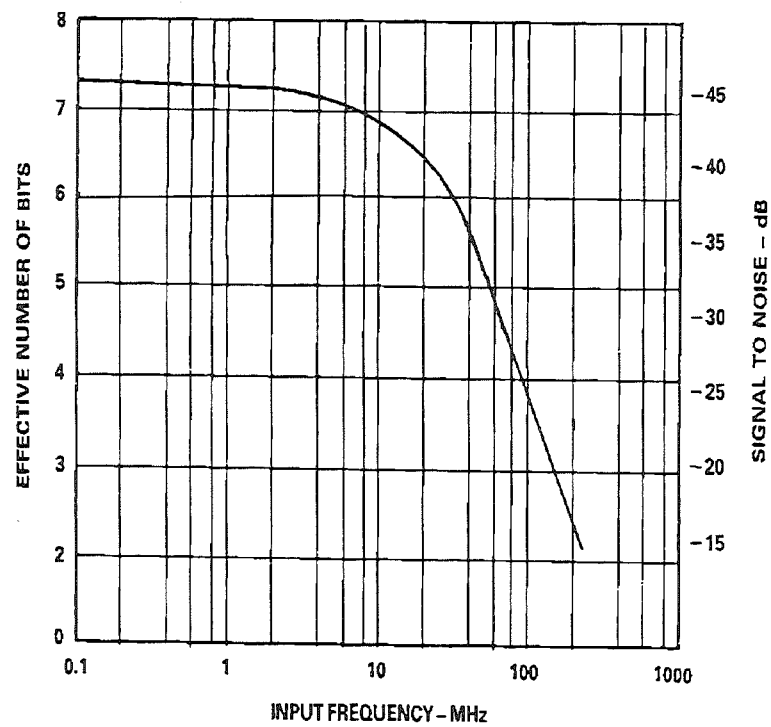
In the majority of video A/D converters (including flash converters), linearity (differential and integral) degrades as the analog input signal slew-rate increases. These errors manifest themselves as increased harmonic distortion, degrada-

tion in signal-to-noise ratio (SNR), missing codes, and spurious or "sparkle" codes. In a flash converter, these degradations occur primarily due to the relative delay mismatch between each comparator in the bank. This delay mismatch is a function of many design-related variables such as IC process variations, chip layout, comparator design, etc. A close to ideal converter would maintain its static performance specifications across the full Nyquist bandwidth (or higher for some applications).

The theoretical RMS signal-to-noise ratio for an N-bit A/D converter is given by the well-known equation

$$SNR = 6.02N + 1.76dB.$$

A typical plot of SNR versus input frequency for an 8-bit flash converter (AD-770) is shown in Figure 1.6 for a 200MHz sampling rate. The dynamic performance can also be evaluated in terms of Effective Number of Bits (ENOB) by solving the equation for N given the measured SNR. See the section on Dynamic Testing for a further discussion of this measurement.



f_S = 200 MSPS

SIGNAL TO NOISE RATIO ANDEFFECTIVE BITS FOR AD-770 8-BIT FLASH CONVERTER

Figure 1.6

Sample-to-sample variations in the effective sampling instant (aperture jitter) can also cause degradation in the overall SNR measurement for high slew-rate inputs. This jitter can be produced internally and/or externally to the flash converter. Proper grounding techniques, power supply decoupling, PC board layout, and clean sampling clock pulses (both phase and frequency stable) are the best techniques to minimize externally produced jitter components.

Glitches or "sparkle codes" due to metastable comparator states as previously discussed, can also occur for high slew-rate input signals.

In addition, high slew-rate inputs may produce what is called a "bubble" in the comparator bank thermometer code output. Ideally, the comparator bank output should be a sequence of logic "1"s followed by a sequence of logic "0"s as shown in Figure 1.2. An out-of-sequence "1" or "0" may occur for high slew-rate inputs due to comparator delay mismatches. This creates a condition which looks like a "bubble" in the normal thermometer code. Depending upon where in the sequence it occurs, the "bubble" may cause the decoding logic to produce a large error code, or "sparkle" code. The probability of getting a "bubble" due to comparator mismatch can be reduced by proper comparator design. The magnitude of the binary error (sparkle code) produced by a "bubble" can be minimized by increasing the sophistication and complexity of the decoding logic.

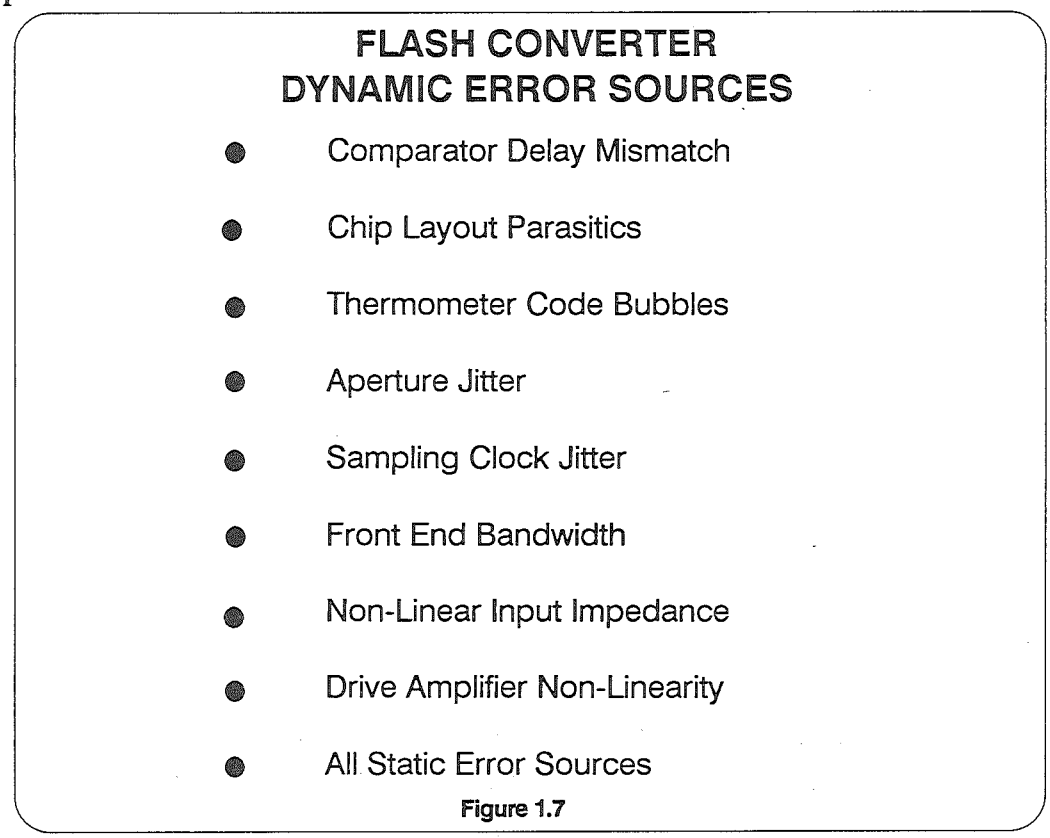


Figure 1.7

Flash Converter Full-Power Bandwidth

Flash converter "full power bandwidth" (FPBW) is a specification for which there is no currently accepted industry-wide definition. Users of flash converters should scrutinize the data sheet carefully and understand both the manufacturer's definition and test method.

In a traditional op-amp, FPBW typically is meant to be the maximum frequency at which the amplifier is capable of producing the maximum specified peak-to-peak output voltage at some level of distortion. Another commonly used definition is to calculate FPBW from the slew rate (SR) of the amplifier using the equation:

$$FPBW = \frac{SR}{2\pi V_o}$$

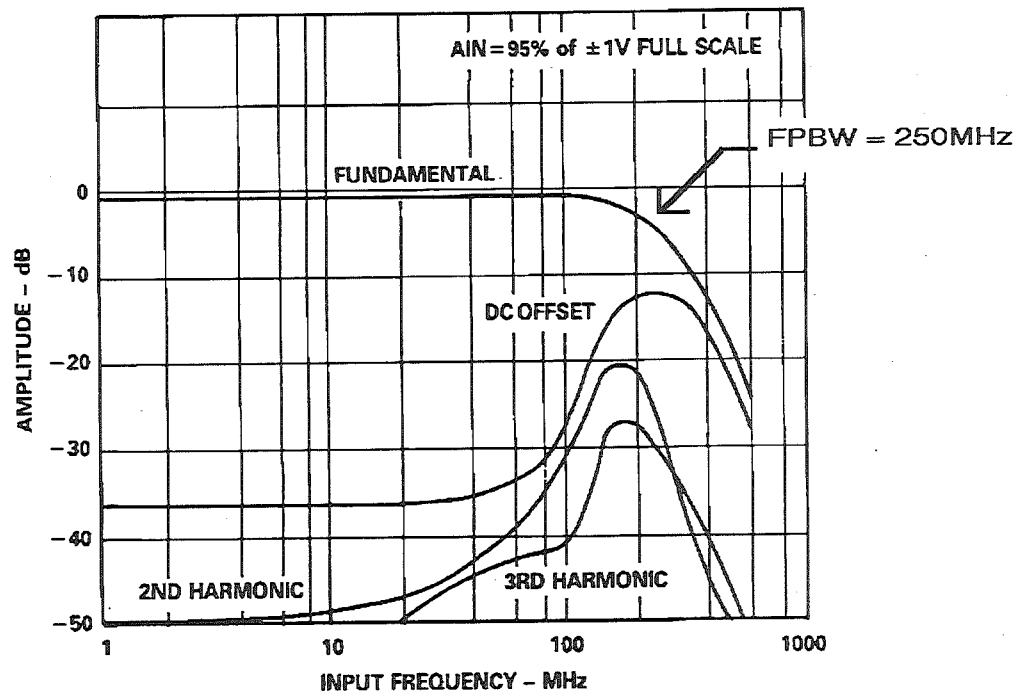
where the output voltage range of the amplifier is $\pm V_o$.

The problem in applying traditional "analog" bandwidth definitions to flash converters is that the results can be very misleading -- typically, the dynamic error sources previously discussed become dominant long before the true analog bandwidth of the comparator front end is approached.

If the FPBW is defined as the frequency at which the peak-to-peak "reconstructed" sinewave output is reduced by 3dB for a fullscale input (a common definition), then the ENOBs or SNR at this input frequency may very well render the flash converter useless in a practical application. Thus, FPBW and ENOB or SNR must be considered together when evaluating flash converter performance. It is also important that the sampling rate be specified, since dynamic degradations are also more likely to worsen as the sampling rate is increased.

Another definition sometimes encountered for FPBW is the maximum fullscale input signal that can be processed by the flash converter at a specified sampling rate without missing any codes. Using this definition will always give the most pessimistic number of any definition previously discussed and, therefore, it appears on only a few A/D data sheets.

A recently proposed definition for FPBW (courtesy Chris Manglesdorf - Senior Scientist at Analog Devices) is that frequency at which the fundamental component of the reconstructed FFT output (neglecting harmonics) of the flash converter is reduced by 3dB from fullscale. Figure 1.8 shows an FFT plot for the AD-770 where the FPBW is measured to be 250MHz using this definition.



HARMONIC DISTORTION VS. INPUT FREQUENCY AT 200 MSPS FOR AD-770

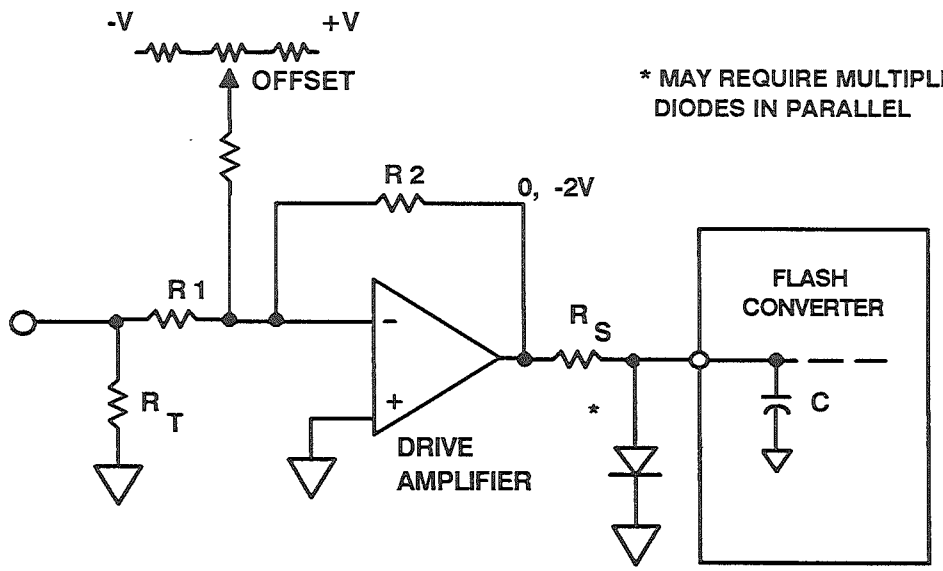
Figure 1.8

Driving Flash Converters

In a system application, the video signal to be digitized by the flash converter usually comes from a 50, 75 or 93 ohm source. This signal may be bipolar or unipolar. Obviously, if the input range of the flash converter is not compatible with the signal, a wideband amplifier will be required to produce the required gain and offset. (See Figure 1.9.)

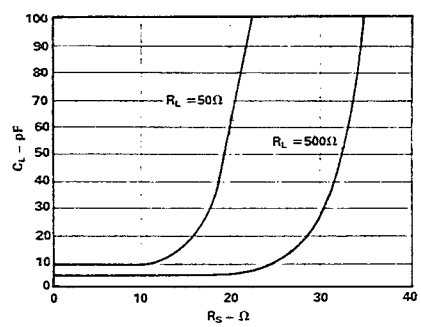
In addition, the input capacitance of some flash converters may vary as a function of the analog input signal, thereby requiring a buffer amplifier for isolation to prevent the non-linear capacitance from producing undesirable harmonics in the digitized signal.

For some flash converters, the input capacitance is so high that a buffer amplifier is required to preserve the signal bandwidth. Figure 1.10 shows the appropriate series resistor value for various load conditions when using the AD-9611 current feedback amplifier as a driver.

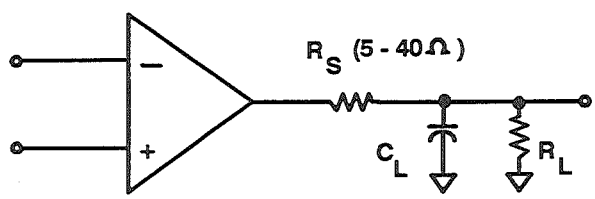


DRIVING FLASH CONVERTERS

Figure 1.9



AD-9611
AD-9615

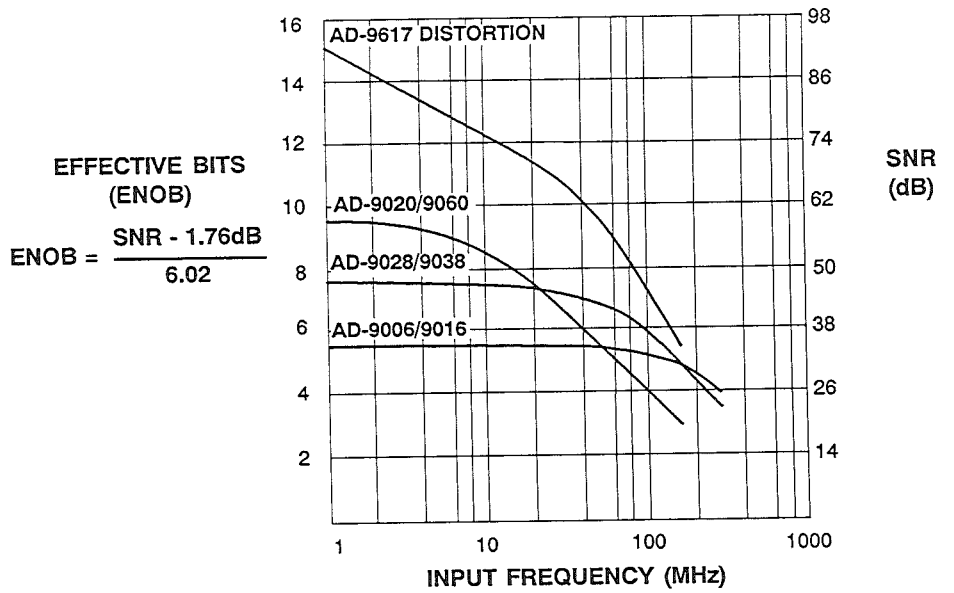


COMPENSATION WHEN DRIVING
CAPACITIVE LOADS

Figure 1.10

Since most applications do require a buffer amplifier ahead of the flash converter, the user must select it carefully. The primary consideration is to match the dynamic performance (harmonics, SNR, etc.) of the amplifier to that of the flash converter so that the inherent performance of the flash converter isn't degraded by the amplifier. Figure 1.11 shows the harmonic distortion of the AD-9617 monolithic current feedback amplifier plotted with the SNR for several flash converters. Fortunately (or unfortunately, depending on your perspective), the flash converter itself is usually the limiting factor to dynamic performance if the amplifier is properly selected. Pay particular attention to the flash converter data sheet, which should list recommended amplifiers and appropriate interface circuits.

Some flash converters have a unipolar negative input voltage range and can be damaged by positive input signals which forward bias the substrate diode. A schottkey diode offers effective protection, as shown in Figure 1.9.



FLASH ADC	RESOLUTION	SAMPLING RATE
AD9020	10 BITS	40 MSPS
AD9060	10 BITS	60 MSPS
AD9028/9038	8 BITS	250 MSPS
AD9006/9016	6 BITS	400 MSPS

FLASH ADC AND OP AMP DYNAMIC PERFORMANCE

Figure 1.11

The value of R_s should be chosen so that the drive amplifier current is limited to an appropriate value for positive output swings. Making the value of R_s too large, however, will reduce the bandwidth because of the input capacitance of the flash converter. Figure 1.12 lists a number of flash converters along with recommended drive amplifiers.

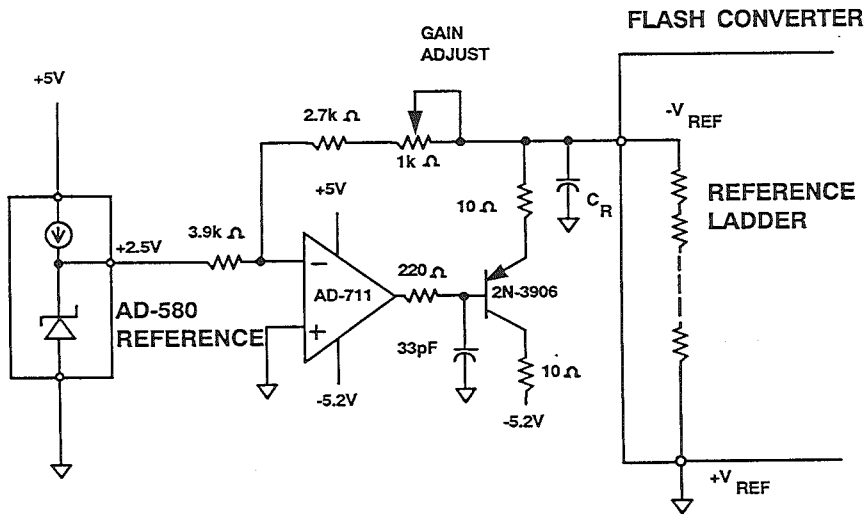
FLASH CONVERTERS AND RECOMMENDED DRIVE AMPLIFIERS

MODEL	RESOLUTION	MAX. SAMPLING RATE	INPUT C	DRIVE AMPLIFIER
AD9688	4-Bits	175 MSPS	10pF	AD5539
AD9000	6-Bits	75 MSPS	35pF	AD844
AD9006/16	6-Bits	500 MSPS	8.5pF	AD9617
AD9048	8-Bits	35 MSPS	16pF	AD847
AD9012	8-Bits	75 MSPS	16pF	AD9617
AD9002	8-Bits	125 MSPS	16pF	AD9617
AD770	8-Bits	200 MSPS	19pF	AD9617
AD9028/38	8-Bits	300 MSPS	17pF	AD9617
AD9020	10-Bits (TTL)	60 MSPS	45pF	AD9617
AD9060	10-Bits (ECL)	75 MSPS	45pF	AD9617

Figure 1.12

Flash Converter Reference Voltage Generation

Since few flash converters contain an internal voltage reference, this must be supplied by the user. A typical reference voltage circuit for a flash converter requiring a single -2V reference is shown in Figure 1.13. A buffer transistor is required since the resistance of the ladder string is usually fairly low and, therefore, fairly large drive currents are required. Also, the reference ladder resistance of a flash converter is process dependent and may vary considerably from part to part. It may also have a large temperature coefficient (see Figure 1.14).



SINGLE-ENDED REFERENCE VOLTAGE GENERATOR

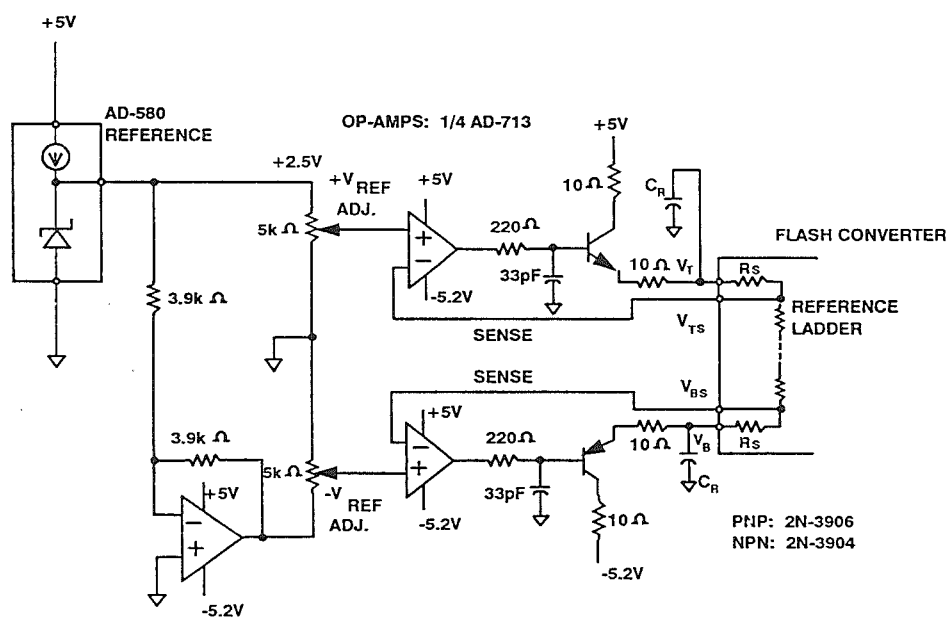
Figure 1.13

NOMINAL REFERENCE LADDER RESISTANCE AND TC

AD-9688	350 Ω, 2000 ppm/°C
AD-9000	150 Ω, 2000 ppm/°C
AD-9006/9016	80 Ω, 2750 ppm/°C
AD-9048	90 Ω, 2500 ppm/°C
AD-9012	90 Ω, 2750 ppm/°C
AD-9002	90 Ω, 2750 ppm/°C
AD-770	200 Ω, 3400 ppm/°C

Figure 1.14

If the flash converter allows bipolar operation (such as the AD-770 and the AD-9000), two reference voltages must be generated. The circuit in Figure 1.15 operates on ±5V power supplies and allows great flexibility in setting the reference voltages for a bipolar flash converter.



BIPOLAR REFERENCE VOLTAGE GENERATOR

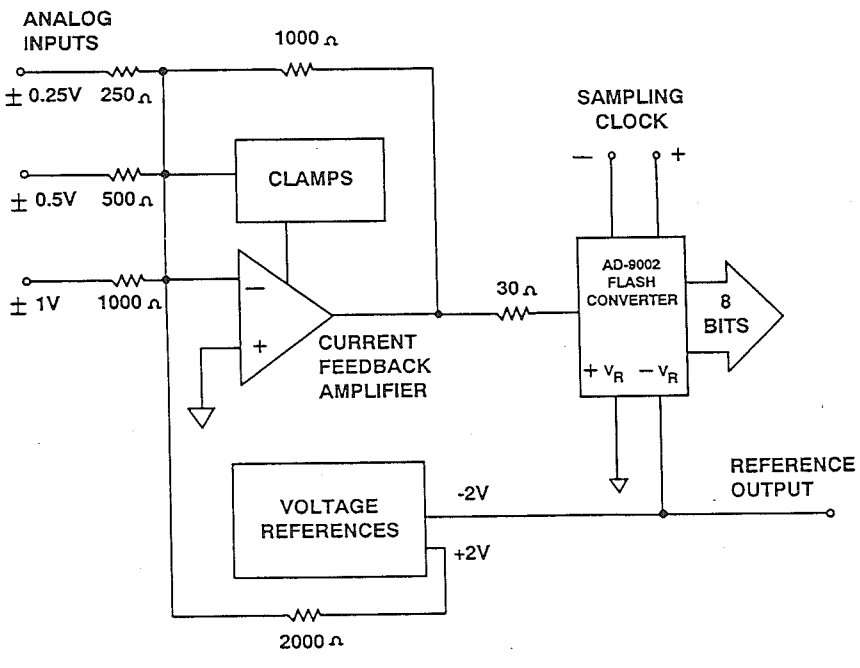
Figure 1.15

Some flash converters have a "sense" pin for the voltage reference which can be used to compensate for the voltage drop due to the package pin and bond wire resistance. This feature is utilized in the circuit shown in Figure 1.15.

Flash converters may provide access to one or more taps along the internal reference ladder resistor string. These taps can be driven from low impedance sources in order to achieve better integral linearity performance. Again, when in doubt, consult the data sheet! Bypass capacitors on the reference voltage inputs are particularly critical at sampling rates of 20MHz or greater. Ceramic chip capacitors are recommended (0.1 μF) and should be located as close to the pins as possible.

Hybrid Circuits Simplify Applications

Several hybrid circuit manufacturers have recently introduced hybrid A/D converters which contain a drive amplifier and a reference voltage as well as the flash converter itself. A block diagram of the AD-9011 8-BIT, 100MSPS hybrid A/D converter is shown in Figure 1.16.

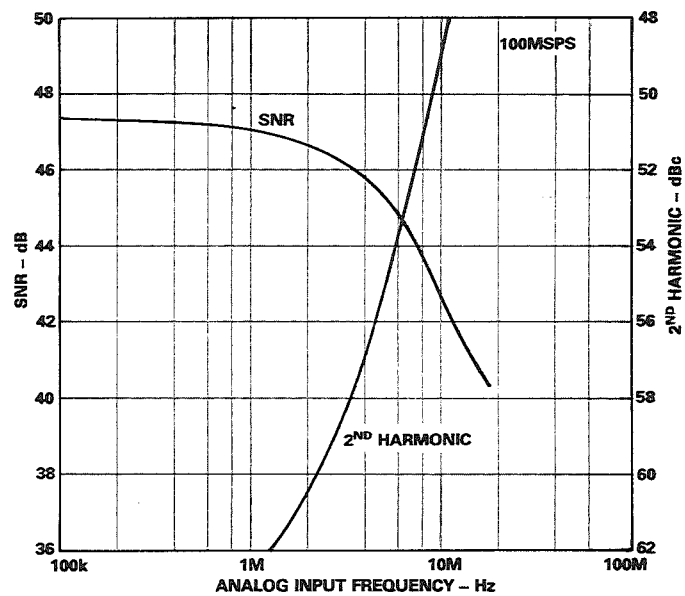


AD-9011 HYBRID: 8-BIT, 100 MSPS

Figure 1.16

The current-feedback amplifier is designed to recover from an overvoltage condition within 20ns. Clamp limits are set to protect the flash converter input. The current feedback amplifier architecture insures that the bandwidth will remain relatively constant regardless of the gain chosen.

The SNR and harmonic distortion characteristics of the AD-9011 are shown in Figure 1.17.



AD-9011 SNR AND HARMONIC PERFORMANCE, f_s = 100 MSPS

Figure 1.17

Capturing Flash Converter Output Data

At high data rates in excess of 200MHz, buffering flash converter output data can be a major challenge. It is always desirable to follow the flash converter with an appropriate buffer register located as close to the converter as possible.

If the digital outputs of a flash converter are routed directly to a backplane data bus through a card edge connector, the overall SNR and harmonic performance of the flash converter may be severely degraded by the digital output signals coupling into the analog input.

The appropriate logic family can be selected using the information in Figure 1.18.

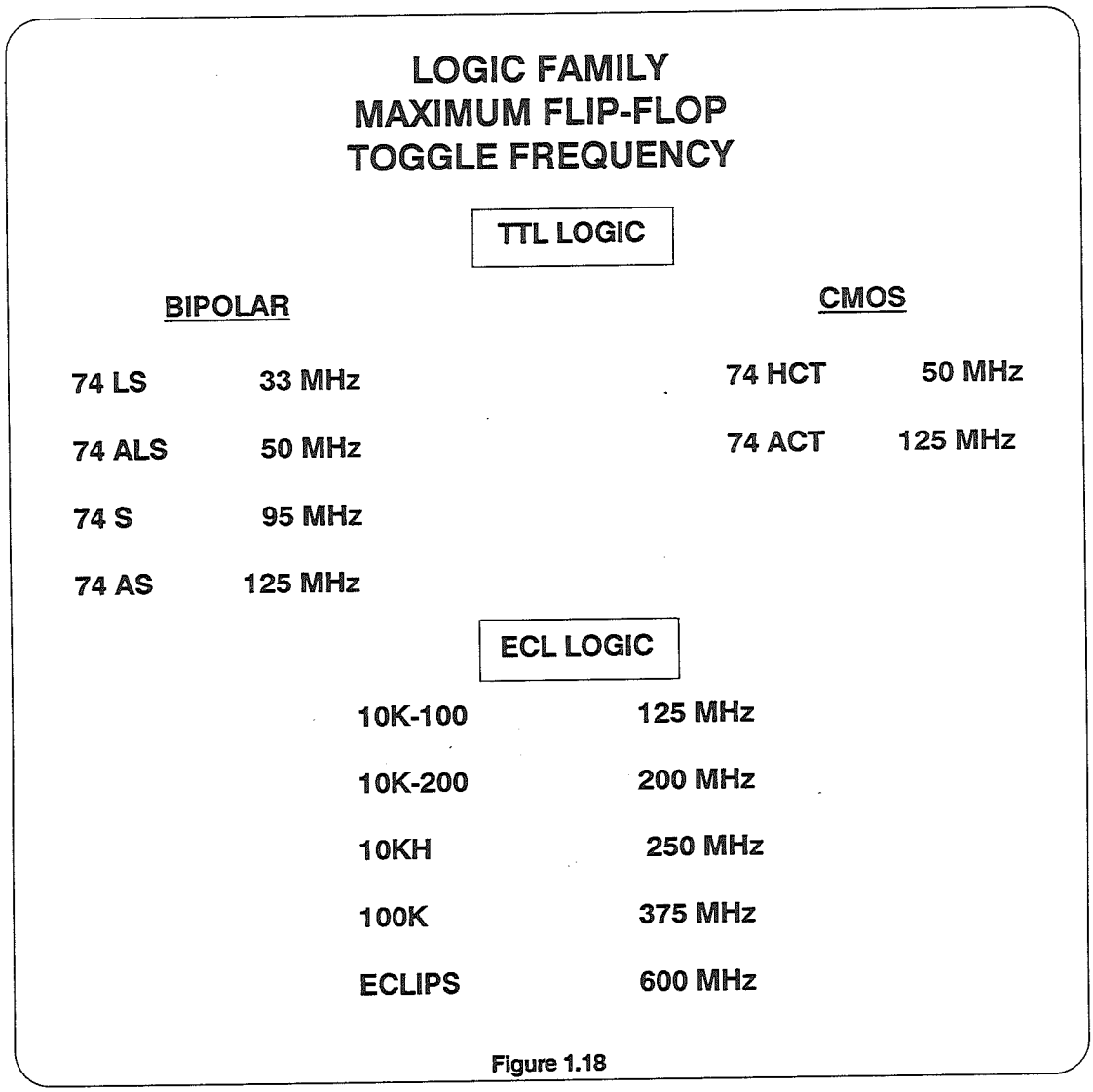
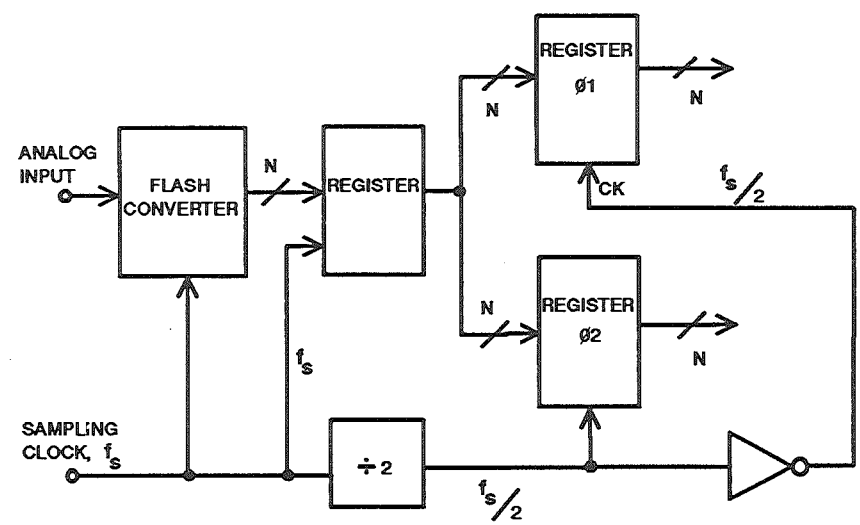


Figure 1.18

Proper timing of the buffer register clock with respect to the flash converter sampling clock is best accomplished by following the recommendations on the data sheet. At high data rates, the setup time and hold time specifications on the selected buffer register become particularly important in optimizing the timing for reliable operation.

In most applications, flash converter output data is stored in a buffer memory of considerable length. Schemes such as that shown in Figure 1.19 are often used to de-multiplex the high-speed data stream down to frequencies which are appropriate for low cost efficient CMOS or TTL memories.

Some of the newer flash converters which operate at sampling rates greater than 200MHz (such as the AD-9006/9016) will have de-multiplexing on-board to minimize the problems associated with high-speed data storage.



DEMULTIPLEXING FLASH CONVERTER OUTPUTS

Figure 1.19

"Stacking" Flash Converters To Achieve Higher Resolutions

The concept of "stacking" flash converters originated in the late 1970's when the only commercially available flash converters that had sampling rates in excess of 50MHz were 4-or 6-bit devices such as the AMD-6688 (4-bit) and the Seimens SDA-6020 (6-bit). The technique is much less popular today because of the availability of 8-bit 100-200MHz flash converters such as the AD-9002 and the AD-770.

Figure 1.20 shows an application where two 6-bit AD-9000 flash converters have been connected to achieve 7-bit resolution. The six LSB's are obtained by wire-oring the 6-bit ECL output of each flash converter -- the MSB is simply the "overflow" output of the bottom flash (the 64th comparator). The overflow output of the top flash converter must be used with additional logic to prevent the six LSB's from going to all zeros when the analog input signal goes out of range positive. Some flash converters have "overflow inhibit" logic which allows them to be used either stacked or unstacked without the need for additional external logic.

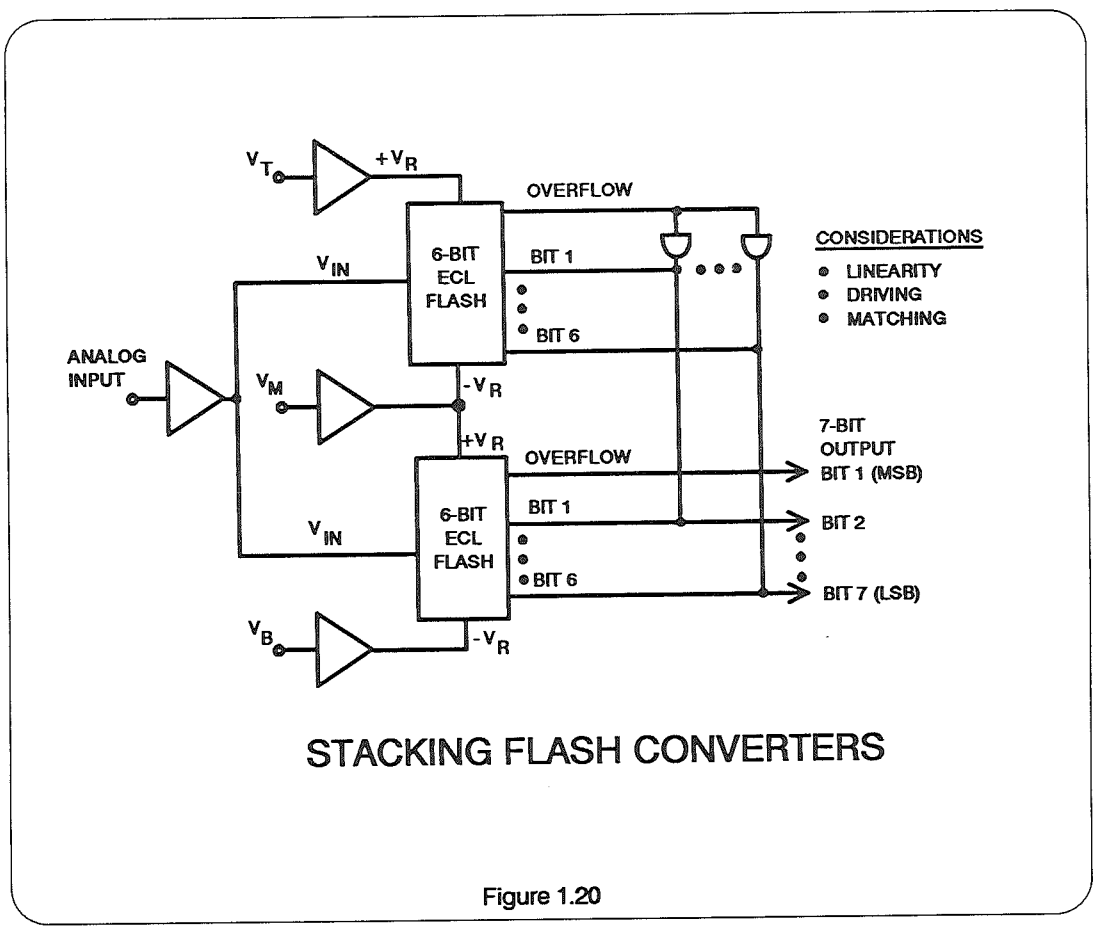


Figure 1.20

Several factors relating to the flash converter's performance must be considered when stacking flashes.

- The flash converter must have the additional "overflow" or 2^{Nth} comparator output available.

- ECL output logic levels are desirable to simplify the external logic.

- The flash converter must have the required linearity when operating at the appropriate reference voltage. For instance, if a flash converter is specified as having ±1/2 LSB linearity for a 2-volt reference, it can be assumed that operating the converter at a 1-volt reference would yield ±1 LSB linearity and produce missing codes. The linearity spec, therefore, needs to be ±1/4 LSB for a 2-volt reference in order to consider stacking two converters and still maintain the overall 2-volt reference range.

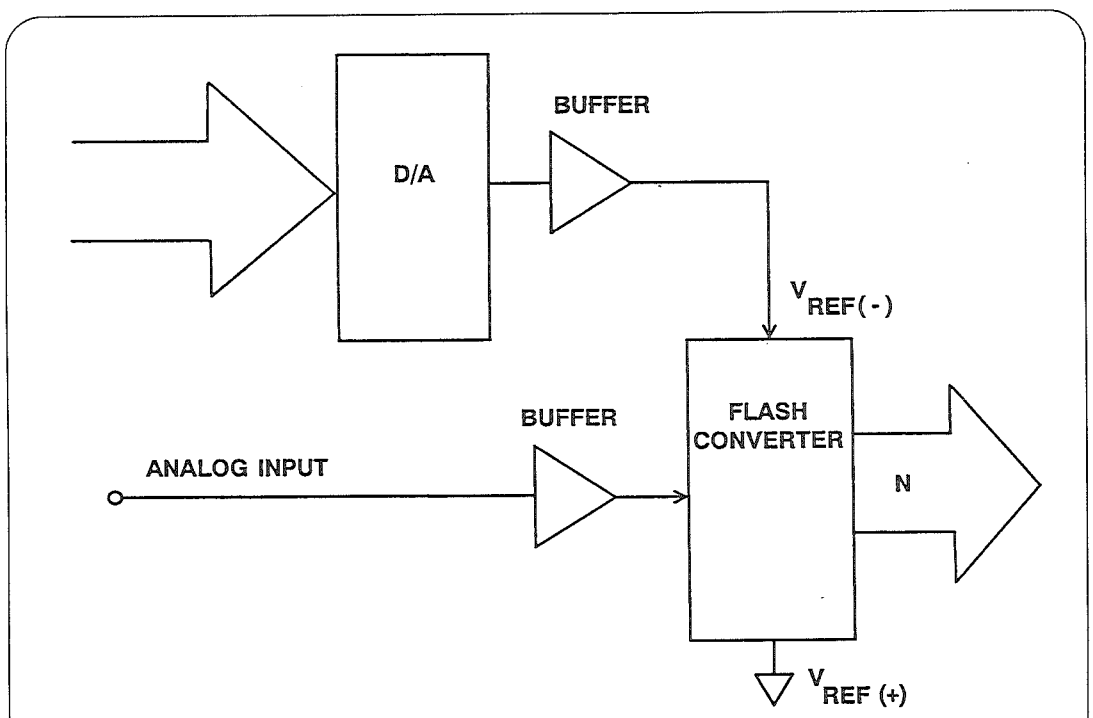
- In order to maintain dynamic performance, the two flash converters need to have well matched comparator delays. This may be difficult to insure since there is no guarantee that the two flash converters come from the same wafer or wafer lot.

In summary, stacking should be avoided except in applications where no other solution is available.

Reducing Flash Converter Reference Voltage to Achieve Greater Dynamic Range

The effective "gain" of a flash converter can be increased by lowering the reference voltage. However, the same precaution referred to in "stacking" must be observed regarding the flash linearity specification at reduced reference voltages. At least ±1/2 LSB linearity should be maintained at the lowest reference voltage. In addition, the maximum reference voltage must not exceed the data sheet spec.

Operating within these constraints, a flash converter can be configured as a Programmable Gain A/D converter if the reference voltage is derived from a D/A converter. The gain switching speed can be fairly high since the flash converter reference voltage input bandwidth specification is typically 10MHz or higher. Reference input capacitances are typically less than 50pF and are, in general, slightly higher than the analog input capacitance. A diagram of a variable-gain flash converter circuit is shown in Figure 1.21.



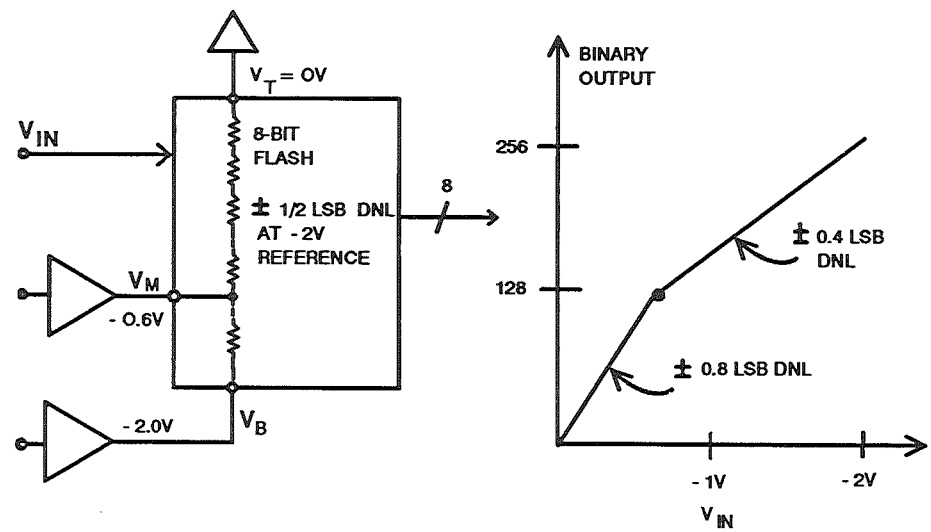
PROGRAMMABLE GAIN FLASH CONVERTER

Figure 1.21

Generation of Non-Linear Flash Converter Transfer Characteristics

If taps are available on the reference ladder string for a flash converter, a piecewise non-linear input/output transfer function can be generated. Figure 1.22 shows how the AD-9002 might be used in such an application to generate a two-piece transfer curve.

In this application, the minimum reference voltage on a portion of the resistor string is that for which the ±1/2 LSB linearity spec can still be maintained, and the maximum reference voltage for a portion of the string is governed by the data sheet spec on maximum allowable reference ladder voltage and current.



GENERATING NON-LINEAR TRANSFER FUNCTIONS

Figure 1.22

Using Two Flash Converters With Common Inputs to Double the Sampling Rate

With certain limitations, it is possible to alternate (or "ping-pong") the encode command pulse between two flash converters and effectively double the sampling rate. Figure 1.23 shows such an application. Several factors should be considered in evaluating the merits of this scheme.

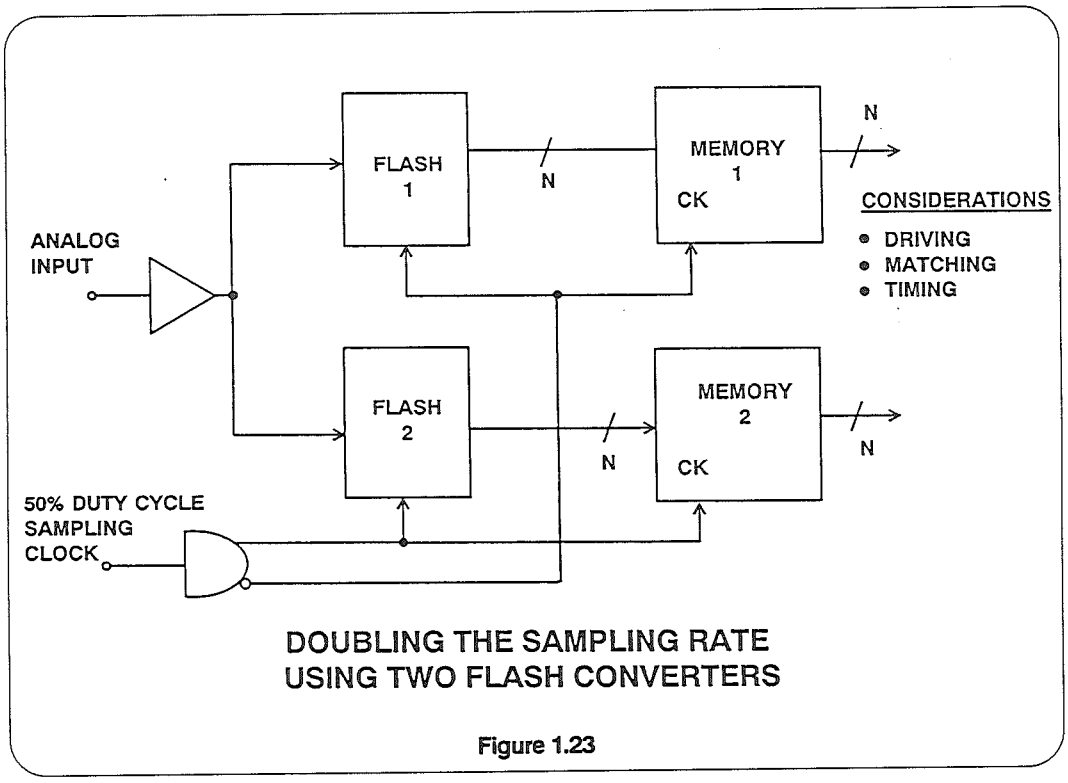


Figure 1.23

- The drive amplifier must be capable of driving the combined impedances of both flash converters to the required dynamic accuracy.

- Although the sampling rate can be doubled using this technique, the individual flash converters must maintain ENOB's, SNR, and harmonic performance at the higher analog input frequencies which will accompany the higher sampling rate. This implies that each individual flash converter be specified for analog input frequencies which are above the Nyquist rate (super-Nyquist) and which approach the maximum sampling rate.

- Delay and bandwidth mismatch between the two flash converters must not be so large as to degrade dynamic performance.

- DC differential linearity, integral linearity, gain, and offset matching between the two flash converters should be better than ±1/2 LSB.

In summary, it is difficult to use this approach and achieve anything close to Nyquist performance, but the technique may be useful for sub-Nyquist or over-sampling applications.

Use Of Track-And-Hold To Improve Flash Converter Dynamic Performance

As has been previously discussed, the effective sample time delay variations among the latched comparators in a flash converter is a primary source of dynamic errors manifested as degradation in ENOB's, SNR, and harmonic performance. Individual comparators within an array can be visualized as having variable delay lines in series with their latch strobe inputs. To understand the effect of this delay on performance, consider an 8-bit, 100MHz flash converter which is digitizing a fullscale 50MHz sinewave input (Nyquist operation). The sinewave can be expressed as:

$$v(t) = V_p \sin 2\pi f t.$$

The maximum rate-of-change of this signal occurs are the zero-crossing and is given by:

$$\left.\frac{dv}{dt}\right|_{max} = 2\pi f V_p \approx \left.\frac{\Delta v}{\Delta t}\right|_{max}$$

Solving for Δt_{max}, we obtain

$$\Delta t_{max} = \frac{\Delta v}{2\pi f V_p}$$

If the input voltage range of the flash converter is 2 volts (V_p=1V), the LSB weight is 8mV for an 8-bit flash. For the flash converter error to be less than 1 LSB (8mV), the equation can be solved for Δt_{max}, and the result is

$$\Delta t_{max} = 25ps$$

This says that the effective sample delay mismatch between comparators cannot exceed 25ps in order to ensure no missing codes when digitizing a 50MHz fullscale sinewave input.

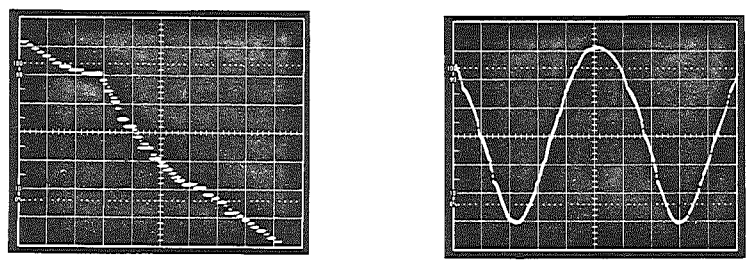
Placing an ideal track-and-hold ahead of the flash converter would theoretically eliminate this problem since the flash converter would be basically digitizing a DC input (the "held" value of the track-and-hold output). In actual practice,

track-and-holds are not ideal -- especially at high speeds. The result is that the signal actually presented to the flash converter is still changing, although at a slower rate. Even this "track-and-slow-down" approach can improve the flash converter performance at sampling rates up to about 25MHz. Above 25MHz sampling rates, the track-and-hold circuit needs to be mounted on the same substrate as the flash converter in a suitable hybrid package. Monolithic track-and-holds have been successfully used in conjunction with 8-bit flash converters in hybrid packages to achieve 7 ENOBs at Nyquist inputs sampling at a rate of 250MHz. The penalty is cost and power (7 watts). (Tektronix Model TKAD20C).

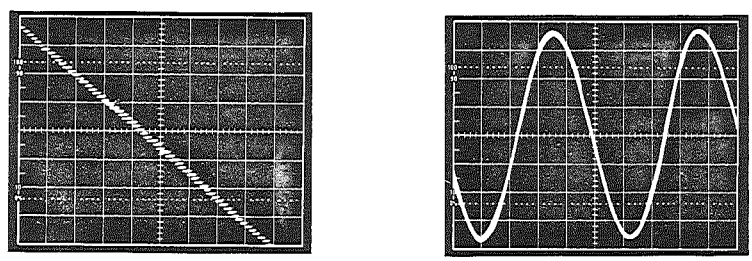
Figure 1.24 shows the improvement in dynamic linearity which can be achieved by putting a hybrid track-and-hold (HTS-0025) ahead of an older flash converter (TDC-1007).

Nevertheless, the user should strive to select a flash converter which does not need a track-and-hold in order to achieve the desired dynamic performance required for the particular application. The performance of the track-and-hold/flash converter pair is almost impossible to determine from the separate data sheet specifications alone, and considerable experimentation may be required to achieve the desired results. The optimum timing relationship between the two devices will also be difficult to determine without considerable experimentation.

In the future, lower cost monolithic track-and-holds will be packaged with the flash converters in high performance hybrids, and be fully specified for dynamic characteristics. For most applications, however, improvements in flash converter designs and IC processes will probably eliminate the need for a separate track-and-hold except for the most exacting user.



T/H INACTIVE



T/H ACTIVE

EFFECTS OF TRACK-AND-HOLD ON FLASH A/D PERFORMANCE

f_{IN} = 19.98 MHz, f_S = 20.00 MHz

Figure 1.24

FLASH CONVERTER SELECTION GUIDE

RESOLUTION	MODEL	MAXIMUM SAMPLING RATE (MSPS)
4-Bits	AD9688	175 - ECL
6-Bits	AD9000	75 - ECL
6-Bits	AD9006/9016	500 - ECL
8-Bits	AD9048	35 - TTL
8-Bits	AD9012	75 - TTL
8-Bits	AD9002	125 - ECL
8-Bits	AD770	200 - ECL
8-Bits	AD9028/9038	300 - ECL
8-Bits	AD9011*	100 - ECL
10-Bits	AD9020	60 - TTL
10-Bits	AD9060	75 - ECL

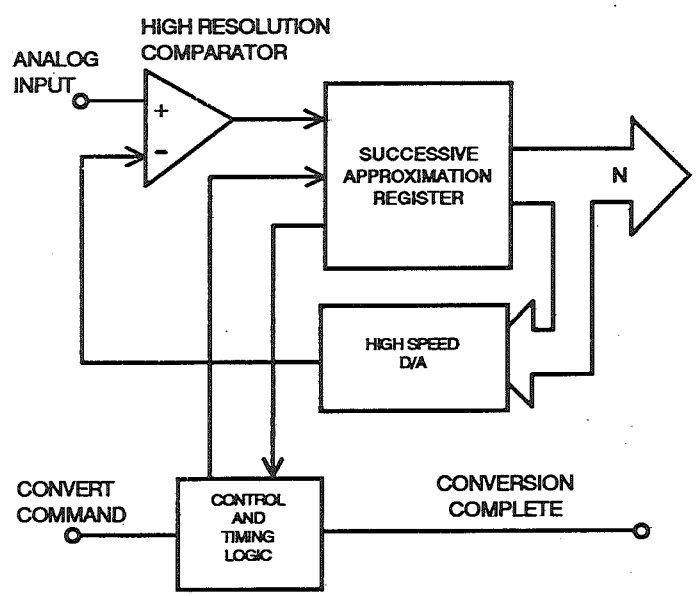
*HYBRID WITH INTERNAL AMP, REFERENCES

Figure 1.25

SUCCESSIVE APPROXIMATION A/D CONVERTERS - Basic Operation

This A/D converter architecture has been the "workhorse" in the industry primarily because it combines relatively high resolution and speed with low cost. New IC process developments in CMOS allow 12-bit, 3 μsec. converters to be achieved in monolithic form (AD-7672). In the past, this performance was only available from more expensive hybrid and modular products.

A block diagram of a successive approximation A/D converter is shown in Figure 1.26. The building blocks consist of a comparator, D/A converter, and control logic (successive approximation register, or SAR). The overall static accuracy is primarily determined by the D/A converter.



SUCCESSIVE APPROXIMATION A/D CONVERTER

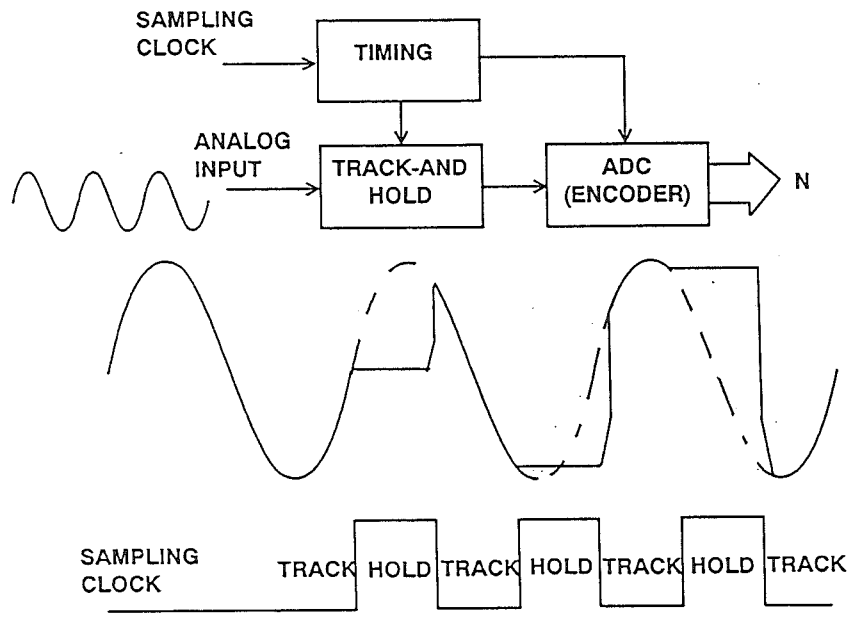
Figure 1.26

The analog input drives one input of the comparator, while the D/A converter output is connected to the other input. The conversion technique consists of comparing the unknown input against a precise voltage or current generated by a D/A converter. The input of the D/A converter is the digital number at the A/D converter's output. The conversion process is strikingly similar to a weighing process using a chemist's balance, with a set of N binary weights (e.g., 1/2 lb, 1/4 lb, 1/16 lb (=1 oz), 1/2 oz, 1/4 oz, etc., for unknowns up to 1 lb.)

After the conversion command is applied, and the converter has been cleared, the D/A converter's MSB output (1/2 full scale) is compared with the input. If the input is greater than the MSB, it remains ON (i.e., "1" in the output register), and the next bit (1/4 FS) is tried. If the input is less than the MSB, it is turned OFF (i.e., "0" in the output register), and the next bit is tried. If the second bit doesn't add enough weight to exceed the input, it is left ON ("1") and the third bit is tried. If the second bit tips the scales too far, it is turned OFF ("0") and the third bit is tried. The process continues in order of descending bit weight until the last bit has been tried. The process completed, the conversion complete line changes state to indicate that the contents of the output register now constitute a valid conversion. The contents of the output register form a binary digital code corresponding to the input signal's magnitude.

Each of the bit decisions requires a clock period. An N-bit converter will have N clock periods (plus an initialization period). Thus, the minimum conversion time of the A/D will be determined by the maximum allowable clock frequency. This frequency is limited by several factors: SAR clock-to-data-output delay, D/A settling time, comparator settling time, and SAR input data setup time. Hybrid 12-bit SAR A/D converters are available which have total conversion times approaching 1μsec.

During the conversion time, it is important that the analog input signal be held constant. This requires that a SAR A/D converter be preceded with an appropriate track-and-hold if dynamic signals are to be digitized. Figure 1.27 shows a typical configuration. As has been previously discussed, it is difficult to determine the overall dynamic performance of this system by examining the separate data sheets for the track-and-hold and the SAR A/D (sometimes called the "encoder"). A more desirable solution is to purchase a "sampling" A/D converter where the track-and-hold, encoder, and appropriate timing circuits are contained in a single package which is fully specified for dynamic performance.



ADC WITH TRACK-AND-HOLD

Figure 1.27

SUCCESSIVE APPROXIMATION A/D CONVERTER SELECTION GUIDE

ENCODERS (NO T/H)

RESOLUTION	MODEL	CONVERSION TIME	TECHNOLOGY
12-Bits	AD-7572	5 μ sec	IC-CMOS
12-Bits	AD-7672	3 μsec	IC-CMOS
12-Bits	HAS-1202-A	1.86 μ sec	Hybrid
12-Bits	AD-1377	10 μ sec	Hybrid

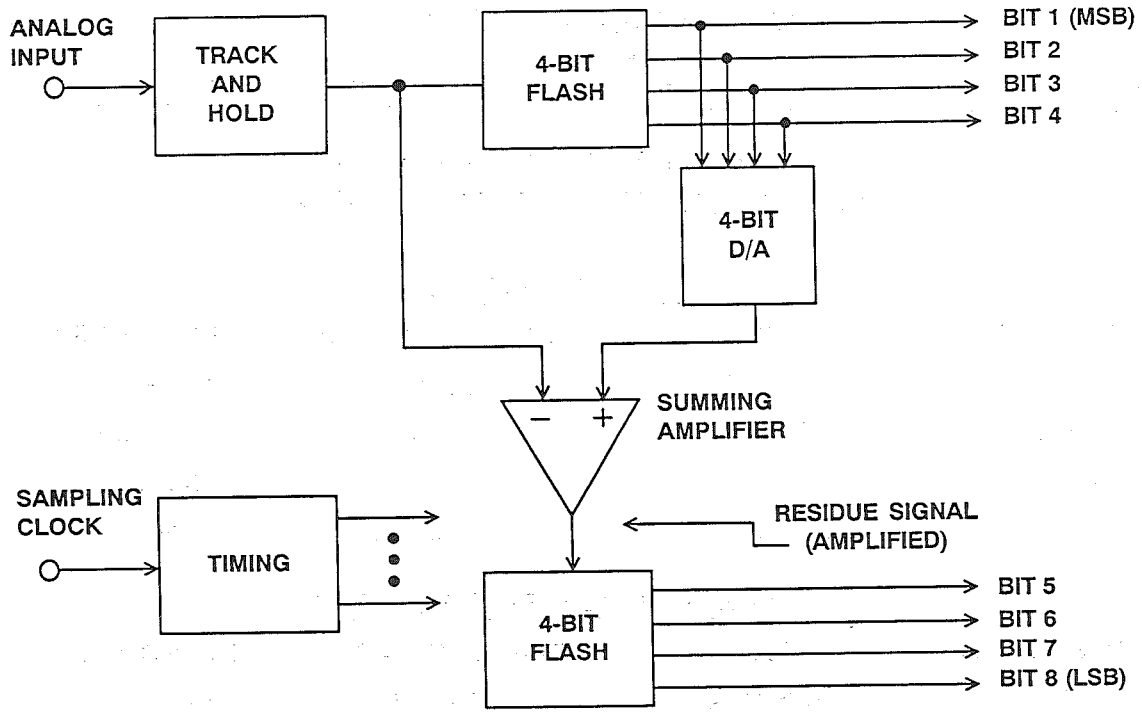
SAMPLING A/D CONVERTERS (WITH T/H)

RESOLUTION	MODEL	SAMPLING RATE	TECHNOLOGY
12-Bits	HAS-1204	500 kHz	Hybrid
12-Bits	AD-7878	100 kHz	IC-CMOS
14-Bits	AD-7871	83 kHz	IC-CMOS
16-Bits	AD-1380	50 kHz	Hybrid

Figure 1.28

SUBRANGING A/D CONVERTERS - Basic Operation

A block diagram of an 8-bit subranging A/D converter based upon two 4-bit flash converters is shown in Figure 1.29. The conversion process is done in two steps. The first four significant bits (MSBs) are digitized by the first flash (to better than 8-bits accuracy), and the 4-bit binary output is applied to a 4-bit D/A converter (better than 8-bit accurate). The D/A converter output is subtracted from the held analog input, and the resulting residue signal is amplified and applied to the second 4-bit flash converter by the summing amplifier. The outputs of the two 4-bit flash converters are then combined into a single 8-bit binary output word. If the amplified residue signal doesn't exactly fill the range of the second flash converter, non-linearities and missing codes will result.



8-BIT SUBRANGING A/D CONVERTER

Figure 1.29

Subranging A/D Converters - Error Sources

The following sources can contribute to errors in the basic subranging A/D converters:

SUBRANGING ERROR SOURCES

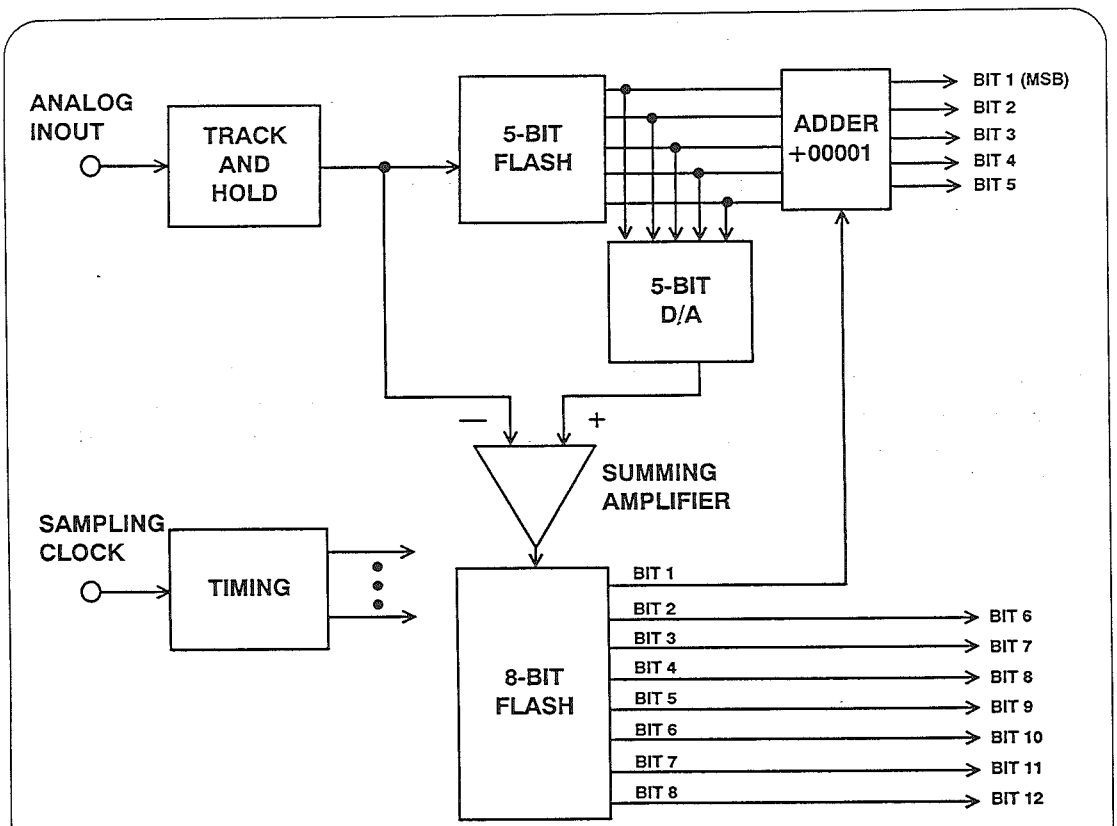
- First flash converter gain, offset, and linearity errors.
- D/A converter gain, offset, and linearity errors.
- D/A converter settling time.
- Summing amplifier gain, offset, and settling time errors.
- Second flash converter gain, offset, and linearity errors.

Figure 1.30

These errors are very troublesome at the "subranging" points and can contribute to non-linearities and missing codes in the overall A/C converter transfer function. Modern subranging A/D converters use a technique called "digital correction" to eliminate most of these problems.

DIGITALLY CORRECTED SUBRANGING (DCS) A/D CONVERTERS - Basic Operation

A block diagram of a 12-bit DCS A/D converter is shown in Figure 1.31. Note that a 5-bit and an 8-bit flash converter have been utilized to achieve a 12-bit DCS output. If there were no errors, the 5-bit "residue" signal applied to the 8-bit flash converter by the summing amplifier would never exceed one-half of the range of the 8-bit flash. The extra range in the second flash converter is used in conjunction with the error correction logic (usually just an adder) to correct the output data for most of the errors inherent in the traditional uncorrected subranging converter previously discussed. An in-depth treatment of DCS A/D converter operation and design is given in the article entitled "Multistage Error Correcting A/D Converters".



12-BIT SUBRANGING A/D CONVERTER - DCS

Figure 1.31

The following error sources can be corrected by proper use of this technique:

ERRORS CORRECTED BY DCS TECHNIQUE

- Track-and-hold droop error.
- Track-and-hold settling time error.
- First flash gain, offset, and linearity error.
- D/A converter offset error.
- Summing amplifier offset error.
- Second flash offset error.

Figure 1.32

Proper use of the DCS technique will either correct for the above errors or translate them into either a gain and/or offset error in the transfer function of the overall A/D converters.

This technique is ideally suited to high-speed cost-effective A/D converters and has been used successfully in card-level, hybrid, and monolithic A/D converters. These products have on-board track-and-hold functions and are completely specified in terms of both static and dynamic performance characteristics.

DCS A/D CONVERTER SELECTION GUIDE

SAMPLING A/Ds (WITH T/H)

RESOLUTION	MODEL	SAMPLING RATE	TECHNOLOGY
10-Bits	CAV1040	40 MHz	PC Card
12-Bits	AD1678/678	200 kHz	IC
12-Bits	AD9003	1 MHz	Hybrid
12-Bits	AD9005	10 MHz	Hybrid
12-Bits	CAV1220	20 MHz	PC Card
14-Bits	AD1679/679	100 kHz	IC
14-Bits	AD1779/779	100 kHz	IC
14-Bits	AD9014	10 MHz	PC Card

ENCODERS (NO T/H)

RESOLUTION	MODEL	CONVERSION TIME	TECHNOLOGY
12-Bits	AD671	500 ns	IC

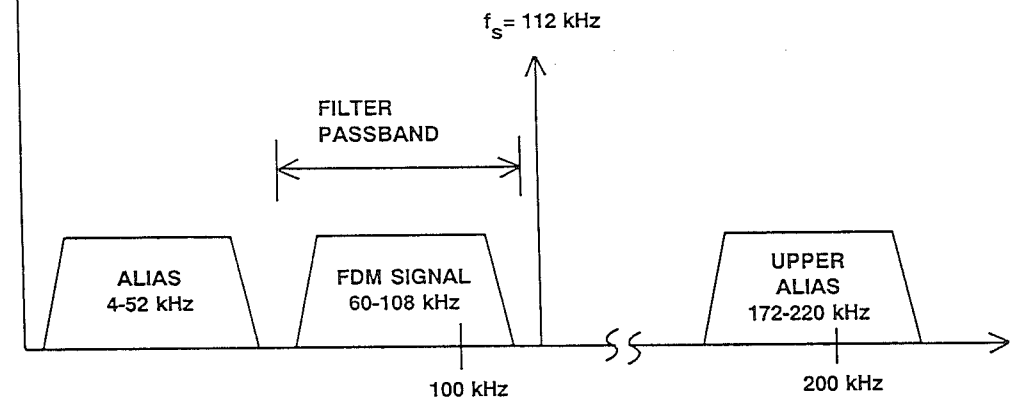
Figure 1.33

A/D CONVERTER APPLICATIONS

- Undersampling (Super-Nyquist)
- Oversampling
- Dithering
- Multiplexing

UNDERSAMPLING, SUPER-NYQUIST, AND DOWN CONVERSION APPLICATIONS

When the analog signal being digitized by an A/D converter exceeds one-half the sampling rate, the condition is often referred to as "super-Nyquist" or "undersampling". Nyquist's criterion state that the bandwidth (not the actual frequency) of the signal being digitized should not exceed one-half the sampling rate for all information to be preserved. As an example, consider a telecommunications transmultiplexer application where Frequency Division Multiplexed (FDM) data occupying the bandwidth of 60 to 108kHz is sampled at a frequency of 112kHz. Figure 1.34 shows the spectrum of the signal and the location of the "aliased" components. At the receiving end of the system, the filter which follows the reconstruction D/A converter is a bandpass rather than a lowpass and must filter out the "aliased" components falling between 4kHz and 52kHz as well as the component located at the sampling frequency of 112kHz.



SUPER-NYQUIST SAMPLING OF FDM SIGNAL

Figure 1.34

Operation of an A/D converter in super-Nyquist applications obviously requires that the dynamic performance of the converter be known for input frequencies above $f_s/2$. The SNR, ENOB, and harmonic performance of an A/D converter typically degrades as the input frequency is increased and may render the converter useless for super-Nyquist applications. For example, it may be necessary to use a track-and-hold ahead of a flash converter in order to achieve acceptable dynamic performance.

Another application for "super-Nyquist" operation is in the direct conversion of IF signals to baseband. Most traditional communication and radar receivers employing A/D converters utilize a system in which the intermediate frequency (IF) from the front end of the receiver is down-converted to a baseband signal by a mixer (see Figure 1.35). This final IF stage uses a local oscillator which is phase coherent with the signal carrier frequency. The mixer output contains a baseband signal which is proportional to the phase difference between the two inputs. Following the mixer is a lowpass filter, DC amplifier, and an A/D converter.

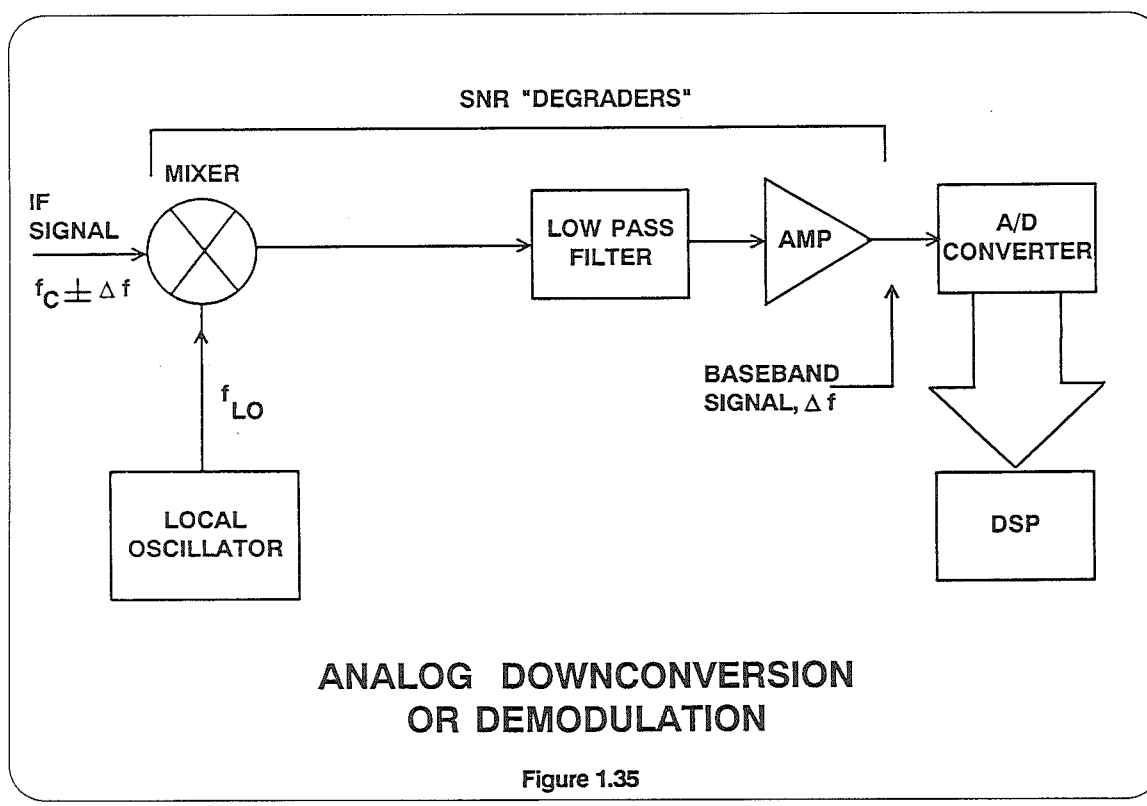
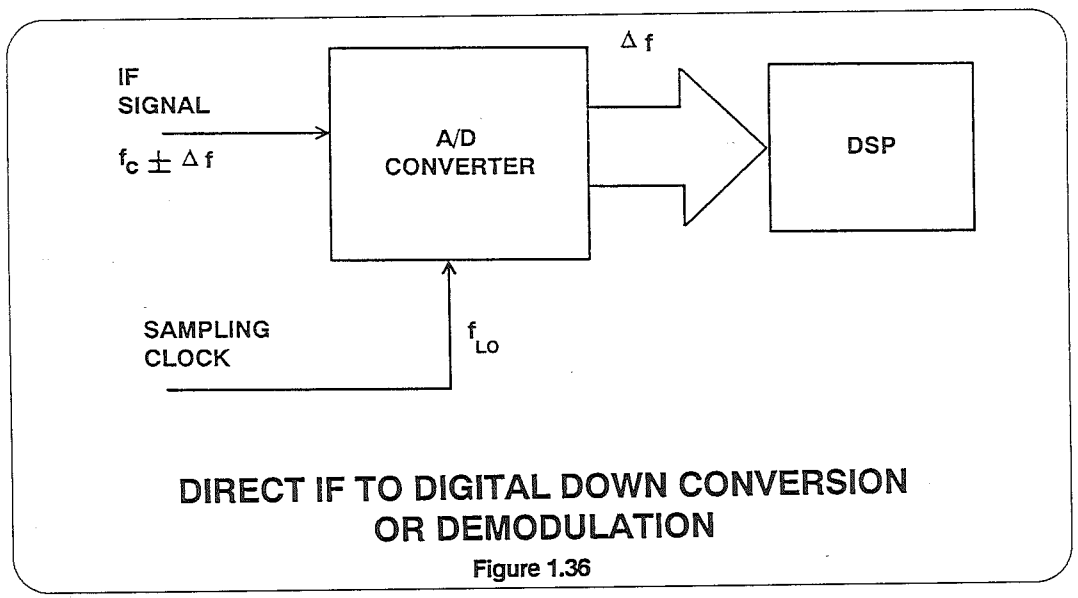


Figure 1.35

Typical mixers have a conversion loss ranging from 4 to 6dB. In cases when the signal-to-noise ratio is limited by the front end, elimination of the mixer will improve the overall noise figure of the receiver. This can be accomplished (as shown in Figure 1.36) if the IF signal is sampled at a rate which is equal to the local oscillator frequency. The A/D converter now looks like a demodulator. If the A/D converter samples an analog signal of the same frequency as the sampling frequency, the digitized output is a DC value. Any deviation in the analog signal from the sampling frequency looks like a "beat" frequency, and the demodulation process is thereby achieved.

The data from the A/D converter must be processed using an FFT which computes both the real and imaginary components of the digitized signal. This is necessary in order to preserve the phase information contained in the demodulated signal. The total bandwidth of the signal to be demodulated must be less than $f_s/2$ in order not to violate the Nyquist criterion.

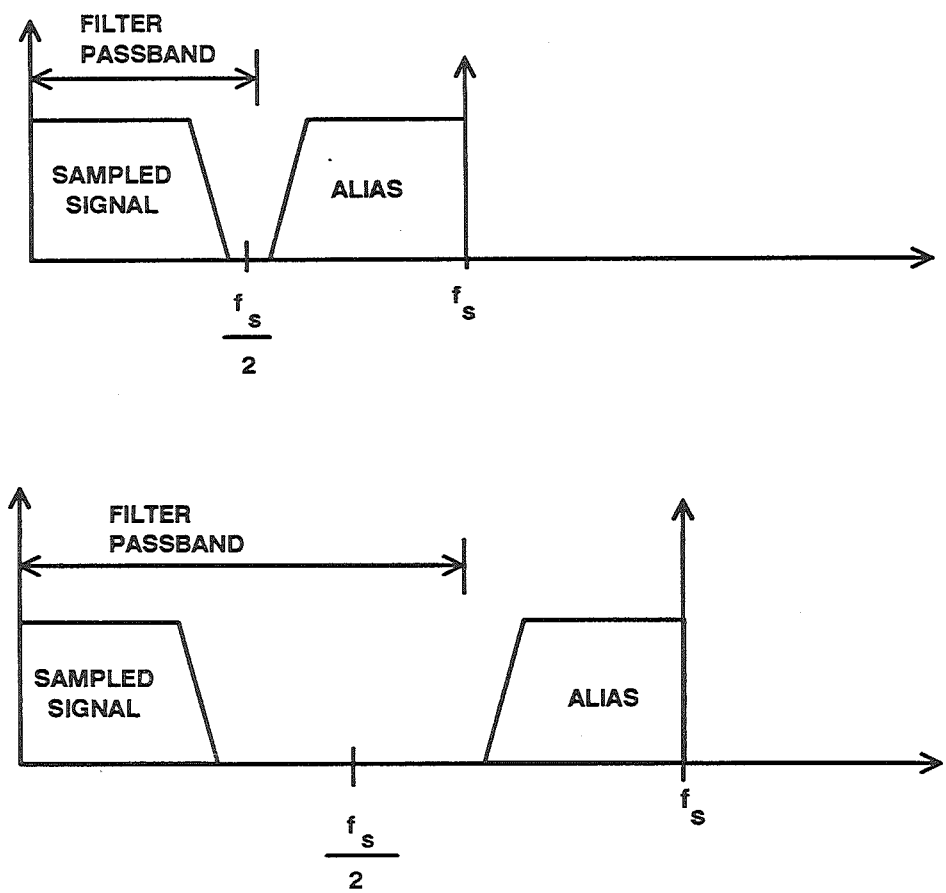


DIRECT IF TO DIGITAL DOWN CONVERSION OR DEMODULATION

Figure 1.36

OVERSAMPLING APPLICATIONS

The technique of sampling a signal at greater than twice its maximum frequency (called "oversampling") has several advantages in A/D converter applications. Increasing the sampling rate beyond the Nyquist rate $f_s/2$ makes the design of the anti-aliasing filter preceding the A/D converter much easier, as shown in Figure 1.37.



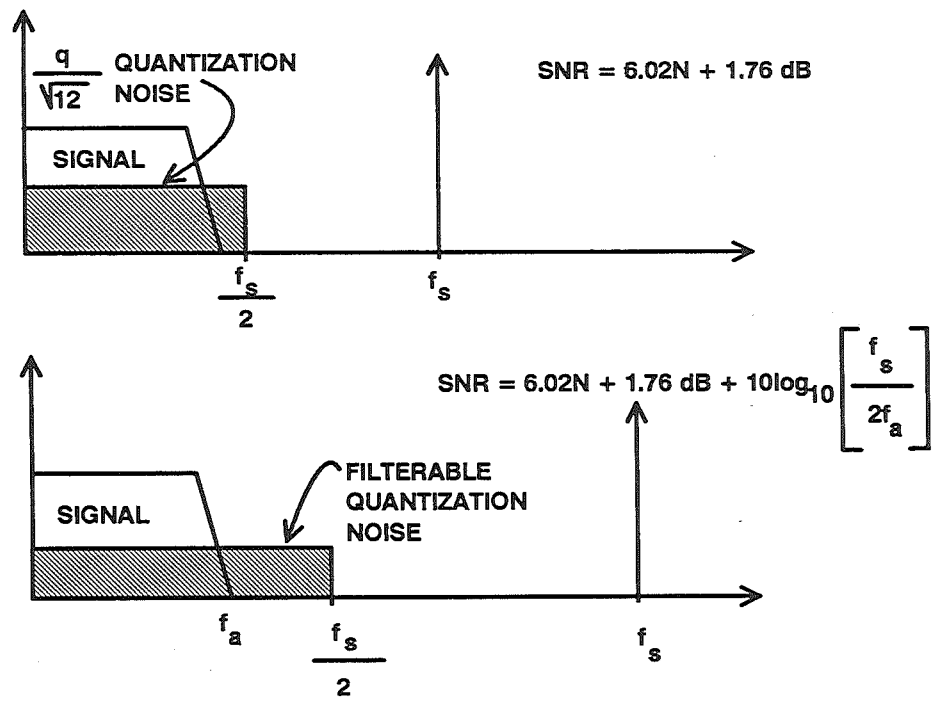
EFFECT OF OVERSAMPLING ON FILTER REQUIREMENTS

Figure 1.37

Also, the effective SNR can be improved by oversampling, as shown in Figure 1.38. For a given sampling rate f_s, the theoretical RMS quantization noise in the bandwidth $f_s/2$ is given by $q/\sqrt{12}$, where q is the weight of the least significant bit. (See derivation given in Reference 15.) From this, the theoretical formula for the SNR of an N-bit A/D converter (SNR = 6.02N + 1.76dB) can be easily derived. If the signal bandwidth f_a is held constant, and the sampling rate is increased, the effect is to "spread" the quantization noise over a wider bandwidth, thereby reducing the RMS noise in the analog bandwidth, f_a. The exact expression for the fullscale sinewave SNR under these conditions is given by

$$SNR = 6.02N + 1.76dB + 10\log_{10}\left[\frac{f_s}{2f_a}\right]$$

where f_s is the sampling rate and f_a is the analog bandwidth of interest. It can be seen that doubling the sampling rate for a constant analog bandwidth has the effect of increasing the SNR by 3dB or increasing the ENOBs by 1/2 bit. Digital post processing of the quantized data in conjunction with a digital lowpass filter of bandwidth f_a is usually used to obtain this improvement. The noise power in the bandwidth f_a to $f_s/2$ is removed by the digital filter. See pp. 15-22 of the February 1988 **Hewlett-Packard Journal** for further discussion of this topic.

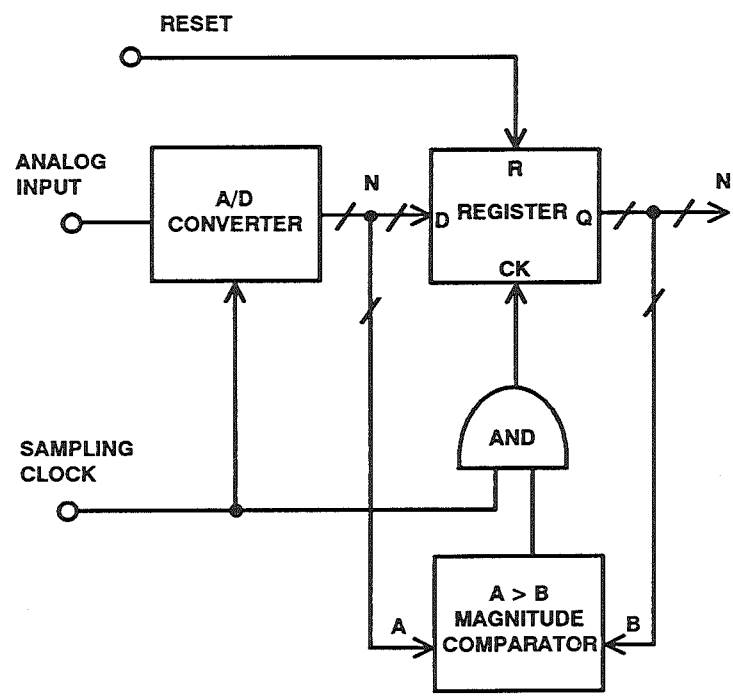


EFFECT OF OVERSAMPLING ON QUANTIZATION NOISE

Figure 1.38

Absolute Peak Detector

An absolute peak detector circuit is shown in Figure 1.39. A reset pulse is first applied to the register at the start of the time period. The A/D converter sampling clock is then initiated. The A/D converter output will only be clocked into the register if it is greater than the previous sample. In this way, the largest sample during the sampling window is always stored in the register. At the end of the period, the sampling clock is stopped, and the peak value is read. The sampling rate must be substantially higher than the analog input frequency in order to capture the peak of interest.



ABSOLUTE PEAK DETECTOR

Figure 1.39

APPLICATIONS OF DITHERING

The assumption of a random quantization error signal which is independent of input signal allows an easy derivation of the familiar expression $q/\sqrt{12}$ (q=1LSB) for the RMS quantization noise (within the Nyquist bandwidth) of an ideal A/D converter. For a sinusoidal input, however, the A/D converter output error is actually composed of a large number of harmonics of the input frequency. These harmonics (regardless of frequency) all appear within the Nyquist bandwidth (due to aliasing produced by the sampling process). If the power of all these harmonics is summed, the RMS quantization power is accurately given by $q/\sqrt{12}$.

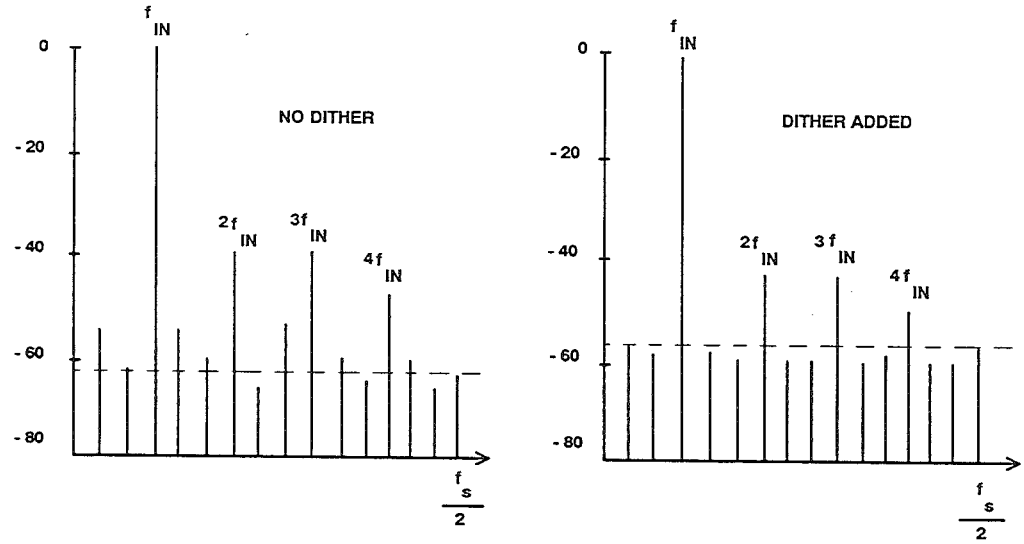
Since the error waveform produced by the quantization of a periodic waveform is itself periodic, and appears as harmonic distortion of tones present at the A/D converter input, this situation is highly undesirable in spectral analysis applications. In receiver application especially, it is more desirable to have the quantization noise power spread uniformly over the Nyquist bandwidth rather than concentrated in a discrete set of spectral lines. Also, the harmonics present in the error waveform are coherently related to the A/D input waveform. This further complicates the task of processing the signal spectrum to differentiate between signals and system-induced spurious components, especially when "searching" the spectrum for the presence of low-level signals in the presence of large signals.

If random noise which has a flat spectrum over the Nyquist bandwidth (dither) is added to the A/D input signal, the effect is to randomize the quantization noise, provided the random noise voltage is at least $q/\sqrt{12}$. Obviously, this has the effect of degrading the overall SNR by 3dB, but also has the effect of destroying any statistical correlation between sample errors. The composite noise spectrum at the A/D converter output is thus made flat over the Nyquist bandwidth. The actual noise level which provides optimum performance is very A/D and application dependent, but typically is chosen to be several dB greater than $q/\sqrt{12}$. The effects of adding noise to a digitized sinewave is shown in Figure 1.40. The process of adding random noise to the input signal is referred to as *dithering*.

In a receiver application, the front-end gain can be adjusted so that the actual receiver noise present at the A/D input is at the correct level to randomize the quantization error as shown in Figure 1.41.

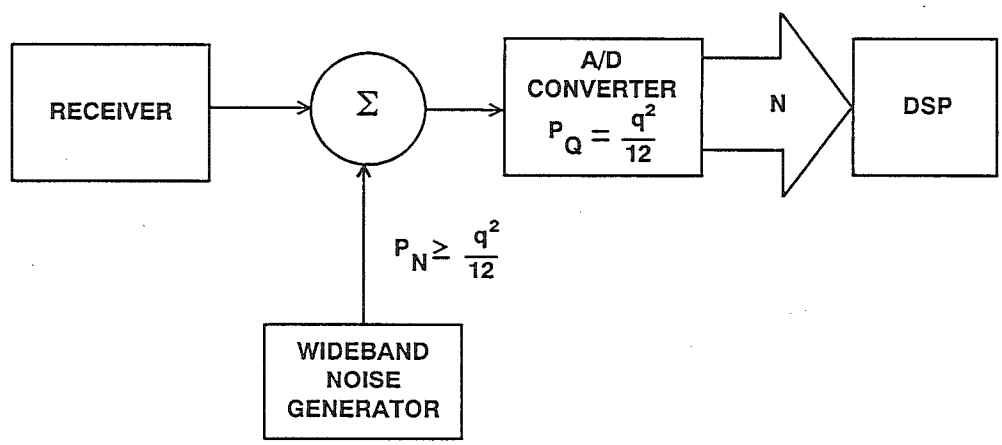
It should also be remembered that dither can be introduced into the system by phase jitter on either the sampling clock or the input sinewave. Either of these will have the effect of increasing the overall noise floor. See the section on Aperture Jitter for further discussion.

Sophisticated dithering signals (other than random noise) have been used in conjunction with digital filtering and processing to achieve improvements in A/D converter performance without degrading SNR performance. This is accomplished by adding the appropriate dither signal to the A/D input and then subtracting it from the A/D output. A detailed discussion of this technique is given on pp. 70-76 in the June 1988 **Hewlett-Packard Journal**.



EFFECTS OF DITHER ON FFT SPECTRAL RESPONSE

Figure 1.40

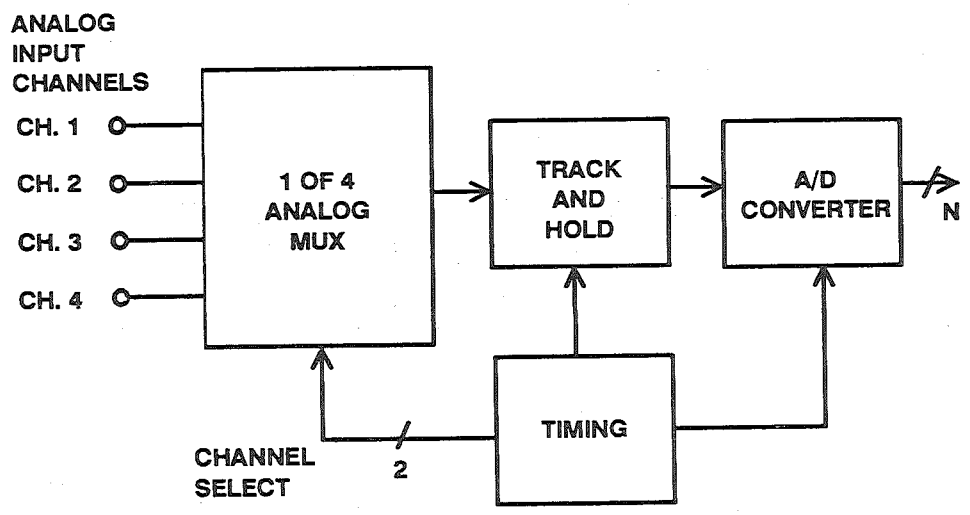


ADDING NOISE TO RECEIVER FOR INCREASED SPECTRAL RESOLUTION

Figure 1.41

MULTIPLEXING APPLICATIONS

Multiplexing many channels of analog data into a single A/D converter is quite common in low-speed data acquisition systems, and a classical block diagram is shown in Figure 1.42. A variation on this scheme, called "simultaneous sampling" is shown in Figure 1.43, where track-and-hold amplifiers are kept in the "hold" mode long enough for the multiplexer to sequence each channel into the A/D converter. These schemes have proven to offer a cost-effective solution to low speed multi-channel digitization, primarily because only one A/D converter (usually the most expensive part) is required.



TRADITIONAL DATA ACQUISITION SYSTEM USING ANALOG MULTIPLEXER

Figure 1.42

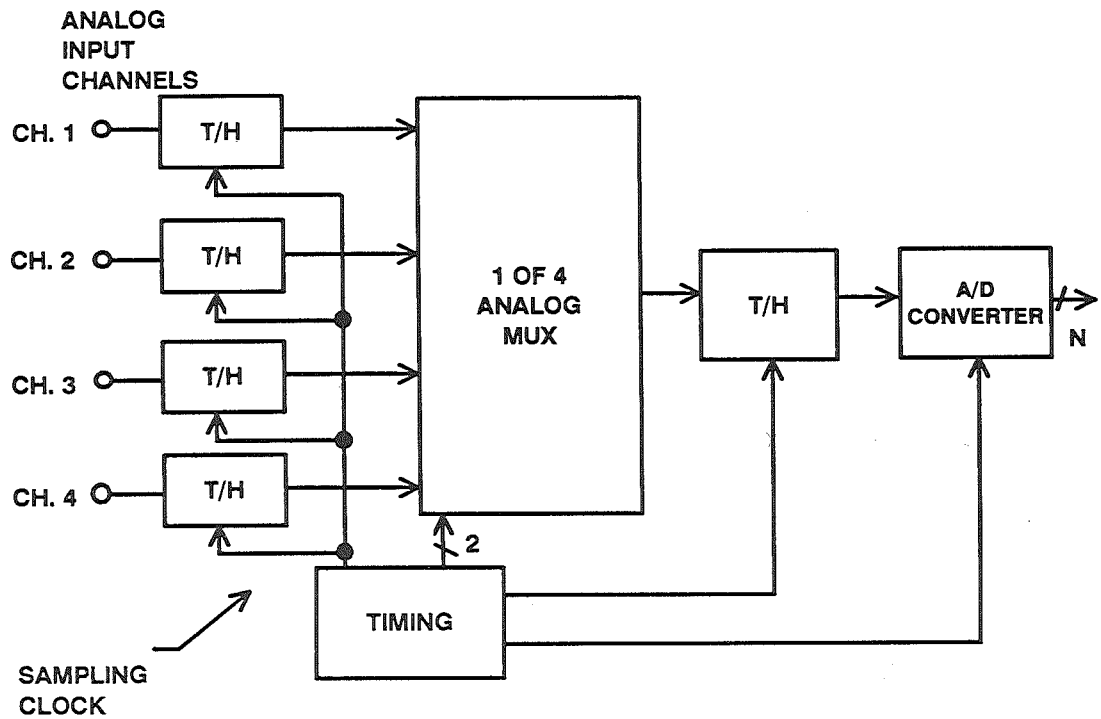


Figure 1.43

With the advent of high-speed A/D converters and faster analog multiplexer/switches, it is tempting to apply the same architecture to high-speed data acquisition systems. The user should be aware of several potential problems associated with using this approach at video speeds.

- There is no way to guarantee the per-channel dynamic performance (SNR, ENOB, etc.) based on the individual component specifications alone.
- Multiplexer settling time and A/D converter transient response become critical specifications. Remember that the multiplexer output can present a fullscale sample-to-sample change to the A/D converter analog input. If the multiplexer and A/D converters have not both settled to the required accuracy, DC channel-to-channel "crosstalk" will result.
- AC crosstalk between channels is much more of a problem when digitizing video speed signals.

In summary, the use of A/D converters on a per-channel basis is definitely the preferred solution for multichannel data acquisition systems at video speeds.

BEWARE OF ANALOG MULTIPLEXING AT VIDEO SPEEDS

- Individual Component Specs Don't Determine System Dynamic Performance
- Multiplexer Settling Time
- A/D Converter Transient Response
- DC Crosstalk Between Channels
- AC Crosstalk Between Channels

Figure 1.44

A/D CONVERTER
DYNAMIC SPECIFICATIONS AND TESTING

- DSP Testing
- Quantization Theory
- DFTs and FFTs
- Signal to Noise Ratio
- Harmonic Distortion
- Two Tone Intermodulation Distortion
- Spurious Free Dynamic Range
- Coherent Sampling
- Non-Coherent Sampling
- Windowing
- Sinewave Curve Fit
- Beat Frequency Tests
- Histogram Tests
- Noise Power Ratio
- Transient Response
- Overvoltage Recovery
- Aperture Time
- Composite Video Tests
- Error Rates

DSP TESTING OF A/D CONVERTERS

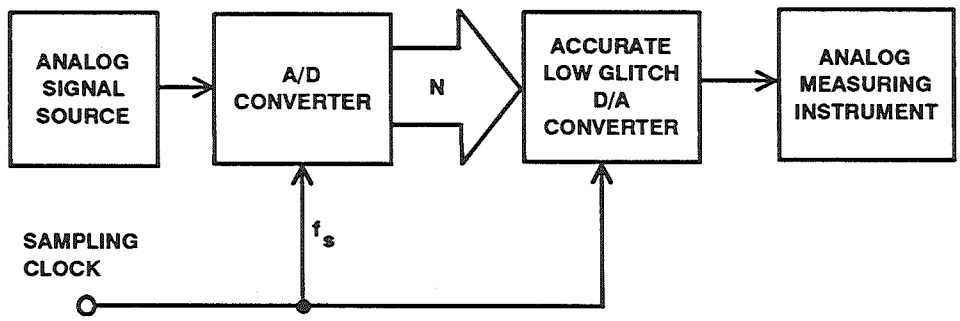
With the advent of "sampling" A/D converters, much emphasis has been placed on the dynamic performance of the converter when digitizing rapidly changing signals. The particular dynamic specifications of interest may very widely with the application as shown in Figure 1.45.

ANALOG-TO-DIGITAL DYNAMIC SPECIFICATIONS VS. APPLICATIONS

SPECIFICATION	APPLICATION
Effective number of bits (ENOB)	All
Signal-to-noise ratio (SNR)	Radar, communications, spectrum analysis
AC linearity	Radar, spectrum analysis
Noise power ratio (NPR)	Communications
Two-tone intermod distortion	Radar, spectrum analysis
Transient response	Transient analysis, radar, multiplexing
Overvoltage recovery	Radar
Aperture jitter	All
Differential gain and phase	Television
Error Rate	Radar, transient analysis, communications
Spurious free dynamic range (SFDR)	Communication receivers, spectrum analysis

Figure 1.45

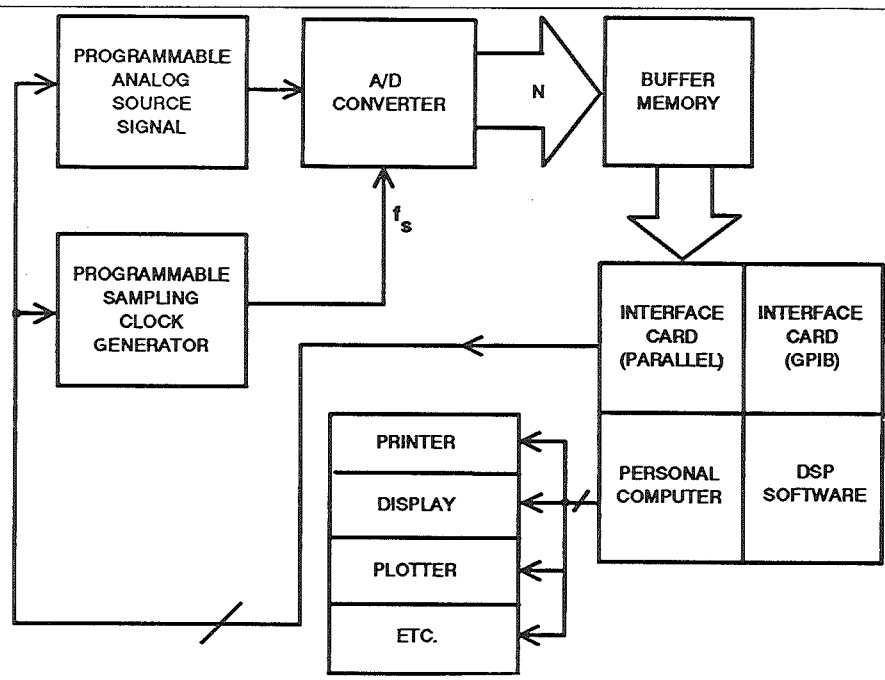
In the early days of video speed A/D converters, most dynamic testing was done in the analog realm using a high performance D/A converter to reconstruct the output of the A/D converter, as shown in Figure 1.46.



DYNAMIC A/D CONVERTER TESTING - THE OLD WAY

Figure 1.46

Today, it is possible to perform sophisticated DSP tests (such as FFTs, AC histograms, etc.), using test systems based upon user-friendly personal computers and standard software packages. The PC-based test system shown in Figure 1.47 is capable of performing a 1024-point FFT in less than one second.



A/D CONVERTER DSP TEST SYSTEM

Figure 1.47

Some key features of this system are shown in Figure 1.48. Specialized A/D converter DSP test systems are currently being offered by large ATE manufacturers such as Teradyne and LTX. These systems are well suited to large volume IC production applications, but are too costly for the end user. Other less expensive benchtop systems are now available from companies such as Tektronix and Hewlett-Packard which allow the end user to implement DSP testing of A/D converters not only at low cost but with a minimum of hardware and software development effort.

Manufacturers of video speed A/D converters such as Analog Devices are supplying product-specific evaluation boards to allow customers to easily interface the A/D converter with their DSP test system. The evaluation boards contain reference voltages, power supply decoupling, timing circuits, output registers, connectors, etc., in order to make performance evaluations as easy as possible. In addition, the evaluation boards usually have a matching D/A converter which is useful in determining the overall functionality of the A/D converter.

PC-BASED TEST SYSTEM

Personal Computer:	AT&T PC-6300
Co-Processor:	8087
Storage:	20 MByte Hard Disk Drive
Interface Card:	Metrobyte PIO-12, 24-bit Parallel
Operating Software:	Microsoft "Quickbasic"
FFT Software:	Micro Way "87 FFT"

Figure 1.48

QUANTIZATION THEORY

The RMS noise voltage measured within the Nyquist bandwidth for an ideal A/D converter is given by the familiar expression $q\sqrt{12}$, where q is the weight of the LSB. This value is also independent of input signal frequency and amplitude.

For a fullscale sinewave input, it can be shown that the theoretical RMS signal to quantification noise ratio is given by

$$SNR = 6.02N + 1.76dB + 10\log_{10}\left[\frac{f_s}{2f_a}\right]$$

where N = number of bits, f_s = sampling rate, and f_a = analog bandwidth. The third term in the above equation represents the increase in SNR due to oversampling, as previously discussed.
The classical deviation of these expressions can be found in the following reference:

W.R. Bennett, "Spectra of Quantized Signals"
BSTJ 27, pp. 446-472, July 1948.

Practical A/D converters exhibit errors which are due to static and dynamic nonlinearities. These dynamic errors increase as input slew-rates become greater. The actual SNR measurement will, therefore, be less than theoretical, and it is useful to calculate the effective number of bits (ENOB) by solving the above equation for N:

$$ENOB = \frac{SNR_{ACTUAL} - 1.76dB - 10\log_{10}\left[\frac{f_s}{2f_a}\right]}{6.02}$$

Note that when the "noise" is calculated using DFT techniques, it includes not only quantization noise but also the harmonics of the input sinewave. Harmonics which fall outside the Nyquist bandwidth are "aliased" back into the Nyquist bandwidth because of the sampling process.

Sinewaves are the most popular signals for evaluating A/D converter dynamic performance because of their ease of generation and mathematical analysis.

QUANTIZATION THEORY BASICS

- RMS Quantization Noise In Nyquist Bandwidth, $\frac{f_s}{2}$: $\frac{q}{\sqrt{12}}$

  q = LSB

- Fullscale Sinewave RMS Signal to RMS Noise in Bandwidth f_a:

  $$SNR = 6.02N + 1.76dB + 10\log_{10}\left[\frac{f_s}{2f_a}\right]$$

- Effective Number of Bits (ENOB):

  $$ENOB = \frac{SNR_{ACTUAL} - 1.76dB - 10_{log}\left[\frac{f_s}{2f_a}\right]}{6.02}$$

Figure 1.49

DISCRETE AND FAST FOURIER TRANSFORMS

The discrete fourier transform (DFT) in the digital domain is analagous to spectrum analysis in the analog domain. The DFT is a mathematical operation which is performed on a finite record of contiguous discrete time samples to produce an equivalent number of frequency samples. Both signal level, noise levels, and harmonic content can then be calculated from the DFT output. The fast fourier transform (FFT) is simply an algorithm which is used to greatly reduce the number of mathematical calculations (and thereby the processing time) required to obtain the DFT output spectrum. An excellent in-depth treatment of DFT and FFT theory can be found in any number of references, particularly

The FFT: Fundamentals and Concepts
Robert W. Ramirez, Prentice Hall, 1985.

Calculating the DFT

To calculate the DFT, a spectrally pure sinewave is applied to A/D converter, and a number of contiguous samples are stored in a buffer memory.
Unless the record time contains an integer number of cycles of the sinewave, time-weighting of the samples is required to reduce frequency sidelobes. Without weighting, the discontinuity produced by not having an integer number of cycles will cause the main lobe energy to "leak" into many other frequency bins making accurate spectral measurements impossible. A popular weighting function is called the "Hanning" function and is given by

$$W_nD_n = D_n \left[0.5 - 0.5\cos\left(\frac{2\pi n}{M}\right)\right]$$

where W_nD_n is the nth weighted data sample, D_n is the nth input data sample, and M is the total number of samples.

By using this weighting function, the leakage energy can be compressed into a small band of frequencies centered on the fundamental sinewave frequency. This eliminates contamination of a large portion of the overall spectrum.

Next the program must find the DFT of the sequence of weighted data samples for M/2 frequencies. To do that, the program must solve the following two equations for the Kth frequency:

$$A_K = \frac{1}{M}\sum_{n=1}^{M} W_nD_n\cos\left[\frac{2\pi k(n-1)}{M}\right]$$

$$B_K = \frac{1}{M}\sum_{n=1}^{M} W_nD_n\sin\left[\frac{2\pi k(n-1)}{M}\right]$$

where A_k and B_k represent the magnitudes of the cosine and sine parts of the Kth spectral line. The total magnitude of the Kth spectral line is then expressed by the equation:

$$MAG_K = \sqrt{A_K^2 + B_K^2}$$

The results yield M/2 components which are the frequency domain representation of the M time samples. The resolution or spacing between the spectral lines is given by the equation

$$\Delta f = \frac{f_s}{M}$$

where f_s is the sampling rate, and M is the total record length. The value, Δf, is often referred to as the "bin" size.

CALCULATING THE SIGNAL-TO-NOISE RATIO FROM THE FFT OUTPUT

Unless the sinewave frequency is chosen such that the record length M contains an integer number of cycles of the sinewave, the signal energy will be contained in several bins located around the fundamental. The RMS energy contained in the fundamental sinewave is computed by taking the square root of the sum of the squares of the appropriate number of samples (including the peak) located on either side of the peak. The number of samples to be included in this calculation can be determined by knowing the resolution of the A/D converter and the sidelobe roll-off characteristics of the particular weighting function being used.

The RMS energy in the remaining frequency bins represents the noise due to theoretical quantization, A/D harmonic distortion and excess noise, and FFT round-off error. This energy is calculated by taking the square root of the sum of the squares of the remaining samples (excluding the DC component).

The overall A/D converter SNR is then calculated by:

$$SNR = 20\log_{10}\left[\frac{\text{RMS SIGNAL LEVEL}}{\text{RMS NOISE LEVEL}}\right]$$

DFT FLOWCHART

- Determine Record Length, M
- Collect M Time Domain Samples at the Sampling Rate, f_S
- Multiply Each Time Sample by Appropriate Weighting or Windowing Function for Non-Coherent Sampling
- Calculate M/2 Spectral Magnitudes using DFT (FFT)
  Spacing Between Spectral Lines is $\Delta f = \frac{f_s}{M}$
- Analyze Frequency Spectrum
- Calculate RMS Signal Level
- Calculate RMS Noise Level, Neglecting DC Component
- Calculate RMS Harmonic Levels
- Calculate SNR, ENOB, Harmonic Distortion, THD, Etc.

Figure 1.50

CALCULATING HARMONIC DISTORTION FROM THE FFT OUTPUT

Harmonic distortion is calculated in a similar manner. The program "searches" the FFT frequency spectrum for the proper location of the desired harmonic (bearing in mind that harmonics above $f_s/2$ will be aliased into the baseband) and calculates the RMS energy in the harmonic. The RMS signal to RMS harmonic ratio is calculated as follows:

$$\text{HARMONIC DISTORTION} = 20\log_{10}\left[\frac{\text{RMS SIGNAL LEVEL}}{\text{RMS HARMONIC LEVEL}}\right]$$

Total harmonic distortion (THD) is often calculated by root-sum-squaring the first five harmonics of the fundamental sinewave and using the resulting number in the above formula for the RMS harmonic level.

TWO-TONE INTERMODULATION TESTS USING FFTs

It is often useful to measure the third-order intermodulation products for two sinewaves of frequency f_1 and f_2 which are applied to an A/D converter (see Figure 1.51).

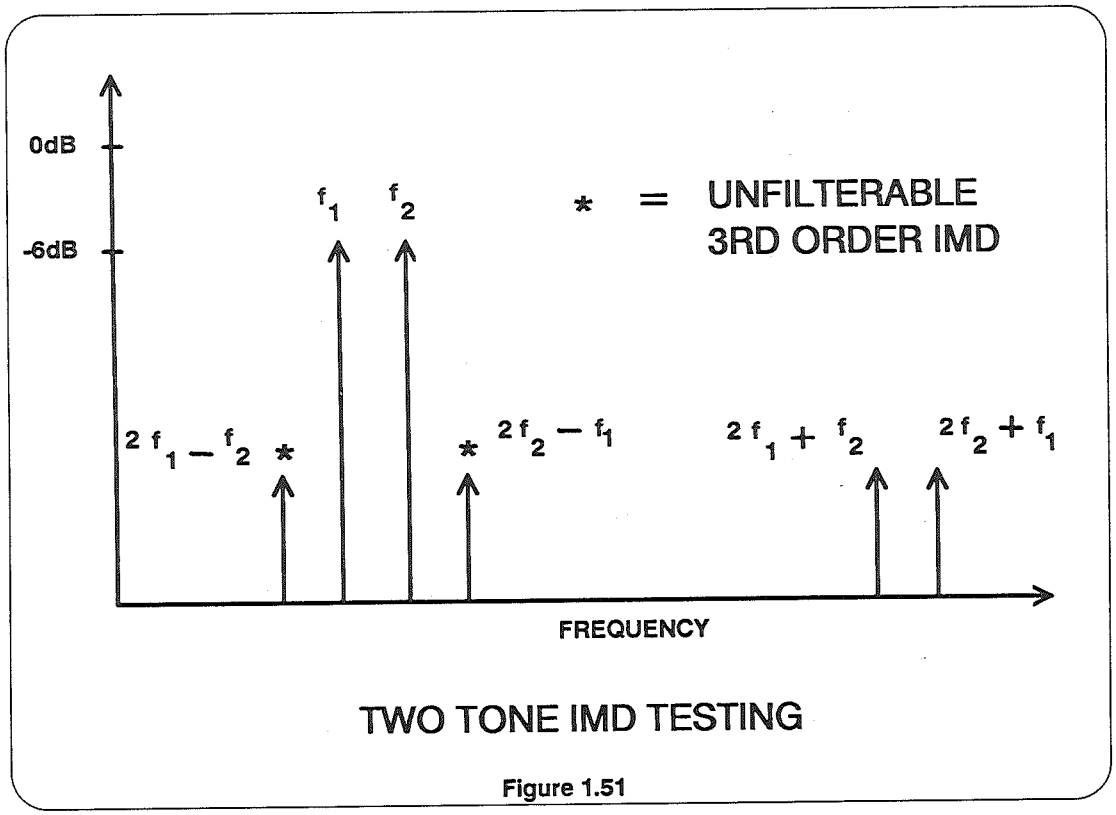


Figure 1.51

These products occur at frequencies:

$2f_1 + f_2$ $\quad$ $2f_2 + f_1$
$2f_1 - f_2$ $\quad$ $2f_2 - f_1$

Most IMD can be filtered out. However, if the two tones are of similar frequencies, the third order IMD ($2f_1$-f_2, $2f_2$-f_1) will be very close to the fundamental frequencies and cannot be easily filtered. The level of these products is of most concern in narrow bandwidth applications.

The amplitudes of the individual tones should be at least 6dB below the fullscale of the A/D converter to avoid distortion due to clipping.

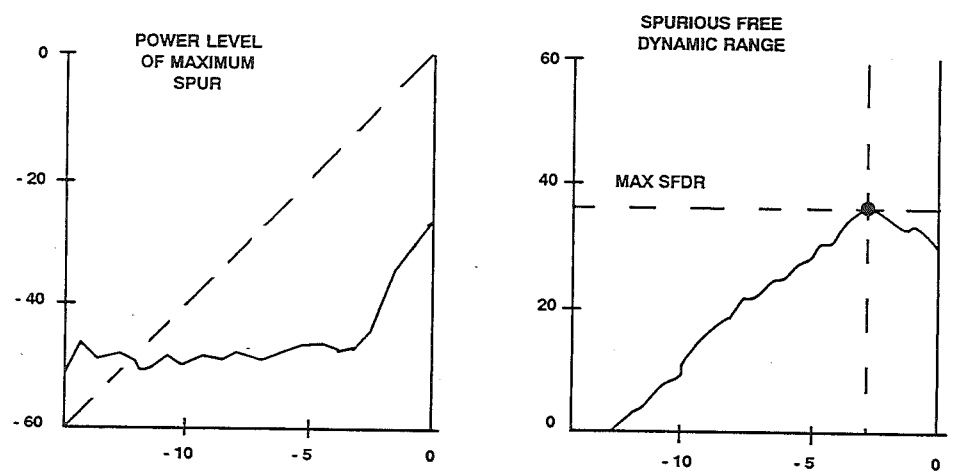
The frequency separation of the two tones should be consistent with the resolution of the FFT. As previously discussed, the spectral resolution of the FFT is a function of record length, M, coherence vs. non-coherence, and the properties of the particular windowing function chosen.

SPURIOUS FREE DYNAMIC RANGE (SFDR)

In receiver applications, it is often desired to know the maximum ratio achievable between the amplitude of a single tone input signal and the amplitude of its maximum spur.

For an ideal A/D converter, this would occur for a fullscale input sinusoid. In a practical A/D, however, spurious content is a function of slew-rate and, therefore, the maximum spurious free dynamic range (SFDR) for a given input frequency usually occurs at a level somewhat below fullscale.

Figure 1.52 shows a typical plot of the maximum spur level vs. input power level.



SPURIOUS FREE DYNAMIC RANGE (SFDR)

Figure 1.52

This corresponding spurious free dynamic range plot is also shown in Figure 1.52. This plot shows that the maximum SFDR occurs for an input signal which is approximately 3dB below fullscale.

The SFDR is slew-rate dependent, and, therefore, a function of the input frequency as well as the amplitude.

The data needed to generate these plots is readily available from the family of FFTs calculated for the different input amplitudes.

By knowing the input signal level that gives the highest SFDR at frequencies close to Nyquist, the gain of the system can be set to take maximum advantage of the A/D converter's spectral characteristics.

Determining The Proper FFT Record Length

The first consideration in choosing the number of time-domain samples required or record length, N, is the required spectral resolution, Δf. Also, in order to perform the FFT computations, N must be equal to an integer which is a power of two. The FFT spectral resolution, Δf, is given by

$$\Delta f = f_s/M$$

where f_s is the sampling rate. This can also be expressed as

$$\Delta f = \frac{1}{M \cdot \Delta t},$$

where Δt is the sampling period, $1/f_s$.

Typically, M is selected to be between 256 and 4096 depending upon the desired resolution and the amount of buffer memory available. (See section on the selection of a windowing function for further discussion on the effects of windowing on spectral leakage).

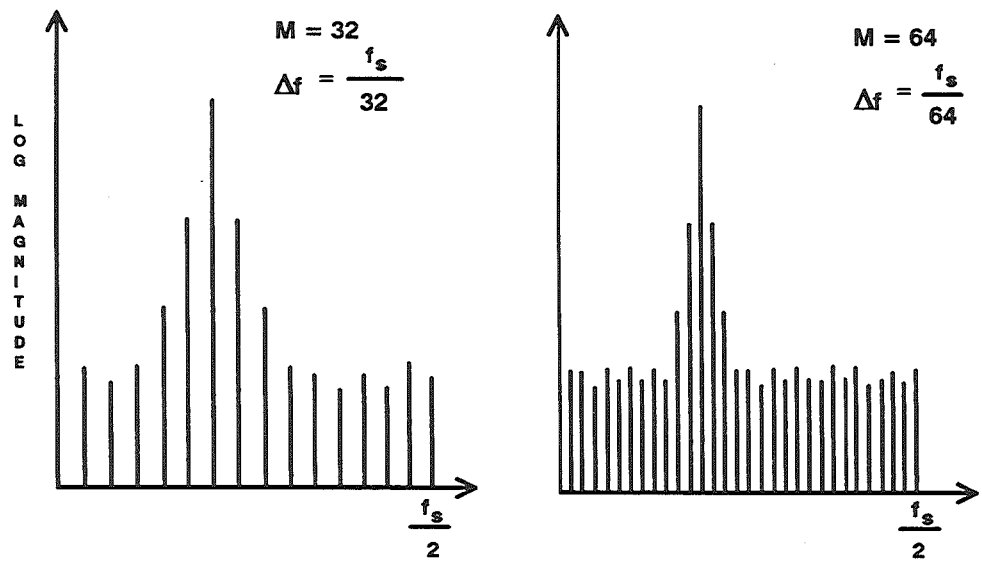
If windowing is used, the main lobe width and sidelobe rolloff (leakage) are measured in units of "bin width", f_s/M. This leakage can be "compressed" around the main lobe by using a larger record length, M, thereby leaving a larger percentage of the Nyquist spectrum uncontaminated, as shown in Figure 1.53.

For example, the Hanning weighting leakage is 10 bins around the fundamental for 68dB sidelobe suppression. If the record length is 256, then the smeared fundamental occupies 20/128, or 16% of the Nyquist bandwidth. For M = 1024, the percentage reduces to 20/512, or 4%.

Another consideration in determining the proper record length is the FFT noise floor itself. Assuming the DSP noise contribution (due to roundoff error) is negligible, the RMS signal to RMS noise level in a single frequency bin of width Δf is given by the expression

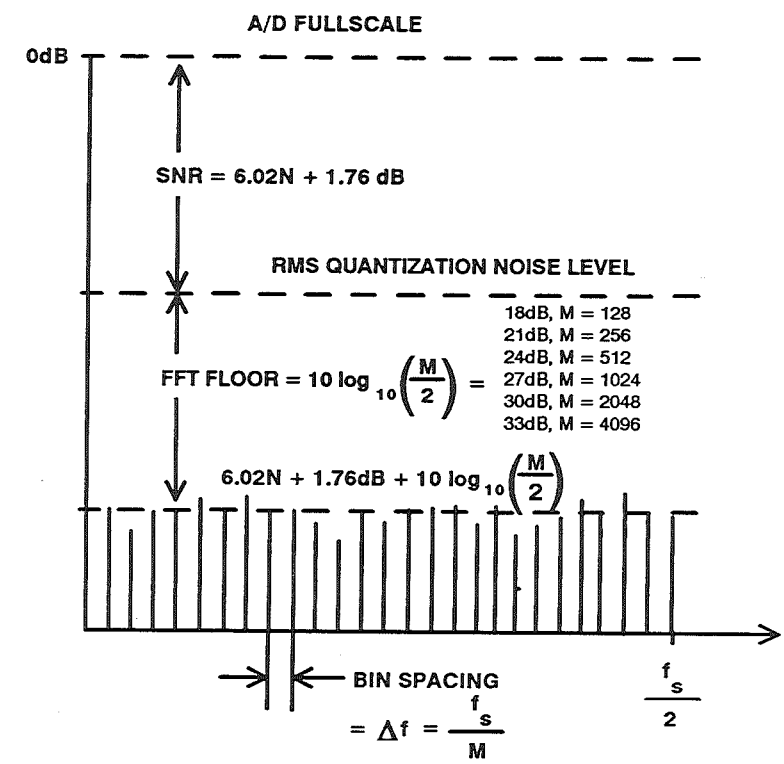
$$SNR_{FFT} = 6.02N + 1.76dB + 10\log_{10}\left(\frac{M}{2}\right)$$

This represents the FFT noise floor. The value should be chosen such that any spurious components which need to be resolved lie at least 10dB above this floor. This is illustrated in Figure 1.54.



EFFECT OF RECORD LENGTH ON LEAKAGE

Figure 1.53



FFT THEORETICAL NOISE FLOOR

Figure 1.54

DETERMINING FFT RECORD LENGTH

- Frequency Resolution

$$\Delta f = \frac{f_s}{M} = \text{"Bin Width"} = \frac{1}{M\,\Delta t}$$

- Effects of Weighting
- FFT Noise Floor

Figure 1.55

DETERMINING SINEWAVE INPUT FREQUENCY FOR COHERENT SAMPLING

As has been previously discussed, the use of coherent sampling eliminates leakage and the requirement for windowing. There are, however, some requirements placed on the choice of the sampling rate and the sinewave frequency.

First, the following ratio must be observed:

$$\frac{f_{IN}}{f_S} = \frac{M_C}{M} \quad \text{where}$$

M_C = Number of integer cycles of the sinewave during the record period.

M = Number of samples in record period.

f_{IN} = Input sinewave frequency.

f_S = Sampling rate.

For a whole number of cycles, M_C must be an integer. For non-repetitive data M_C should also be odd and prime - i.e., 1, 3, 5, 7, 11, 13, 17, etc. This insures that all samples during the record period will be unique.

When using coherent sampling, the ratio must be constant! This implies that the frequencies f_s and f_{in} be derived from sources that are locked to each other, such as two locked frequency synthesizers.

REQUIREMENTS FOR COHERENT SAMPLING

f_s = Sampling Rate

f_{IN} = Input Sinewave Frequency

M = Number of Samples in Record, Integer Power of 2

M_c = Number of Cycles of Sinewave During Record Period

$$\frac{f_{IN}}{f_s} = \frac{M_c}{M}$$

M_c:

- Integer, No Weighting Needed
- Odd
- Prime

> All Samples Unique

- 1, 3, 5, 7, 11, 13, 17, 19, 23, etc.

Figure 1.56

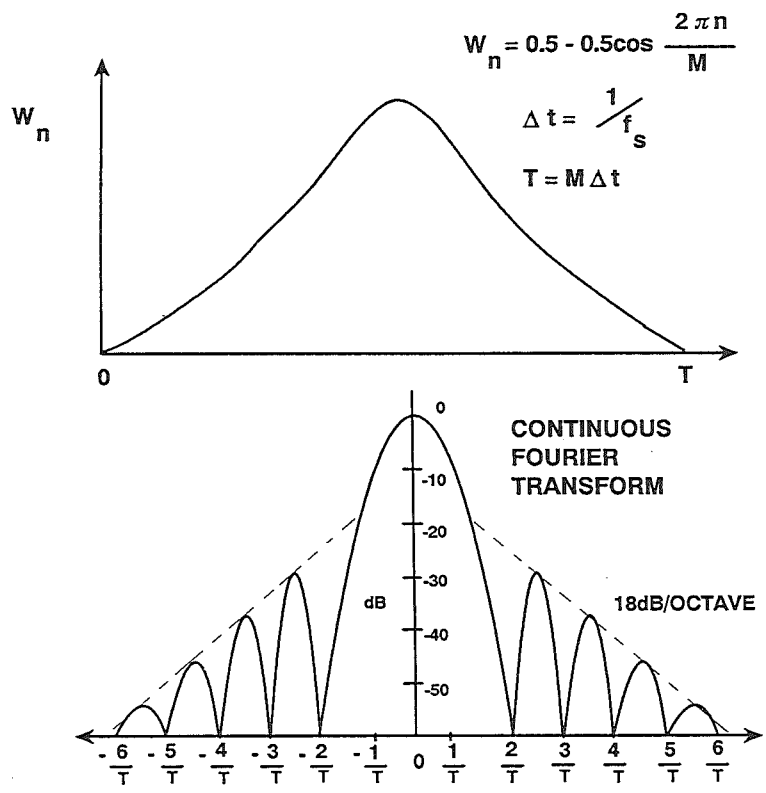
CHOOSING THE WINDOWING FUNCTION FOR NON-COHERENT SAMPLING

If non-coherent sampling is chosen, fewer restrictions apply to the selection of the input frequency. However, integer submultiples of the sampling frequency should be avoided to prevent masking out harmonics of the fundamental. It is also desirable to make the input frequency an odd multiple of the FFT frequency bin size to ensure this condition does not occur.

The selection of the weighting function is primarily a tradeoff between main-lobe spreading and sidelobe rolloff. The following reference is highly recommended for an in-depth look at windows:

> Fredric J. Harris, "On The Use of Windows for Harmonic Analysis with the Discrete Fourier Transform," IEEE Proceedings, Vol. 66, No. 1, Jan. 1978, pp. 51-83.

The effects of "windowing" a sinewave are shown in Figure 1.57 for the popular "Hanning" window.



TIME AND FREQUENCY REPRESENTATION OF HANNING WINDOW

Figure 1.57

This window has the following characteristics:

- Highest Sidelobe Level: 32dB below fundamental
- 6dB point of main lobe: 2 bins wide
- Location of highest sidelobe: 2.5 "bins" from fundamental (recall that the width of a "bin" = f_s /M).

  Sidelobe envelope rolloff: 18dB per octave, i.e., at 5 bins from the fundamental, the sidelobe envelope will be down 32 + 18 = 50dB from the fundamental.
- The following table is useful in determining the number of samples to be included in calculating the energy in the fundamental:

BINS FROM FUNDAMENTAL	SIDELOBE ATTENUATION
2.5	32dB
5.0	50dB
10.0	68dB
20.0	86dB

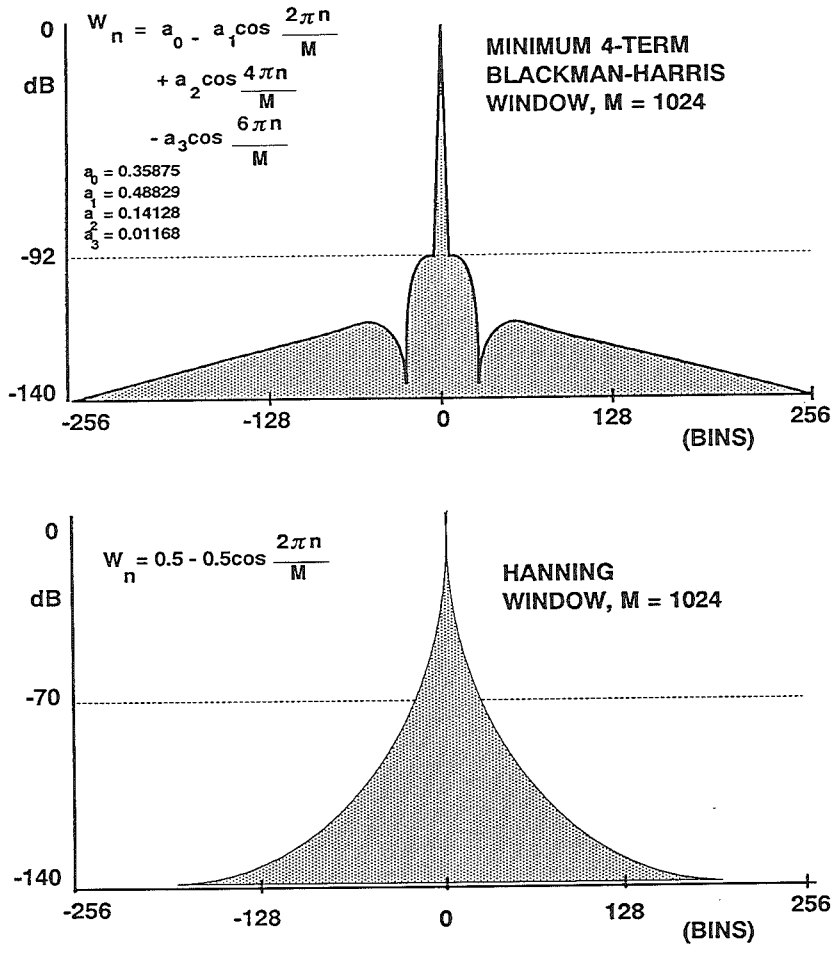
For a 12-bit A/D converter with a theoretical SNR of 74dB, it would, therefore, be appropriate to include 20 samples on either side of the fundamental in calculating the RMS signal energy (if Hanning weighting was used). It would also be appropriate to use a record length, M, of at least 1024 samples in order to achieve reasonable spectral resolution for harmonic analysis.

In order to make efficient use of the FFT processor, the weighting function coefficients should be calculated one time then stored in a lookup table. In this manner, more complex weighting functions can be used without any sacrifice in FFT processing speed.

If better spectral resolution is required, the minimum 4-term Blackman-Harris function is recommended. Figure 1.58 shows a spectral plot of this function and the Hanning function for reference (M = 1024). The equation for the minimum 4-term Blackman-Harris window is given by:

$$Wn = a_0 - a_1\cos\left(\frac{2\pi \cdot n}{M}\right) + a_2\cos\left(\frac{2\pi \cdot 2n}{M}\right) - a_3\cos\left(\frac{2\pi \cdot 3n}{M}\right)$$

where $a_0 = 0.35875$; $a_1 = 0.48829$; $a_2 = 0.14128$; $a_3 = 0.01168$



COMPARISON OF WEIGHTING FUNCTIONS

Figure 1.58

COHERENT VS. NON-COHERENT SAMPLING

The primary application of coherent sampling using FFTs is in the testing of A/D converters using sinewave inputs. If the proper ratios between f_{in} and f_s are observed, the need for windowing is eliminated, as previously discussed. This greatly increases the spectral resolution of the FFT and creates an ideal environment for critically evaluating the spectral response of the A/D converter. Great care must be taken, however, to insure the spectral purity and phase stability of f_{in} and f_s. The choice of the frequencies and their proper ratio is somewhat tedious, and high quality frequency synthesizers are needed (sometimes with additional filtering) in order to generate the phase locked signals.

In practical A/D converter applications, the precise frequency content of the signal being digitized is not usually known. If the A/D converter is being used in a spectral analysis application (as opposed to a transient recorder, for instance), a windowing function is required to process the signal, and the end user may be interested in the performance of the A/D using an identical or similar window.

In summary, both methods can be used effectively to evaluate the A/D converter performance if the proper ground rules are observed. Coherent sampling requires careful attention in the selection of the frequencies while non-coherent sampling requires careful attention and use of the windowing function. In either case, the purity of the sampling clock and the input sinewave are critical in order to achieve accurate and repeatable results. Coherent testing is more suited to a laboratory environment, while non-coherent testing is a better representation of the A/D converter performance in a "real world" application.

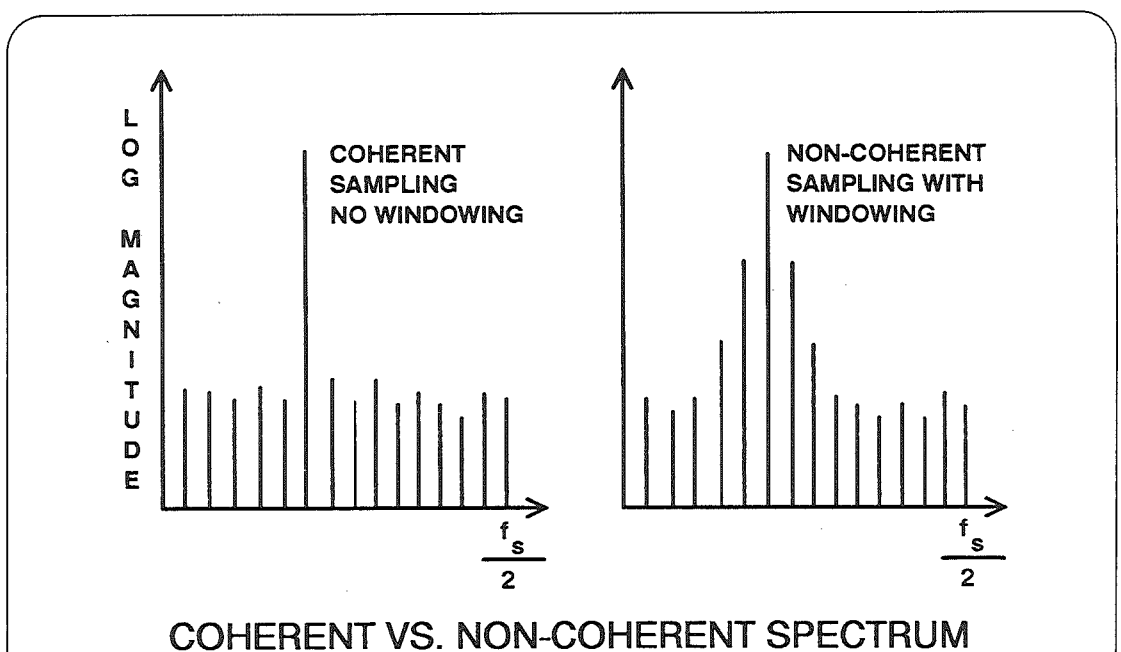


Figure 1.59

COHERENT SAMPLING	NON-COHERENT
• Increased Spectral Resolution, Repeatability	• Windowing Required
• Careful Selection of Frequencies, Ratio	• Real World Environment
• Phase/Frequency/Ratio Stability	
• Lab/Test Environment	

Figure 1.60

Verifying The FFT Accuracy

After selecting the record length, determining the weighting function (for non-coherent sampling), and writing the FFT program, the user should verify the overall accuracy of the program by inputting an ideal "N" bit sinewave. The SNR should be 6.02N + 1.76dB, and the spurious spectral components should be at least 10dB below those expected from the A/D converter. The ideal N-bit sinewave can be easily generated in BASIC software by using the INTEGER (INT) function to truncate the value to the proper resolution.

For instance, if the input signal whose frequency is f_{in} is given by

$$v(n) = V_o \sin\left(\frac{2\pi n f_{in}}{f_s}\right)$$

where n is the nth time sample for an ideal A/D with infinite resolution, then the corresponding quantized value can be calculated from

$$v_q(n) = \text{INT}\left[\frac{V_o \sin\left(\frac{2\pi n f_{in}}{f_s}\right)}{q}\right]$$

where $q = \frac{2V_o}{2^N}$

Substituting

$$v_q(n) = \text{INT}\left[2^{N-1} \cdot \sin\left(\frac{2\pi n f_{in}}{f_s}\right)\right]$$

The "INT" function simply truncates the fractional portion of v(n).

The overall dynamic range of the FFT can be checked by calculating the SNR for increasing values of N and observing the point at which the SNR no longer increases by 6.02dB per bit.

In the limit, the sinewave inputted to the weighting function and the FFT can be made ideal ($N \rightarrow \infty$), and the true noise floor of the FFT itself can be analyzed. This method allows the characteristics of the weighting function to also be examined in detail.

IDEAL N-BIT SINEWAVE GENERATOR

$$v(n) = V_o \sin\left(\frac{2\pi n f_{in}}{f_s}\right) \qquad \text{IDEAL}$$

$$v_q(n) = \text{INT}\left[\frac{V_o \sin\left(\frac{2\pi n f_{in}}{f_s}\right)}{q}\right] \qquad \text{IDEAL N-BITS}$$

$$q = \frac{2V_o}{2^N} = 1\text{LSB}$$

$$v_q(n) = \text{INT}\left[2^{N-1} \sin\left(\frac{2\pi n f_{in}}{f_s}\right)\right]$$

f_{in} = Input Frequency
f_s = Sampling Rate
n = nth Time Sample

Figure 1.61

SINEWAVE CURVE FITTING

This test is a global description of the dynamic performance of an A/D converter. A fullscale sinewave is digitized by the A/D converter and stored in memory (typically, 1024 samples is sufficient). The sinewave frequency is chosen to be non-subharmonically related to the sampling rate, much as in the case of non-coherent FFT testing.

The software then calculates the "best-fit" ideal N-bit sinewave to fit the data points. The sinewave amplitude, offset, frequency, and phase are chosen to minimize the RMS error between the actual sinewave and the ideal sinewave. A detailed description of the algorithms used is given in the following references:

HP Journal, November 1982, Vol 33, No. 11, pp. 24-25.

HP Journal, February 1988, Vol. 39, No. 1, p. 48.

It should be noted that the curve-fit algorithm is much simpler if the precise sinewave frequency is known. Also, the probability of the algorithm converging is much higher.

After the software computes the RMS error, Q_A, between the ideal sinewave and the actual sinewave, the ENOB can be calculated from the following equation:

$$ENOB = N - \log_2\left(\frac{Q_A}{Q_T}\right)$$

where Q_T is the theoretical RMS quantization error, $q/\sqrt{12}$.

This measurement includes errors due to differential non-linearity, integral non-linearity, missing codes, aperture jitter, noise, etc., as well as quantization noise.

The value for ENOB calculated using the sinewave curvefit method correlates well with the value obtained from the fullscale FFT SNR measurement,

$$ENOB = \frac{SNR_{ACTUAL} - 1.76dB}{6.02}$$

If the input signal is less than fullscale, a correction factor must be added to the latter equation in order to achieve correlation between the two methods:

$$ENOB = \frac{SNR_{ACTUAL} - 1.76dB + \begin{matrix}\text{LEVEL OF}\\ \text{SIGNAL}\\ \text{BELOW}\\ \text{FULLSCALE}\end{matrix}}{6.02}$$

CALCULATING ENOB USING SINEWAVE CURVE FITTING

Q_A = Actual RMS Error from Best Fit Sinewave

Q_T = Theoretical N-Bit RMS Error From Best Fit Sinewave = $q/\sqrt{12}$

$$ENOB = N - \log_2 \left(\frac{Q_A}{Q_T} \right)$$

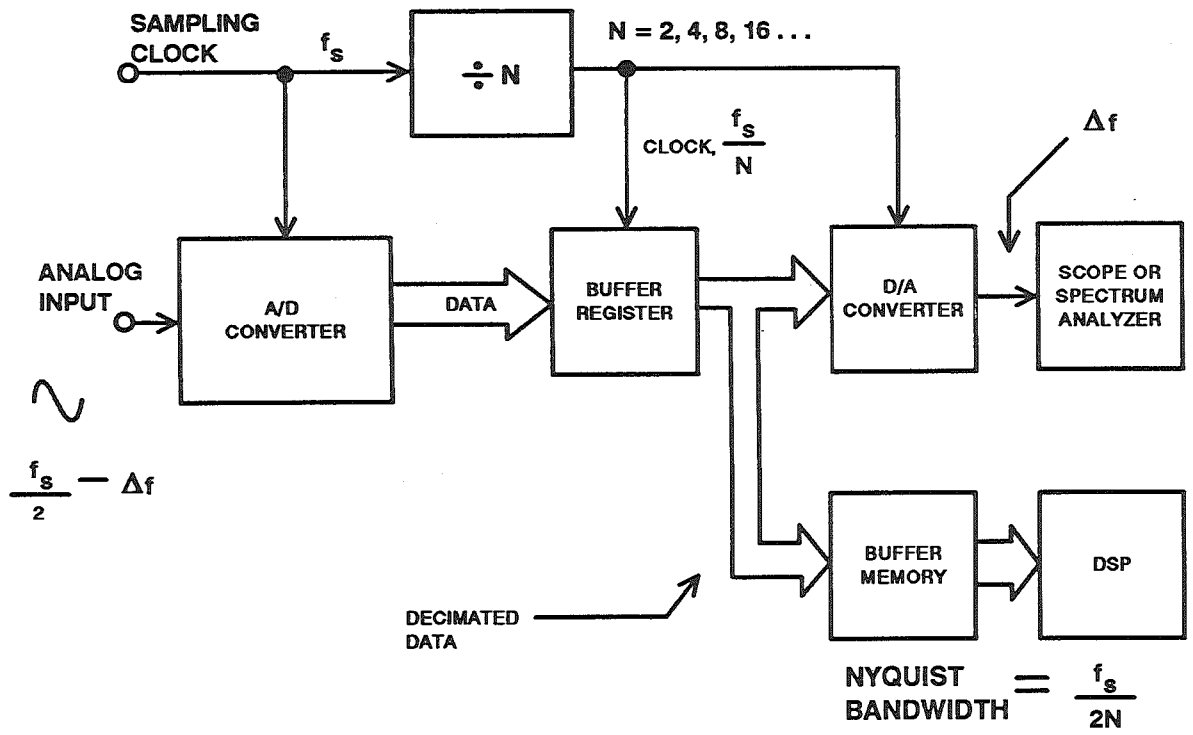
Correlates To

$$ENOB = \frac{SNR_{ACTUAL} - 1.76dB + \text{Level of Signal Below FS}}{6.02}$$

Figure 1.62

TESTING A/D CONVERTER DYNAMIC PERFORMANCE USING THE "BEAT FREQUENCY" METHOD

A useful method for reducing the effects of the D/A converter in making gross back-to-back measurements on an A/D converter is shown in Figure 1.63. Here, the analog input sinewave is slightly lower in frequency than one-half the sampling frequency. The registers driving the D/A converter are updated at an even submultiple of the sampling rate, f_s/N, where N is a power of 2 (not the A/D resolution). The resulting signal from the D/A converter is a low frequency sinewave having a frequency equal to the difference between one-half the sampling rate and the analog input frequency.



BEAT FREQUENCY TEST

Figure 1.63

In this method, the A/D converter is being stressed with a near-Nyquist signal and is operating at its maximum sampling rate. The D/A converter is being clocked at a much lower decimated rate, f_s/N, thereby reducing the effects of glitches and other dynamic errors. Signal-to-noise measurements can be made over the Nyquist bandwidth $f_s/2N$. The low frequency "beat" can be examined easily on an oscilloscope for missing codes and other non-linearities. A standard low frequency spectrum analyzer can measure the harmonic content of the "beat" frequency.

The harmonics of the low frequency "beat" are directly related to the harmonics of the actual A/D converter analog input frequency.

In practice, a "beat" frequency of a few hundred kilohertz works well. Both the analog input sinewave and the sampling frequency should be derived from the frequency synthesizers or crystal oscillators to prevent "smearing" of the low frequency "beat" signal.

The beat frequency test is also effective in measuring the A/D converter's performance for input signals which are near the sampling frequency. The A/D performance under these conditions is of particular interest in radar I and Q systems, and in IF-to-Digital applications. In this test, the analog input frequency to the A/D is made slightly less than the sampling rate, f_s. In this case, a low frequency "beat" would be generated even if the D/A converter were updated at the sampling rate. It is still desirable, however, to update the D/A converter at f_s/N to reduce the effects of D/A dynamic errors on the measurements.

Evaluation boards which are designed to allow the user to evaluate high-speed flash converters usually have on-board D/A converters to make "coarse" performance measurements easy. The addition of output register clock frequency "decimation" circuitry on the board greatly facilitates beat frequency tests.

NON-LINEARITY TESTING USING HISTOGRAMS

In order to make a histogram analysis of an A/D converter, a known periodic input signal is digitized at a rate which is asynchronous relative to the input signal. After a statistically significant number of samples (usually at least 100,000) have been taken, the relative number of occurrences of each digital code (code density) is determined. This data is then normalized based upon the input signal, and the results are analyzed for linearity errors.

For an ideal A/D converter with a full scale triangular wave input, an equal number of codes should occur in each bin. The number of counts in the nth bin, H(n) divided by the total number of samples taken, M, is the width of the bin as a fraction of full scale. The ratio of the actual bin width to the ideal bin width P(n) is the differential linearity and should be unity. Subtracting one LSB gives the differential non-linearity in LSBs.

$$DNL(n) = \frac{H(n)}{M \cdot P(n)} - 1.$$

Integral non-linearity can be determined by compiling a cumulative histogram. The cumulative bin widths are the transition levels. The histogram approach is more often used, however, in evaluating differential non-linearity, since the cumulative effects of errors can make the integral non-linearity measurements somewhat inaccurate.

Since high speed triangles are difficult to generate to the required level of accuracy, sinewave inputs are usually selected for histogram DNL measurements. Because all codes are not equally probable with a sinewave input, the histogram data must be normalized using the probability density function for a sinewave as shown in Figure 1.65.

In order to obtain accurate results, a large number of samples must be taken. For example, to determine the DNL for an 8-bit converter to within 0.1 bit with 99 percent confidence, 268,000 samples are needed. It should be noted that these samples can be "counted" in hardware rather easily, thereby speeding up the software processing time. For high speed sampling, the output data can be decimated to rates which are compatible with slower speed memory.

An excellent treatment of this subject can be found in the following:

Joey Doernberg, Hae-Seung Lee, David A. Hodges, "Full Speed Testing of A/D Converters", **IEEE Journal of Solid State Circuits**, Vol. SC-19, No. 6, December 1984, pp. 820-827.

HP Product Note 5180A-2, pp. 3-9.

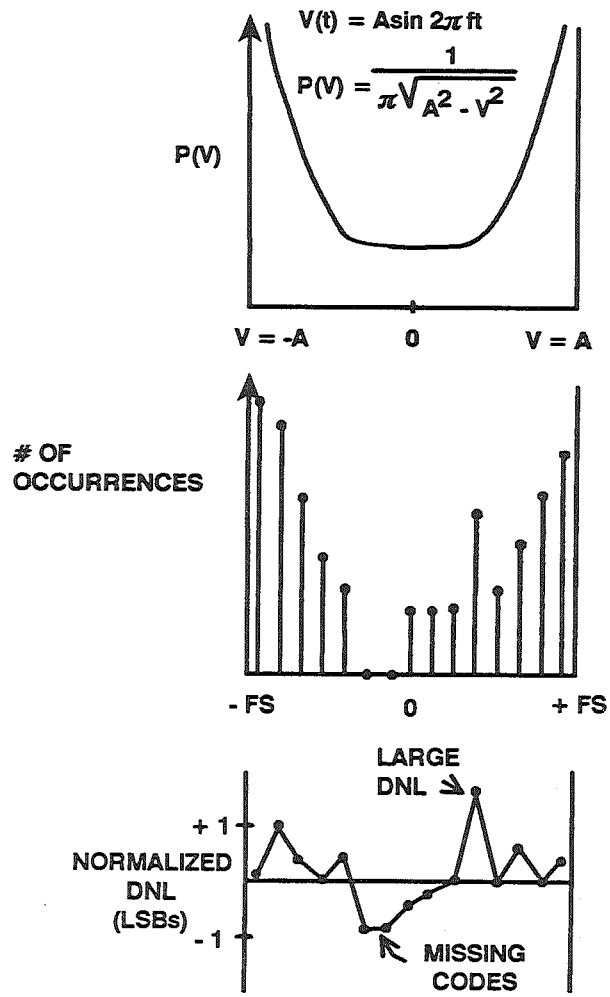
DNL HISTOGRAM USING TRIANGLE INPUT SIGNAL

$$DNL\ (Code\ n) = \frac{\#\ of\ times\ Code\ n\ Occurs}{M \cdot Probability\ of\ Code\ n} - 1$$

M = Total Number of Samples Taken.

$$For\ Triangle,\ Probability\ of\ Code\ n = \frac{1}{2^N}$$

Figure 1.64

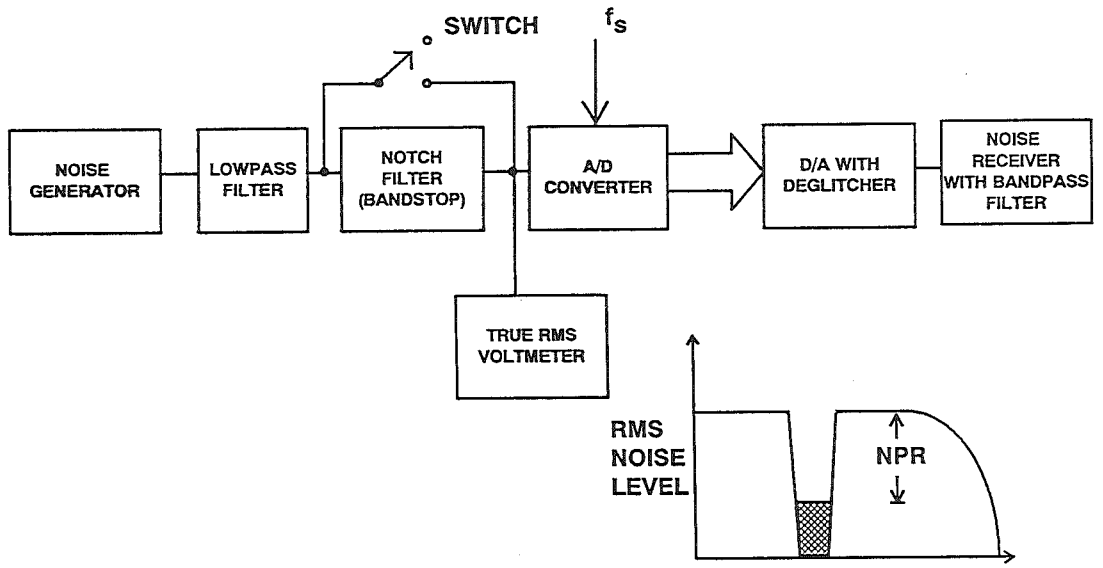


DNL HISTOGRAM USING SINEWAVE INPUT SIGNAL

Figure 1.65

NOISE POWER RATIO (NPR) TESTING

Noise power ratio testing has been used extensively to measure the transmission characteristics of Frequency Division Multiplexed (FDM) communications links. In a typical FDM system, 4kHz wide voice channels are "stacked" in frequency for transmission over coaxial, microwave, or satellite equipment. At the receiving end, the FDM data is demultiplexed and returned to 4kHz individual baseband channels. In an FDM system having more than approximately 100 channels, the FDM signal can be approximated by Gaussian noise with the appropriate bandwidth. The test setup of Figure 1.66 shows how an individual 4kHz channel can be measured for "quietness" using a narrow-band notch (bandstop) filter and a special tuned receiver which measures the noise power inside the 4kHz "notch".



NOISE POWER RATIO TEST SETUP

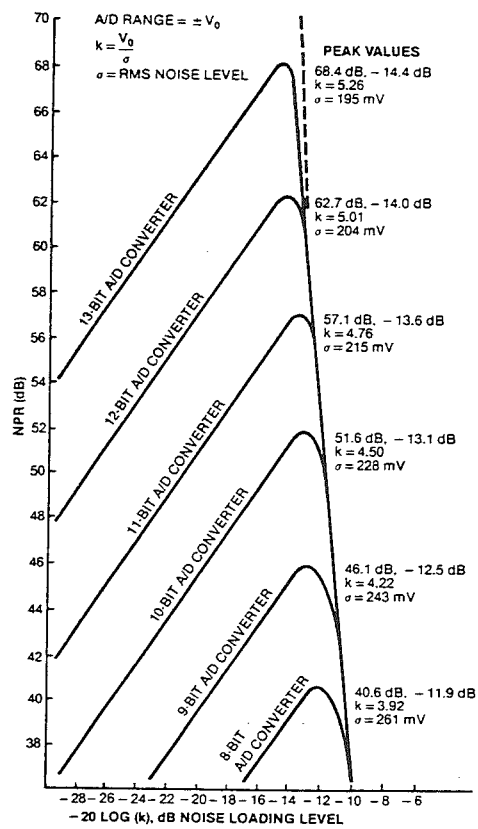
Figure 1.66

Noise Power Ratio (NPR) measurements are straightforward. With the notch filter out, the rms noise power of the signal inside the notch is measured by the receiver. The notch filter is then switched in, and the residual noise inside the slot is measured. The ratio of the two readings expressed in dB is the NPR. Several slot frequencies across the noise bandwidth (low, midband, and high) are tested to characterize the system adequately.

Noise Power Ratio is usually plotted on an NPR curve. The NPR is plotted as a function of rms noise level referred to the peak range of the system. For very low

noise loading levels, the undesired noise (in non-digital systems) is primarily thermal noise and is independent of the input noise level. Over this region of the curve, a 1dB increase in noise loading level causes a 1dB increase in NPR. As the noise loading level is increased, the amplifiers in the system begin to overload, creating intermodulation products which cause the noise floor of the system to increase. As the input noise increases further, the effects of "overload" noise predominate, and the NPR is reduced dramatically. FDM systems are usually operated at a noise loading level a few dB below the point of maximum NPR.

In a digital system containing an A/D converter, the noise within the slot is primarily quantizing noise when low values of noise input signals are applied. The NPR curve is linear in this region. As the noise input level increases, "clipping" noise caused by the hard-limiting action of the A/D converter begins to predominate. A set of theoretical NPR curves for A/D converters of various resolutions is shown in Figure 1.67.



THEORETICAL NPR CURVES FOR DIGITAL SYSTEMS

Figure 1.67

In a practical A/D converter, any dc or ac non-linearities will cause a departure from the theoretical NPR. Although the peak value of NPR occurs at a fairly low input noise level (RMS noise $\pm V_o/4$ where $\pm V_o$ is the range of the A/D converter), the broadband nature of the noise signal stresses the A/D converter, and the test provides a good indication of its dynamic performance.

Theoretically, NPR readings should not be dependent on any particular slot frequency. However, because of increased non-linearities for the higher input frequencies, NPR readings in the higher slots tend to give lower readings.

The following references are recommended for further study on NPR:

G.A. Gray and G.W. Zeoli, "Quantization and Saturation Noise Due to Analog-to-Digital Conversion," IEEE Trans. Aerospace and Electronic Systems, pp. 222-223, Jan. 1971.

M.J. Tant, "The White Noise Book", Marconi Instruments, July 1974.

NPR Testing Using DSP Techniques

Making NPR measurements on an A/D converter using FFT analysis techniques as described in the previous SNR section presents a real challenge. Consider the case where the record length is 1024 and the sampling rate is 20MHz. The FFT of 1024 contiguous time samples would place a spectral component every 19.53 kHz (20MHz/1024). Obviously, since the notch filter slot width is approximately 4kHz, the probability of a spectral component falling within the notch is very low.

To achieve reasonable data stability in the FFT NPR analysis, a number of samples must fall within the notch. If ten samples were required within the 4kHz notch, the resolution of the FFT would need to be 400Hz, necessitating a record length of 50,000 for a sampling rate of 20MHz. To avoid the need for an extremely large buffer memory (and hence more demands on the FFT processor), the notch filter can be widened to provide more samples within the notch. For 20MHz sampling and a 1024 word buffer memory, a notch filter having a width of 200kHz will provide ten frequency bins inside the notch. Even under these conditions, however, the NPR calculations for several records should be averaged to provide reasonable data stability.

DIGITAL NPR TESTING CONSIDERATIONS

- M = 1024 = Record Length
- f_s = 20.48 MHz
- $\Delta f = \frac{f_s}{M}$ = 20kHz = FFT Bin Width
- For 10 Samples in "Notch",
  Make Notch Filter Width = 200kHz
- Average Several Runs

Figure 1.68

A/D CONVERTER TRANSIENT RESPONSE TESTING

The response of an A/D converter to a transient input such as a square wave is often critical in radar applications. The major difficulty in implementing this test is obtaining a pulse which is known to be "flat" to the desired accuracy consistent with the A/D converter resolution.

A test setup for measuring the transient response of an A/D converter is shown in Figure 1.69 along with a recommended flat pulse generator. If the simple flat pulse generator is mounted as close as possible to the analog input of the A/D converter, the input applied to the A/D converter can be assumed to be flat to at least 10-bit accuracy a few nanoseconds after the schottkey diodes have been reverse biased. The programmable delay can be used to vary the phase of the sampling clock with respect to the flat pulse.

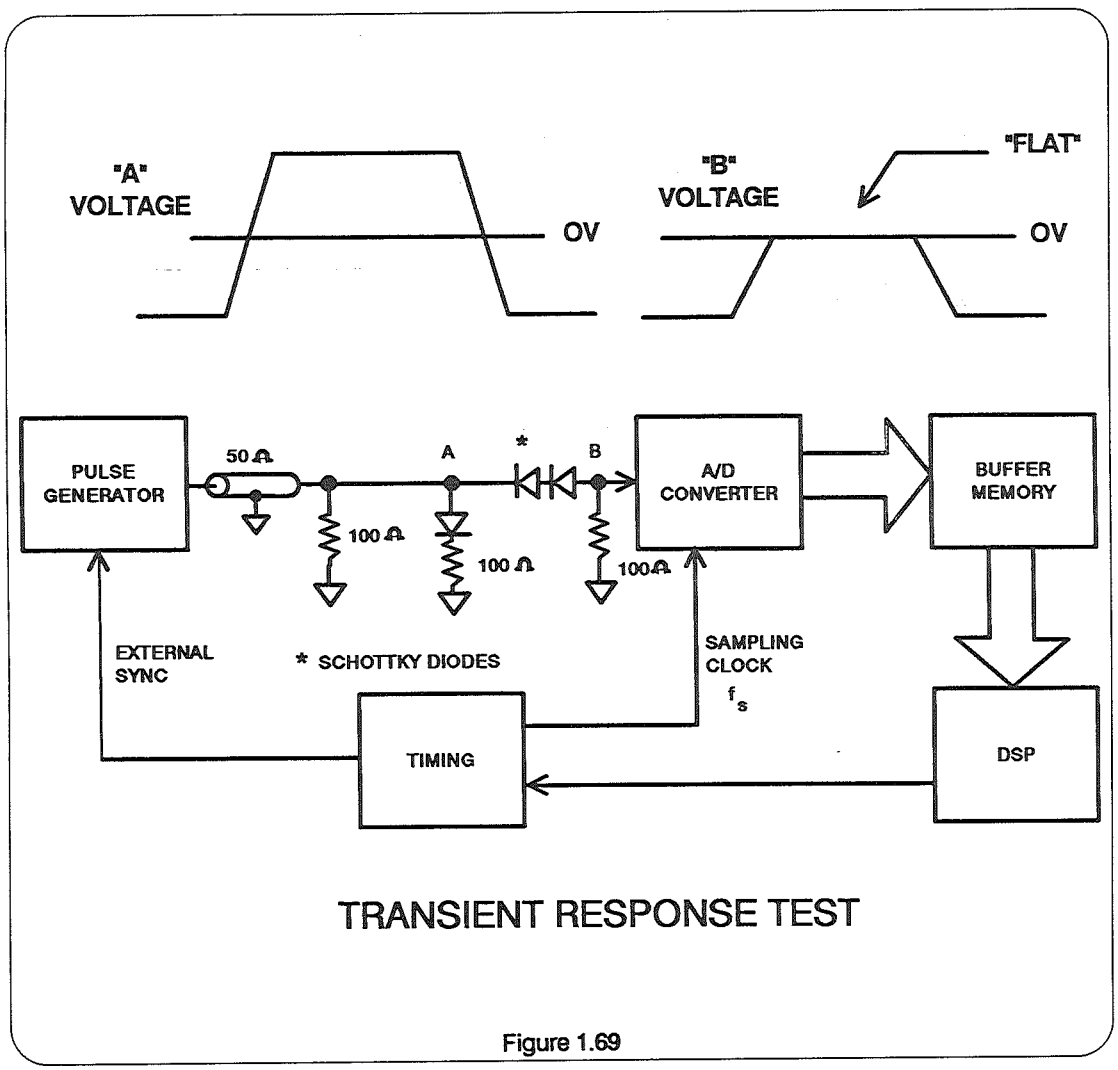


Figure 1.69

The time required for the A/D converter output to settle within 1 LSB of the final value can be measured easily using the delay generator in conjunction with the buffer memory and the computer. The effective aperture delay time must be considered when making the transient response measurement.

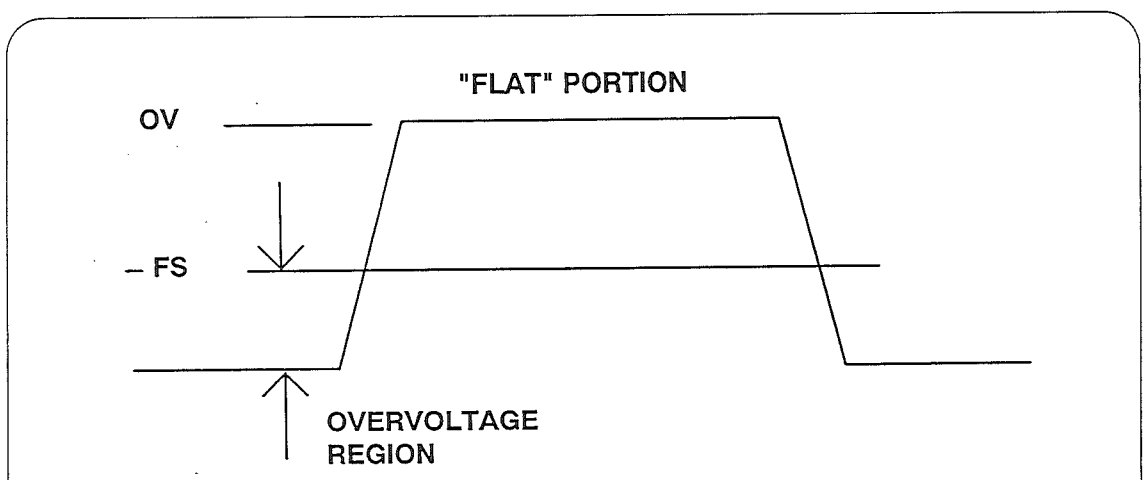
Further details regarding the generation of flat pulses can be found in:

"A Programmable Precision Voltage-Step Generator for Testing Waveform Recorders" IEEE Transactions on Instrumentation and Measurement, Vol. IM-33, No. 3, Sept. 1984, pp.

"Reference Waveforms Flat Pulse Generator," IEEE Transactions on Instrumentation and Measurement, Vol. IM-32, No. 1, March 1983, pp. 27-32.

A/D CONVERTER OVERVOLTAGE RECOVERY TESTING

The time required for an A/D converter to recover from a signal which falls outside the converter's range can be measured in a manner similar to the transient response measurement. Overvoltage recovery time is defined as that amount of time required for the A/D converter to achieve a specified amount of accuracy when measured from the time the overvoltage signal re-enters the converter's range, as shown in Figure 1.70. The amount of overvoltage is generally specified as a percentage of the A/D converter's range. For a converter with a 2-volt input range, 50% overvoltage would correspond to 1 volt above or below the nominal 2-volt input range.



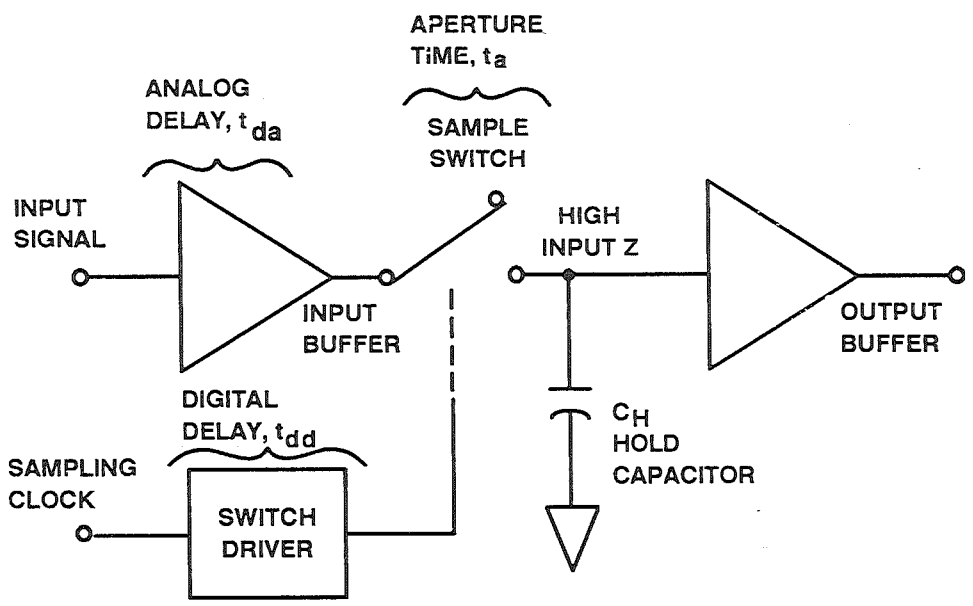
OVERVOLTAGE RECOVERY WAVEFORM

Figure 1.70

The same test setup used for measuring transient response (Figure 1.69) can be used to measure overvoltage recovery time. The "starting point" of the flat pulse is made to correspond to the desired overvoltage condition. The actual overvoltage recovery time is referenced to the time the input signal re-enters the A/D converter input range. As in the transient response test, the effective aperture delay time must be considered when making this measurement.

APERTURE TIME AND APERTURE JITTER

The aperture time and aperture jitter specifications on video A/D converters have been probably the most misunderstood and misused specifications in the entire field. The original concept of aperture time centered around the classic sample and hold circuit shown in Figure 1.71. In an ideal sample and hold, says the theory, the switch has zero resistance when closed, and opens instantly on receipt of a sampling clock. In practice, however, the sampling switch transits from a low to high resistance over some finite time interval. According to the



IDEALIZED SAMPLE-AND-HOLD CIRCUIT

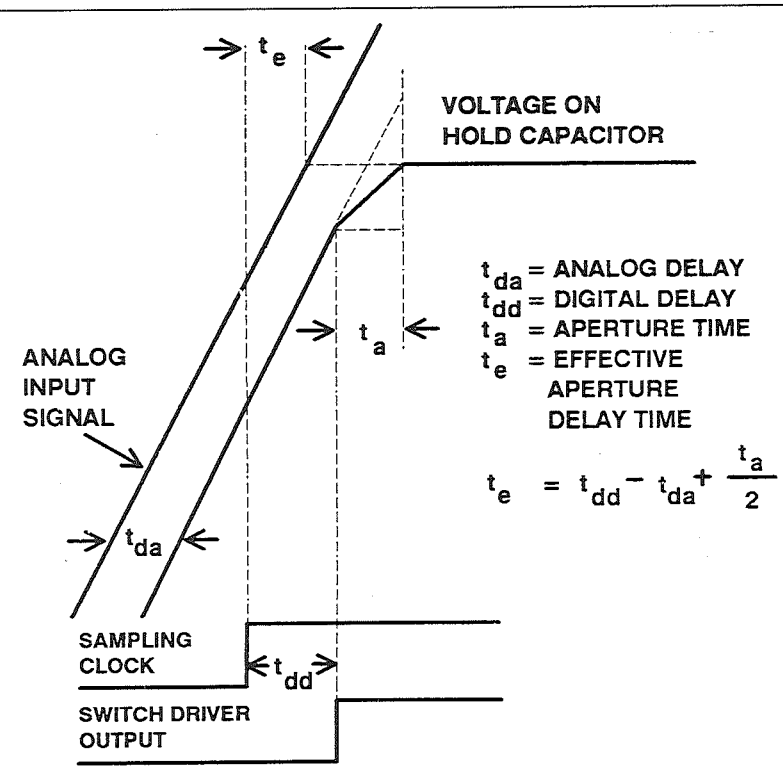
Figure 1.71

argument, an error occurs because the input signal tends to be averaged over the finite time interval required for opening the switch. The sampled voltage, therefore - the argument continues - does not exactly correspond to the voltage at the instant the switch starts to open. The time required to open the switch was referred to as aperture time. The classic formula then arose,

$$E_a = t_a \frac{dv}{dt}$$

where E_a is the aperture error, t_a is the aperture time, and dV/dt is the rate at which the input signal changes.

A simple first-order analysis which neglects non-linear effects shows that no real error exists for such a switch. As long as the switch opens in a repeatable fashion, there exists an effective sampling point in time which will cause an ideal sample and hold ($t_{dd} = t_{da} = t_a = 0$) to produce the same held voltage (see Figure 1.72). The difference between this effective sampling point and the leading



SAMPLE-AND-HOLD WAVEFORMS

Figure 1.72

edge of the actual sampling clock is a fixed delay and does not constitute an error. This delay is appropriately called effective aperture delay time, or the interval of time between the leading edge of the sampling clock and the instant when the input signal was equal to the held value. This specification is important because it helps the A/D converter user to know when to apply the sampling clock with respect to the input signal timing. The variation or tolerance placed on this value from part to part is important in simultaneous sampling applications or other applications where the A/D converters are required to track each other when processing dynamic signals. Adjustable delays in the sampling clock signals to match the effective aperture delay times of several A/D converters may be required in exacting applications such as I and Q radar receivers. Effective aperture delay time tracking over temperature may also be a consideration.

True aperture errors, however, do result from variable sample-to-sample time delays. These errors generally emanate from several sources. In a practical A/D, the sampling clock is often phase-modulated by some unwanted source; the source can be wideband random noise, power-line noise, or digital noise due to poor grounding techniques. The resulting error can be expressed in terms of an rms time jitter, and can be properly referred to as aperture jitter. The corresponding rms voltage error caused by rms aperture jitter qualifies as a valid aperture error. Phase jitter on the input sinewave can produce the same effect as jitter on the sampling clock.

The aperture jitter specification on an A/D converter is sometimes interpreted as a measure of the converter's ability to digitize rapidly changing input signals accurately. While the aperture jitter specification is important, it does not tell the entire story. An A/D converter with an impressive aperture jitter specification still may lose ENOBs when digitizing a sinewave having a maximum slew-rate calculated from the aperture formula

$$E_a = t_a dV/dt.$$

For example, assume a 20MHz, 10-bit A/D converter has a bipolar input range of $\pm V_o$ ($2V_o$ peak-to-peak) and an aperture jitter specification of 10 ps rms. To calculate the maximum aperture jitter error, the rms aperture jitter must be converted into a maximum value rather than an rms value. If one assumes that aperture jitter follows a Gaussian distribution similar to white noise, the rms aperture jitter, t_a, corresponds to the sigma (σ) of the distribution. The 2σ point on the distribution is a good place to set the maximum, and the maximum aperture jitter becomes $2t_a$.

If the corresponding maximum voltage error, Δv, at the zero crossing of a fullscale sinewave, is set to 1/2 LSB (1/2 LSB = $2V_o/2^{N+1}$, where N is the number of bits of resolution), the maximum fullscale sinewave frequency, f_{max}, which will produce the 1/2 LSB aperture error, can be calculated:

FREQUENCY REQUIRED TO PRODUCE 1/2 LSB APERTURE JITTER ERROR

$$v(t) = V_o \sin 2\pi ft$$

$$\frac{dv}{dt} = 2\pi f V_o \cos 2\pi ft$$

$$\left.\frac{dv}{dt}\right|_{MAX} = \frac{\Delta v}{2t_a} = 2\pi V_o f_{MAX}$$

$$\therefore f_{MAX} = \frac{\Delta v}{4\pi V_o t_a} = \frac{2\ V_o/2^{N+1}}{4\pi V_o t_a} = \frac{1}{2\pi t_a\ 2^{N+1}}$$

For t_a = 10psec, N=10, f_{MAX} = 7.8Mhz

Figure 1.73

For t_a = 10 ps rms, and N = 10, f_{max} is calculated to be 7.8MHz. These calculations imply the 20MHz A/D converter under consideration can accurately digitize a fullscale sinewave of 7.8MHz. In actual practice, however, the A/D converter may begin to suffer from skipped codes, decreased ENOBs and SNR, ac non-linearities, etc., at much lower frequencies. These other limitations to good high frequency performance may, in fact, be significantly greater than errors caused by the aperture jitter of the track-and-hold.

The Effects Of Aperture Jitter On A/D SNR Measurements

The effects of aperture jitter on fullscale sinewave SNR can be calculated as follows:

$$v(t) = V_0 \sin 2\pi ft$$

$$\frac{dv}{dt} = 2\pi f V_0 \cos 2\pi ft$$

$$\left.\frac{dv}{dt}\right|_{rms} = \frac{2\pi f V_0}{\sqrt{2}}$$

For an rms error voltage, Δv_{rms}, and an rms aperture jitter of t_a,

$$\frac{\Delta v_{rms}}{t_a} = \frac{2\pi f V_0}{\sqrt{2}}$$

$$\Delta v_{rms} = \frac{2\pi f V_0 t_a}{\sqrt{2}}$$

The rms signal to rms noise ratio expressed in dB becomes:

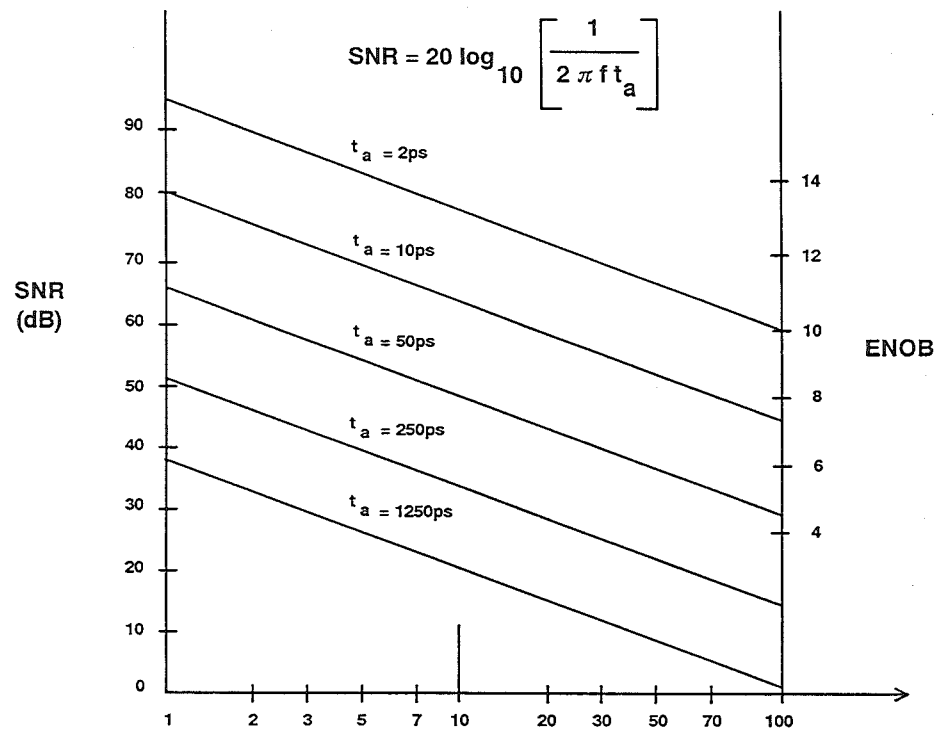
$$SNR = 20\log_{10}\left[\frac{V_0/\sqrt{2}}{\Delta v_{rms}}\right] dB$$

$$= 20\log_{10}\left[\frac{1}{2\pi f t_a}\right] dB$$

The SNR due exclusively to aperture jitter in the equation above is plotted in Figure 1.74 as a function of fullscale input sinewave frequency for various values of aperture jitter.

Consider the example above for a 10-bit, 20MHz A/D converter with an rms aperture jitter of 10 ps. For an 8-MHz fullscale input, the SNR due to only aperture jitter is 66dB as calculated from the equation. The theoretical SNR due to quantizing noise in a 10-bit A/D converter is 62dB. Combining the SNR of 66dB with the SNR of 62dB, a theoretical SNR of 60.5dB is obtained for the A/D; this encompasses both the ideal quantizing noise and the noise due to aperture jitter. A practical 10-bit A/D having an rms aperture jitter specification of 10 ps may, however, only achieve an SNR of 50dB.

From this analysis, one can conclude that the SNR, ENOB, and aperture jitter specifications must all be examined in order to truly evaluate the A/D converter's dynamic performance.



SIGNAL TO NOISE RATIO DUE TO APERTURE JITTER

Figure 1.74

Measurement Of Aperture Jitter Using A Locked Sinewave Histogram

The aperture jitter of an A/D converter can be measured using the test setup shown in Figure 1.75. The sampling clock and the analog input signal are derived from the same low-jitter pulse generator to minimize the phase jitter between them. The phase shifter is adjusted until the A/D converter is repetitively sampling the sinewave at its point of maximum slew-rate at midscale. A histogram is then taken on the digitized A/D converter output data.

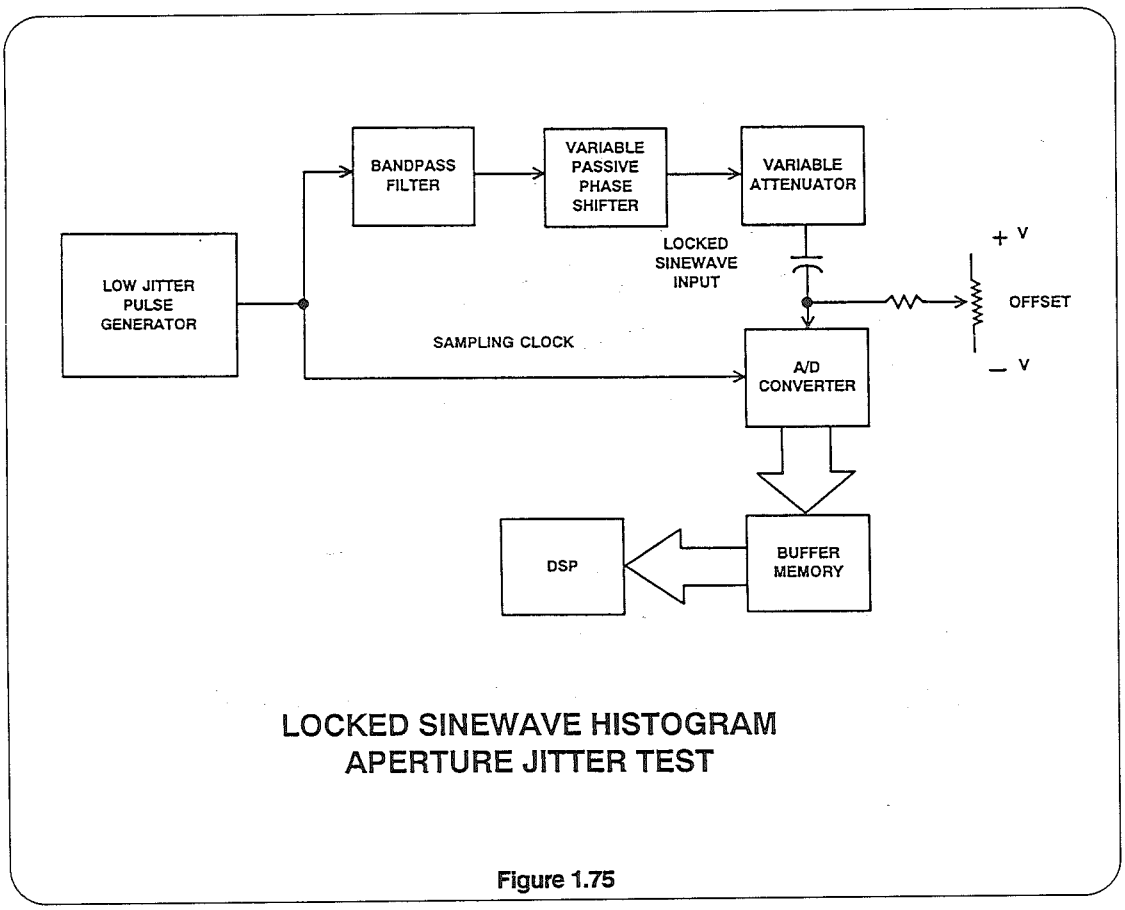
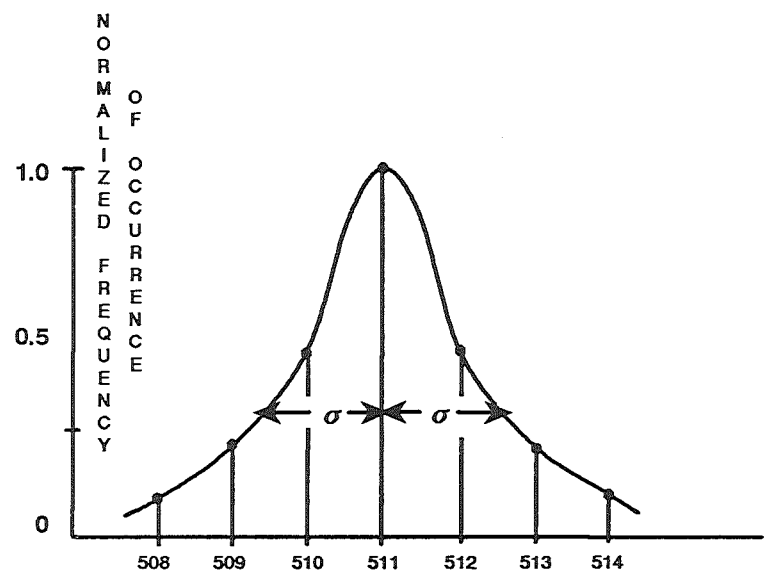


Figure 1.75

An ideal A/D converter with no aperture jitter would have only one code present on the histogram. A practical converter will give a distribution of codes as shown in Figure 1.76. The sigma (σ) of the distribution is calculated and corresponds to the rms error voltage Δv_{rms}, produced by the rms aperture jitter, t_a. The aperture jitter, t_a, can then be calculated from the formula,

$$t_a = \frac{\Delta v_{rms}}{dv/dt}$$

where dV/dt is the rate-of-change of the sinewave at zero-crossing.



APERTURE JITTER HISTOGRAM

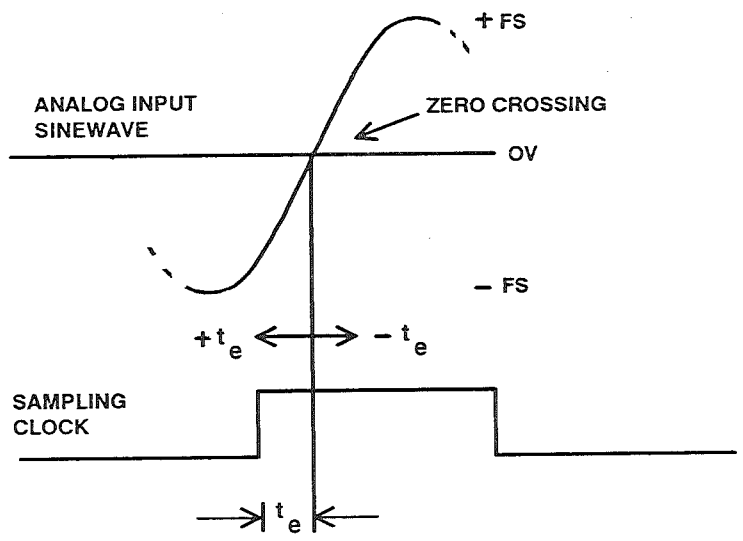
Figure 1.76

If the input sinewave is attenuated sufficiently, the width of the distribution around the nominal code is due to intrinsic A/D converter noise. As the input sinewave is increased in amplitude, the slew-rate, dV/dt, becomes proportionally greater, and the distribution begins to spread due to the aperture jitter. Caution must be exercised in interpreting the histogram for high slew-rate inputs since the ac differential linearity of the converter can also be affected by the higher slew-rate input.

The offset adjustment shown in Figure 1.75 allows the sinewave to be positioned at different points on the A/D converter range. In this way, histograms can be plotted around several nominal codes, and any variations can be attributed to range-dependent differential linearity characteristics. The A/D converter's range can be exceeded when offsetting the sinewave in this manner, so careful control of the offset is necessary.

Measurement Of Effective Aperture Delay Time

Effective aperture delay time can also be measured using the locked sinewave technique as previously shown in Figure 1.75. The phase shifter is adjusted until the A/D converter output reads midscale (i.e., the zero-crossing of the sinewave input signal). A dual trace oscilloscope is then used to measure the difference between the leading edge of the A/D converter sampling clock and the actual zero-crossing of the sinewave input (see Figure 1.77). The difference is the effective aperture delay time and can be either positive or negative depending upon the values of the internal analog and digital delays in the track-and-hold portion of the A/D converter.



MEASUREMENT OF EFFECTIVE APERTURE DELAY TIME

Figure 1.77

TESTING A/D CONVERTERS FOR COMPOSITE VIDEO APPLICATIONS

Differential gain and phase performance are of special importance when an A/D converter is to be used to digitize a composite video waveform. Differential gain is defined as the percentage difference between the output amplitudes of two stated levels of a small high frequency sinewave superimposed on a low frequency signal. Differential phase is the difference in the output phases of two stated levels of a small high frequency sinewave superimposed on a low frequency signal. Distortion free processing of a color signal requires that neither the amplitude nor the phase of the chrominance signal be altered significantly as a function of the associated luminance signal. These tests are generally performed in the analog world (A/D and D/A back-to-back) using conventional video test equipment. These and other tests relating to video applications have been described previously in the literature:

W.A. Kester, "PCM Signal Codecs for Video Applications," SMPTE Journal 88, November 1979, pp. 770-778.

DIGITAL VIDEO SPECIFICATIONS

- Differential Gain
- Differential Phase
- Bandwidth
- Linearity - Low Frequency
- "2T" Pulse Response
- "12.5T" Modulated Sin^2 Pulse Response
- Chrominance-to-Luminance Distortion
- Chrominance Phase Linearity
- Color Bar Performance

Figure 1.78

ERROR RATE AND SPARKLE CODE TESTS

At the present time, there is no industry standard for either the definition or the test for A/D converter error rates. As has been discussed in the section on flash converters, comparator metastable states can occur for low or high frequency input signals. At high frequencies, "bubbles" in the thermometer code of the comparator bank output can also produce erroneous output codes. Subranging A/D converters are subject to error codes since they use flash converters as building blocks. The measurement of error rate requires that a large number of samples be taken, since error rates less than $1x10^{-6}$ are typical for well behaved A/D converters. Great care must be taken in the error rate test set layout, grounding, shielding, and power supply decoupling so that AC 60Hz, EMI, or RFI glitches don't give false errors.

The error rate for low frequency input signals can be measured as follows. A low frequency fullscale sinewave (or triangle wave) is applied to the A/D converter and its rate of change is selected to be much less than 1 LSB per sample. This ensures that the transition zones between codes are all adequately exercised. An error amplitude of X LSBs is established as the lower limit for the definition of a "qualified" error. Usually, X is selected to be several LSBs so that random noise doesn't produce false errors. The software or hardware then examines the difference between each adjacent sample and records the number of times (NQ) this difference exceeds the error threshold X. If NQ is the number of qualified errors that occur and NT is the total number of samples taken, then the error rate, ER, is given by the equation,

$$ER = \frac{NQ}{2 \cdot NT}$$

As an example, consider an 8-bit, 100 MHz flash converter where it is desired to take at least ten samples at each code level. For one slope of the triangle wave input, this implies 10 x 256 = 2560 samples. The frequency of the triangle wave can be calculated:

$$f_T = \frac{1}{2560 \cdot 2 \cdot 10ns} = 19.5kHz$$

At a 100MHz sampling rate, the average time required to make an error for an error rate of $1x10^9$ is 10 seconds.

Dynamic errors which occur due to fast input signals can be measured in a similar manner by using the "beat frequency" approach. The low frequency beat frequency is chosen to give the proper number of samples per code level, and the decimated digital outputs are examined for adjacent sample differences which exceed the allowable error amplitude.

In summary, determining an appropriate error rate criterion for an A/D converter depends upon both the application and the characteristics of the A/D under consideration. Flash converters which use straight binary decoding are most subject to large metastable errors at midscale. For this situation, a low amplitude "dither" input signal centered on the midscale code transition might be an appropriate stimulus. In a subranging A/D converter, a fullscale signal which exercises all the "subranging" points might be desirable.

Hopefully, as this error rate phenomenon becomes more fully understood, it will be possible to establish industry standards which are meaningful to a variety of applications and A/D converters.

ERROR RATE TESTING

- Define "Error", X LSBs
- Low or High Frequency Input?
- Examine Difference Between Adjacent Codes
- Take NT Samples
- Record NQ Qualified Errors

$$\text{Error Rate} = \frac{NQ}{2\,NT}$$

- Shielding, EMI, RFI Considerations
- Industry Standards?
- A/D Converter Architecture?

Figure 1.79

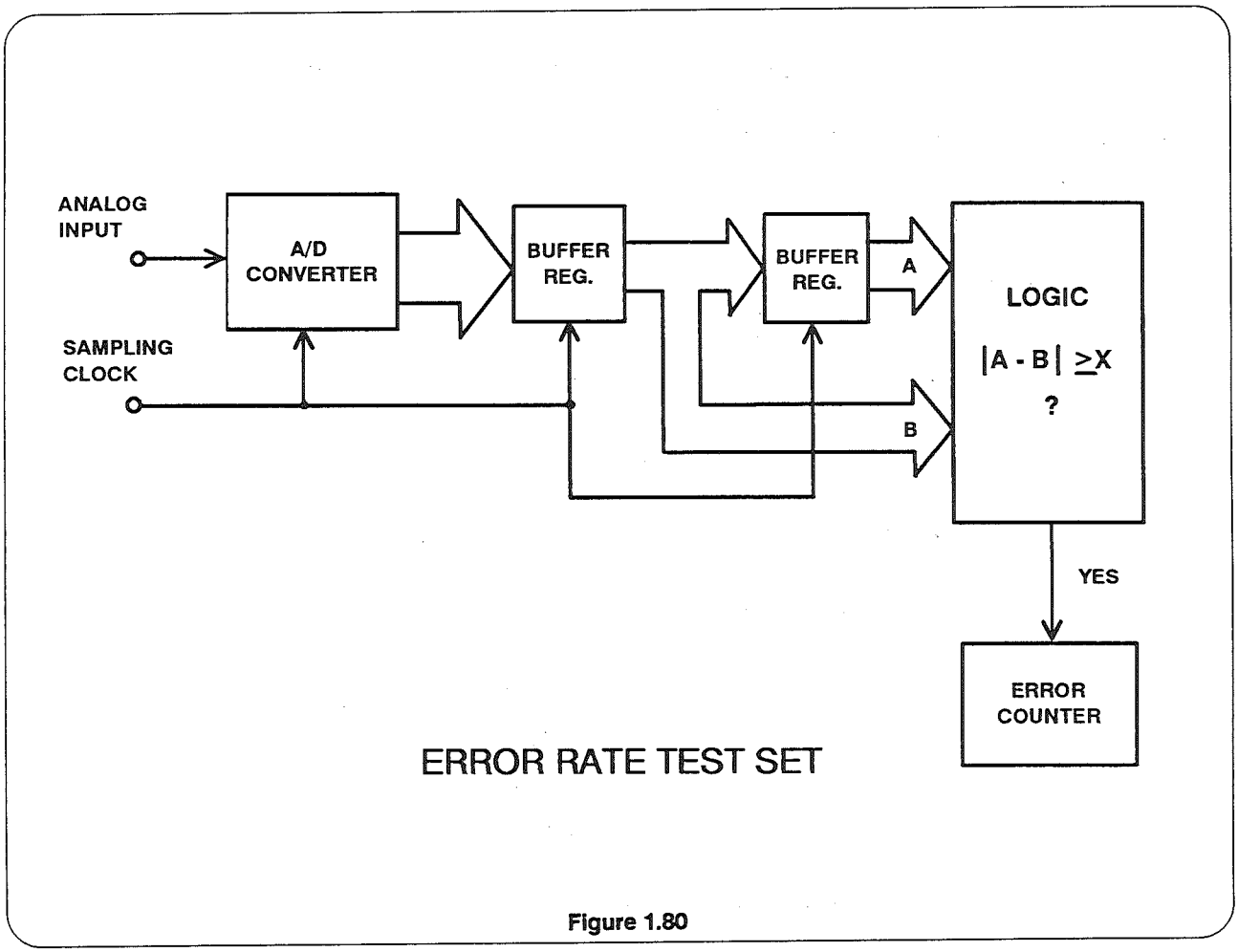

ANALOG
INPUT
A/D
CONVERTER
BUFFER
REG.
BUFFER
REG.
A
LOGIC
|A - B| ≥X
?
SAMPLING
CLOCK
B
YES
ERROR
COUNTER
ERROR RATE TEST SET

Figure 1.80

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MULTISTAGE ERROR CORRECTING A/D CONVERTERS

Analog Devices, Inc.

1

INTRODUCTION

The accelerating growth of digital signal processing has expanded the applications for high-speed data converters. High-speed (> 1 Megasample per second) analog-to-digital converters (ADC's) are required in a rapidly growing number of applications, such as video, radar, and medical instrumentation. The three primary ADC types used to meet these needs are the parallel or "flash" converter, the successive approximation converter, and the subranging converter.

This paper is intended as a tutorial on error-correcting ADC's. ADC's will be classified into two fundamental groups, and the limitations of each will be examined. The basic concepts of error correction will be developed, and a specific case will be studied in further detail. Finally, logical extensions of the basic technique will be considered.

BASIC CONVERTERS

All ADC's have three conceptual "parts" as shown in Figure 1; a reference source; a comparator; and a digital translator, which is also assumed to include control logic. The most common form of reference is the digital-to-analog converter (DAC). This is the reference element in successive approximation converters. A parallel ADC ("flash" converter) contains a multiport DAC, in the form of a resistor ladder with an output corresponding to each quantization level of the converter's transfer function. In some types of converters, the reference is not obvious. For example, the reference source of a cyclic or Grey code ADC is "hidden" in the manipulation of the input signal in each sequential stage. The actual analog-to-digital conversion element is the comparator. It can take the form of a single comparator, as in a successive approximation converter; a large bank of comparators, as in a flash; or something in between. Finally, some form of digital logic is required to convert the comparator output(s) into a digital representation of the input signal, and control the sequence. This is obviously a simplistic look at the operation of ADC's, but it is important to be able to sort out these basic functions. Sometimes a "new" technique comes along which, on a closer look, is actually one of the more familiar types.

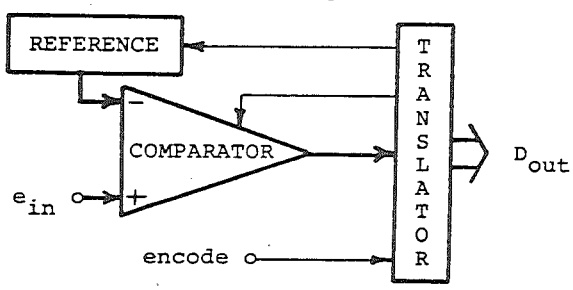

Fig. 1. Basic ADC.

Stages

The two main ADC categories germane to this session are single-stage and multistage. This categorization is somewhat misleading to anyone unfamiliar with these terms as used to describe converters. The term "single-stage" denotes any comparator which does its comparison at a single point in time. Converters in this category are full parallel or "flash" converters. All other converters are multistage. Although flash converters must perform a sequence of operations, there is only one comparison time.

"Multi-stage" ADC's can be further divided into two types. Subranging ADC's first "narrow down" the value of the analog input to a subrange of the total quantization range. This subrange is then subdivided further. A subranging ADC can have two or more stages, each of which could be further characterized as single-stage or multi-, subranging, etc. The second type of

multistage ADC's are non-subranging. This category is a catchall for such methods as integrating and tracking ADC's, whose general use is at substantially lower conversion rates. As a result, for the purposes of this paper, multi-stage and subranging can be considered the same.

Single-Stage Converters

Parallel, or "flash," converters represent a brute force approach to very high-speed conversion. The flash converter is covered in another part of this session. Because flash converters require a comparator, voltage reference, and digital translation for every quantization level, an upper limit now exists on flash resolution and linearity. This is due in part to the incredible circuit size, and also to the small differential voltage between quantization levels. If the number of converter bits increases by one, either the quantization level is reduced by one-half, or the full-scale input voltage must be doubled. The first situation puts a severe demand on comparator design, while the latter requires a higher-slew-rate, higher-power driving source. The current practical limit on this converter type (in monolithic form) is 8-9 bits. Although the theoretical resolution of a flash converter can be higher if implemented in discrete form, the cost, size, and power are generally prohibitive.

Multi-Stage Converters

Multi-stage converters provide high resolution with far fewer elements than single-stage converters. The obvious tradeoff is conversion speed. As discussed earlier, multi-stage converters common in high-speed converters are all of the subranging type. Subranging converters are used when higher resolution and/or lower power and complexity are required. A basic subranging ADC is shown in Figure 2. The first ADC is an N_1-bit encoder, usually a FLASH, which quantizes the analog input (e_{in}) into one of 2^{N_1} levels.

A DAC converts this into an equivalent voltage. This digitized, reconstructed signal is subtracted from the input e_{in} to yield the difference between the output of the first encoder and e_{in}. This, in turn, is quantized by the second encoder; and the output of N_2 LSB's and N_1 MSB's should represent the input. The primary sources of

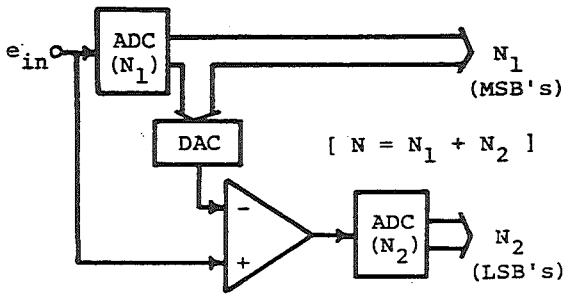

Fig. 2. N-bit Subranging ADC.

error in this type of converter are in the first conversion. Although it is only N_1 bits, it must be better than N bits accurate, and the input must settle to better than N bits accuracy before the first conversion. These requirements conflict with the need for high speed. It should be noted that this technique can be extended to any number of stages (up to N).

The successive approximation ADC is actually 12 one-bit encoders with a common DAC and comparator. This technique of using ADC stages more than once is called RECIRCULATING. The new SONY 8-bit monolithic encoder uses subranging with two 4-bit stages.[1] This is substantially less complex than an 8-bit flash, with correspondingly higher yields and lower cost.

Error Correction

The sources of error mentioned above can be overcome by use of a technique called error correction. The term error correction is a popular one and has a number of different meanings. Error correction in the context of this tutorial implies that the first stage(s) of a multi-stage ADC can make a priori unknown errors within a bounded range which are correctable via subsequent stage(s) of the converter. A more precise term is digitally corrected subranging, even though the errors to be corrected are analog in nature.

DIGITALLY CORRECTED SUBRANGING

Before developing the error correction technique, consider again the 2-stage ADC of Figure 2. The first encoder, DAC, and subtractor could also represent a circuit for testing the first encoder. The output of the subtractor vs. e_{in} should be a "sawtooth" waveform as shown in Figure 3. This will be referred to as an ERROR WAVE-

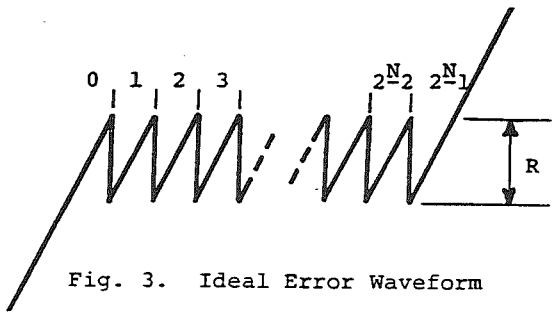

Fig. 3. Ideal Error Waveform

FORM. This waveform has 2^{N_1}-1 "teeth." Each vertical line represents the encoder changing state. Its height is the change in value of the DAC. The height of the sloped line represents the size of the corresponding quantization level of the encoder. All heights are the same because the encoder and DAC are assumed ideal. The height R represents the range of the second encoder. If each "tooth" does not exactly fill R, there will be an error in the overall converter transfer function.

For purposes of illustration, assume in Figure 2 that N_1=4(16 levels), and N_2=8(256 levels). This makes a 12-bit converter (4096 levels). Figure 4 shows the error waveform for this con-

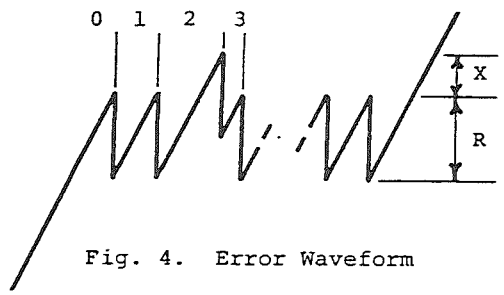

Fig. 4. Error Waveform

verter, but this time the first encoder is not perfect. Since code 2 is 1.5 times the expected quantization level and code 3 is 0.5, these codes are off by 1/2 a least significant bit (LSB) of the first encoder. This encoder, then, is 4 bits accurate. This is a perfectly respectable 4-bit ADC, but a disaster in a subranging converter. When the first "tooth" goes out of range, the code corresponding to code 2 of the first converter plus the full scale of the second converter (255) gives an output of 2 X 256 + 255 = 767. This code remains until the encoder switches to code 3. This results in an output of 3 X 256 + 128 = 896. The result is 128 missing codes! Note that this still assumed the DAC was perfect. It should be evident the missing codes can never be recovered unless the area X can be quantized with the second ADC.

What must be done to recover the "missing" codes? First, if the signal exceeds the range R, the value of the first encode must be increased by one. Then the value of the X quantization, rather than the R, is added. Therefore, the first code as the "tooth" starts to exceed R, would be (2 + 1) X 256 + 0 = 768. This would continue increasing to a peak value of (2 + 1) X 256 + 127 = 895. Thus, all the codes are found.

If the error waveform falls below the range of R, as in Figure 5, the

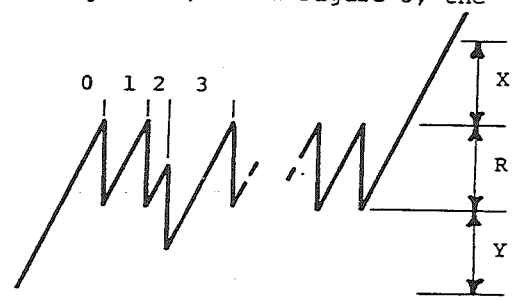

Fig. 5. Another Error Waveform.

range needs to be quantized. If the error waveform falls below the range R, the quantization of the difference between the signal and the bottom of R must be subtracted. At the top of the short "tooth," the output is 2 X 256 + 127 = 639. After switching to the next level, 3 X 256 - 128 = 640, and there are no missing codes.

The two scenarios described above could have been accomplished by adding or subtracting one count from the DAC, which would restore the error waveform to the range of the second ADC (R). This consumes significant time (DAC settling plus determining if the error waveform falls out of the range R). It is far more desirable to extend the range of the second ADC.

In the example above, to correct first stage errors of $\pm\frac{1}{2}$ LSB, the second stage would have to encode from -128 to +383 rather than from 0 to +255. The second stage could then be added directly to 256 X (first stage output). This requires a 9-bit second stage rather than an 8-bit. In effect,

this converter has one bit of correction. In general, if a stage has C bits of correction, it can correct for errors of $\pm\frac{1}{2}(2^C-1)$ LSB's. If 2 bits of correction are used in the second stage, the first stage could have errors up to $\pm 1\frac{1}{2}$ LSB's.

Returning to the example, the suggested second stage seems a bit odd, requiring a range of -128 to +383. An alternative approach is to use a "normal" 9-bit encoder (0-511); and use an offset voltage to center the error waveform in the second encoder range as shown in Figure 6. The digital output

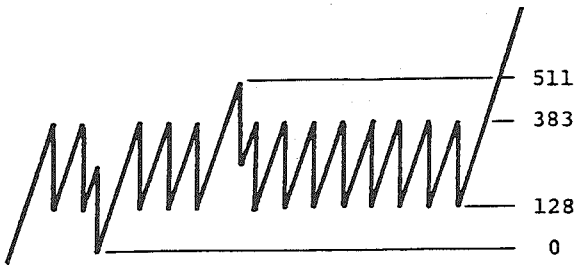

Fig. 6. Still Another Error Waveform.

will now be too high by 128 counts. This can be corrected by a digital subtractor on the output or more conveniently, by adding a voltage offset to the front end of the ADC. The converter with these modifications is shown in Figure 7.

crease, the second encoder goes to 256, which forces the adder output to all zeros! The second encoder will continue to encode until it reaches 511. Figure 8 shows the transfer function of

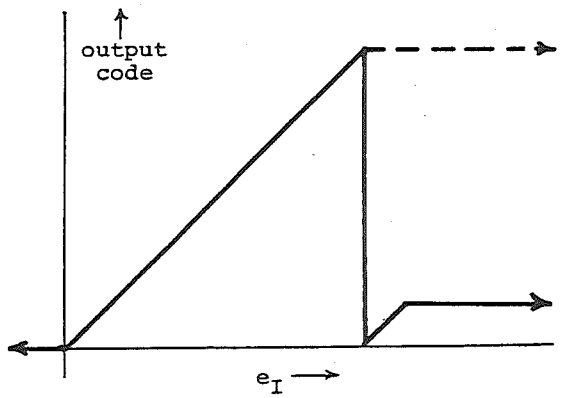

Fig. 8. Need For Overrange Correction.

this ADC, with the dotted line indicating the desired characteristic. The solution to this dilemma is to use the carry from the adder to force all output bits to a logical 1. There are several ways to implement this OVERRANGE CORRECTION, with tradeoffs available between speed and circuit complexity.

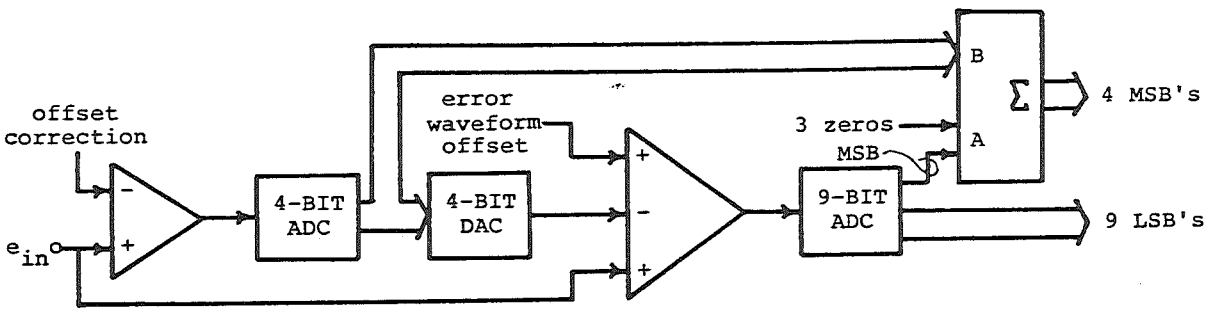

Fig. 7. Basic 12-bit Digitally Corrected Subranging ADC.

The adder would typically be implemented as a '283 for TTL or a '181 for ECL. It could also be implemented using exclusive-or gates. This circuit of Figure 7 still has a problem, although it is not at all obvious. As the waveform approaches full scale, the output will reach 2^N-1 when the second encoder is only at halfscale (255). As the input continues to in-

Implications

With a basic understanding of digital error correction, it becomes easier to take stock of its implications. Relatively simple digital logic removes the constraint of high accuracy from the first stage, allowing use of high-speed, low-accuracy monolithic "flash" converters. In fact, there are

several errors which can be virtually ignored as long as the error waveform remains in the correction range:

- o T/H droop error
- o T/H settling time error
- o 1st stage gain error
- o 1st stage offset error
- o 1st stage linearity error
- o operational amplifier offset error
- o 2nd stage offset error

Figure 9 illustrates the effect of some

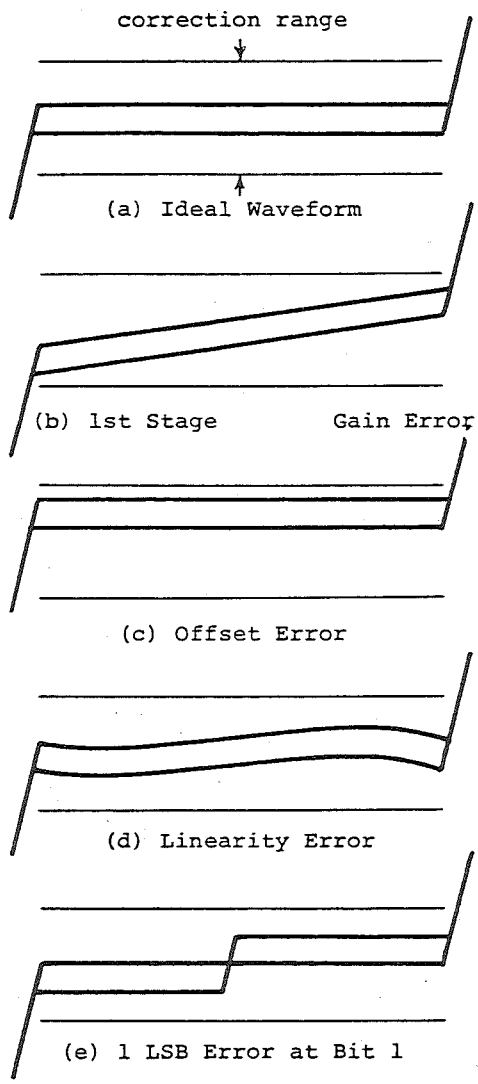

Fig. 9. Correctable Error Waveforms

common errors on the error waveform. Since each waveform shown remains in the correction range, these errors have no effect on the overall converter linearity.

The advantages of digital error correction are not without cost. Besides digital logic and the larger second encoder, each correcting stage requires three new analog adjustments. The first of these is the gain of the DAC relative to the input. This controls the "tilt" of the error waveform which, ideally, should be flat. The second is the centering of the error waveform in the range of the next stage, or error waveform "offset." The final adjustment is the gain of the error amplifier, which must make each DAC step equal to the appropriate fraction of the range of the next stage. Fortunately, consideration of each adjustment indicates its accuracy need be only somewhat better than the first stage resolution, rather than the total converter resolution.

DESIGN RULES

The first and foremost design rule is this: MAKE THE NUMBER OF BITS IN THE FIRST STAGE(s) AS SMALL AS PRACTICAL. The main reason for this is that the error waveform requires amplification to fit the range of the second encoder properly. Each additional bit in the first stage doubles the required gain; and higher gain requires longer settling time of the error amplifier. The design of this amplifier is generally the primary limitation of the overall converter speed.

A second reason is that a small number of bits in the first stage allows a larger tolerance for T/H errors and offset errors. Since it is possible, for example, to obtain 6- or 8-bit-accurate 4-bit flashes, the encoder error is a relatively small part of the correction range. This allows the majority of the range to be used to correct other errors such as temperature drift. The third reason is that fewer bits in the first stage(s) simplify the error correction circuit and reduce the size of the DAC.

The second design rule is that the overall circuit can be no better than the error DAC(s). A design goal should be that the DAC has an accuracy at least one bit better than the desired accuracy for the total converter. Cur-

rent technology can supply high-speed DAC's with 13-bit accuracy.

Figure 10 shows a general error-correcting encoder stage and the configuration of a k-stage digitally corrected subranging ADC. Of course, the DAC and subtractor for the last stage are not necessary, and an actual implementation might combine the subtraction and gain functions.

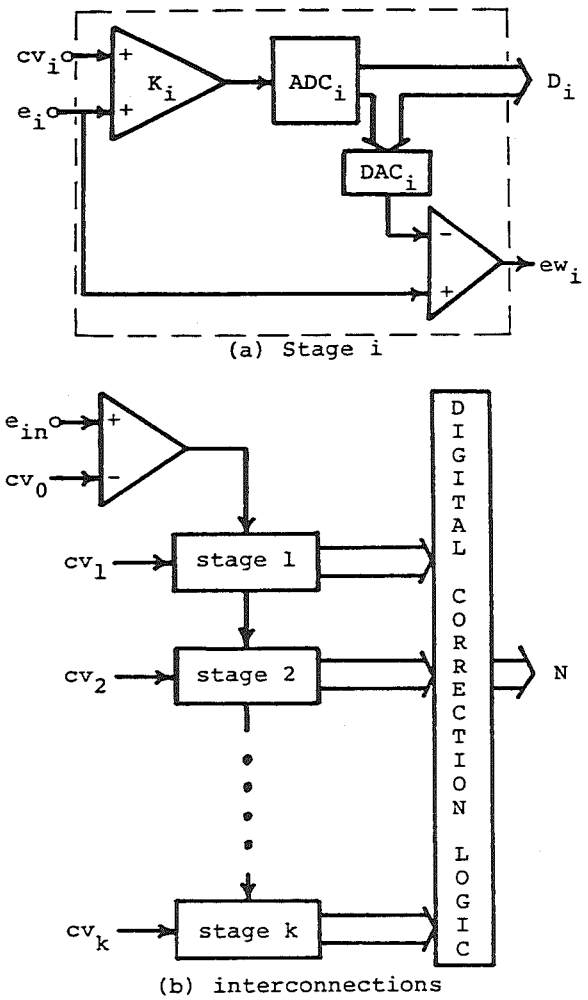

Fig. 10. Multi-stage Correcting ADC.

Table 1 provides definitions and equations for designing a k-stage correcting converter. It is assumed each DAC provides an ideal signal such that the analog output is an error waveform with "teeth" from zero volts to E_i/n_i volts. The equations neglect polarities or offsets, required by real components, which must be controlled by the circuit designer. Also, gains can be obtained in different ways. For example, rather than e_i, the output of the adder with gain K_i could be used to obtain an ew_i of higher amplitude. This would reduce the gain requirement of the next stage error amplifier. Equation 1-8 basically says that the correction bits of stage i are added to the LSB's of the previous stage; that the LSB of this sum is one bit more significant than the most significant non-correcting bit of stage i; and that the output must be limited by OVERRANGE CORRECTION.

Table 1. Digital Correction Design Calculations

k - number of stages.
N_i - number of bits of stage i encoder.
C_i - number of bits of digital correction for stage i (C_1=0).
R_i - range of encoder i in volts.
E_i - range of input voltage e_i.
EW_i - range of output voltage ew_i.
cv_i - error waveform offset voltage for stage i.
cv_0 - input offset correction for total converter.
R_0 - input voltage range for total ADC.
$D(C_i)$ - value of binary word formed by the C_i MSB's of the stage i encoder.
$D(M_i)$ - value of binary word formed by the remaining LSB's of stage i.
D(N) - value of corrected output of the complete converter.

$$n_i=2^{N_i} \quad (1\text{-}1) \qquad c_i=2^{C_i} \quad (1\text{-}2) \qquad N=\sum_{i=1}^{k} N_i-\sum_{i=1}^{k} C_i \quad (1\text{-}3)$$

$$K_i=\frac{R_i}{E_i c_i}=\frac{R_i}{R_0 c_i}\prod_{j=1}^{i-1} n_j \quad (1\text{-}4) \qquad EW_i=\frac{E_i}{n_i} \quad (1\text{-}5)$$

$$cv_i=\frac{(c_i-1)E_i}{2}=\frac{(c_i-1)}{2}\,\frac{R_0}{\prod_{j=1}^{i-1} n_j} \quad (1\text{-}6) \qquad cv_0=\sum_{i=1}^{k} cv_i \quad (1\text{-}7)$$

$$D(N)=\min\left\{2^N-1,\; D(M_k)+\sum_{i=2}^{k}[D(C_i)+D(M_{i-1})]2^{\sum_{j=i}^{k} M_j}\right\} \quad (1\text{-}8)$$

An Example

In order to get an understanding of the equations, an example will be worked. The important numbers are the gain of each input, and each of the offset voltages. These numbers are computed in Table 2.

Table 2. Sample Design Calculations

N=12	k=3	R_0=10
N_1=3	N_2=6	N_3=6
C_1=0	C_2=1	C_3=2
R_1=2	R_2=1	R_3=1

From equation 1-4:

$$K_1 = \frac{2}{10x1} \times 1 = 0.2$$

$$K_2 = \frac{2}{10x2} \times 8 = 0.8$$

$$K_3 = \frac{1}{10x4} \times 8x64 = 12.8$$

From equation 1-6:

$$cv_1 = \frac{(1-1)}{2} \times \frac{10}{1} = 0$$

$$cv_2 = \frac{(2-1)}{2} \times \frac{10}{8} = 0.625$$

$$cv_3 = \frac{(4-1)}{2} \times \frac{10}{8x64} = 0.0293$$

From equation 1-7:

$$cv_0 = 0 + .625 + .0293 = .654$$

Note that two of the computed gains are less than unity. This is due to the input voltage range being substantially greater than the input range of the first stages, and the low number of bits in the first stage. Implementation of these calculations is shown in Figures 11 and 12.

The first two adders, with gains of less than one, would simply be resistive dividers. In the last stage, the subtractor and adder with gain of 12.8 could be combined into one operational amplifier. The correcting adder in Figure 11 would normally be implemented as two 4-bit adders.

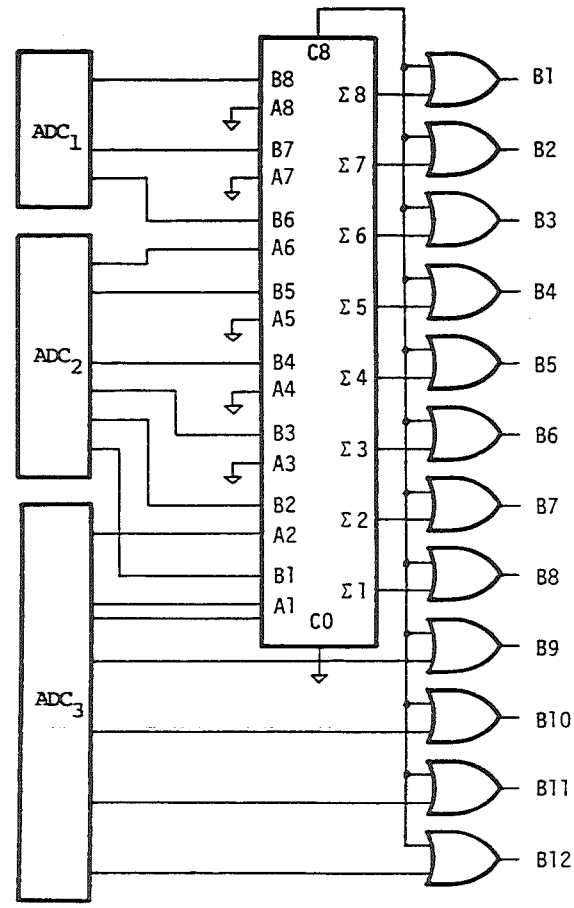

Fig. 11. Implementation of Error Correction.

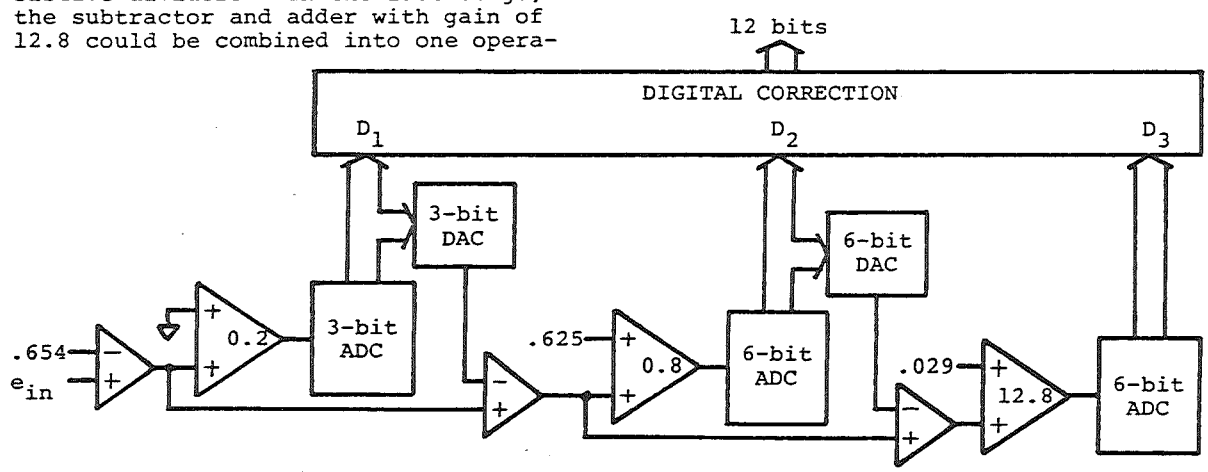

Fig. 12. 12-bit 3-stage Correcting ADC.