Chapter V

APPLYING IN-AMPS EFFECTIVELY

Dual-Supply Operation

The conventional way to power an in-amp has been from a *split* or dual polarity power supply. This has the obvious advantage of allowing both a positive and a negative input and output swing.

Single-Supply Operation

Single-supply operation has become an increasingly desirable characteristic of a modern in-amp. Many present day data acquisition systems are powered from a single low voltage supply. For these systems, there are two vitally important characteristics. First, the in-amp's input range should extend between the positive supply and the negative supply (or ground). Second, the amplifier's output should be rail-to-rail as well.

The Need for True R-R Devices in Low Voltage, Single-Supply IA Circuits

Sometimes problems arise when designers forget about amplifier headroom and use standard (non rail-to-rail) products in low voltage, single-supply in-amp applications. Many dual-supply in-amps will only have an output swing within about 2 V of either rail. However, even the very best cannot swing as close to the rails as a single-supply device.

A good quality rail-to-rail in-amp, such as the AD623, can swing its output to within 0.5 V of the supply and within 0.1 V above ground. Its input voltage range is similar. Note that these numbers are conservative: with very light output loading the performance is even better. So, when using a 5 V single supply, the amplifier has at least a 4 V output swing, in many cases, more than that.

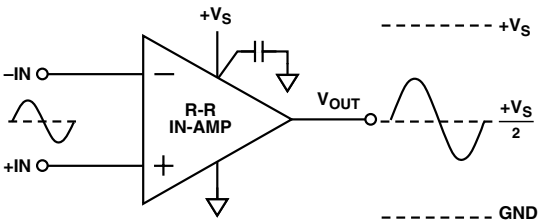


Figure 5-1. A modern rail-to-rail in-amp can swing more than 4 V p-p with a 5 V supply, but this is NOT possible using a standard dual-supply device. Note that the in-amp's V_{REF} pin would normally be set at $V_S/2$ for maximum output swing.

In the example shown in Figure 5-1, the p-p output swing would only be about 1 V p-p for a standard product vs. 4 V p-p or more for a rail-to-rail in-amp.

Power Supply Bypassing, Decoupling, and Stability Issues

Power supply decoupling is an important detail that is often overlooked by designers. Normally, bypass capacitors (values of 0.1 μF are typical) are connected between the power supply pins of each IC and ground. Although usually adequate, this practice can be ineffective or even create worse transients than no bypassing at all. It is important to consider where the circuit's currents originate, where they will return, and by what path. Once that has been established, bypass these currents around ground and other signal paths.

In general, like op amps, most monolithic in-amps have their integrators referenced to one or both power supply lines and should be decoupled with respect to the output reference terminal. This means that for each chip, a bypass capacitor should be connected between each power supply pin and the point on the board where the in-amp's reference terminal is connected, as shown in Figure 5-2.

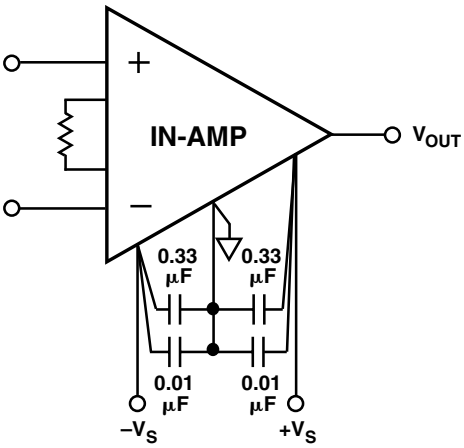


Figure 5-2. Recommended method for power supply bypassing.

For a much more comprehensive discussion of these issues, refer to Application Note AN-202, *An IC Amplifier User's Guide to Decoupling, Grounding, and Making Things Go Right for a Change*, by Paul Brokaw, on the ADI website at *www.analog.com*.

THE IMPORTANCE OF AN INPUT GROUND RETURN

AC coupling is an easy way to block dc voltages that are present at the in-amp's inputs. But ac coupling into a high impedance in-amp input without providing a dc return renders the circuit nonfunctional! This is one of the most common applications problems that arises when using in-amp circuits. Figure 5-3 shows two common (incorrect) arrangements.

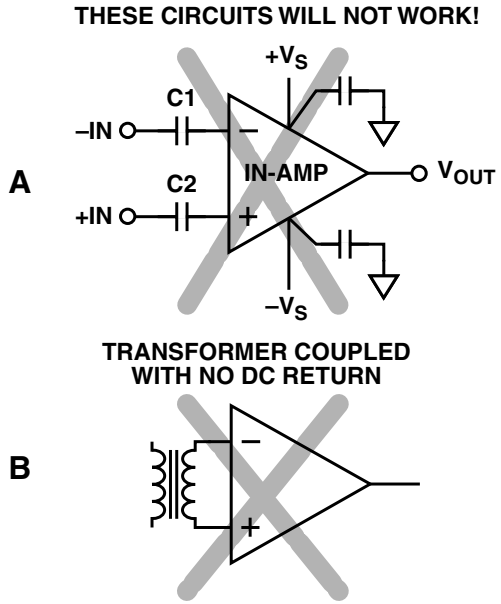
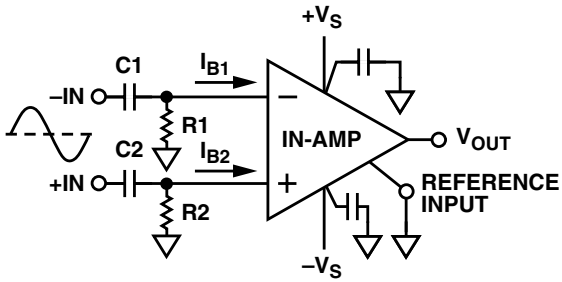


Figure 5-3. Nonfunctional, ac-coupled in-amp circuits.

In Figure 5-3A, the input bias currents will charge up the ac coupling capacitors until the input common-mode voltage is exceeded. In other words, the caps will charge up to the supply line or down to ground depending on the direction of the input bias currents. Now, with a FET input device, and very large capacitors, it could take several minutes before the in-amp is rendered inoperative. As a result, a casual lab test might not detect this problem, so it's very important to avoid it altogether. Figure 5-3B shows a transformer-coupled input with no center tap or other means for a dc return; so, the same problem occurs.

A simple solution for the circuit in Figure 5-3A is to add a high value resistance (R1, R2) between each input and ground, as shown in Figure 5-4. The input bias currents can now flow freely to ground and do not build up a large input offset as before.



$V_{OS} = (I_{B1} \times R_1) - (I_{B1} \times R_2)$

Figure 5-4. A high value resistor between each input and ground provides an effective dc return path (see Table 5-1).

This is a simple and practical solution for dual-supply in-amp circuits. The resistors allow a discharge path for input bias currents. Now both inputs are referenced to ground. There will be a small offset voltage error due to the mismatch between the input bias currents flowing through the two nonidentical resistors. To avoid errors due to an R1/R2 mismatch, a third resistor, about one-tenth their value, can be connected between the two in-amp inputs.

Figure 5-5 shows the recommended dc return for a transformer-coupled input.

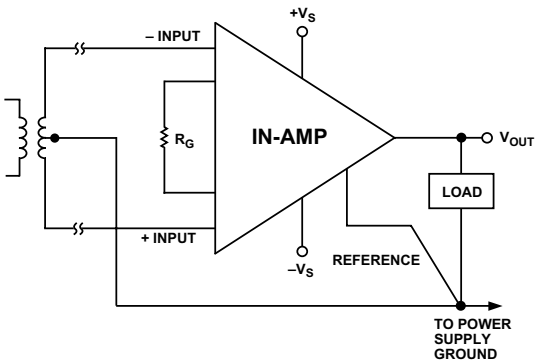


Figure 5-5. Recommended dc return path for a transformer-coupled input.

For transformers without a center tap, two resistors, one from each input pin to ground, can be used to provide a dc return path.

Providing Adequate Input and Output Swing ("Headroom") When AC Coupling a Single-Supply In-Amp

AC coupling using an in-amp powered by a single supply is more complicated than dual-supply operation and normally requires applying a dc common-mode voltage, V_{CM}, to both inputs, as shown in Figure 5-6. This is necessary because the internal buffer amplifiers of a typical 3-op amp in-amp cannot swing more than a few millivolts below the negative supply (in this case ground) without clipping the signal. In addition, the output can never swing below the negative supply.

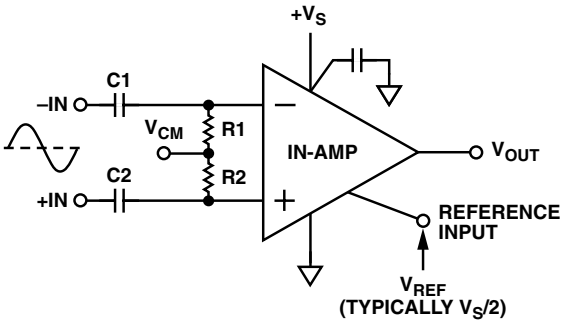


Figure 5-6. An ac-coupled, single-supply, in-amp circuit. For maximum dynamic range, set V_{CM} to the center of the maximum input range. V_{REF} is typically set to $V_S/2$.

Choosing appropriate voltages for V_{CM} and V_{REF} is an important design consideration, especially in low supply voltage applications. In general terms, V_{CM} should be set to the middle of the expected *input* dynamic range, while V_{REF} should be centered on the expected *output* dynamic rage. As an example, say the input signal (the difference between +IN and –IN) is expected to be between +1 V and –2 V. Under these conditions, the in-amp's input buffers will need to swing both positive and negative with respect to ground. Assume the in-amp is operating at unity gain, V_{CM} can be set to +2 V (or a bit higher), which will allow 2 V of headroom in the minus direction. The trade-off is that there is now 2 V less swing in the positive direction. If the in-amp is operating with gain, V_{CM} needs to be tailored to allow the buffer outputs to swing fully without clipping (that is, without exceeding their maximum voltage swing in either direction).

Output centering is similar: estimate the amount and the direction of the in-amp's output swing (in most cases this will be $V_{IN} \times$ gain + V_{REF}) and then apply a reference voltage at V_{REF} that is in the center of that range.

Selecting and Matching RC Coupling Components

In ac-coupled applications, selecting values for the capacitors and dc return resistors is a trade-off between –3 dB bandwidth, noise, input bias current, and the physical size of the capacitors. RC components should be reasonably matched so that the time constant of R1/C1 is close to that of R2, C2. Otherwise, a common-mode voltage can be converted into a differential error.

Higher value input capacitors provide greater low frequency bandwidths and allow smaller value input resistors. But these caps are physically larger, requiring more board space. As a rule, capacitors larger than 0.1 microFarad need to be polarized types such as tantalums to keep their size manageable. But polarized caps require a known, constant polarity dc voltage to keep them properly biased.

Smaller cap values require higher value input resistors which have higher noise. And with larger input resistors, dc offset voltage errors also become larger. So, there is always a trade-off that needs to be made here.

Since $(I_{B1}R_1) - (I_{B2}R_2) = \Delta V_{OS}$, any mismatch between R1 and R2 will cause an input offset imbalance $(I_{B1} - I_{B2})$. The input bias currents of Analog Devices in-amps vary widely, depending on input architecture. However, the vast majority have maximum input bias currents between 1.5 nA and 10 nA. A good guideline is to keep $I_BR < 10$ mV.

Table 5-1. Recommended Component Values for AC Coupling In-Amp Inputs

–3 dB BW	RC Coupling Components C1, C2	RC Coupling Components R1, R2	Input Bias Current (IB)	V_{OS} at Each Input	V_{OS} Error for 2% R1, R2 Mismatch
2 Hz	0.1 µF	1 MΩ	2 nA	2 mV	40 µV
2 Hz	0.1 µF	1 MΩ	10 nA	10 mV	200 µV
30 Hz	0.047 µF	115 kΩ	2 nA	230 µV	5 µV
30 Hz	0.1 µF	53.6 kΩ	10 nA	536 µV	11 µV
100 Hz	0.01 µF	162 kΩ	2 nA	324 µV	7 µV
100 Hz	0.01 µF	162 kΩ	10 nA	1.6 mV	32 µV
500 Hz	0.002 µF	162 kΩ	2 nA	324 µV	7 µV
500 Hz	0.002 µF	162 kΩ	10 nA	1.6 mV	32 µV

Table 5-1 gives typical R and C cookbook values for ac coupling using 1% metal film resistors and two values of input bias current.

Properly Driving an In-Amp's Reference Input

Another common applications problem occurs when a high impedance source is used to drive an in-amp's reference terminal. In the example shown in Figure 5-7, R2's added resistance unbalances the otherwise closely matched resistors in subtractor amplifier A3. A resistor divider is shown here, but the same problem is created with any input source that is even a small percentage of R_{REF}. This results in both a CMR error and a reference voltage error.

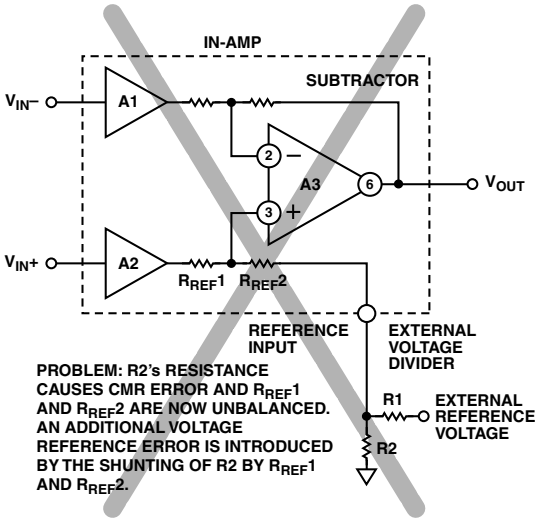


Figure 5-7. When using this simple voltage divider, $R_{REF}1$ and $R_{REF}2$ are now unbalanced, which introduces a large CMR error in A3.

A CMR error is introduced because $R_{REF}2$ no longer equals $R_{REF}1$ (R2 is in series). Note that $R_{REF}1$ and $R_{REF}2$ are not always equal but that introducing any significant series resistance between the V_{REF} terminal and ground will unbalance A3 and cause a CMR error. A reference voltage error is also produced because R2 becomes loaded by the in-amp's finite reference impedance.

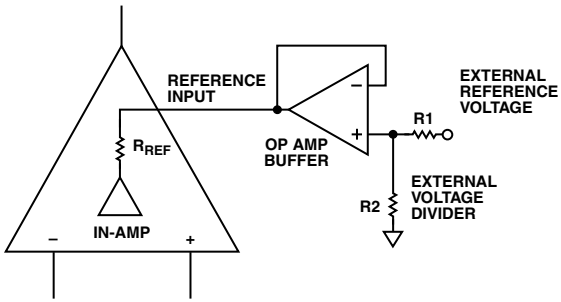


Figure 5-8. A simple op amp buffer provides a low impedance for driving an in-amp's input.

Figure 5-8 shows a simple solution to this problem. An op amp buffer is added between the voltage divider (or other high-Z source) and the in-amp's reference terminal. Now, the in-amp only sees the very low output impedance of the op amp, which typically is much less than one ohm.

Many other solutions are possible, as long as the impedance driving the reference terminal is kept very low.

CABLE TERMINATION

When in-amps are used at frequencies above a few hundred kilohertz, properly terminated 50 Ω or 75 Ω coaxial cable should be used for input and output connections. Normally, cable termination is simply a 50 Ω or 75 Ω resistor connected between the cable center conductor, and its shield is at the end of the coaxial cable. Note that a buffer amplifier may be required to drive these loads to useful levels.

INPUT PROTECTION BASICS FOR ADI IN-AMPS

Input Protection from ESD and DC Overload

As interface amplifiers for data acquisition systems, instrumentation amplifiers are often subjected to input overloads, i.e., voltage levels in excess of their full scale for the selected gain range or even in excess of the supply voltage. These overloads fall into two general classes: steady state and transient (ESD, etc.), both of which occur for only a fraction of a second. With 3-op amp in-amp designs, when operating at low gains (10 or less), the gain resistor acts as a current-limiting element in series with their resistor inputs. At high gains, the lower value of R_G may not adequately protect the inputs from excessive currents.

Standard practice is to place current-limiting resistors in each input, but adding this protection also increases the circuit's noise level. A reasonable balance needs to be found between the protection provided and the increased resistor (Johnson) noise introduced. Circuits using in-amps with a relatively high noise level can tolerate more series protection without seriously increasing their total circuit noise.

Of course, the less added noise the better, but a good guideline is that circuits needing this extra protection can easily tolerate resistor values that generate 30% of the total circuit noise. For example, a circuit using an in-amp with a rated noise level of 20 nV/√Hz can tolerate an additional 6 nV/√Hz of Johnson noise.

Use the following cookbook method to translate this number into a practical resistance value. The Johnson noise of a 1 kΩ resistor is approximately 4 nV/√Hz. This value varies as the square root of the resistance. So, a 20 kΩ resistor would have √20 times as much noise as the 1 kΩ resistor, which is 17.88 nV/√Hz (4.4721 × 4 nV/√Hz). Because *both* inputs need to be protected, two resistors are needed, and their combined noise will add as the square root of the number of resistors (the root sum of squares value). In this case, the total added noise from the two 20 kΩ resistors will be 25.3 nV/√Hz (17.88 × 1.414).

Figure 5-9 provides details on the input architecture of the AD8221 in-amp. As shown, they have internal 400 Ω resistors that are in series with each input transistor junction.

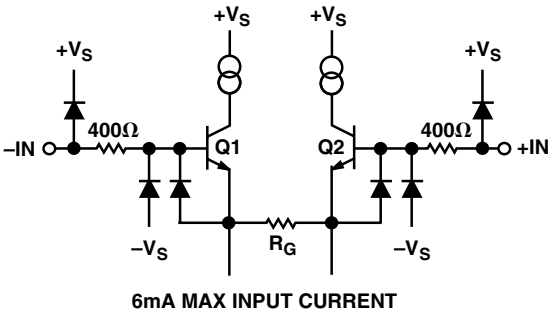


Figure 5-9. AD8221 in-amp input circuit.

The AD8221 was designed to handle maximum input currents of 6 mA steady state (or dc), at room temperature. Its internal resistors and diodes will protect the device from input voltages 0.7 V above the positive supply, or 2.4 V more negative than the minus supply (6 mA × 0.4 kΩ). Therefore, for ±15 V supplies, the maximum safe input level is +15.7 V, –17.4 V. Additional external series resistors can be added to increase this level considerably, at the expense of a higher circuit noise level.

The AD8221 in-amp is a very low noise device, with a maximum (e_{NI}) 8 nV/√Hz. A single 1 kΩ resistor will add approximately 4 nV/√Hz of Johnson noise. The addition of this resistor would raise the maximum dc level to approximately 22.5 V above each supply or ±37.5 V with ±15 V supplies.

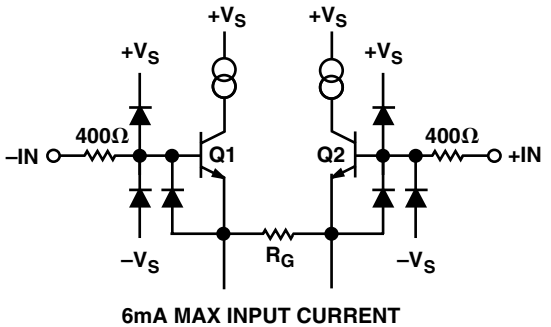


Figure 5-10. AD8222 and AD8225 in-amp input circuit.

The AD8222 and AD8225 have a very similar input section to that of the AD8221. Except that now, all six diodes are located on the Q1/Q2 side of the 400 Ω input resistor (see Figure 5-10).

Figure 5-11 shows the input section of the AD620 series (AD620, AD621, and AD622) in-amps. This is very similar to that of the AD8221: Both use a 400 Ω resistor in series with each input, and both use diode protection. The chief differences are the four additional AD8221 diodes. One set is tied between each input and the positive supply, and the other set is connected between the base of each input transistor and the negative supply. The AD620 uses its 400 Ω internal resistor and a single set of diodes to protect against negative input voltages. For positive voltage overloads, it relies on its own base-emitter input junction to act as the clamping diode.

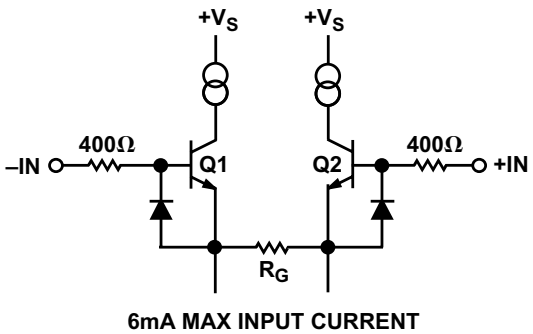


Figure 5-11. AD620 series (AD620, AD621, and AD622) in-amp input circuit.

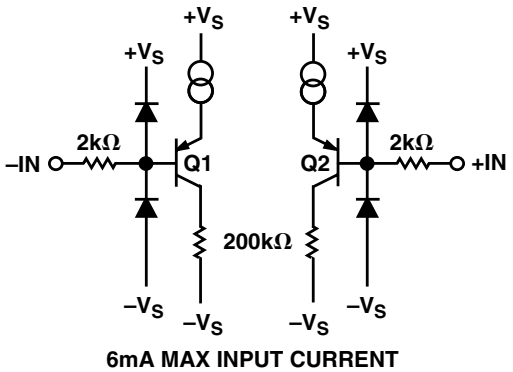


Figure 5-12. AD627 in-amp input circuit.

The AD627 can tolerate 20 mA transient input currents (Figure 5-12). In addition, it has built-in 2 kΩ resistors and can handle input voltages 40 volts higher than its supply lines (20 mA × 2 kΩ). This level of protection is quite beneficial. Because of its low power, many of the AD627's applications will use a low voltage single power supply. If even more protection is needed, quite large external resistors can be added without seriously degrading the AD627's 38 nV/√Hz noise level. In this case, adding two 5 kΩ resistors will raise the circuit's noise approximately 13 nV/√Hz (30 percent) but would provide an additional ±100 V of transient overload protection.

Figure 5-13 shows the input architecture of the AD623 in-amp. In this design, the internal (ESD) diodes are located *before* the input resistors and, as a consequence, provide less protection than the designs previously discussed. The AD623 can tolerate 10 mA maximum input current, but in many cases, some external series resistance will be needed to keep input current below this level.

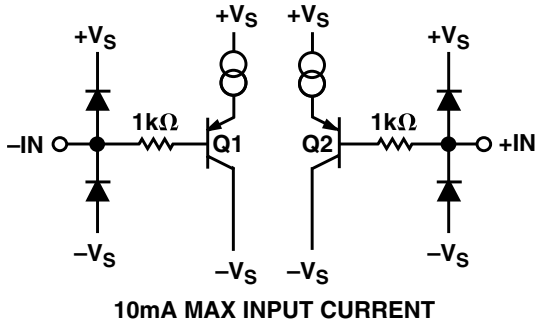


Figure 5-13. AD623 in-amp input circuit.

Since the AD623's device noise is approximately 35 nV/√Hz, up to 5 kΩ of external resistance can be added here to provide 50 V of dc overload protection, while only increasing input noise to 38 nV/√Hz total.

Figure 5-14 shows the simplified input circuitry for the AD8230 zero-drift in-amp. As shown, the AD8230 only has a single ESD diode connected between each input and the negative supply line. This diode offers ESD protection for negative pulses larger than 0.7 below the negative supply. However, it was not designed to protect the in-amp against positive voltage transients or long duration voltage overloads in either direction. To protect against these, external low leakage diodes and resistors are needed, as shown in Figure 5-20.

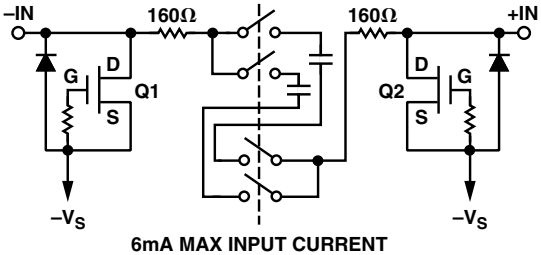


Figure 5-14. AD8230 in-amp input circuit.

Figure 5-15 is a simplified diagram showing the input structure for the AD8220 JFET in-amp. The input circuit has a very high impedance: typically 1000 GΩ and 6 pF. There are two ESD protection diodes at each input but no internal series resistance between the input terminals and the JFET input stage. Therefore, external resistors need to be added to limit the current in applications subject to an input overvoltage condition.

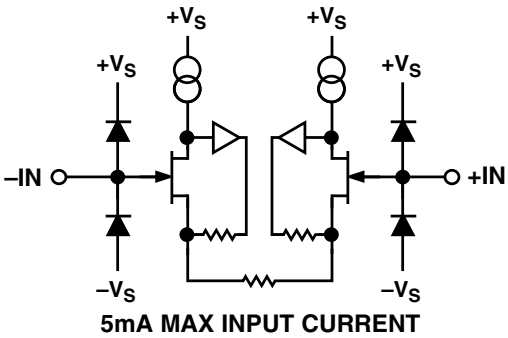


Figure 5-15. AD8220 in-amp input circuit.

Figure 5-16 shows a simplified version of the AD8250 input circuitry. Here, two internal resistors and two diodes protect each input. The AD8250 can tolerate maximum sustained input currents of 20 mA. Note that there are two pairs of input protection resistors—one between each input and the two ESD diodes, and the other between these diodes and the transistor base. This offers more protection to the transistor bases than to the ESD diodes. Therefore, designers should take precautions to protect the ESD diodes from being destroyed.

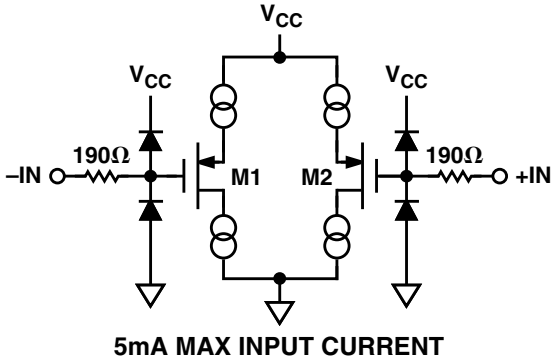


Figure 5-17. AD8553 in-amp simplified input circuit.

Figure 5-17 shows the input section of the AD8553 zero drift in-amp. This has a 190 Ω internal protection resistor between each input pin and the diode clamping circuitry.

The maximum input current of the AD8553 is approximately 5 mA, so additional external resistance may be needed in some applications (see table 5-2).

Also note that when the input voltage approaches $V_{CC} - 0.2$ V (outside the input common-mode range), current will begin to flow into the inputs of the AD8553. If the enable pin is also held low during this period of time, the output of the AD8553 will no longer be high impedance. In some applications, multiple AD8553 instrumentation amplifier outputs can be connected together to mux many inputs to one output. In these applications, only one AD8553 enable pin will be high, while all of the other AD8553 enable pins will be low.

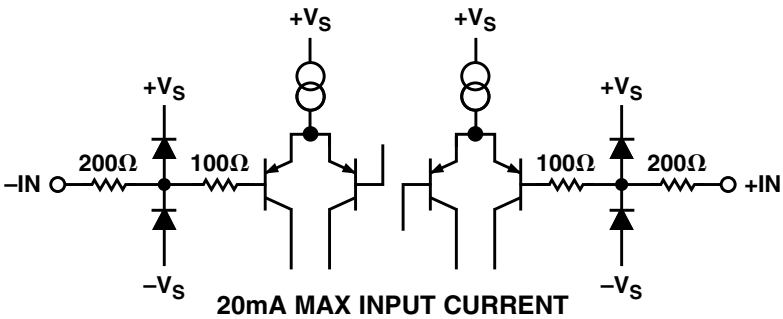


Figure 5-16. AD8250 in-amp input circuit.

If an input overload voltage of V_{CC} – 0.2 V or greater occurs on any of the AD8553 instrumentation amplifier inputs while its enable pin is low, the output of that amplifier can overload the AD8553 that is driving the output (enable pin is high).

The AD8555 and AD8556 products are instrumentation amplifiers designed to be used in sensor applications. Figure 5-18 is a simplified input circuit for the AD8555. Here, protection diodes are connected between each input terminal and the supplies. The input signal then travels through a series resistor before arriving at the amplification and switching circuitry.

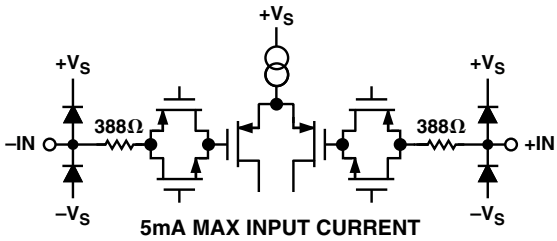


Figure 5-18. AD8555 in-amp simplified input circuit.

The AD8556 input circuitry (Figure 5-19) is very similar to that of the AD8555, except that there is a larger value resistor (3.6 kΩ) and other components between the diode and the amplifying and switching circuitry. These provide an internal RFI/EMI filtering capability.

Because the input circuitry in both products lacks an internal resistor, before the first set of clamping diodes, some external resistance is usually necessary to ensure adequate overvoltage protection.

Table 5-2 provides recommended series protection resistor values for a 10% or 40% increase in circuit noise.

Table 5-2. Recommended Series Protection Resistor Values

Device	In-Amp Noise (e_{NI})	Max Input Overload Current	Recommended External Protection Resistors Adding Additional Noise*	
			of 10%	of 40%
AD8220	15 nV/√Hz	5 mA	1.74 kΩ	6.98 kΩ
AD8221	8 nV/√Hz	6 mA	500 Ω	2.0 kΩ
AD8222	8 nV/√Hz	6 mA	500 Ω	2.0 kΩ
AD8225	8 nV/√Hz	6 mA	500 Ω	2.0 kΩ
AD8230	160 nV/√Hz	6 mA	4.99 kΩ	4.99 kΩ
AD8250	13 nV/√Hz	20 mA	1.30 kΩ	5.23 kΩ
AD8251	13 nV/√Hz	20 mA	1.30 kΩ	5.23 kΩ
AD8553	30 nV/√Hz	5 mA	6.98 kΩ	28.0 kΩ
AD8555	32 nV/√Hz	5 mA	8.06 kΩ	32.4 kΩ
AD8556	32 nV/√Hz	5 mA	8.06 kΩ	32.4 kΩ
AD620	9 nV/√Hz	6 mA	634 Ω	2.55 kΩ
AD621	9 nV/√Hz	6 mA	634 Ω	2.55 kΩ
AD622	9 nV/√Hz	6 mA	634 Ω	2.55 kΩ
AD623	35 nV/√Hz	10 mA	9.53 kΩ	38.3 kΩ
AD627	38 nV/√Hz	20 mA	11.3 kΩ	45.3 kΩ

*This noise level is for two resistors, one in series with each input.

Adding External Protection Diodes

Device input protection may be increased with the addition of external clamping diodes as shown in Figure 5-20. As high current diodes are used, input protection is increased, which allows the use of much lower resistance input protection resistors that, in turn, reduces the circuit's noise.

Unfortunately, most ordinary diodes (Schottky, silicon, etc.) have high leakage currents that will cause large offset errors at the in-amp's output; this leakage increases exponentially with temperature. This tends to rule out the use of external diodes in applications where the in-amp is used with high impedance sources.

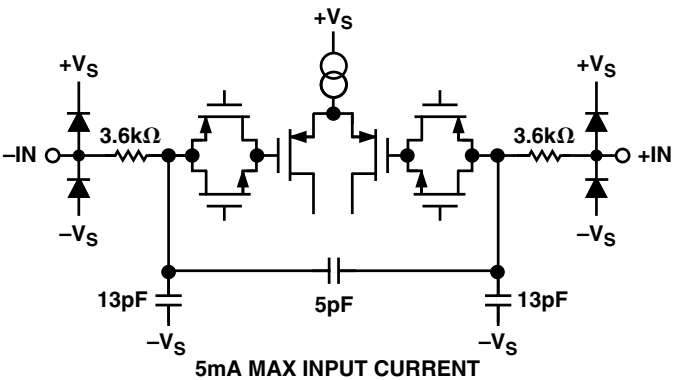
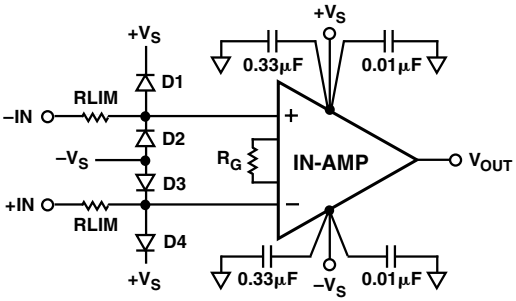


Figure 5-19. AD8556 simplified input circuit.

Specialty diodes with much lower leakage are available, but these are often difficult to find and are expensive. For the vast majority of applications, limiting resistors alone provide adequate protection for ESD and longer duration input transients.



D1–D4 ARE INTERNATIONAL RECTIFIER SD101 SERIES FAST SCHOTTKY BARRIER RECTIFIERS

Figure 5-20. Using external components to increase input protection.

Despite their limitations, external diodes are often required in some special applications, such as electric shock defibrillators, which utilize short duration, high voltage pulses. The combination of external diodes and very large input resistors (as high as 100 kΩ) may be needed to adequately protect the in-amp.

It is a good idea to check the diodes' specifications to ensure that their conduction begins well before the in-amp's internal protection diodes start drawing current. Although they provide excellent input protection, standard Schottky diodes can have leakage up to several mA. However, as in the example of Figure 5-20, fast Schottky barrier rectifiers, such as the international rectifier type SD101 series, can be used; these devices have 200 nA max leakage currents and 400 mW typical power dissipation.

ESD and Transient Overload Protection

Protecting in-amp inputs from high voltage transients and ESD events is very important for a circuit's long-term reliability. Power dissipation is often a critical factor, as input resistors, whether internal or external, must be able to handle most of the power of the input pulse without failing.

ESD events, while they may be very high voltage, are usually of very short duration and are normally one-time events. Since the circuit has plenty of time to cool down before the next event occurs, modest input protection is sufficient to protect the device from damage.

On the other hand, regularly occurring short duration input transients can easily overheat and burn out the input resistors or the in-amps input stage. A 1 kΩ resistor, in series with an in-amp input terminal drawing 20 mA, will dissipate 0.4 W, which can easily be handled by a standard 0.5 W or greater surface-mount resistor. If the input current is doubled, power consumption quadruples as it increases as the square of the input current (or as the square of the applied voltage).

Although it is a simple matter to use a higher power protection resistor, this is a dangerous practice, as the power dissipation will also increase in the in-amp's input stage. This can easily lead to device failure (see the preceding section on input protection basics for input current limitations of ADI in-amps). Except for ESD events, it is always best to adopt a conservative approach and treat all transient input signals as full duration inputs.

Designs that are expected to survive such events over long periods of time must use resistors with enough resistance to protect the in-amp's input circuitry from failure and enough power to prevent resistor burnout.

DESIGN ISSUES AFFECTING DC ACCURACY

The modern in-amp is continually being improved, providing the user with ever increasing accuracy and versatility at a lower price. Despite these improvements in product performance, there remain some fundamental applications issues that seriously affect device accuracy. Now that low cost, high resolution ADCs are commonly used, system designers need to ensure that if an in-amp is used as a preamplifier ahead of the converter, the in-amp's accuracy matches that of the ADC.

Designing for the Lowest Possible Offset Voltage Drift

Offset drift errors include not just those associated with the active device being used (IC in-amp or discrete in-amp design using op amps), but also thermocouple effects in the circuit's components or wiring. The in-amp's input bias and input offset currents flowing through unbalanced source impedances also create additional offset errors. In discrete op amp in-amp designs, these errors can increase with temperature unless precision op amps are used.

Designing for the Lowest Possible Gain Drift

When planning for gain errors, the effects of board layout, the circuit's thermal gradients, and the characteristics of any external gain setting resistors are often overlooked. A gain resistor's absolute tolerance, its thermal temperature coefficient, its physical position relative to other resistors in the same gain network, and even its physical orientation (vertical or horizontal) are all-important design considerations if high dc accuracy is needed.

In many ADC preamp circuits, an external user-selected resistor sets the gain of the in-amp, so the absolute tolerance of this resistor and its variation over temperature, compared to that of the IC's on-chip resistors, will affect the circuit's gain accuracy. Resistors commonly used include through-hole 1% 1/4 W metal film types and 1% 1/8 W chip resistors. Both types typically have a 100 ppm/°C temperature coefficient. However, some chip resistors can have TCs of 200 ppm/°C or even 250 ppm/°C.

Even when a 1% 100 ppm/°C resistor is used, the gain accuracy of the in-amp will be degraded. The resistor's initial room temperature accuracy is only ±1%, and the resistor will drift another 0.01% (100 ppm/°C) for every °C change in temperature. The initial gain error can easily be subtracted out in software, but to correct for the error vs. temperature, frequent recalibrations (and a temperature sensor) would be required.

If the circuit is calibrated initially, the overall gain accuracy is reduced to approximately 10 bits (0.1%) accuracy for a 10°C change. An in-amp with a standard 1% metal film gain resistor should never be used ahead of even a 12-bit converter: It would destroy the accuracy of a 14-bit or 16-bit converter.

Additional error sources associated with external resistors also affect gain accuracy. The first are variations in resistor heating caused by input signal level. Figure 5-21, a simple op amp voltage amplifier, provides a practical example.

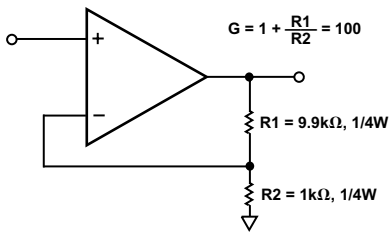


Figure 5-21. An example of how differences in input signal level can introduce gain errors.

Under zero signal conditions, there is no output signal and no resistor heating. When an input signal is applied, however, an amplified voltage appears at the op amp output. When the amplifier is operating with gain, Resistor R1 will be greater than R2. This means that there will be more voltage across R1 than across R2. The power dissipated in each resistor equals the square of the voltage across it divided by its resistance in ohms. The power dissipated and, therefore, the internal heating of the resistor will increase in proportion to the value of the resistor.

In the example, R1 is 9.9 kΩ and R2 is 1 kΩ. Consequently, R1 will dissipate 9.9 times more power than R2. This leads to a gain error that will vary with input level. The use of resistors with different temperature coefficients can also introduce gain errors.

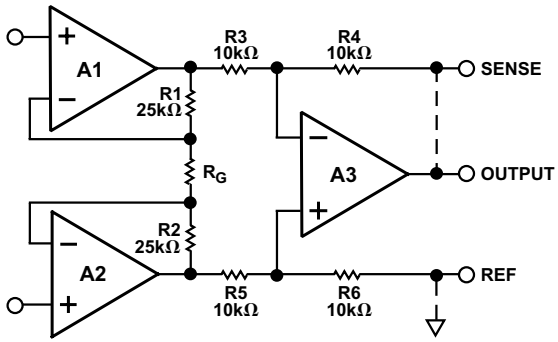


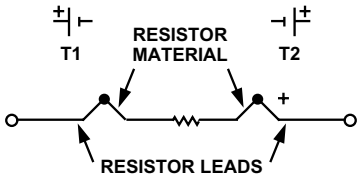
Figure 5-22. A typical discrete 3-op amp in-amp using large value, low TC feedback resistors.

Even when resistors with matched temperature coefficients (TC) are used, gain errors that vary with input signal level can still occur. The use of larger (i.e., higher power) resistors will reduce these effects, but accurate, low TC power resistors are expensive and hard to find.

When a discrete 3-op amp in-amp is used, as shown in Figure 5-22, these errors will be reduced. In a 3-op amp in-amp, there are two feedback resistors, R1 and R2, and one gain resistor, R_G. Since the in-amp uses two feedback resistors while the op amp uses only one, each of the in-amp's resistors only needs to dissipate half the power (for the same gain). Monolithic in-amps, such as the AD620, offer a further advantage by using relatively large value (25 kΩ) feedback resistors. For a given gain and output voltage, large feedback resistors will dissipate less power (i.e., $P = V^2/R_F$). Of course, a discrete in-amp can be designed to use large value, low TC resistors as well, but with added cost and complexity.

Another less serious but still significant error source is the so-called thermocouple effect, sometimes referred to as thermal EMF. This occurs when two different conductors, such as copper and metal film, are tied together. When this bimetallic junction is heated, a simple thermocouple is created. When using similar metals, such as a copper-to-copper junction, a thermoelectric error voltage of up to 0.2 mV/°C may be produced. An example of these effects is shown in Figure 5-23.

A final error source occurs when there is a thermal gradient across the external gain resistor. Something as simple as mounting a resistor on end to conserve board space will invariably produce a temperature gradient across the resistor. Placing the resistor flat down against the PC board will cure this problem unless there is air flowing along the axis of the resistor (where the air flow cools one side of the resistor more than the other side). Orienting the resistor so that its axis is perpendicular to the airflow will minimize this effect.



TYPICAL RESISTOR THERMOCOUPLE EMFs	
• CARBON COMPOSITION	400μV/°C
• METAL FILM	20μV/°C
• EVENOHM OR MANGANIN WIRE-WOUND	2μV/°C
• RCD COMPONENTS HP-SERIES	0.05μV/°C

Figure 5-23. Thermocouple effects inside discrete resistors.

Practical Solutions

As outlined, a number of dc offset and gain errors are introduced when external resistors are used with a monolithic in-amp. Discrete designs tend to have even larger errors. There are three practical solutions to this problem: use higher quality resistors, use software correction, or, better still, use an in-amp that has *all* of its gain resistors on-chip, such as the AD621.

Option 1: Use a Better Quality Gain Resistor

As a general rule, only 12-bit or 13-bit gain performance is possible using commonly available 1% resistors, which assumes that some type of initial calibration is performed.

A practical solution to this problem is to simply use a better quality resistor. A significant improvement can be made using a 0.1%, 1/10 W, surface-mount resistor. Aside from having a 10× better initial accuracy, it typically has a TC of only 25 ppm/°C, which will provide better than 13-bit accuracy over a 10°C temperature range.

If even better gain accuracy is needed, there are specialty houses that sell resistors with lower TCs, but these are usually expensive military varieties.

Option 2: Use a Fixed-Gain In-Amp

By far, the best overall dc performance is provided by using a monolithic in-amp, such as the AD621 or AD8225, in which all the resistors are contained within the IC. Now all resistors have identical TCs, all are at virtually the same temperature. Any thermal gradients across the chip are very small, and gain error drift is guaranteed and specified to very high standards.

At a gain of 10, the AD621 has a guaranteed maximum dc offset shift of less than 2.5 μV/°C and a maximum gain drift of ±5 ppm/°C, which is only 0.0005%/°C.

The AD8225 is an in-amp with a fixed gain of 5. It has a maximum offset shift of 2 μV/°C and a maximum drift of 0.3 μV/°C.

RTI AND RTO ERRORS

Another important design consideration is how circuit gain affects many in-amp error sources such as dc offset and noise. An in-amp should be regarded as a two stage amplifier with both an input and an output section. Each section has its own error sources.

Because the errors of the output section are multiplied by a fixed gain (usually 2), this section is often the principal error source at low circuit gains. When the in-amp is operating at higher gains, the gain of the input stage is increased. As the gain is raised, errors contributed by the input section are multiplied, while output errors are not. So, at high gains, the input stage errors dominate.

Since device specifications on different data sheets often refer to different types of errors, it is very easy for the unwary designer to make an inaccurate comparison between products. Any (or several) of four basic error categories may be listed: input errors, output errors, total error RTI, and total error RTO. Here follows an attempt to list, and hopefully simplify, an otherwise complicated set of definitions.

Input errors are those contributed by the amplifier's input stage alone; output errors are those due to the output section. Input related specifications are often combined and classified together as a referred to input (RTI) error, while all output related specifications are considered referred to output (RTO) errors.

For a given gain, an in-amp's input and output errors can be calculated using the following formulas:

$$\textit{Total Error, RTI} = \textit{Input Error} + (\textit{Output Error}/\textit{Gain})$$

$$\textit{Total Error, RTO} = (\textit{Gain} \times \textit{Input Error}) + \textit{Output Error}$$

Sometimes the specifications page will list an error term as RTI or RTO for a specified gain. In other cases, it is up to the user to calculate the error for the desired gain.

Offset Error

Using the **AD620A** as an example, the total voltage offset error of this in-amp when operating at a gain of 10 can be calculated using the individual errors listed on its specifications page. The (typical) input offset of the AD620 (V_{OSI}) is listed as 30 μV. Its output offset (V_{OSO}) is listed as 400 μV. Thus, the total voltage offset referred to input (RTI) is equal to

$$Total\ RTI\ Error = V_{OSI} + (V_{OSO}/G) = 30\ \mu V + (400\ \mu V/10) = 30\ \mu V + 40\ \mu V = 70\ \mu V$$

The total voltage offset referred to the output (RTO) is equal to

$$Total\ Offset\ Error\ RTO = (G\ (V_{OSI})) + V_{OSO} = (10\ (30\ \mu V)) + 400\ \mu V = 700\ \mu V$$

Note that the two error numbers (RTI vs. RTO) are different: the RTO numbers are 10× larger, and logically they should be, as at a gain of 10, the error at the output of the in-amp should be 10 times the error at its input.

Noise Errors

In-amp noise errors also need to be considered in a similar way. Since the output section of a typical 3-op amp in-amp operates at unity gain, the noise contribution from the output stage is usually very small. But there are 3-op amp in-amps that operate the output stage at higher gains, and 2-op amp in-amps regularly operate the second amplifier at gain. When either section is operated at gain, its noise is amplified along with the input signal. Both RTI and RTO noise errors are calculated the same way as offset errors, except that the noise of two sections adds as the root mean square. That is,

$$Input\ Noise = eni, Output\ Noise = eno$$

$$Total\ Noise\ RTI = \sqrt{(eni)^2 + (eno/Gain)^2}$$

$$Total\ Noise\ RTO = \sqrt{(Gain(eni))^2 + (eno)^2}$$

For example, the (typical) noise of the AD620A is specified as 9 nV/√Hz eni and 72 nV/√Hz eno. Therefore, the total RTI noise of the AD620A operating at a gain of 10 is equal to

$$Total\ Noise\ RTI = \sqrt{(eni)^2 + (eno/Gain)^2} = \sqrt{(9)^2 + (72/10)^2} = 11.5\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$$

REDUCING RFI RECTIFICATION ERRORS IN IN-AMP CIRCUITS

Real-world applications must deal with an ever increasing amount of radio frequency interference (RFI). Of particular concern are situations in which signal transmission lines are long and signal strength is low. This is the classic application for an in-amp, since its inherent common-mode rejection allows the device to extract weak differential signals riding on strong common-mode noise and interference.

One potential problem that is frequently overlooked, however, is that of radio frequency rectification inside the in-amp. When strong RF interference is present, it may become rectified by the IC and then appear as a dc output offset error. Common-mode signals present at an in-amp's input are normally greatly reduced by the amplifier's common-mode rejection.

Unfortunately, RF rectification occurs because even the best in-amps have virtually no common-mode rejection at frequencies above 20 kHz. A strong RF signal may become rectified by the amplifier's input stage and then appear as a dc offset error. Once rectified, no amount of low-pass filtering at the in-amp output will remove the error. If the RF interference is of an intermittent nature, this can lead to measurement errors that go undetected.

Designing Practical RFI Filters

The best practical solution is to provide RF attenuation *ahead* of the in-amp by using a differential low-pass filter. The filter needs to do three things: remove as much RF energy from the input lines as possible, preserve the ac signal balance between each line and ground (common), and maintain a high enough input impedance over the measurement bandwidth to avoid loading the signal source.

Figure 5-24 provides a basic building block for a wide number of differential RFI filters. Component values shown were selected for the AD8221, which has a typical –3 dB bandwidth of 1 MHz and a typical voltage noise level of 7 nV/√Hz. This same filter is recommended for the AD8222 dual in-amp and for the AD8220 JFET input in-amp. In addition to RFI suppression, the filter provides additional input overload protection, as resistors R1a and R1b help isolate the in-amp's input circuitry from the external signal source.

Figure 5-25 is a simplified version of the RFI circuit. It reveals that the filter forms a bridge circuit whose output appears across the in-amp's input pins. Because of this, any mismatch between the time constants of C1a/R1a and C1b/R1b will unbalance the bridge and reduce high frequency common-mode rejection. Therefore, resistors R1a and R1b and capacitors C1a and C1b should always be equal.

As shown, C2 is connected across the bridge output so that C2 is effectively in parallel with the series combination of C1a and C1b. Thus connected, C2 very effectively reduces any ac CMR errors due to mismatching. For example, if C2 is made 10 times larger than C1, this provides a 20× reduction in CMR errors due to C1a/C1b mismatch. Note that the filter does not affect dc CMR.

The RFI filter has two different bandwidths: differential and common mode. The differential bandwidth defines the frequency response of the filter with a differential input signal applied between the circuit's two inputs, +IN and –IN. This RC time constant is established by the sum of the two equal-value input resistors (R1a, R1b), together with the differential capacitance, which is C2 in parallel with the series combination of C1a and C1b.

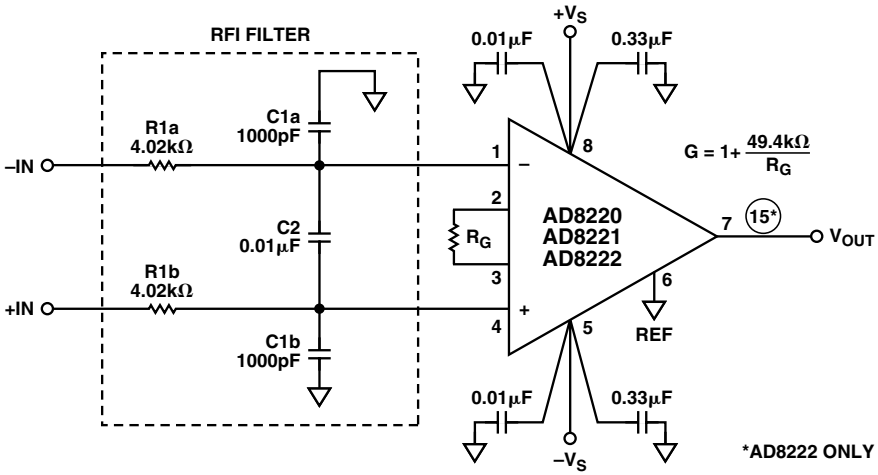


Figure 5-24. LP filter circuit used to prevent RFI rectification errors in AD8220, AD8221, and AD8222 in-amps.

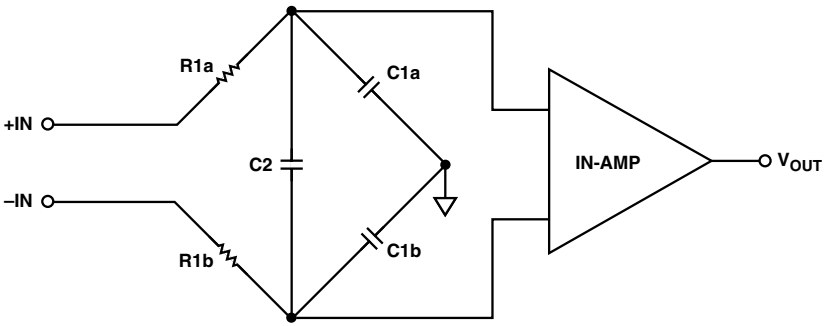


Figure 5-25. Capacitor C2 shunts C1a/C1b and very effectively reduces ac CMR errors due to component mismatching.

The –3 dB *differential* bandwidth of this filter is equal to

$$BW_{DIFF} = \frac{1}{2\pi R(2C2 + C1)}$$

The common-mode bandwidth defines what a common-mode RF signal *sees* between the two inputs tied together and ground. It's important to realize that C2 does not affect the bandwidth of the common-mode RF signal, as this capacitor is connected between the two inputs (helping to keep them at the same RF signal level). Therefore, common-mode bandwidth is set by the parallel impedance of the two RC networks (R1a/C1a and R1b/C1b) to ground.

The –3 dB *common-mode* bandwidth is equal to

$$BW_{CM} = \frac{1}{2\pi R1C1}$$

Using the circuit of Figure 5-24, with a C2 value of 0.01 μF as shown, the –3 dB differential signal bandwidth is approximately 1900 Hz. When operating at a gain of 5, the circuit's measured dc offset shift over a frequency range of 10 Hz to 20 MHz was less than 6 μV RTI. At unity gain, there was no measurable dc offset shift.

The RFI filter should be built using a PC board with ground planes on both sides. All component leads should be made as short as possible. The input filter common should be connected to the amplifier common using the most direct path. Avoid building the filter and the in-amp circuits on separate boards or in separate enclosures, as this extra lead length can create a loop antenna. Instead, physically locate the filter right at the in-amp's input terminals. A further precaution is to use good quality resistors that are both noninductive and nonthermal (low TC). Resistors R1 and R2 can be common 1% metal film units. However, all three capacitors need to be reasonably high Q, low loss components. Capacitors C1a and C1b need to be ±5% tolerance devices to avoid degrading the circuit's common-mode rejection. The traditional 5% silver micas, miniature size micas, or the new Panasonic ±2% PPS film capacitors (Digi-Key part # PS1H102G-ND) are recommended.

Selecting RFI Input Filter Component Values Using a Cookbook Approach

The following general rules will greatly ease the design of an RC input filter.

1. First, decide on the value of the two series resistors while ensuring that the previous circuitry can adequately drive this impedance. With typical values between 2 kΩ and 10 kΩ, these resistors should not contribute more noise than that of the in-amp itself. Using a pair of 2 kΩ resistors will add a Johnson noise of 8 nV/√Hz; this increases to 11 nV/√Hz with 4 kΩ resistors and to 18 nV/√Hz with 10 kΩ resistors.
2. Next, select an appropriate value for capacitor C2, which sets the filter's differential (signal) bandwidth. It's always best to set this as low as possible without attenuating the input signal. A differential bandwidth of 10 times the highest signal frequency is usually adequate.
3. Then select values for capacitors C1a and C1b, which set the common-mode bandwidth. For decent ac CMR, these should be 10% the value of C2 or less. The common-mode bandwidth should always be less than 10% of the in-amp's bandwidth at unity gain.

Specific Design Examples

An RFI Circuit for AD620 Series In-Amps

Figure 5-26 is a circuit for general-purpose in-amps such as the AD620 series, which have higher noise levels (12 nV/√Hz) and lower bandwidths than the AD8221. Accordingly, the same input resistors were used, but capacitor C2 was increased approximately five times to 0.047 µF to provide adequate RF attenuation. With the values shown, the circuit's –3 dB bandwidth is approximately 400 Hz; the bandwidth may be increased to 760 Hz by reducing the resistance of R1 and R2 to 2.2 kΩ. Note that this increased bandwidth does not come free. It requires the circuitry preceding the in-amp to drive a lower impedance load and results in somewhat less input overload protection.

An RFI Circuit for Micropower In-Amps

Some in-amps are more prone to RF rectification than others and may need a more robust filter. A micropower in-amp, such as the AD627, with its low input stage operating current, is a good example. The simple expedient of increasing the value of the two input resistors, R1a/R1b, and/or that of capacitor C2, will provide further RF attenuation, at the expense of a reduced signal bandwidth.

Since the AD627 in-amp has higher noise (38 nV/√Hz) than general-purpose ICs, such as the AD620 series devices, higher value input resistors can be used without seriously degrading the circuit's noise performance. The basic RC RFI circuit of Figure 5-24 was modified to include higher value input resistors, as shown in Figure 5-27.

The filter bandwidth is approximately 200 Hz. At a gain of 100, the maximum dc offset shift with a 1 V p-p input applied is approximately 400 µV RTI over an input range of 1 Hz to 20 MHz. At the same gain, the circuit's RF signal rejection (RF level at output/RF applied to the input) will be better than 61 dB.

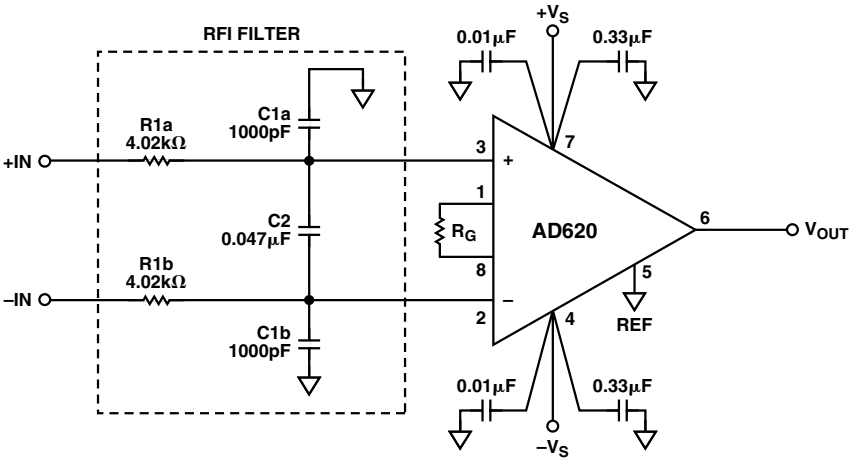


Figure 5-26. RFI circuit for AD620 series in-amp.

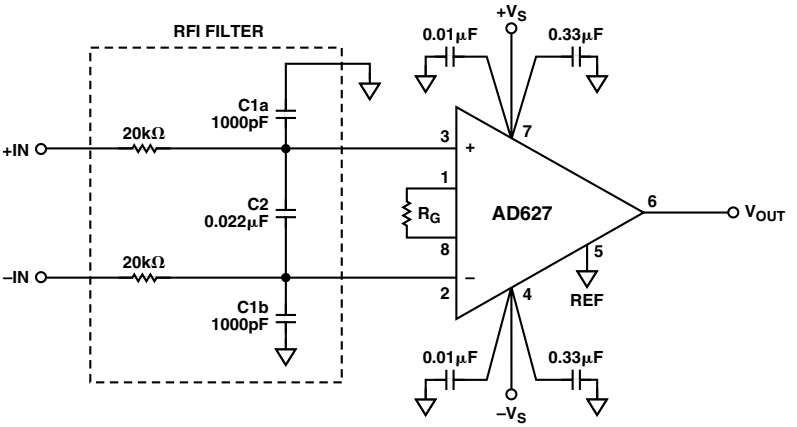


Figure 5-27. RFI suppression circuit for the AD627.

An RFI Filter for the AD623 In-Amp

Figure 5-28 shows the recommended RFI circuit for use with the AD623 in-amp. Because this device is less prone to RFI than the AD627, the input resistors can be reduced in value from 20 kΩ to 10 kΩ; this increases the circuit's signal bandwidth and lowers the resistors' noise contribution. Moreover, the 10 kΩ resistors still provide very effective input protection. With the values shown, the bandwidth of this filter is approximately 400 Hz. Operating at a gain of 100, the maximum dc offset shift with a 1 V p-p input is less than 1 μV RTI. At the same gain, the circuit's RF signal rejection is better than 74 dB.

AD8225 RFI Filter Circuit

Figure 5-29 shows the recommended RFI filter for this in-amp. The AD8225 in-amp has a fixed gain of 5 and a bit more susceptibility to RFI than the AD8221. Without the RFI filter, with a 2 V p-p, 10 Hz to 19 MHz sine wave applied, this in-amp measures about 16 mV RTI of dc offset. The filter used provides a heavier RF attenuation than that of the AD8221 circuit by using larger resistor values: 10 kΩ instead of 4 kΩ. This is permissible because of the AD8225's higher noise level. Using the filter, there was no measurable dc offset error.

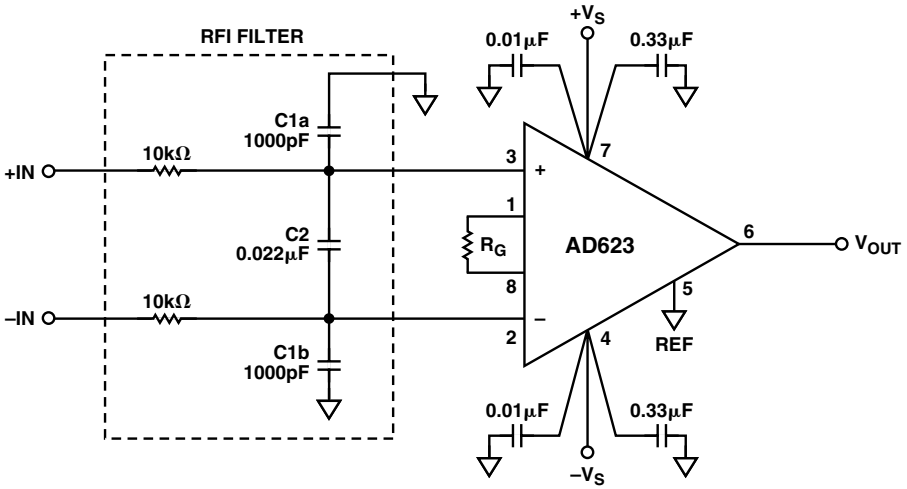


Figure 5-28. AD623 RFI suppression circuit.

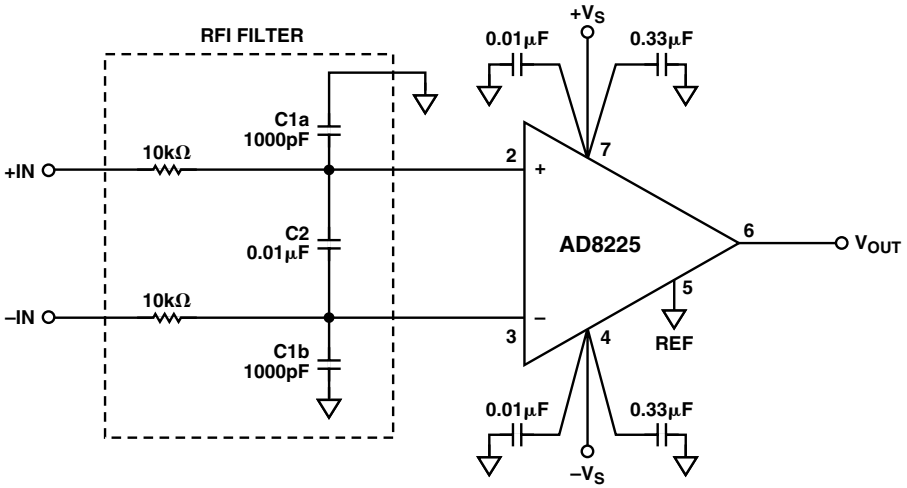


Figure 5-29. AD8225 RFI filter circuit.

AN RFI FILTER FOR THE AD8555 SENSOR AMPLIFIER

The circuit in Figure 5-30 provides good RFI suppression without reducing performance within the AD8555 pass band. Using the component values shown, this filter has a common-mode bandwidth of approximately 40 kHz. To preserve common-mode rejection in the AD8555's pass band, capacitors need to be 5% (silver mica) or better and should be placed as close to its inputs as possible. Resistors should be 1% metal film. The circuit's differential bandwidth is approximately 4 kHz when a C3 value of 0.047 μF is used.

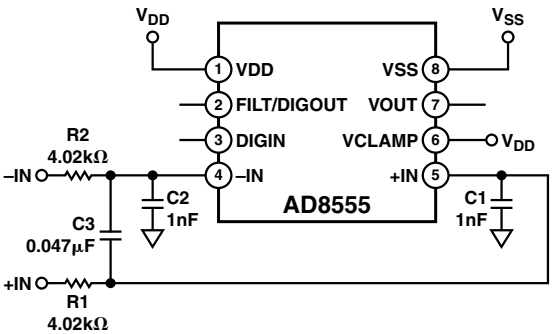


Figure 5-30. AD8555 RFI filter circuit.

In-Amps with On-Chip EMI/RFI Filtering

The AD8556 is very similar to the AD8555. The AD8556 features internal EMI filters on the –IN, +IN, FILT, and VCLAMP pins. These built-in filters on the pins limit the interference bandwidth and provide good RFI suppression without reducing performance within the pass band of the in-amp. A functional diagram of AD8556 along with its EMI/RFI filters is shown in Figure 5-31.

AD8556 has on-chip filters on its inputs, VCLAMP, and filter pins. The first-order low-pass filters inside the AD8556 are useful to reject high frequency EMI signals picked up by wires and PCB traces outside the AD8556. The most sensitive pin of any amplifier to RFI/EMI signal is the noninverting pin. Signals present at this pin appear as common-mode signals and create problems.

The filters at the input of the AD8556 have two different bandwidths: common and differential mode. The EMI filters placed on the input pins of the AD8556 reject EMI/RFI suppressions that appear as common-mode signals.

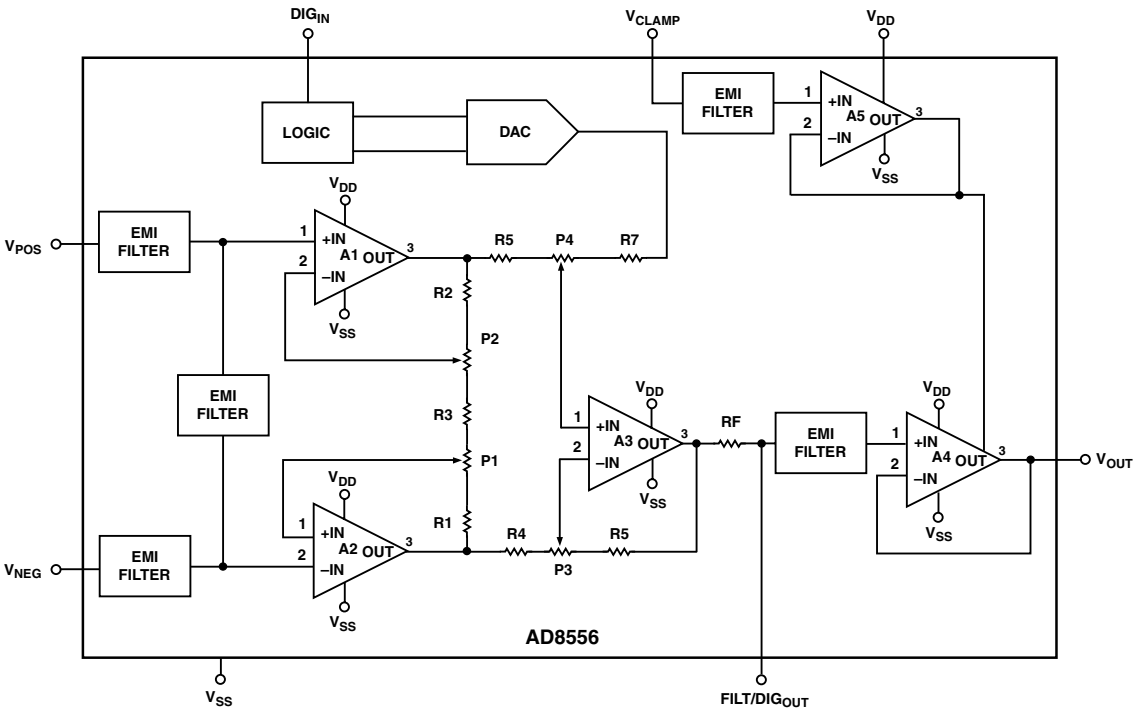


Figure 5-31. AD8556 block diagram showing on-chip EMI/RFI filter.

Figure 5-32 simulates the presence of a noisy common-mode signal, and Figure 5-33 shows the response dc values at V_{OUT}.

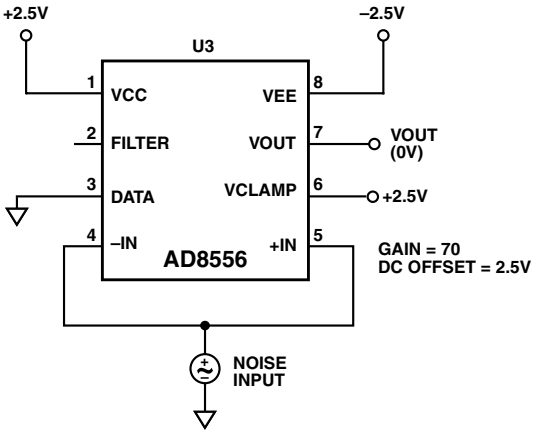


Figure 5-32. Test circuit to show AD8556 performance exposed to common-mode RFI/EMI signals.

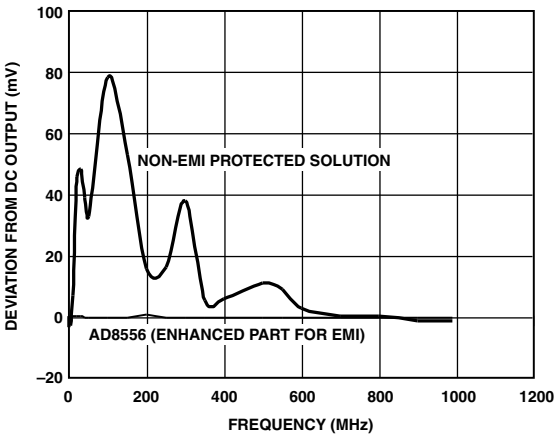


Figure 5-33. DC input offset values at V_{OUT} caused by common-mode RFI vs. frequency.

The differential bandwidth defines the frequency response of the filters with a differential signal applied between the two inputs, VPOS (that is, +IN) and VNEG (that is, –IN). Figure 5-34 shows the test circuit for AD8556 EMI/RFI susceptibility.

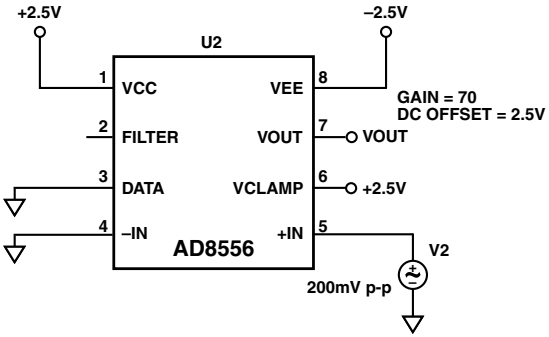


Figure 5-34. Test circuit to show AD8556 performance exposed to differential-mode RFI/EMI signals.

The response of AD8556 to EMI/RFI differential signals is shown in Figure 5-35.

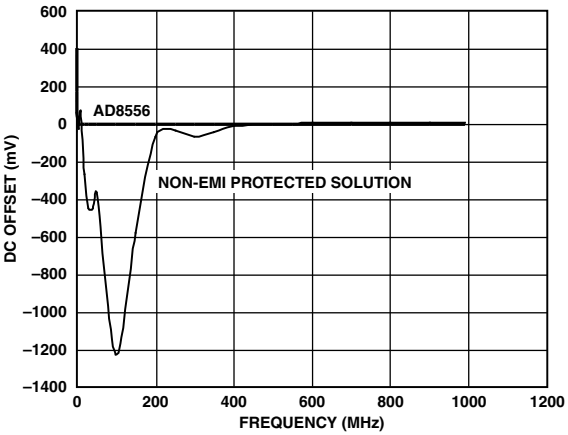


Figure 5-35. DC offset shift of AD8556 due to EMI/RFI differential signals vs. frequency.

For the most effective EMI rejection, the printed circuit board leads at VPOS and VNEG should be as similar as possible. In this way, any EMI received by the VPOS and VNEG pins will be similar (that is, a common-mode input), and rejected by the AD8556. Furthermore, additional filtering at the VPOS and VNEG pins should provide better reduction of unwanted behavior compared with filtering at the other pins.

Common-Mode Filters Using X2Y® Capacitors*

Figure 5-36 shows the connection diagram for an X2Y capacitor. These are very small, three terminal devices with four external connections—A, B, G1, and G2. The G1 and G2 terminals connect internally within the device. The internal plate structure of the X2Y capacitor forms an integrated circuit with very interesting properties. Electrostatically, the three electrical nodes form two capacitors that share the G1 and G2 terminals. The manufacturing process automatically matches both capacitors very closely. In addition, the X2Y structure includes an effective autotransformer/common-mode choke. As a result, when these devices are used for common-mode filters, they provide greater attenuation of common-mode signals above the filter's corner frequency than a comparable RC filter. This usually allows the omission of capacitor C2, with subsequent savings in cost and board space.

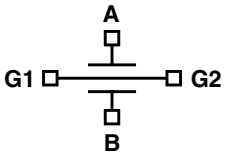


Figure 5-36. X2Y electrostatic model.

Figure 5-37a illustrates a conventional RC common-mode filter, while Figure 5-37b shows a common-mode filter circuit using an X2Y device. Figure 5-38 is a graph contrasting the RF attenuation provided by these two filters.

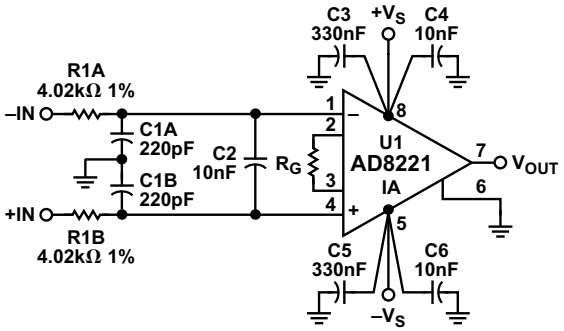


Figure 5-37a. Conventional RC common-mode filter.

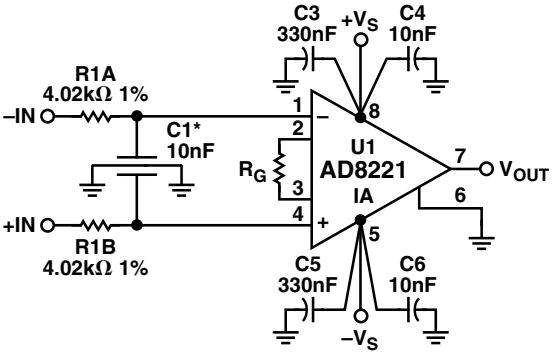


Figure 5-37b. Common-mode filter using X2Y capacitor.

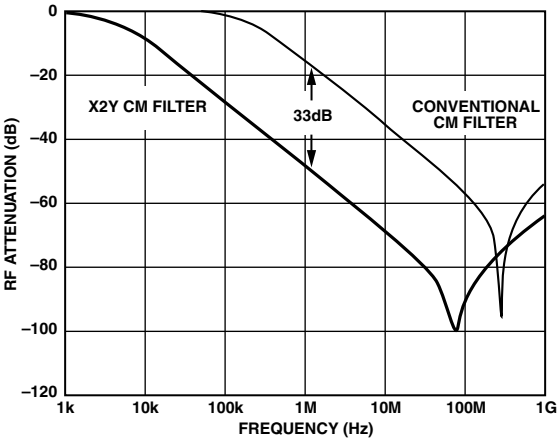


Figure 5-38. RF attenuation, X2Y vs. conventional RC common-mode filter.

*C1 is part number 500X14W103KV4. X2Y components may be purchased from Johanson Dielectrics, Sylmar, CA 91750, (818) 364-9800. For a full listing of X2Y manufacturers, visit *www.x2y.com/manufacturers*.

Using Common-Mode RF Chokes for In-Amp RFI Filters

As an alternative to using an RC input filter, a commercial common-mode RF choke may be connected in front of an in-amp, as shown in Figure 5-39. A common-mode choke is a two-winding RF choke using a common core. Any RF signals that are common to both inputs will be attenuated by the choke. The common-mode choke provides a simple means for reducing RFI with a minimum of components and provides a greater signal pass band, but the effectiveness of this method depends on the quality of the particular common-mode choke being used. A choke with good internal matching is preferred. Another potential problem with using the choke is that there is no increase in input protection as is provided by the RC RFI filters.

Using an AD620 in-amp with the RF choke specified, at a gain of 1000, and a 1 V p-p common-mode sine wave applied to the input, the circuit of Figure 5-39 reduces the dc offset shift to less than 4.5 μV RTI. The high frequency common-mode rejection ratio was also greatly improved, as shown in Table 5-3.

Table 5-3. AC CMR vs. Frequency Using the Circuit of Figure 5-39

Frequency	CMRR (dB)
100 kHz	100
333 kHz	83
350 kHz	79
500 kHz	88
1 MHz	96

Because some in-amps are more susceptible to RFI than others, the use of a common-mode choke may sometimes prove inadequate. In these cases, an RC input filter or an X2Y-based filter is a better choice.

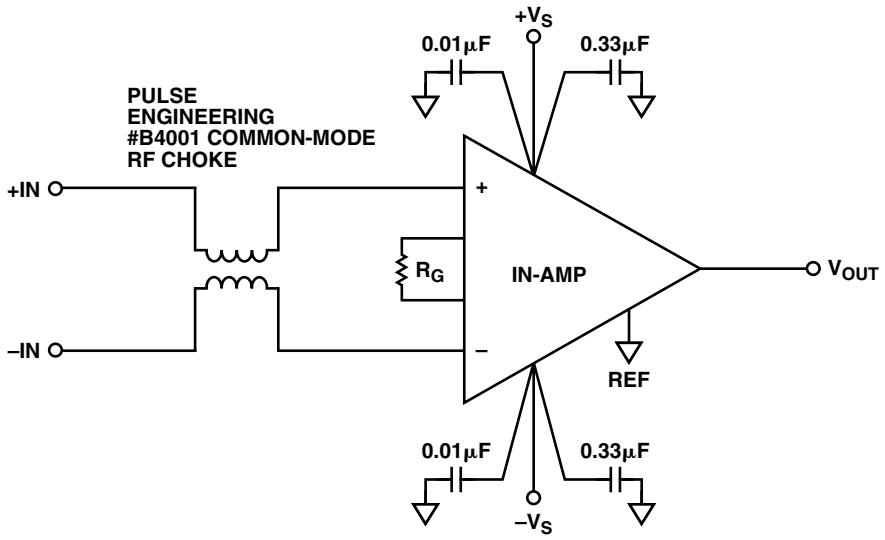


Figure 5-39. Using a commercial common-mode RF choke for RFI suppression.

RFI TESTING

Figure 5-40 shows a typical setup for measuring RFI rejection. To test these circuits for RFI suppression, connect the two input terminals together using very short leads. Connect a good quality sine wave generator to this input via a 50 Ω terminated cable.

Using an oscilloscope, adjust the generator for a 1 V peak-to-peak output at the generator end of the cable. Set the in-amp to operate at high gain (such as a gain of 100). DC offset shift is simply read directly at the in-amp's output using a DVM. For measuring high frequency CMR, use an oscilloscope connected to the in-amp output by a compensated scope probe and measure the peak-to-peak output voltage (i.e., feedthrough) vs. input frequency. When calculating CMRR vs. frequency, remember to take into account the input termination ($V_{IN}/2$) and the gain of the in-amp.

$$CMR = 20\log\frac{\left(\frac{V_{IN}}{2}\right)}{\left(\frac{V_{OUT}}{Gain}\right)}$$

USING LOW-PASS FILTERING TO IMPROVE SIGNAL-TO-NOISE RATIO

To extract data from a noisy measurement, low-pass filtering can be used to greatly improve the signal-to-noise ratio of the measurement by removing all signals that are not within the signal bandwidth. In some cases, band-pass filtering (reducing response both below and above the signal frequency) can be employed for an even greater improvement in measurement resolution.

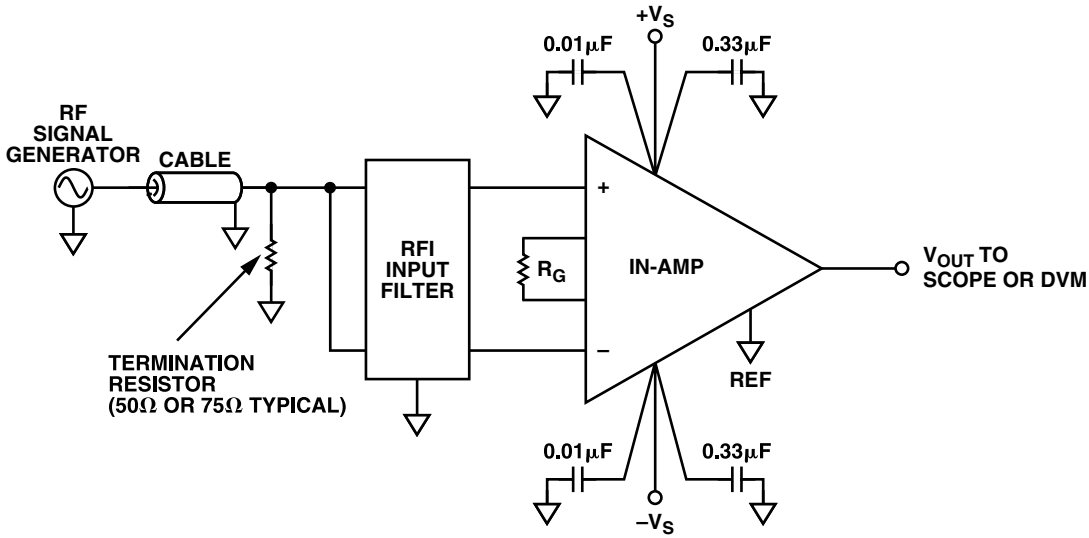


Figure 5-40. Typical test setup for measuring an in-amp's RFI rejection.

The 1 Hz, 4-pole, active filter of Figure 5-41 is an example of a very effective low-pass filter that normally would be added after the signal has been amplified by the in-amp. This filter provides high dc precision at low cost while requiring a minimum number of components.

Note that component values can simply be scaled to provide corner frequencies other than 1 Hz (see Table 5-4). If a 2-pole filter is preferred, simply take the output from the first op amp.

The low levels of current noise, input offset, and input bias currents in the quad op amp (either an **AD704** or **OP497**) allow the use of 1 MΩ resistors without sacrificing the 1 μV/°C drift of the op amp. Thus, lower capacitor values may be used, reducing cost and space.

Furthermore, since the input bias current of these op amps is as low as their input offset currents over most of the MIL temperature range, there is rarely a need to use the normal balancing resistor (along with its noise-reducing bypass capacitor). Note, however, that adding the optional balancing resistor will enhance performance at temperatures above 100°C.

Specified values are for a –3 dB point of 1.0 Hz. For other frequencies, simply scale capacitors C1 through C4 directly; i.e., for 3 Hz Bessel response, C1 = 0.0387 μF, C2 = 0.0357 μF, C3 = 0.0533 μF, and C4 = 0.0205 μF.

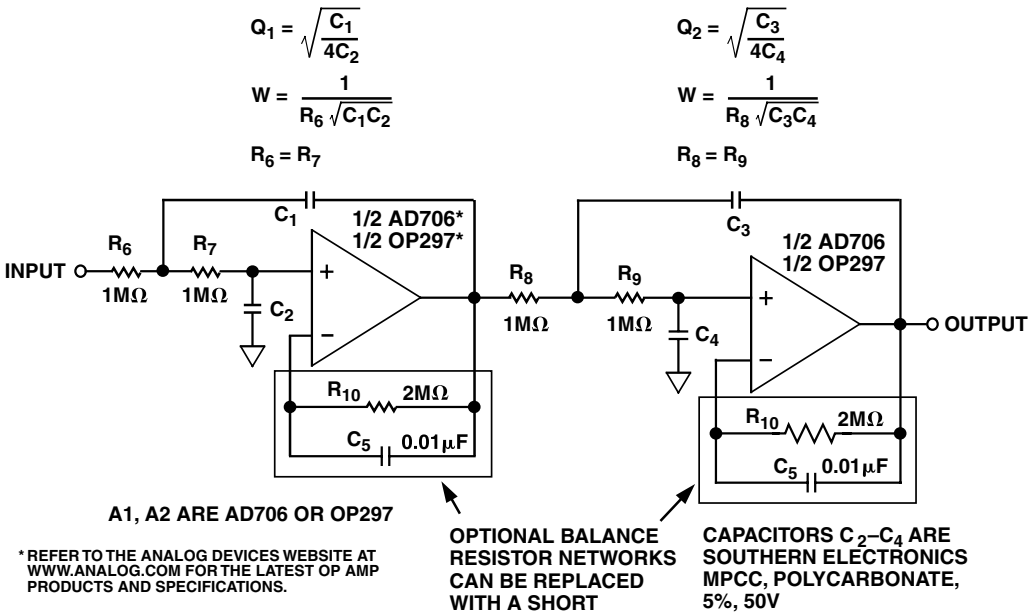


Figure 5-41. A 4-pole low-pass filter for data acquisition.

Table 5-4. Recommended Component Values for a 1 Hz, 4-Pole, Low-Pass Filter

Desired Low-Pass Response	Section 1 Frequency (Hz)	Section 1 Q	Section 2 Frequency (Hz)	Section 2 (Q)	C1 (μF)	C2 (μF)	C3 (μF)	C4 (μF)
Bessel	1.43	0.522	1.60	0.806	0.116	0.107	0.160	0.0616
Butterworth	1.00	0.541	1.00	1.31	0.172	0.147	0.416	0.0609
0.1 dB Chebychev	0.648	0.619	0.948	2.18	0.304	0.198	0.733	0.0385
0.2 dB Chebychev	0.603	0.646	0.941	2.44	0.341	0.204	0.823	0.0347
0.5 dB Chebychev	0.540	0.705	0.932	2.94	0.416	0.209	1.00	0.0290
1.0 dB Chebychev	0.492	0.785	0.925	3.56	0.508	0.206	1.23	0.0242

EXTERNAL CMR AND SETTLING TIME ADJUSTMENTS

When a very high speed, wide bandwidth in-amp is needed, one common approach is to use several op amps or a combination of op amps and a high bandwidth subtractor amplifier. These discrete designs may be readily tuned up for best CMR performance by external trimming. A typical circuit is shown in Figure 5-42. The dc CMR should always be trimmed first, since it affects CMRR at all frequencies.

The $+V_{IN}$ and $-V_{IN}$ terminals should be tied together and a dc input voltage applied between the two inputs and ground. The voltage should be adjusted to provide a 10 V dc input. A dc CMR trimming potentiometer would then be adjusted so that the outputs are equal and as low as possible, with both a positive and a negative dc voltage applied.

AC CMR trimming is accomplished in a similar manner, except that an ac input signal is applied. The input frequency used should be somewhat lower than the –3 dB bandwidth of the circuit.

The input amplitude should be set at 20 V p-p with the inputs tied together. The ac CMR trimmer is then nulled-set to provide the lowest output possible. If the best possible settling time is needed, the ac CMR trimmer may be used, while observing the output wave form on an oscilloscope. Note that, in some cases, there will be a compromise between the best CMR and the fastest settling time.

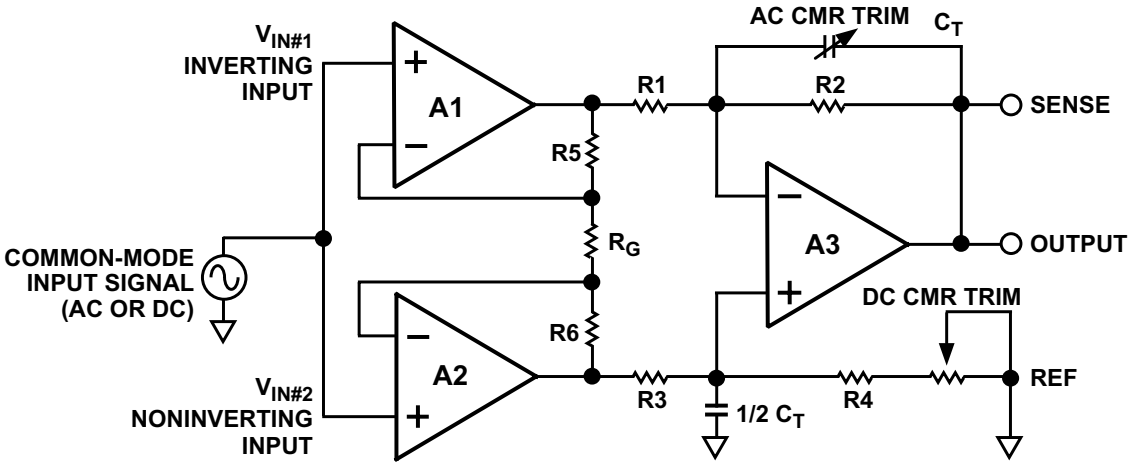


Figure 5-42. External dc and ac CMR trim circuit for a discrete 3-op amp in-amp.