Chapter IV

MONOLITHIC DIFFERENCE AMPLIFIERS

Difference (Subtractor) Amplifier Products

Monolithic difference amplifiers are a special category of in-amps that are usually designed to be used in applications where large dc or ac common-mode voltages are present. This includes many general current sensing applications, such as motor control, battery chargers, and power converters. In addition, there are numerous high common-mode voltage automotive current sensing applications, including: battery cell voltage monitoring, transmission controls, fuel injection controls, engine management, suspension controls, electronic steering, electronic parking brake, and hybrid vehicle drive/hybrid battery control. Because these amplifiers are typically used to sense current by accurately amplifying the small differential voltage across a shunt resistor in the load path, they are often called current shunt amplifiers.

The **AD8200 family** of current shunt amplifiers is based on a traditional difference amplifier input stage which includes a resistor-divider configuration. These on-chip precision resistors provide matching to within 0.01%, which results in very good total error when compared with a difference amplifier built from discrete op amps and resistors. Unlike the AD8200 amplifiers, which can withstand high common-mode input voltages by dividing these voltages down at the input, the **AD8210** amplifiers tolerate the high common-mode input voltages by virtue of the high breakdown voltages of their input transistors. This provides numerous advantages over the AD8200 series amplifiers, including higher bandwidth, higher input impedance, and lower overall noise amplification. Combined, these advantages reduce total system error.

Table 4-1 provides a performance summary of Analog Devices difference amplifier products.

Table 4-1. Latest Generation of Analog Devices Difference Amps Summarized[1]

Product	Features	Power Supply Current Typ	–3 dB BW Typ (G = 10)	CMR G = 10 (dB) Min	Input Offset Voltage Max	V_{OS} Drift (µV/°C) Max	RTI Noise[2] (nV/√Hz) (G = 10)
AD8202	S.S., 28 V CMV, G = 20	250 µA	50 kHz	80[3, 4, 5]	1 mV[6]	10	300 typ[3]
AD8203	S.S., 28 V CMV, G = 14	250 µA	60 kHz[7]	80[5, 7]	1 mV[6]	10	300 typ[7]
AD8205	S.S., 65 V CMV, G = 50	1 mA	50 kHz[8]	80[4, 5, 6]	2 mV[6]	15 typ	500 typ[8]
AD8206	S.S., 65 V CMV, G = 20	1 mA	100 kHz[3]	76[3, 9]	2 mV[6]	15 typ	500 typ[3]
AD8210	S.S., current shunt monitor	500 µA	500 kHz[3]	100[3, 5]	1 mV[6]	5 typ	80 typ[3]
AD8212	Adjustable gain; CMV up to 500 V[10]	200 µA	500 kHz	90	1 mV	10	100 typ
AD8213	Dual channel	1.3 mA[11]	500 kHz	100	1 mV	10	70 typ
AD8130	270 MHz receiver	12 mA	270 MHz	83[12, 13]	1.8 mV	3.5 mV	12.5 typ[12, 14]
AD628	High CMV	1.6 mA	600 kHz[15]	75[15]	1.5 mV	4	300 typ[15]
AD629	High CMV, G = 1	0.9 mA	500 kHz	77[12]	1 mV	6	550 typ[12]
AD626	High CMV	1.5 mA	100 kHz	55[16]	500 µV	1	250 typ
AMP03	High BW, G = 1	3.5 mA	3 MHz	85[12]	400 µV	NS	750 typ[12]

NOTES
NS = not specified, NA = not applicable, S.S. = single supply.
[1]Refer to ADI website at www.analog.com for latest products and specifications.
[2]At 1 kHz. RTI noise = $\sqrt{(e_{ni})^2 + (e_{no}/G)^2}$.
[3]Operating at a gain of 20.
[4]For 10 kHz, <2 kΩ source imbalance.
[5]DC to 10 kHz.
[6]Referred to input (RTI).
[7]Operating at a gain of 14.
[8]Operating at a gain of 50.
[9]DC to 20 kHz.
[10]With inexpensive external transistor.
[11]Note that this is 0.65 mA per channel.
[12]Operating at a gain of 1.
[13]At frequency = 4 MHz.
[14]At frequency ≥ 10 kHz.
[15]Operating at a gain of 0.1.
[16]f = 10 kHz, V_{CM} = 6 V.

The AD8200 family of current sensing difference amplifiers has multiple gain options, which provide design flexibility for the following important trade-offs:

1.) The shunt resistance value vs. the power dissipated in the circuit being measured

2.) The shunt resistance value vs. the signal-to-noise ratio

3.) The shunt resistance value vs. the amplifier gain needed

The automotive industry standard calls for a gain of 20, which, in most cases, gives an excellent trade-off between all three variables. However, there are conditions which favor other gains. For example, the AD8203 operates at a gain of 14. This allows for convenient scaling of the output to accommodate both 5 V and 3.3 V A/D converters, while still using the same value resistive shunt.

Similarly, the **AD8205** has a gain of 50, for use in applications where it is most important to minimize the power dissipation in the resistive shunt. This higher gain is used with lower resistance shunts, which, of course, have a lower output voltage. This slightly reduces the signal-to-noise performance of the system.

The **AD8202** consists of a preamp and buffer arranged as shown in Figure 4-1.

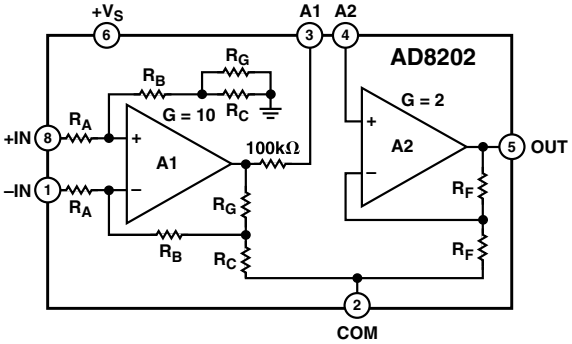

Figure 4-1. AD8202 connection diagram.

Figure 4-2 provides more details. The preamp incorporates a dynamic bridge (subtractor) circuit. Identical networks (within the shaded areas) consisting of R_A, R_B, R_C, and R_G attenuate input signals applied to Pins 1 and 8. Note that when equal amplitude signals are asserted at inputs 1 and 8, and the output of A1 is equal to the common potential (i.e., zero), the two attenuators form a balanced-bridge network. When the bridge is balanced, the differential input voltage at A1, and thus its output, will be zero.

Any common-mode voltage applied to both inputs will keep the bridge balanced and the A1 output at zero. Because the resistor networks are carefully matched, the common-mode signal rejection approaches this ideal state. However, if the signals applied to the inputs differ, the result is a difference at the input to A1. A1 responds by adjusting its output to drive R_B, by way of R_G, to adjust the voltage at its inverting input until it matches the voltage at its noninverting input.

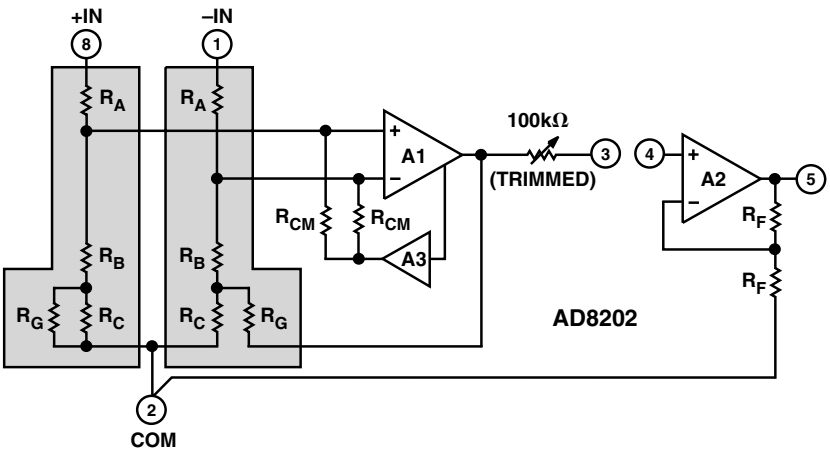

Figure 4-2. AD8202 simplified schematic.

By attenuating voltages at Pins 1 and 8, the amplifier inputs are held within the power supply range, even if the input levels of Pins 1 and 8 exceed the supply or fall below common (ground). The input network also attenuates normal (differential) mode voltages. R_C and R_G form an attenuator that scales A1 feedback, forcing large output signals to balance relatively small differential inputs. The resistor ratios establish the preamp gain at 10.

Because the differential input signal is attenuated and then amplified to yield an overall gain of 10, the amplifier A1 operates at a higher noise gain, multiplying deficiencies such as input offset voltage and noise with respect to Pins 1 and 8.

To minimize these errors while extending the common-mode range, a dedicated feedback loop is employed to reduce the range of common-mode voltage applied to A1 for a given overall range at the inputs. By offsetting the range of voltage applied to the compensator, the input common-mode range is also offset to include voltages more negative than the power supply. Amplifier A3 detects the common-mode signal applied to A1 and adjusts the voltage on the matched R_{CM} resistors to reduce the common-mode voltage range at the A1 inputs. By adjusting the common voltage of these resistors, the common-mode input range is extended while the normal mode signal attenuation is reduced, leading to better performance referred to input.

The output of the dynamic bridge taken from A1 is connected to Pin 3 by way of a 100 kΩ series resistor, provided for low-pass filtering and gain adjustment. The resistors in the input networks of the preamp and the buffer feedback resistors are ratio-trimmed for high accuracy.

The output of the preamp drives a gain-of-2 buffer amplifier, A2, implemented with carefully matched feedback resistors, R_F.

The two-stage system architecture of the AD8202 (Figure 4-2) enables the user to incorporate a low-pass filter prior to the output buffer. By separating the gain into two stages, a full-scale, rail-to-rail signal from the preamp can be filtered at Pin 3, and a half-scale signal resulting from filtering can be restored to full scale by the output buffer amp. The source resistance seen by the inverting input of A2 is approximately 100 kΩ, to minimize the effects of A2's input bias current. Typically, this current is quite small, and errors resulting from applications that mismatch the resistance are correspondingly small. The simplified schematic and theory of operation given for the AD8202 also applies to the **AD8203**. The two products are almost identical, except for their internal preset gains and their power consumption.

AD8205 Difference Amplifier

The **AD8205** is a single-supply difference amplifier that uses a unique architecture to accurately amplify small differential current shunt voltages in the presence of rapidly changing common-mode voltages. It is offered in both packaged and die form.

In typical applications, the AD8205 is used to measure current by amplifying the voltage across a current shunt placed across the inputs.

The gain of the AD8205 is 50 V/V, with an accuracy of 1.2%. This accuracy is guaranteed over the operating temperature range of –40°C to +125°C. The die temperature range is –40°C to +150°C with a guaranteed gain accuracy of 1.3%.

The input offset is less than 2 mV referred to the input at 25°C, and 4.5 mV maximum referred to the input over the full operating temperature range for the packaged part. The die input offset is less than 6 mV referred to the input over the die operating temperature range.

The AD8205 operates with a single supply from 4.5 V to 10 V (absolute maximum = 12.5 V). The supply current is less than 2 mA.

High accuracy trimming of the internal resistors allows the AD8205 to have a common-mode rejection ratio better than 78 dB from dc to 20 kHz. The common-mode rejection ratio over the operating temperature is 76 dB for both the die and the packaged part.

The output offset can be adjusted from 0.05 V to 4.8 V (V+ = 5 V) for unipolar and bipolar operation.

The AD8205 consists of two amplifiers (A1 and A2), a resistor network, a small voltage reference, and a bias circuit (not shown). See Figure 4-3.

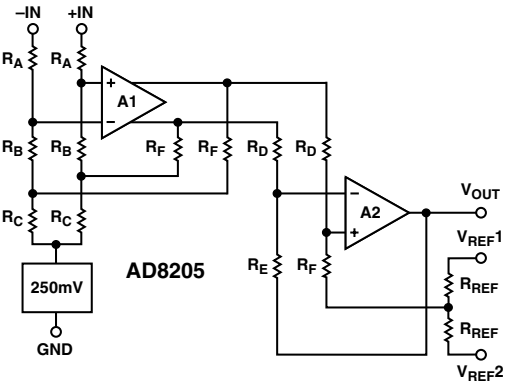

Figure 4-3. AD8205 simplified schematic.

The set of input attenuators preceding A1 consists of R_A, R_B, and R_C, which reduces the common-mode voltage to match the input voltage range of A1. The two attenuators form a balanced-bridge network. When the bridge is balanced, the differential voltage created by a common-mode voltage is 0 V at the inputs of A1. The input attenuation ratio is 1/16.7. The combined series resistance of R_A, R_B, and R_C is approximately 200 kΩ ± 20%.

By attenuating the voltages at Pin 1 and Pin 8, the A1 amplifier inputs are held within the power supply range, even if Pin 1 and Pin 8 exceed the supply or fall below common (ground). A reference voltage of 250 mV biases the attenuator above ground. This allows the amplifier to operate in the presence of negative common-mode voltages.

The input network also attenuates normal (differential) mode voltages. A1 amplifies the attenuated signal by 26. The input and output of this amplifier are differential to maximize the ac common-mode rejection.

A2 converts the differential voltage from A1 into a single-ended signal and provides further amplification. The gain of this second stage is 32.15.

The reference inputs, $V_{REF}1$ and $V_{REF}2$, are tied through resistors to the positive input of A2, which allows the output offset to be adjusted anywhere in the output operating range. The gain is 1 V/V from the reference pins to the output when the reference pins are used in parallel. The gain is 0.5 V/V when they are used to divide the supply.

The ratios of Resistors R_A, R_B, R_C, R_D, and R_F are trimmed to a high level of precision to allow the common-mode rejection ratio to exceed 80 dB. This is accomplished by laser trimming the resistor ratio matching to better than 0.01%.

The total gain of 50 is made up of the input attenuation of 1/16.7 multiplied by the first stage gain of 26 and the second stage gain of 32.15.

The output stage is Class A with a PNP pull-up transistor and a 300 μA current sink pull-down.

The **AD8206** is nearly identical to the AD8205, except for gain and power consumption. Please see the AD8205 circuit description for AD8206 theory of operation.

The **AD8210** is a current shunt monitor IC. Figure 4-4 shows the block diagram.

The gain of the AD8210 is 20 V/V, with an accuracy of 0.7%. This accuracy is guaranteed over the operating temperature range of –40°C to +125°C.

The AD8210 operates with a single supply between 4.5 V to 5.5 V. The supply current is typically less than 2 mA.

The AD8210 is comprised of two main blocks: a differential amplifier and an instrumentation amplifier. A load current flowing through the external shunt resistor produces a voltage at the input terminals. The input terminals are connected to the differential amplifier (A1) by Resistors R1 and R2. A1 nulls the voltage appearing across its own input terminals by adjusting (balancing) the current through R1 and R2 with Transistors Q1 and Q2. When the input signal to the AD8210 is zero, the currents in R1 and R2 are equal. When the differential signal is nonzero, the current increases through one of the resistors and decreases in the other. The current difference is proportional to the size and polarity of the input signal. Since the differential input voltage is converted into a current, common-mode rejection is not dependent on resistor matching; therefore, both high accuracy and performance are provided throughout the wide common-mode voltage range.

The differential currents through QI and Q2 are converted into a differential voltage due to R3 and R4. A2 is configured as an instrumentation amplifier, and this differential input signal is converted into a single-ended output voltage by A2. The gain is internally set with thin-film resistors to 20 V/V.

The output reference voltage is easily programmed by the $V_{REF}1$ and $V_{REF}2$ pins. In a typical configuration, $V_{REF}1$ is connected to V_{CC} while $V_{REF}2$ is connected to GND. In this case, the output is centered at $V_{CC}/2$ when the input signal is zero.

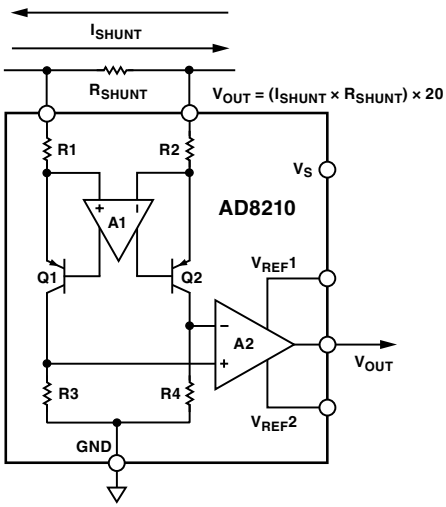

Figure 4-4. AD8210 block diagram.

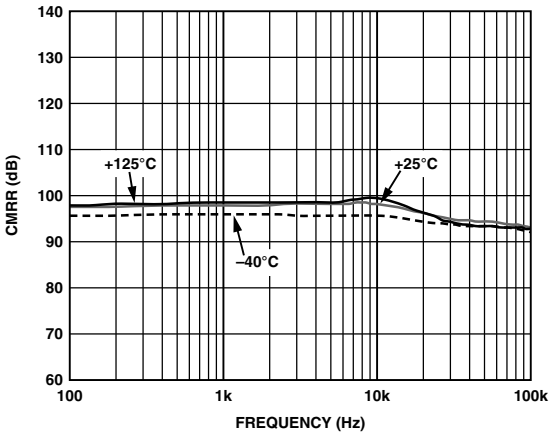

Figure 4-5. AD8210 CMRR vs. frequency and temperature (common-mode voltage < 5 V).

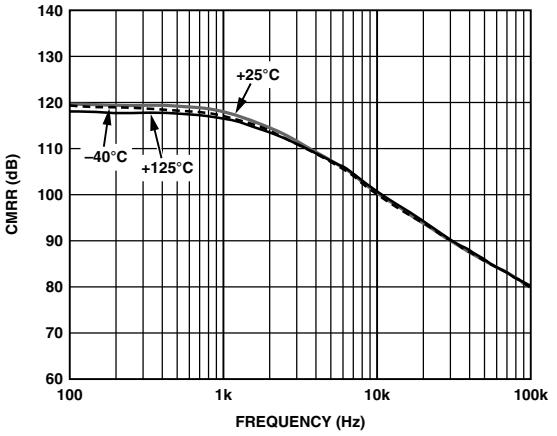

Figure 4-6. AD8210 CMRR vs. frequency and temperature (common-mode voltage > 5 V).

The **AMP03** is a monolithic, unity-gain, 3 MHz differential amplifier. Incorporating a matched thin-film resistor network, the AMP03 features stable operation over temperature without requiring expensive external matched components. The AMP03 is a basic analog building block for differential amplifier and instrumentation applications (Figure 4-7).

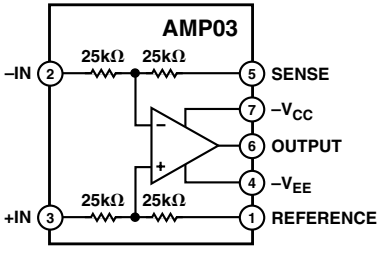

Figure 4-7. AMP03 functional block diagram.

The differential amplifier topology of the AMP03 serves both to amplify the difference between two signals and to provide extremely high rejection of the common-mode input voltage. With a typical common-mode rejection of 100 dB, the AMP03 solves common problems encountered in instrumentation design. It is ideal for performing either the addition or subtraction of two input signals without using expensive externally matched precision resistors. Because of its high CMRR over frequency, the AMP03 is an ideal general-purpose amplifier for data acquisition systems that must operate in a noisy environment. Figures 4-8 and 4-9 show the AMP03's CMRR and closed-loop gain vs. frequency.

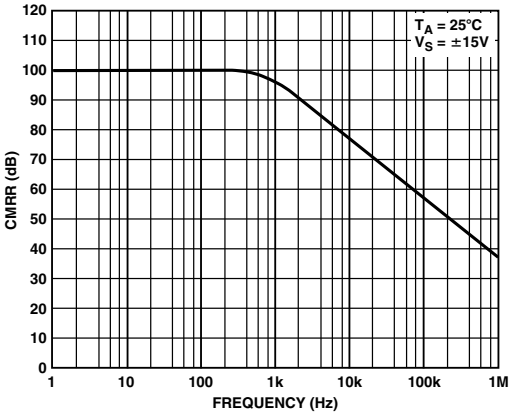

Figure 4-8. AMP03 CMRR vs. frequency.

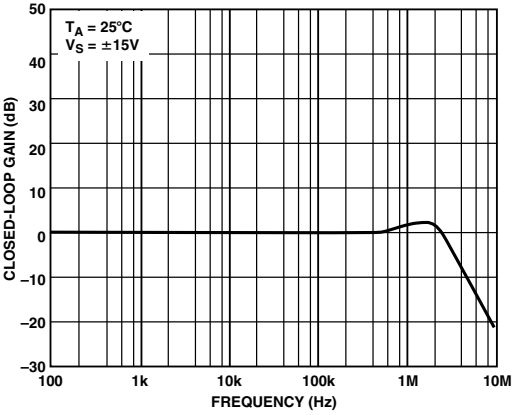

Figure 4-9. AMP03 closed-loop gain vs. frequency.

Figure 4-10 shows the small signal pulse response of the AMP03.

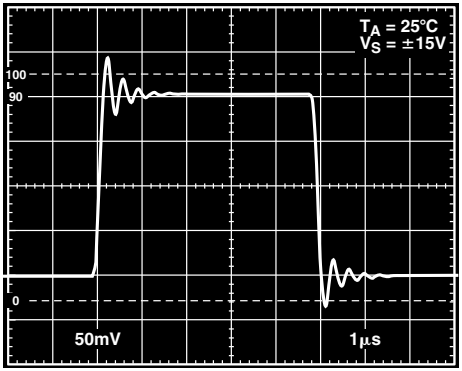

Figure 4-10. AMP03 small signal pulse response.

The **AD628** is a high common-mode voltage difference amplifier, combined with a user-configurable output amplifier (see Figure 4-11 and Figure 4-12). Differential mode voltages in excess of 120V are accurately scaled by a precision 11:1 voltage divider at the input. A reference voltage input is available to the user at Pin 3 (V_{REF}). The output common-mode voltage of the difference amplifier is the same as the voltage applied to the reference pin. If the uncommitted amplifier is configured for gain, connecting Pin 3 to one end of the external gain resistor establishes the output common-mode voltage at Pin 5 (OUT).

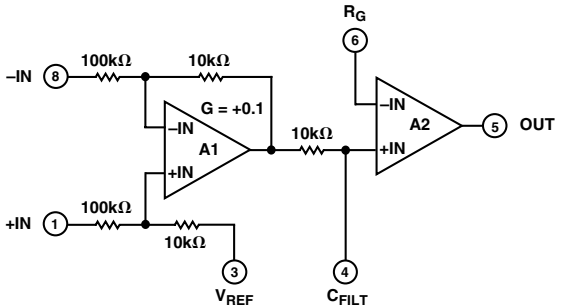

Figure 4-11. AD628 simplified schematic.

The output of the difference amplifier is internally connected to a 10 kΩ resistor trimmed to better than ±0.1% absolute accuracy. The resistor is connected to the noninverting input of the output amplifier and is accessible to the user at Pin 4 (C_{FILT}). A capacitor can be connected to implement a low-pass filter, a resistor can be connected to further reduce the output voltage, or a clamp circuit can be connected to limit the output swing.

The uncommitted amplifier is a high open-loop gain, low offset, low drift op amp, with its noninverting input connected to the internal 10 kΩ resistor. Both inputs are accessible to the user.

Careful layout design has resulted in exceptional common-mode rejection at higher frequencies. The inputs are connected to Pin 1 (+IN) and Pin 8 (–IN), which are adjacent to the power pins, Pin 2 ($-V_S$) and Pin 7 ($+V_S$). Because the power pins are at ac ground, input impedance balance and, therefore, common-mode rejection are preserved at higher frequencies.

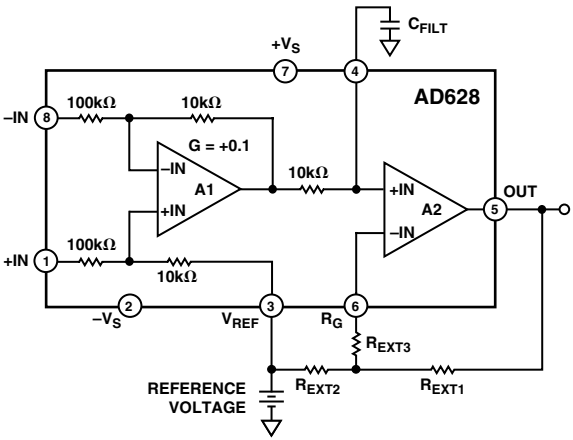

Figure 4-12. AD628 circuit connections.

Gain Adjustment

The AD628 system gain is provided by an architecture consisting of two amplifiers. The gain of the input stage is fixed at 0.1; the output buffer is user-adjustable as $G_{A2} = 1 + R_{EXT1}/R_{EXT2}$.

$$G_{TOTAL} = 0.1 \times \left(1 + \frac{R_{EXT1}}{R_{EXT2}}\right)$$

At 2 nA maximum, the input bias current of the buffer amplifier is very low, and any offset voltage induced at the buffer amplifier by its bias current may normally be neglected (2 nA × 10 kΩ = 20 µV). However, to absolutely minimize bias current effects, R_{EXT1} and R_{EXT2} can be selected so that their parallel combination is 10 kΩ. If practical resistor values force the parallel combination of R_{EXT1} and R_{EXT2} below 10 kΩ, a series resistor (R_{EXT3}) can be added to make up for the difference. Table 4-2 lists several values of gain and corresponding resistor values.

Table 4-2. Nearest Standard 1% Resistor Values for Various Gains (See Figure 4-12)

Total Gain (V/V)	A2 Gain (V/V)	R_{EXT1} (Ω)	R_{EXT2} (Ω)	R_{EXT3} (Ω)
0.1	1	10 k	∞	0
0.2	2	20 k	20 k	0
0.25	2.5	25.9 k	18.7 k	0
0.5	5	49.9 k	12.4 k	0
1	10	100 k	11 k	0
2	20	200 k	10.5 k	0
5	50	499 k	10.2 k	0
10	100	1 M	10.2 k	0

To set the system gain to less than 0.1, an attenuator can be created by placing a resistor, R_{EXT4}, from Pin 4 (C_{FILT}) to the reference voltage. A divider would be formed by the 10 kΩ resistor, which is in series with the positive input of A2 and R_{EXT4}. A2 would be configured for unity gain.

Using a divider and setting A2 to unity gain yields

$$G_{W/DIVIDER} = 0.1 \times \left(\frac{R_{EXT4}}{10\,k\Omega + R_{EXT4}} \right) \times 1$$

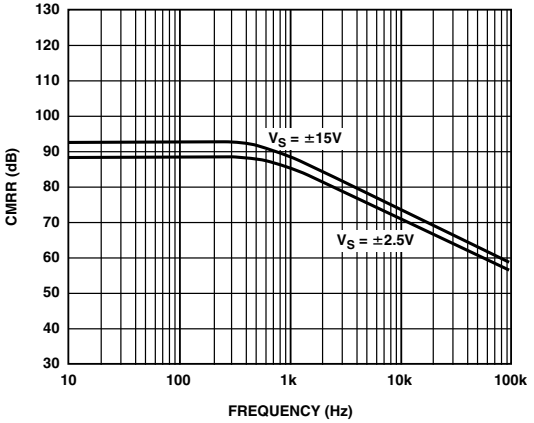

Figure 4-13. AD628 CMRR vs. frequency.

For extensive coverage of AD628 applications circuits, refer to Chapter 6 of this guide.

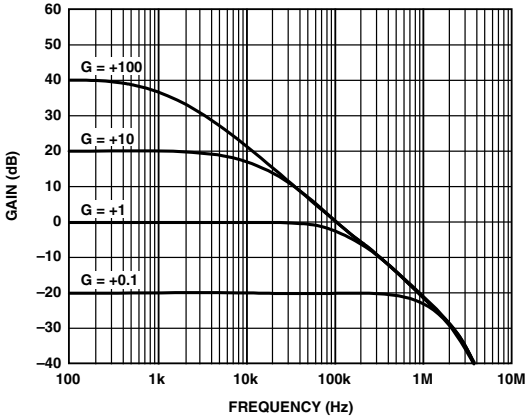

Figure 4-14. AD628 small signal frequency response, V_{OUT} = 200 mV p-p, G = +0.1, +1, +10, and +100.

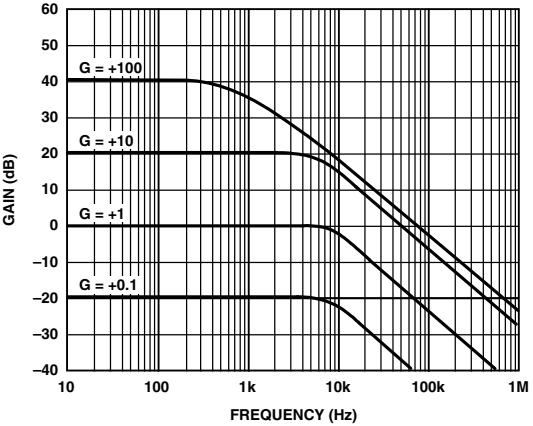

Figure 4-15. AD628 large signal frequency response, V_{OUT} = 20 V p-p, G = +0.1, +1, +10, and +100.

The **AD626** is a single- or dual-supply differential amplifier consisting of a precision balanced attenuator, a very low drift preamplifier (A1), and an output buffer amplifier (A2). It has been designed so that small differential signals can be accurately amplified and filtered in the presence of large common-mode voltages (much greater than the supply voltage) without the use of any other active components.

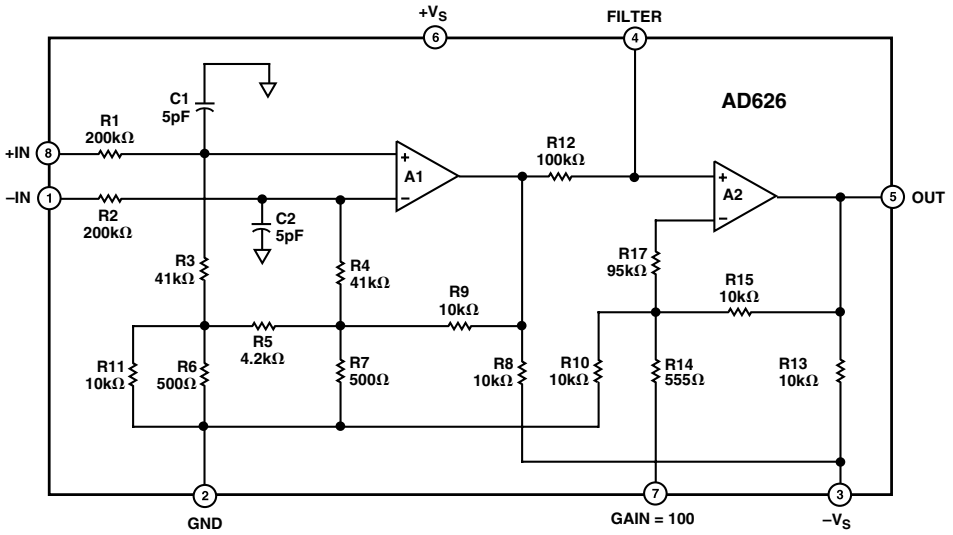

Figure 4-16. AD626 simplified schematic.

Figure 4-16 shows the main elements of the AD626. The signal inputs at Pins 1 and 8 are first applied to dual resistive attenuators, R1 through R4, whose purpose is to reduce the peak common-mode voltage at the input to the preamplifier—a feedback stage based on the very low drift op amp A1. This allows the differential input voltage to be accurately amplified in the presence of large common-mode voltages—six times greater than that which can be tolerated by the actual input to A1. As a result, the input common-mode range extends to six times the quantity ($V_S - 1V$). The overall common-mode error is minimized by precise laser trimming of R3 and R4, thus giving the AD626 a common-mode rejection ratio of at least 10,000:1 (80 dB). The output of A1 is connected to the input of A2 via 100 kΩ (R12) resistor to facilitate the low-pass filtering of the signal of interest. The AD626 is easily configured for gains of 10 or 100. For a gain of 10, Pin 7 is simply left unconnected; similarly, for a gain of 100, Pin 7 is grounded. Gains between 10 and 100 are easily set by connecting a resistor between Pin 7 and analog GND. Because the on-chip resistors have an absolute tolerance of ±20% (although they are ratio matched to within 0.1%), at least a 20% adjustment range must be provided. The nominal value for this gain setting resistor is equal to

$$R = \left(\frac{50{,}000\ \Omega}{GAIN - 10}\right) - 555\ \Omega$$

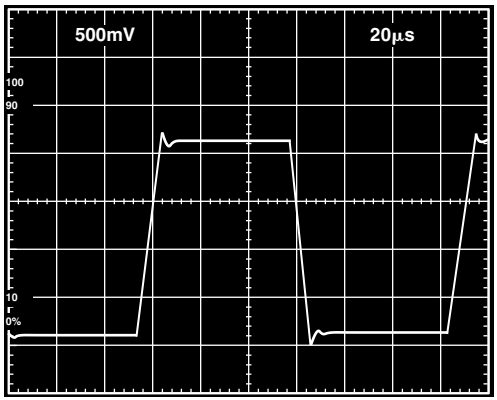

Figure 4-17. The large signal pulse response of the AD626. G = 10.

Figure 4-17 shows the large signal pulse response of the AD626.

The **AD629** is a unity-gain difference amplifier designed for applications that require the measurement of signals with common-mode input voltages of up to ±270 V. The AD629 keeps error to a minimum by providing excellent CMR in the presence of high common-mode input voltages. Finally, it can operate from a wide power supply range of ±2.5 V to ±18 V.

The AD629 can replace costly isolation amplifiers in applications that do not require galvanic isolation. Figure 4-18 is the connection diagram of the AD629. Figure 4-19 shows the AD629's CMR vs. frequency.

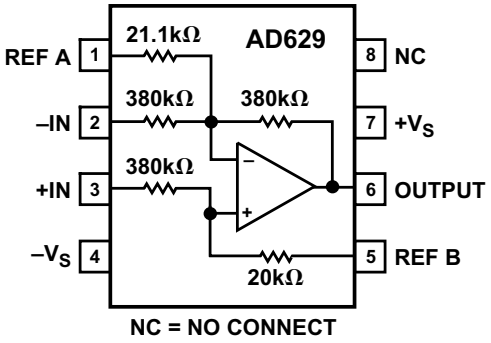

Figure 4-18. AD629 connection diagram.

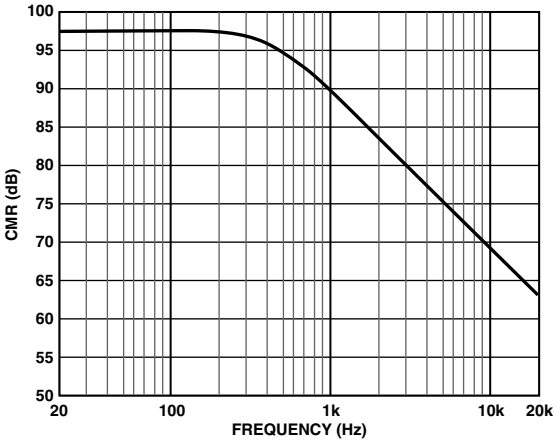

Figure 4-19 AD629 common-mode rejection vs. frequency.

High Frequency Differential Receiver/Amplifiers

Although not normally associated with difference amplifiers, the **AD8130** series of very high speed differential receiver/amplifiers represent a new class of products that provide effective common-mode rejection at VHF frequencies. The AD8130 has a –3 dB bandwidth of 270 MHz, an 80 dB CMR at 2 MHz, and a 70 dB CMR at 10 MHz.

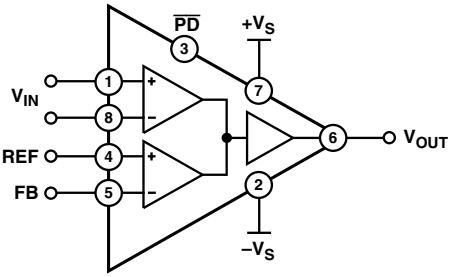

Figure 4-20. AD8130 block diagram.

Figure 4-20 is a block diagram of the AD8130. Its design uses an architecture called active feedback, which differs from that of conventional op amps. The most obvious differentiating feature is the presence of two separate pairs of differential inputs compared to a conventional op amp's single pair. Typically for the active feedback architecture, one of these input pairs is driven by a differential input signal, while the other is used for the feedback. This active stage in the feedback path is where the term *active feedback* is derived. The active feedback architecture offers several advantages over a conventional op amp in several types of applications. Among these are excellent common-mode rejection, wide input common-mode range, and a pair of inputs that are high impedance and totally balanced in a typical application.

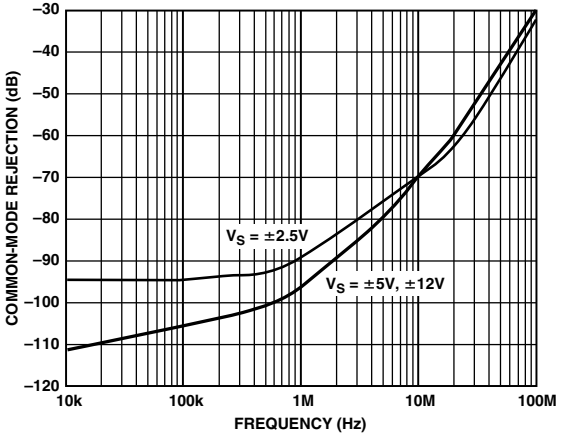

Figure 4-21. AD8130 CMR vs. frequency.

In addition, while an external feedback network establishes the gain response as in a conventional op amp, its separate path makes it totally independent of the signal input. This eliminates any interaction between the feedback and input circuits, which traditionally causes problems with CMRR in conventional differential-input op amp circuits.

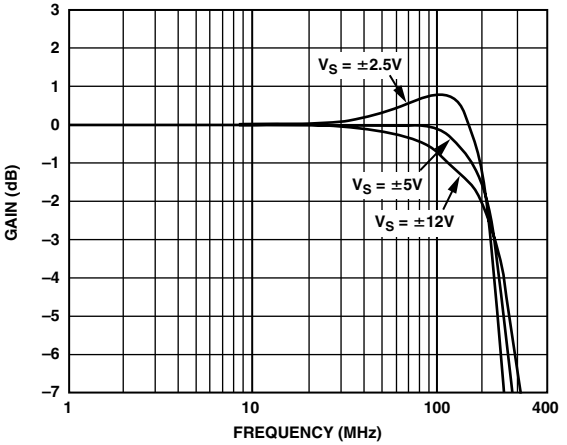

Figure 4-22. AD8130 frequency response vs. gain and supply voltage.

Figure 4-21 shows the CMR vs. frequency of the AD8130. Figure 4-22 shows its gain vs. frequency for various supply voltages.