Chapter II

INSIDE AN INSTRUMENTATION AMPLIFIER

A Simple Op Amp Subtractor Provides an In-Amp Function

The simplest (but still very useful) method of implementing a differential gain block is shown in Figure 2-1.

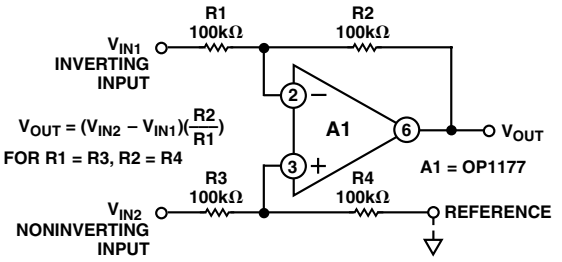

Figure 2-1. A 1-op amp in-amp difference amplifier circuit functional block diagram.

If R1 = R3 and R2 = R4, then

$$V_{OUT} = \left(V_{IN2} - V_{IN1}\right)\left(R2/R1\right)$$

Although this circuit provides an in-amp function, amplifying differential signals while rejecting those that are common mode, it also has some limitations. First, the impedances of the inverting and noninverting inputs are relatively low and unequal. In this example, the input impedance to V_{IN1} equals 100 kΩ, while the impedance of V_{IN2} is twice that, at 200 kΩ. Therefore, when voltage is applied to one input while grounding the other, different currents will flow depending on which input receives the applied voltage. (This unbalance in the sources' resistances will degrade the circuit's CMRR.)

Furthermore, this circuit requires a very close ratio match between resistor pairs R1/R2 and R3/R4; otherwise, the gain from each input would be different—directly affecting common-mode rejection. For example, at a gain of 1, with all resistors of equal value, a 0.1% mismatch in just one of the resistors will degrade the CMR to a level of 66 dB (1 part in 2000). Similarly, a source resistance imbalance of 100 Ω will degrade CMR by 6 dB.

In spite of these problems, this type of bare bones in-amp circuit, often called a difference amplifier or subtractor, is useful as a building block within higher performance in-amps. It is also very practical as a standalone functional circuit in video and other high speed uses, or in low frequency, high common-mode voltage (CMV) applications, where the input resistors divide down the input voltage as well as provide input protection for the amplifier. Some monolithic difference amplifiers such as Analog Devices' AD629 employ a variation of the simple subtractor in their design. This allows the IC to handle common-mode input voltages higher than its own supply voltage. For example, when powered from a ±15 V supply, the AD629 can amplify signals with common-mode voltages as high as ±270 V.

Improving the Simple Subtractor with Input Buffering

An obvious way to significantly improve performance is to add high input impedance buffer amplifiers ahead of the simple subtractor circuit, as shown in the 3-op amp instrumentation amplifier circuit of Figure 2-2.

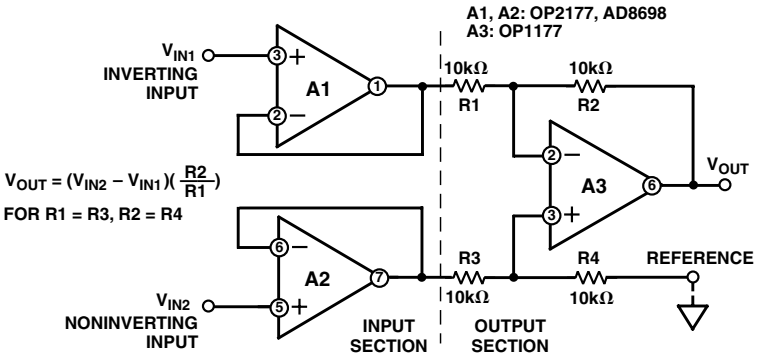

Figure 2-2. A subtractor circuit with input buffering.

This circuit provides matched, high impedance inputs so that the impedances of the input sources will have a minimal effect on the circuit's common-mode rejection. The use of a dual op amp for the 2-input buffer amplifiers is preferred because they will better track each other over temperature and save board space. Although the resistance values are different, this circuit has the same transfer function as the circuit of Figure 2-1.

Figure 2-3 shows further improvement: Now the input buffers are operating with gain, which provides a circuit with more flexibility. If the value of R5 = R8 and R6 = R7 and, as before, R1 = R3 and R2 = R4, then

$$V_{OUT} = (V_{IN2} - V_{IN1})\ (1 + R5/R6)\ (R2/R1)$$

While the circuit of Figure 2-3 does increase the gain (of A_1 and A_2) equally for differential signals, it also increases the gain for common-mode signals.

The 3-Op Amp In-Amp

The circuit of Figure 2-4 provides further refinement and has become the most popular configuration for instrumentation amplifier design. The classic 3-op amp in-amp circuit is a clever modification of the buffered subtractor circuit of Figure 2-3. As with the previous circuit, op amps A1 and A2 of Figure 2-4 buffer the input voltage. However, in this configuration, a single gain resistor, R_G, is connected between the summing junctions of the two input buffers, replacing R6 and R7. The full differential input voltage will now appear across R_G (because the voltage at the summing junction of each amplifier is equal to the voltage applied to its positive input). Since the amplified input voltage (at the outputs of A1 and A2) appears differentially across the three resistors, R5, R_G, and R6, the differential gain may be varied by just changing R_G.

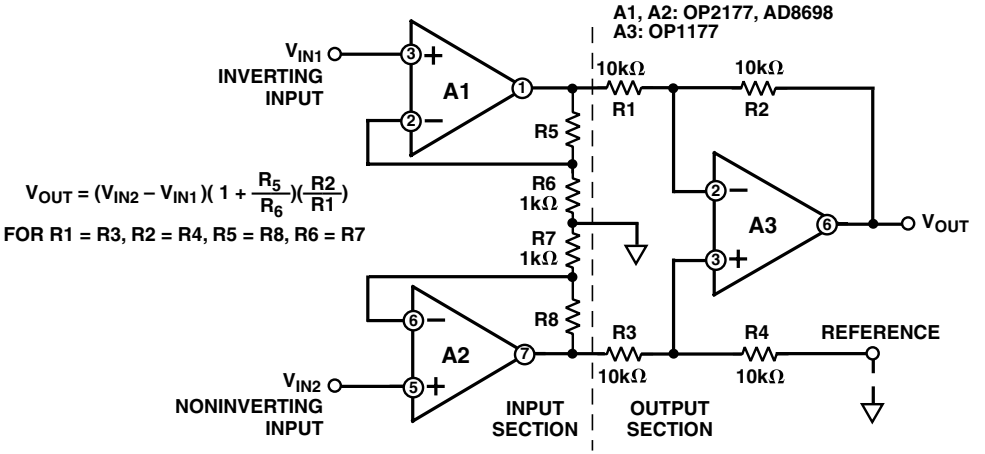

Figure 2-3. A buffered subtractor circuit with buffer amplifiers operating with gain.

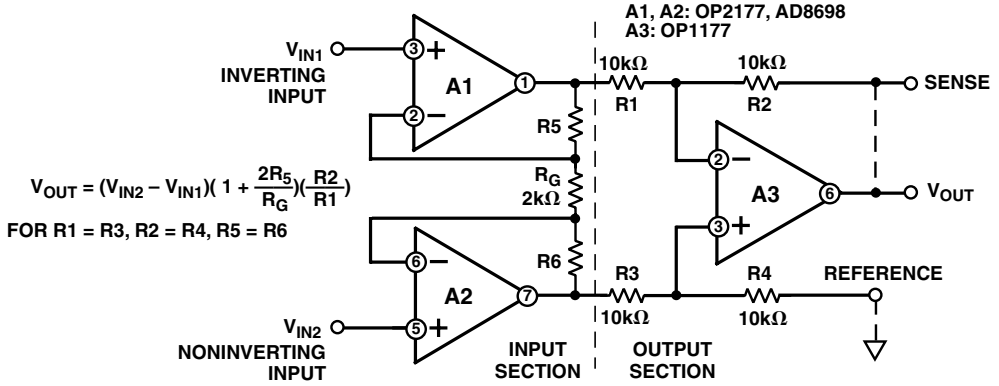

Figure 2-4. The classic 3-op amp in-amp circuit.

There is another advantage of this connection: Once the subtractor circuit has been set up with its ratio-matched resistors, no further resistor matching is required when changing gains. If the value of R5 = R6, R1 = R3, and R2 = R4, then

$$V_{OUT} = (V_{IN2} - V_{IN1})\ (1 + 2R5/R_G)(R2/R1)$$

Since the voltage across R_G equals V_{IN}, the current through R_G will equal (V_{IN}/R_G). Amplifiers A1 and A2, therefore, will operate with gain and amplify the input signal. Note, however, that if a common-mode voltage is applied to the amplifier inputs, the voltages on each side of R_G will be equal, and no current will flow through this resistor. Since no current flows through R_G (nor, therefore, through R5 and R6), amplifiers A1 and A2 will operate as unity-gain followers. Therefore, common-mode signals will be passed through the input buffers at unity gain, but differential voltages will be amplified by the factor ($1 + (2\ R_F/R_G)$).

In theory, this means that the user may take as much gain in the front end as desired (as determined by R_G) without increasing the common-mode gain and error. That is, the differential signal will be increased by gain, but the common-mode error will not, so the ratio (Gain (V_{DIFF})/($V_{ERROR\ CM}$)) will increase. Thus, CMRR will theoretically increase in direct proportion to gain—a very useful property.

Finally, because of the symmetry of this configuration, common-mode errors in the input amplifiers, if they track, tend to be canceled out by the output stage subtractor. This includes such errors as common-mode rejection vs. frequency. These features explain the popularity of this configuration.

3-Op Amp In-Amp Design Considerations

Two alternatives are available for constructing 3-op amp instrumentation amplifiers: using FET or bipolar input operational amplifiers. FET input op amps have very low bias currents and are generally well-suited for use with very high (>10^6 Ω) source impedances. FET amplifiers usually have lower CMR, higher offset voltage, and higher offset drift than bipolar amplifiers. They also may provide a higher slew rate for a given amount of power.

The sense and reference terminals (Figure 2-4) permit the user to change A3's feedback and ground connections. The sense pin may be externally driven for servo applications and others for which the gain of A3 needs to be varied. Likewise, the reference terminal allows an external offset voltage to be applied to A3. For normal operation, the sense and output terminals are tied together, as are reference and ground.

Amplifiers with bipolar input stages tend to achieve both higher CMR and lower input offset voltage drift than FET input amplifiers. Superbeta bipolar input stages combine many of the benefits of FET and bipolar processes, with even lower IB drift than FET devices.

A common (but frequently overlooked) issue for the unwary designer using a 3-op amp in-amp design is the reduction of common-mode voltage range that occurs when the in-amp is operating at high gain. Figure 2-5 is a schematic of a 3-op amp in-amp operating at a gain of 1000.

In this example, the input amplifiers, A1 and A2, are operating at a gain of 1000, while the output amplifier is providing unity gain. This means that the voltage at the output of each input amplifier will equal one-half

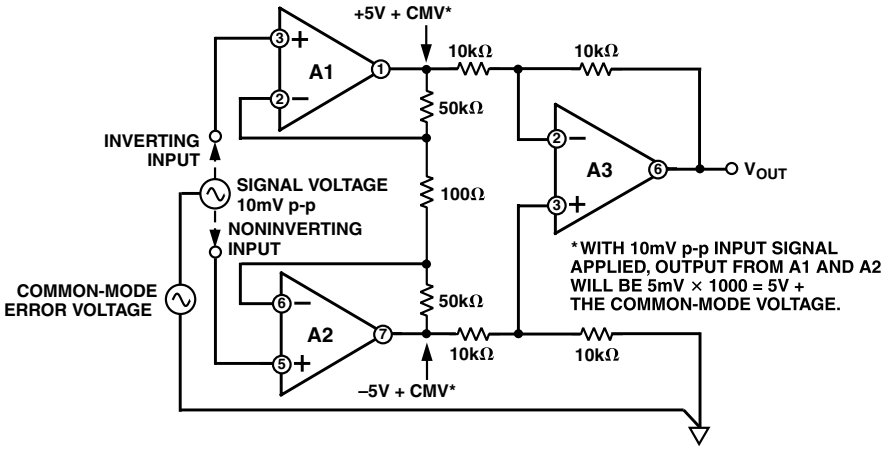

Figure 2-5. A 3-op amp in-amp showing reduced CMV range.

the peak-to-peak input voltage × 1000, plus any common-mode voltage that is present on the inputs (the common-mode voltage will pass through at unity gain regardless of the differential gain). Therefore, if a 10 mV differential signal is applied to the amplifier inputs, amplifier A1's output will equal +5 V, plus the common-mode voltage, and A2's output will be –5 V, plus the common-mode voltage. If the amplifiers are operating from 15 V supplies, they will usually have 7 V or so of headroom left, thus permitting an 8 V common-mode voltage—but not the full 12 V of CMV, which, typically, would be available at unity gain (for a 10 mV input). Higher gains or lower supply voltages will further reduce the common-mode voltage range.

The Basic 2-Op Amp Instrumentation Amplifier

Figure 2-6 is a schematic of a typical 2-op amp in-amp circuit. It has the obvious advantage of requiring only two, rather than three, operational amplifiers and providing savings in cost and power consumption. However, the nonsymmetrical topology of the 2-op amp in-amp circuit can lead to several disadvantages, most notably lower ac CMRR compared to the 3-op amp design, limiting the circuit's usefulness.

The transfer function of this circuit is

$$V_{OUT} = (V_{IN2} - V_{IN1})\ (1 + R4/R3)$$

$$for\ R1 = R4\ and\ R2 = R3$$

Input resistance is high and balanced, thus permitting the signal source to have an unbalanced output impedance. The circuit's input bias currents are set by the input current requirements of the noninverting input of the two op amps, which typically are very low.

Disadvantages of this circuit include the inability to operate at unity gain, a decreased common-mode voltage range as circuit gain is lowered, and poor ac common-mode rejection. The poor CMR is due to the unequal phase shift occurring in the two inputs, V_{IN1} and V_{IN2}. That is, the signal must travel through amplifier A1 *before* it is subtracted from V_{IN2} by amplifier A2. Thus, the voltage at the output of A1 is slightly delayed or phase-shifted with respect to V_{IN1}.

Minimum circuit gains of 5 are commonly used with the 2-op amp in-amp circuit because this permits an adequate dc common-mode input range, as well as sufficient bandwidth for most applications. The use of rail-to-rail (single-supply) amplifiers will provide a common-mode voltage range that extends down to $-V_S$ (or ground in single-supply operation), plus true rail-to-rail output voltage range (i.e., an output swing from $+V_S$ to $-V_S$).

Table 2-1 shows amplifier gain vs. circuit gain for the circuit of Figure 2-6 and gives practical 1% resistor values for several common circuit gains.

Table 2-1. Operating Gains of Amplifiers A1 and A2 and Practical 1% Resistor Values for the Circuit of Figure 2-6.

Circuit Gain	Gain of A1	Gain of A2	R2, R3	R1, R4
1.10	11.00	1.10	499 kΩ	49.9 kΩ
1.33	4.01	1.33	150 kΩ	49.9 kΩ
1.50	3.00	1.50	100 kΩ	49.9 kΩ
2.00	2.00	2.00	49.9 kΩ	49.9 kΩ
10.1	1.11	10.10	5.49 kΩ	49.9 kΩ
101.0	1.01	101.0	499 Ω	49.9 kΩ
1001	1.001	1001	49.9 Ω	49.9 kΩ

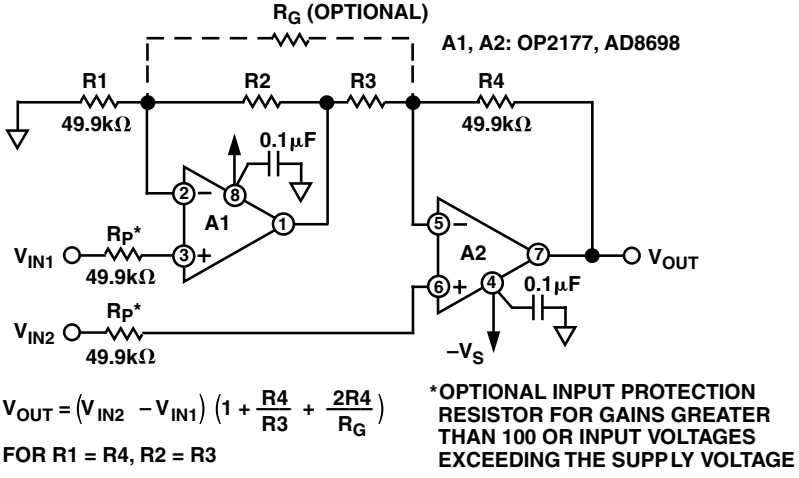

Figure 2-6. A 2-op amp in-amp circuit.

2-Op Amp In-Amps—Common-Mode Design Considerations for Single-Supply Operation

When the 2-op amp in-amp circuit of Figure 2-7 is examined from the reference input, it is apparent that it is simply a cascade of two inverters.

Assuming that the voltage at both of the signal inputs, V_{IN1} and V_{IN2}, is 0, the output of A1 will equal

$$V_{O1} = -V_{REF}\ (R2/R1)$$

A positive voltage applied to V_{REF} will tend to drive the output voltage of A1 negative, which is clearly *not* possible if the amplifier is operating from a single power supply voltage (+V_S and 0 V).

The gain from the output of amplifier A1 to the circuit's output, V_{OUT}, at A2, is equal to

$$V_{OUT} = -V_{O1}\ (R4/R3)$$

The gain from V_{REF} to V_{OUT} is the product of these two gains and equals

$$V_{OUT} = (-V_{REF}\ (R2/R1))(-R4/R3)$$

In this case, R1 = R4 and R2 = R3. Therefore, the reference gain is +1, as expected. Note that this is the result of two inversions, in contrast to the noninverting signal path of the reference input in a typical 3-op amp in-amp circuit.

Just as with the 3-op amp in-amp, the common-mode voltage range of the 2-op amp in-amp can be limited by single-supply operation and by the choice of reference voltage.

Figure 2-8 is a schematic of a 2-op amp in-amp operating from a single 5 V power supply. The reference input is tied to $V_S/2$, which in this case is 2.5 V. The output voltage should ideally be 2.5 V for a differential input voltage of 0 V and for any common-mode voltage within the power supply voltage range (0 V to 5 V).

As the common-mode voltage is increased from 2.5 V toward 5 V, the output voltage of A1 (V_{O1}) will equal

$$V_{O1} = V_{CM} + ((V_{CM} - V_{REF})\ (R2/R1))$$

In this case, V_{REF} = 2.5 V and R2/R1 = 1/4. The output voltage of A1 will reach 5 V when V_{CM} = 4.5 V. Further increases in common-mode voltage obviously cannot be rejected. In practice, the input voltage range limitations of amplifiers A1 and A2 may limit the in-amp's common-mode voltage range to less than 4.5 V.

Similarly, as the common-mode voltage is reduced from 2.5 V toward 0 V, the output voltage of A1 will hit zero for a V_{CM} of 0.5 V. Clearly, the output of A1 cannot go more negative than the negative supply line (assuming no charge pump), which, for a single-supply connection, equals 0 V. This negative or zero-in common-mode range limitation can be overcome by proper design of the in-amp's internal level shifting, as in the **AD627** monolithic 2-op amp instrumentation amplifier. However, even with good design, some positive common-mode voltage range will be traded off to achieve operation at zero common-mode voltage.

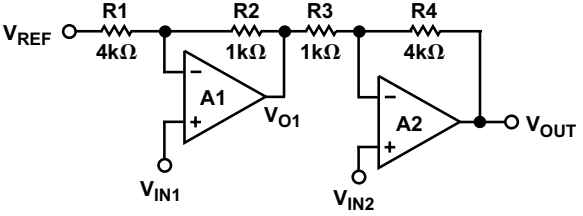

Figure 2-7. The 2-op amp in-amp architecture.

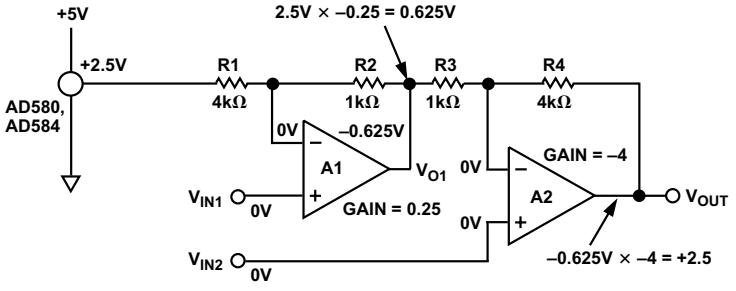

Figure 2-8. Output swing limitations of 2-op amp in-amp using a 2.5 V reference.

Another, and perhaps more serious, limitation of the standard 2-amplifier instrumentation amplifier circuit compared to 3-amplifier designs, is the intrinsic difficulty of achieving high ac common-mode rejection. This limitation stems from the inherent imbalance in the common-mode signal path of the 2-amplifier circuit.

Assume that a sinusoidal common-mode voltage, V_{CM}, at a frequency, F_{CM}, is applied (common mode) to inputs V_{IN1} and V_{IN2} (Figure 2-8). Ideally, the amplitude of the resulting ac output voltage (the common-mode error) should be 0 V, independent of frequency, F_{CM}, at least over the range of normal ac power line (mains) frequencies: 50 Hz to 400 Hz. Power lines tend to be the source of much common-mode interference.

If the ac common-mode error is zero, amplifier A2 and gain network R3, R4 must see zero instantaneous difference between the common-mode voltage, applied directly to V_{IN2}, and the version of the common-mode voltage that is amplified by A1 and its associated gain network R1, R2. Any dc common-mode error (assuming negligible error from the amplifier's own CMRR) can be nulled by trimming the ratios of R1, R2, R3, and R4 to achieve the balance

$$R1 \equiv R4 \text{ and } R2 \equiv R3$$

However, any phase shift (delay) introduced by amplifier A1 will cause the phase of V_{O1} to slightly lag behind the phase of the directly applied common-mode voltage of V_{IN2}. This difference in phase will result in an instantaneous (vector) difference in V_{O1} and V_{IN2}, even if the amplitudes of both voltages are at their ideal levels. This will cause a frequency-dependent common-mode error voltage at the circuit's output, V_{OUT}. Further, this ac common-mode error will increase linearly with common-mode frequency because the phase shift through A1 (assuming a single-pole roll-off) will increase directly with frequency. In fact, for frequencies less than 1/10th the closed-loop bandwidth (f_{T1}) of A1, the common-mode error (referred to the input of the in-amp) can be approximated by

$$\%CM\ Error = \frac{V_E/G}{V_{CM}}(100\%) = \frac{f_{CM}}{f_{TI}}(100\%)$$

where V_E is the common-mode error voltage at V_{OUT}, and G is the differential gain—in this case, 5.

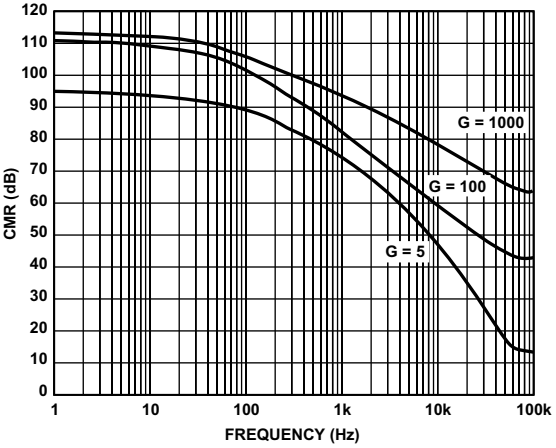

Figure 2-9. CMR vs. frequency of AD627 in-amp circuit.

For example, if A1 has a closed-loop bandwidth of 100 kHz (a typical value for a micropower op amp), when operating at the gain set by R1 and R2, and the common-mode frequency is 100 Hz, then

$$\%CM\ Error = \frac{100\,\text{Hz}}{100\,\text{kHz}}(100\%) = 0.1\%$$

A common-mode error of 0.1% is equivalent to 60 dB of common-mode rejection. So, in this example, even if this circuit were trimmed to achieve 100 dB CMR at dc, this would be valid only for frequencies less than 1 Hz. At 100 Hz, the CMR could never be better than 60 dB.

The AD627 monolithic in-amp embodies an advanced version of the 2-op amp instrumentation amplifier circuit that overcomes these ac common-mode rejection limitations. As illustrated in Figure 2-9, the AD627 maintains over 80 dB of CMR out to 8 kHz (gain of 1000), even though the bandwidth of amplifiers A1 and A2 is only 150 kHz.

The four resistors used in the subtractor are normally internal to the IC and are usually of very high resistance. High common-mode voltage difference amps (diff amps) typically use input resistors selected to provide voltage attenuation. Therefore, both the differential signal voltage and the common-mode voltage are attenuated, the common mode is rejected, and then the signal voltage is amplified.