

Section 5. Reference Clock Considerations

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Direct Clocking of a DDS

The output signal quality of a direct digital synthesizer is dependent upon the signal quality of the reference clock that is driving the DDS. Important quality aspects of the clock source, such as frequency stability (in PPM), edge jitter (in ps or ns), and phase noise (in dBc/Hz) will be reflected in the DDS output. One quality, phase noise, is actually reduced according to: $20 \text{ LOG} (F_{\text{out}}/F_{\text{clk}})$. This means that a 10 MHz output signal will have 20 dB less phase noise than the 100 MHz reference clock that “created” it. The figure below illustrates how DDS processing is affected by phase noise and jitter of the input clock.

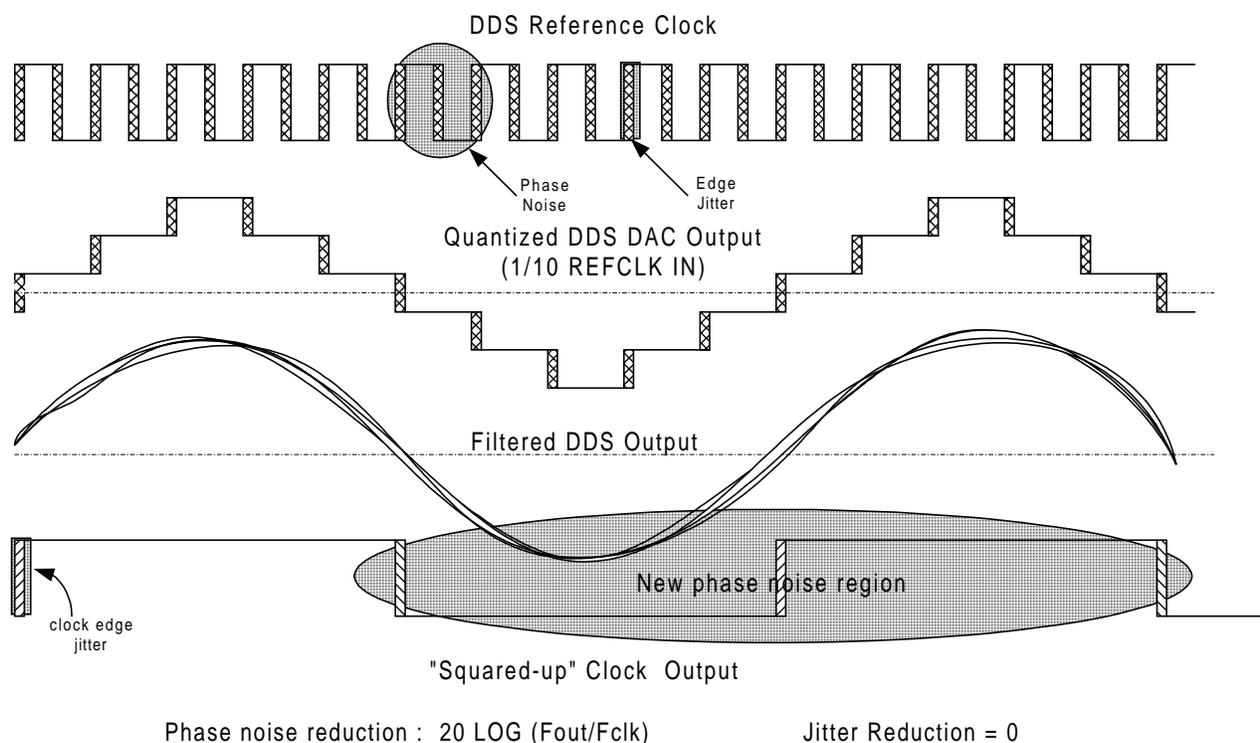


Figure 5-1. Reference clock edge uncertainty adversely affects DDS output signal quality

Figure 5-1 shows how phase noise, expressed in the time domain as period jitter with units of percent, is relative to the period of the waveform, and that absolute edge jitter is unaffected by changes in frequency or period. The “DDS Reference Clock” signal in Figure 5-1 shows that edge jitter is a much higher percentage of the total period than the same edge jitter in the “Squared-up Clock Output”. This accounts for phase noise improvement through frequency division even though the same amount of edge jitter is present on both clock periods.

Reference clock edge jitter has nothing to do with the accuracy of the phase increment steps taken by the phase accumulator. These step sizes are fixed by the frequency “tuning” word and are mathematically manipulated with excellent precision regardless of the quality of the clock.

In order for the digital phase step to be properly positioned in the analog domain, two criteria must be met:

- Appropriate **amplitude** (this is the DAC's job)
- Appropriate **time** (the clock's job)

The Complete-DDS IC's from Analog Devices provide an appropriately accurate DAC to translate the digital phase steps to an analog voltage or current. But that is only half of the job. The remaining half involves accurate timing of these amplitude steps that constitute the output sine wave. This is where minimum clock edge jitter and low phase noise are required to support the precise capabilities of DDS.

The phase noise improvement of the DDS output relative to the input clock becomes more apparent in the frequency domain. Figure 5-2 is a screen-capture from a spectrum analyzer showing the phase noise of two different DDS reference clocks. The phase noise/jitter of 100 MHz DDS clock source 1 is much more pronounced than that of clock source 2.

Figure 5-3 shows the 10 MHz DDS output response to the two clock sources. Output 1 shows a 20 dB (10X improvement) in phase noise relative to clock 1. Output 2 shows less phase noise than clock 2, although 20 dB is not apparent since the noise floor of the instrument is limiting the measurement. Notice the presence of low level output "spurs" on the skirt of output 2. These spurious signals are due to the necessary truncation of phase bits in the DDS phase-to-amplitude stage and the algorithm used to perform the transformation. These spurious signals are also present in output 1 but the signal's excessive phase noise is masking their presence. This demonstrates why phase noise is important in maintaining good signal-to-noise ratio in radio and other noise-sensitive systems.

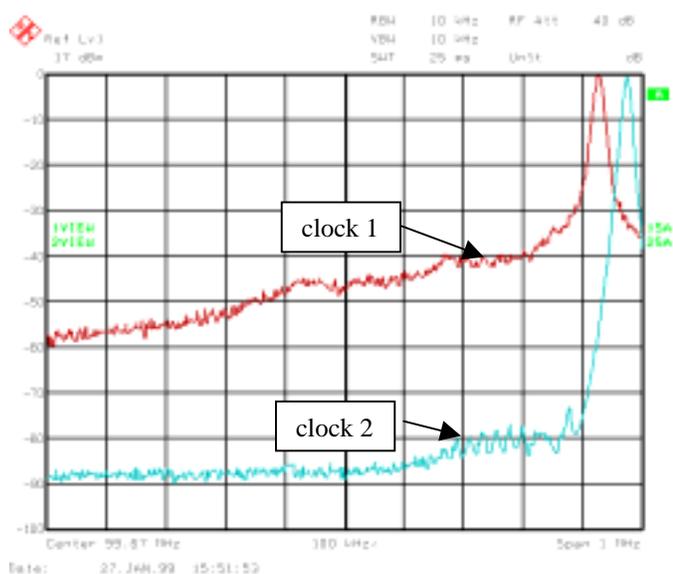


Figure 5-2: Good and poor clock phase noise

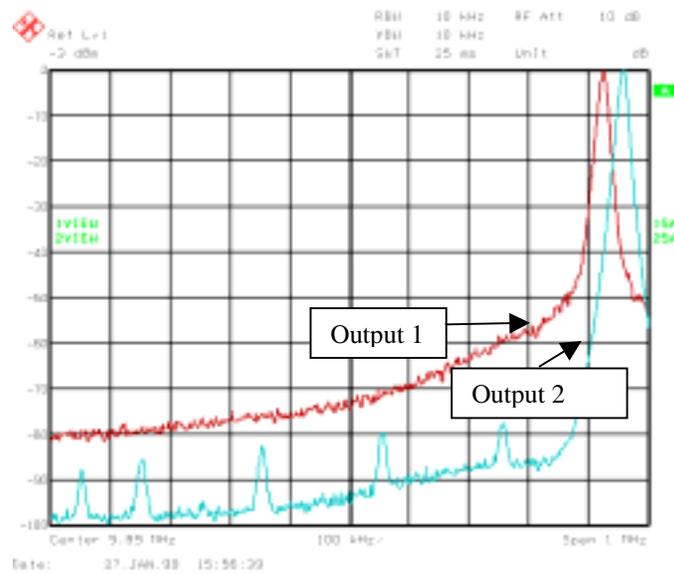


Figure 5-3: DDS output Response

There is a point at which the DDS can not mirror the quality of the input clock. For example, typical phase noise contribution of a DDS & DAC might be -130 dBc/Hz at a 1 kHz offset from the carrier. If the reference clock phase noise is better than -130 dBc/Hz then regardless of the reference oscillators good phase noise performance, the DDS & DAC output will never be better than -130 dBc/Hz at a 1 kHz offset. This DDS specification is listed as “Residual Phase Noise”. One should not “over-design” with regard to the reference oscillator’s phase noise specification. The DDS output phase noise performance will never exceed that of its inherent phase noise.

Overall DDS output phase noise is the sum of the phase noise of the reference clock source (after it has been enhanced by the frequency division quality of the DDS) and the residual phase noise of the DDS. For example: A reference clock oscillator has a phase noise of -110 dBc/Hz at a 1 kHz offset. The F_{out}/F_{clk} ratio is 1/10 and therefore the output phase noise reduction is -20 dB. This reduction in phase noise makes the reference oscillator’s phase noise at 10 MHz output equal to that of the residual phase noise of the DDS (which is given as -130 dBc/Hz at a 1 kHz offset). Adding -130 dBc/Hz to -130 dBc/Hz gives a doubling of noise power and equals -127 dBc/Hz. Even if the reference clock phase noise was -200 dBc/Hz the overall DDS output phase noise will still be approximately -130 dBc.

Using an Internal Reference Clock Multiplier Circuit

Many Analog Devices DDS and digital modulator products have on-chip reference clock multiplier circuits. These multipliers, which can be engaged or bypassed, allow lower frequency clock oscillators to be used to clock the DDS at much higher frequencies. Programmable or fixed multiplier values from $4\times$ to $20\times$ are available. They are desirable because they can easily solve a high-speed clocking problem or allow synchronization of the DDS to a “master clock” of

another existing system clock. They permit simplified applications and reduce the cost of supplying a high frequency clock oscillator.

The REFCLK Multiplier feature is not the optimum solution for every application though. There is a tradeoff in terms of output signal quality whenever REFCLK frequency multiplication is involved. Multiplication will degrade reference oscillator phase noise within the PLL loop bandwidth by 20 LOG (F_{out}/F_{clk}), where F_{out} is the multiplied output frequency and F_{clk} is the PLL reference clock. For example, a 6X clock multiplier will degrade the input clock phase noise of a -110 dBc/Hz oscillator by 15.5 dB which results in a -94.5 dBc/Hz reference clock phase noise. Furthermore, the PLL loop filter characteristics may cause “peaking” of the phase noise response near cutoff. Figure 5-4 demonstrates typical DDS output phase noise degradation in the AD9851 device which has the entire loop filter on-chip. Other DDS devices with sections of the loop filter off-chip will generally not demonstrate peaking in the filter response.

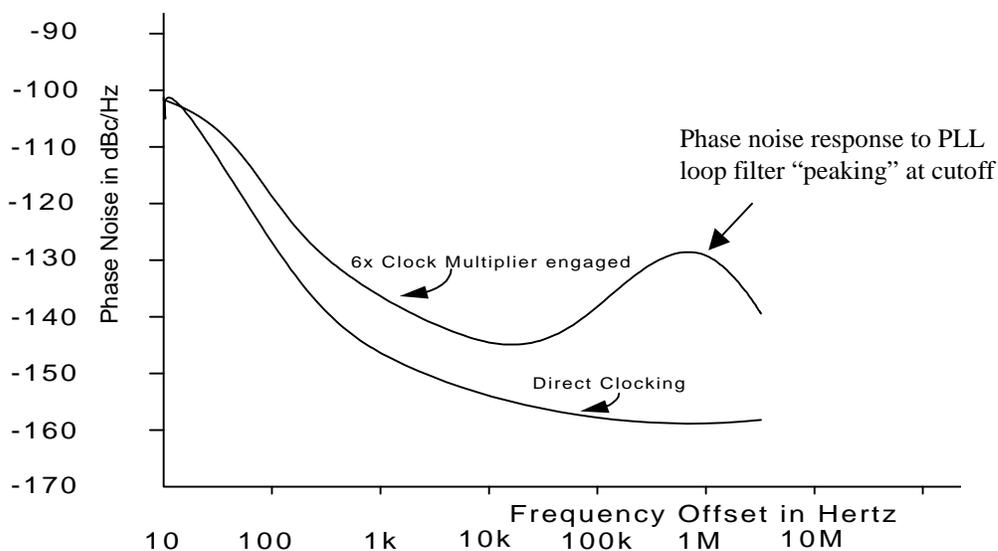


Figure 5-4. Typical DDS Phase Noise With and Without Clock Multiplier Function

DDS SFDR Performance

Use of reference clock multiplication also has an impact on SFDR (spurious-free dynamic range). Figure 5-5 shows two spectral plots of the same output frequency except output 1 has a 6× clock multiplier function engaged and output 2 is directly clocked. Close-in SFDR (± 1 MHz) shows SFDR of -68 dBc for the clock multiplied output and -78 dBc for the direct-clocked output. Also noticeable is the slightly elevated noise floor of output 1.

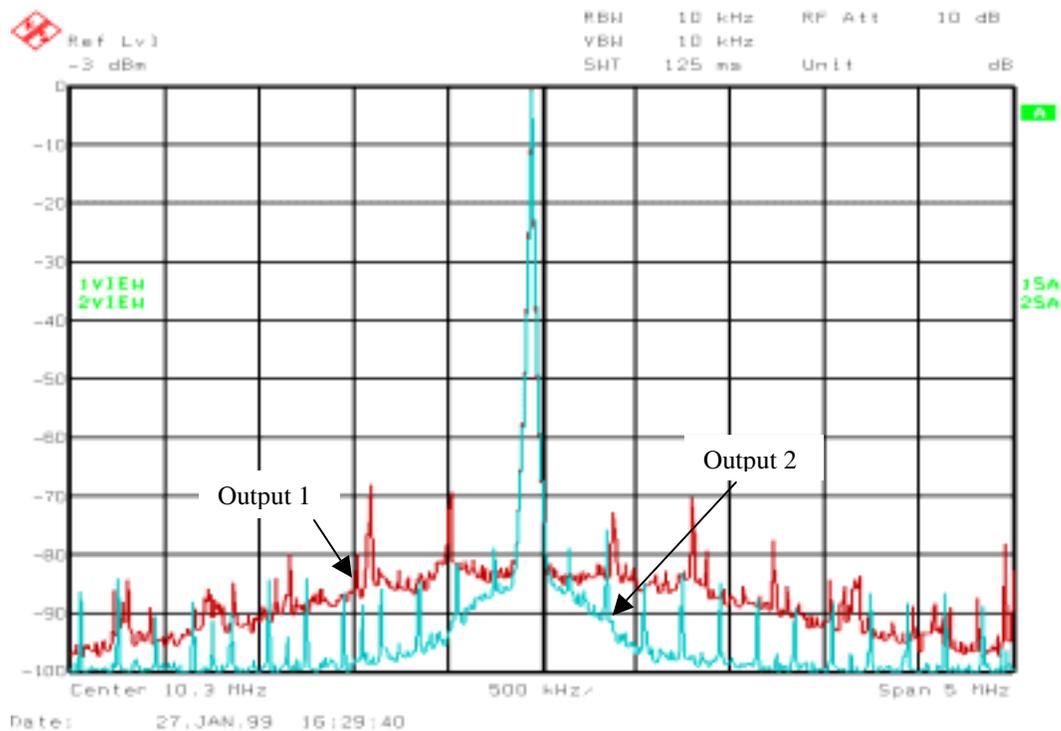


Figure 5-5. Spectral Plot of DDS Output With & Without Reference Clock Multiplication

Even considering the performance tradeoffs, the good performance, convenience and cost savings of an on-chip reference clock multiplier support its use for many, if not most, DDS applications. However, for the very best SFDR and phase noise performance, direct clocking of a DDS with a good quality clock oscillator (or sine source) is necessary.