Section 3. Frequency/phase-hopping Capability of DDS

Calculating the Frequency Tuning Word

The output frequency of a DDS device is determined by the formula:

$F_{OUT} = (M (REFCLK)) /2^N$

Where: F_{OUT} = the output frequency of the DDS
M = the binary tuning word
REFCLK = the internal reference clock frequency
N = The length in bits of the phase accumulator

The length of the phase accumulator (N) is the length of the tuning word which determines the degree of frequency tuning resolution of the DDS implementation. Let's find the frequency tuning word for an output frequency of 41 MHz where REFCLK is 122.88 MHz and the tuning word length is 32 bits (binary). The resulting equation would be:

$41 \text{ MHz} = (M (122.8 \text{ MHz})) /2^{32}$

solving for M…

$M = (41 \text{ MHz}(2^{32}))/122.8 \text{ MHz}$

M= 556AAAAB hex

Loading this value of M into the frequency control register would result in a frequency output of 41 MHz, given a reference clock frequency of 122.8 MHz.

Determining Maximum Tuning Speed

The maximum tuning speed of a DDS implementation is determined by the loading configuration selected, parallel byte or serial word, and the speed of the control interface. In some DDS applications, maximum output frequency tuning speed is desired. Applications such as GMSK and ramped-FSK modulation, require maximum frequency tuning speeds to support spectrally-shaped transitions between modulation frequencies. When the tuning word is loaded by the control interface, the constraint to frequency update is in the speed of the interface port. Typically a DDS device will provide a parallel byte load which facilitates getting data into the control registers at a higher rate. Control data clocking rates of 100 MHz are typically supported for a byte-load parallel control interface. This means that a new tuning word can be present on the output of a DDS device every 10 nS. The phase-continuous output of DDS frequency transitions is well-suited for high-speed frequency-hopping applications.

DDS devices also usually provide a set of registers that can be pre-programmed with tuning words. The contents of these registers are executed with an external pin on the device package. This provides for the maximum output frequency hopping speed between pre-programmed frequency values. This arrangement is especially suitable for FSK modulation applications where the "mark" and "space" frequencies can be readily pre-programmed. When using the pre-

programmed registers, DDS output frequency hopping speeds of up to 250 MHz can be achieved with the latest technology devices.

The DDS Control Interface

All of the functions, features, and configurations of a DDS device are generally programmed through the device's control interface port. The control interface for DDS devices is available in a variety of configurations. The common configurations are serial interface and byte-load parallel interface. The interface conventions range from a single 40-bit register that stores all of the functional control words, to a microprocessor-compatible a synchronous serial communications port. Control interface functionality and timing diagrams are detailed in the data sheets for the individual DDS devices.

Profile Registers

Pre-programmed registers are typically available in a DDS device that allow enhanced frequency or phase hopping of the output signal. The data contained in these registers are executed via a dedicated pin on the package and allow the use to change an operating parameter without going through the control interface instruction cycle. Examples of the types of functions that can be pre-programmed are:

- Output frequency tuning word – this allows the user to achieve the maximum frequency hopping capability with a DDS device. The availability of frequency select registers also facilitates using the DDS device as an FSK modulator where the input data directly steers the output to the desired mark and space frequencies.

- Phase of the output frequency – this function allows the user to execute pre-programmed increments of phase delay to the output signal. The amount of delay resolution ranges from ± 11.5° increments (5-bits) to ± .02° increments (14-bits). Phase-shift keying modulation (PSK) can readily be accomplished with the use of pre-programmed phase registers.

- In digital modulator and quadrature upconverter implementations of DDS architectures (to be covered in Section 8 of this seminar), additional functions can be pre-programmed in profile registers. These functions include FIR filter response, interpolation (upsampling) rates , and output spectral inversion enable/disable.