

Section 11. Ancillary DDS Techniques, Features, and Functions

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Improving FSDR with Phase Dithering

In Section 4 the effects of phase truncation in the architecture of a DDS were covered. The net result is that phase truncation can result in spurs in the DDS output spectrum depending on the choice of the tuning word. In some applications, it is desirable to reduce the spur energy at all costs. Phase dithering offers a means of reducing spur energy. However, this is at the expense of an elevated noise floor and increased phase noise.

Figure 11.1 is a simple functional block diagram of a DDS. In Figure 11.1(a) the T-bit tuning word feeds the input to the accumulator. The most significant A-bits of the accumulator output are fed to the angle-to-amplitude conversion (AAC) block, which then drives a D-bit DAC. The assumption is made that $T > A > D$.

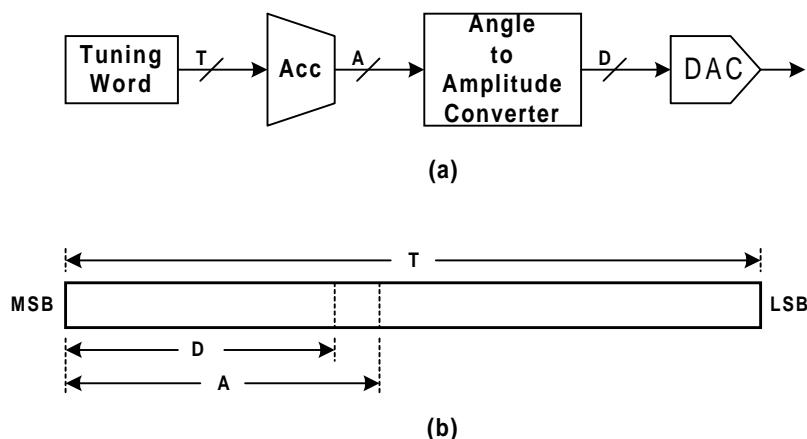


Figure 11.1. DDS Block Diagram

Figure 11.1(b) shows the relationship of the various word widths in the DDS. Note that the bits at the output of the accumulator constitute a word size (A) that is a subset of the tuning word size (T). Similarly, the output of the AAC constitutes a word size (D) that is a subset of the accumulator output word size (A). The relationship between the various word sizes in Figure 11.1(b) is typical of DDS architectures.

Phase dithering requires that the phase values generated by the accumulator contain a certain amount of noise. This can be accomplished by adding a small random number to each phase value generated at the output of the accumulator. This method is shown in the Figure 11.2.

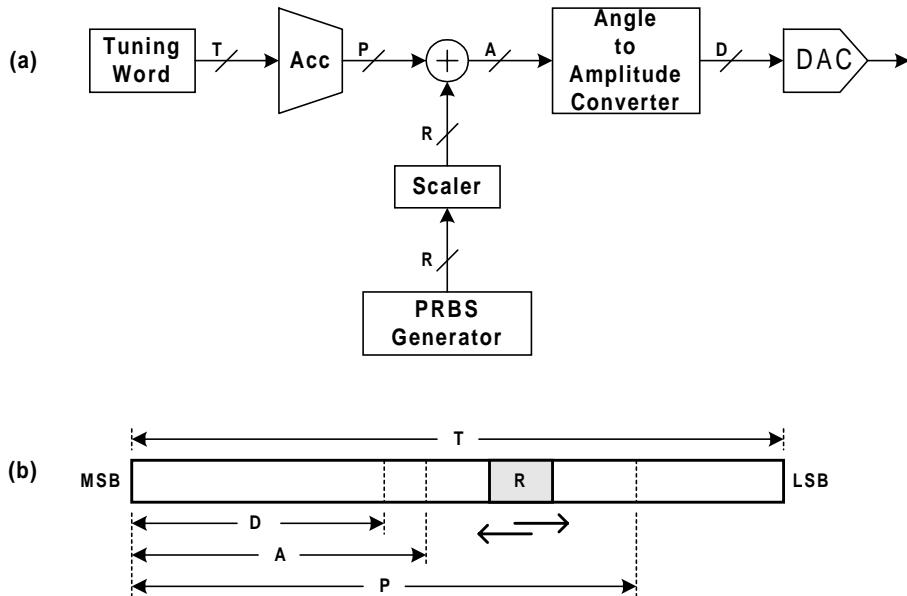


Figure 11.2. DDS Block Diagram

In the phase dithering model, a pseudorandom binary sequence (PRBS) generator is used to produce a new R-bit random number with each update of the accumulator (PRBS generators are covered in the Appendix). The PRBS numbers are scaled by powers of 2 (left- or right-shifted) to fit into the desired range of the P-bit word at the output of the accumulator. The random number is positioned so that its MSB is less than the LSB of the A-bit word at the input to the AAC. It should be noted that shifting the random number so that it overlaps the A-bit word is not recommended. Doing so defeats the purpose of having A-bits of phase resolution in the first place, since it adds noise that is greater than the quantization noise associated with the A-bit word.

The position of the R-bit word has significant impact on the magnitude of the phase dithering. This should be obvious since left-shifting the random number increases its impact when summed with the P-bit word taken from the output of the accumulator. Typically, the MSB of the random number is positioned one bit less than the LSB of the A-bit word that is fed to the AAC.

The width of the random number has an impact on the way in which the random phase is spread across the output spectrum of the DDS. Typically, a 3 or 4 bit random number is sufficient.

Understanding DDS Frequency “Chirp” Functionality

Frequency chirp is a method of transitioning between two different output frequencies, f_1 and f_2 , over a specified time interval. The simplest chirp is a linear sweep from f_1 to f_2 . However, in more advanced chirp systems the frequency transition from f_1 to f_2 can be a nonlinear function of time. A DDS-based chirp system is shown in Figure 11.3.

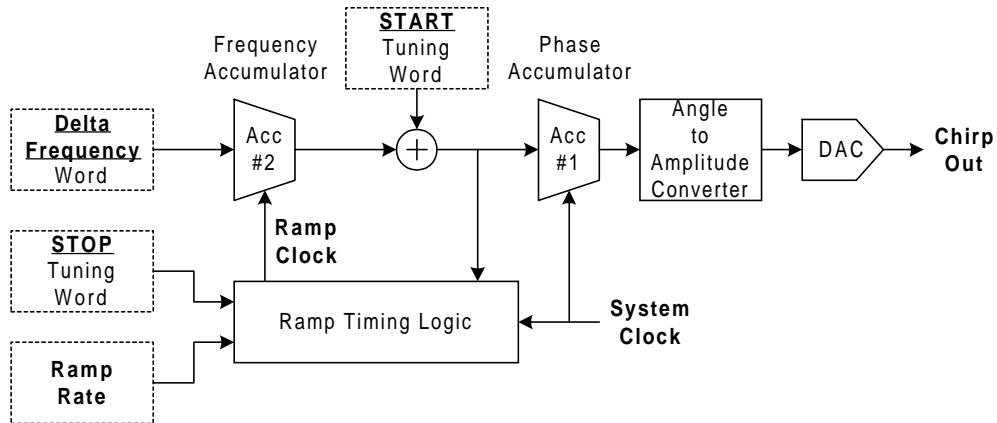


Figure 11.3. DDS-Based Chirp System

Beginning with the Phase Accumulator and working to the right, the system is a duplicate of the basic DDS. However, note that the Phase Accumulator is not driven by a static tuning word value, as it is the basic DDS. Instead, the input to the Phase Accumulator is the sum of the START Tuning Word and the output of the Frequency Accumulator. The START Tuning Word is the frequency tuning word that marks f_1 (the beginning frequency of the chirp).

The Frequency Accumulator recursively sums the Delta Frequency Word at a rate prescribed by the Ramp Clock. Thus, each occurrence of the Ramp Clock increments the value of the input to the Phase Accumulator by the Delta Frequency Word. Since the input to the Phase Accumulator determines the output frequency of the DDS and this value is changing with time, then the output frequency of the DDS is changing with time, also. This is the basic mechanism for generating a chirp waveform.

Assuming that the Ramp Clock generates an clock pulse at regular intervals and the Delta Frequency Word is constant, then the Frequency Accumulator output grows at linear rate. That is, the slope of the frequency vs. time function is constant. This constitutes a linear chirp.

It is also possible to generate nonlinear chirp frequency profiles. Notice that if the Delta Frequency Word is modified the rate at which the DDS output frequency changes is also modified. That is, the slope of the frequency vs. time function is modified. So, changing the Delta Frequency Word during the chirp interval changes the slope of the frequency vs. time function in mid-chirp. This provides a means to generate almost any chirp function using piecewise linear approximation.

Implementing chirp functionality in a DDS requires additional timing and control. This is the function of the Ramp Timing Logic. It actually serves two purposes. First, it must divide down the System Clock to produce the appropriate Ramp Clock frequency as defined by the Ramp Rate input. Second, it must terminate the Ramp Clock when the output frequency reaches f_2 (the STOP frequency of the chirp). Note that the STOP Tuning Word defines frequency, f_2 . Terminating the Ramp Clock is accomplished by monitoring the output of the Frequency Accumulator and the STOP Tuning Word value. When the output of the Frequency Accumulator is greater than or equal to the STOP Tuning Word, the Ramp Clock is disabled. It should be noted that the Ramp Timing Logic should also ensure that Frequency Accumulator

does not exceed the STOP Tuning Word value. That is, it should clamp its value to the value of the STOP Tuning Word.

This basic architecture is implemented in ADI's **AD9852** DDS. The device offers a high degree of flexibility in implementing a variety of chirp applications.

Achieving Output Amplitude Control/Modulation Within a DDS Device

In some applications it is desirable to control the amplitude of the DDS output signal. An obvious application would be a DDS-based AM transmitter. Another use would be for those applications in which a carrier is only present during data transmission and is absent, otherwise. Burst applications such as this can cause a problem when multiple devices share the transmission medium. This is because when the carrier transitions from one power level to another, the abrupt change creates a burst of broadband noise. This may cause transmission errors for the other devices sharing the medium. Amplitude control allows the user to gradually change carrier power rather than have it abruptly switch from one state to the other. This significantly reduces the noise generated during the switching transient.

The basic DDS architecture does not provide for amplitude control. However, amplitude control is made possible by a simple modification; insertion of a multiplier preceding the DAC. A DDS with amplitude control is available in ADI's **AD9852**. A block diagram of a DDS with amplitude control is shown in Figure 11.4.

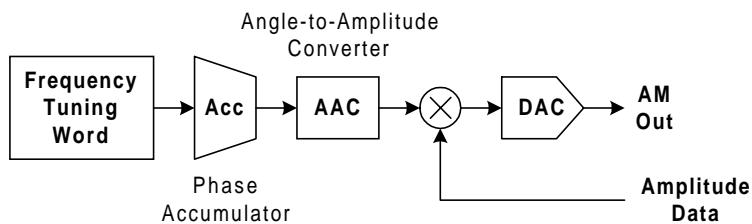


Figure 11.4. DDS With Amplitude Control

In Figure 11.4, assume that the value of the Amplitude Control word can take on values between 0 and 1, inclusive. When it is multiplied with the output of the Angle to Amplitude Converter (AAC), it effectively scales the AAC results. Thus, the data arriving at the input of the DAC is a scaled version of the AAC output. For example, if the Amplitude Control word is 0, then the input to the DAC is 0 and there is no AM signal present at the output of the DAC. As the value of the Amplitude Control word increases, the data arriving at the input to the DAC increases. For a Control Word of 1, the DAC data is the same as the data generated by the AAC. Thus, variations of the Amplitude Control word as a function of time effectively modulates the output of the DAC. This provides for a means to generate AM signals, as well as a means to gradually control carrier ON/OFF transients.

Synchronization of Multiple DDS Devices

There are applications in which it is desirable to synchronize two or more DDS's. A particular case is when it is necessary to generate time-synchronous analog I and Q channels. One DDS

can be used to generate the analog I channel and a second DDS the analog Q channel. However, it is imperative that the two devices be synchronized to minimize I-Q imbalance. A method for synchronizing two AD9850's or AD9851's is contained in the Appendix.

Alternatively, the AD9854 offers an integrated solution. It provides two output DACs; one for the I channel and one for the Q channel. Synchronization is handled on-chip, thus virtually eliminating phase imbalance between its quadrature outputs.