

## **Section 1. Fundamentals of DDS Technology**

### Overview

Direct digital synthesis (DDS) is a technique for using digital data processing blocks as a means to generate a frequency- and phase-tunable output signal referenced to a fixed-frequency precision clock source. In essence, the reference clock frequency is “divided down” in a DDS architecture by the scaling factor set forth in a programmable binary tuning word. The tuning word is typically 24-48 bits long which enables a DDS implementation to provide superior output frequency tuning resolution.

Today’s cost-competitive, high-performance, functionally-integrated, and small package-sized DDS products are fast becoming an alternative to traditional frequency-agile analog synthesizer solutions. The integration of a high-speed, high-performance, D/A converter and DDS architecture onto a single chip (forming what is commonly known as a *Complete-DDS* solution) enabled this technology to target a wider range of applications and provide, in many cases, an attractive alternative to analog-based PLL synthesizers. For many applications, the DDS solution holds some distinct advantages over the equivalent agile analog frequency synthesizer employing PLL circuitry.

### DDS advantages:

- Micro-Hertz tuning resolution of the output frequency and sub-degree phase tuning capability, all under complete digital control.
- Extremely fast “hopping speed” in tuning output frequency (or phase), phase-continuous frequency hops with no over/undershoot or analog-related loop settling time anomalies.
- The DDS digital architecture eliminates the need for the manual system tuning and tweaking associated with component aging and temperature drift in analog synthesizer solutions.
- The digital control interface of the DDS architecture facilitates an environment where systems can be remotely controlled, and minutely optimized, under processor control.
- When utilized as a quadrature synthesizer, DDS afford unparalleled matching and control of I and Q synthesized outputs.

### Theory of Operation

In its simplest form, a direct digital synthesizer can be implemented from a precision reference clock, an address counter, a programmable read only memory (PROM), and a D/A converter (see Figure 1-1).

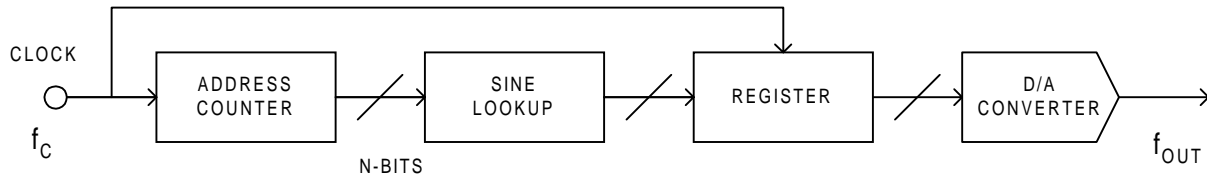


Figure 1-1. Simple Direct Digital Synthesizer

In this case, the digital amplitude information that corresponds to a complete cycle of a sine wave is stored in the PROM. The PROM is therefore functioning as a sine lookup table. The address counter steps through and accesses each of the PROM's memory locations and the contents (the equivalent sine amplitude words) are presented to a high-speed D/A converter. The D/A converter generates an analog sine wave in response to the digital input words from the PROM. The output frequency of this DDS implementation is dependent on 1.) the frequency of the reference clock, and 2.) the sine wave step size that is programmed into the PROM. While the analog output fidelity, jitter, and AC performance of this simplistic architecture can be quite good, it lacks tuning flexibility. The output frequency can only be changed by changing the frequency of the reference clock or by reprogramming the PROM. Neither of these options support high-speed output frequency hopping.

With the introduction of a phase accumulator function into the digital signal chain, this architecture becomes a numerically-controlled oscillator which is the core of a highly-flexible DDS device. As figure 1-2 shows, an N-bit variable-modulus counter and phase

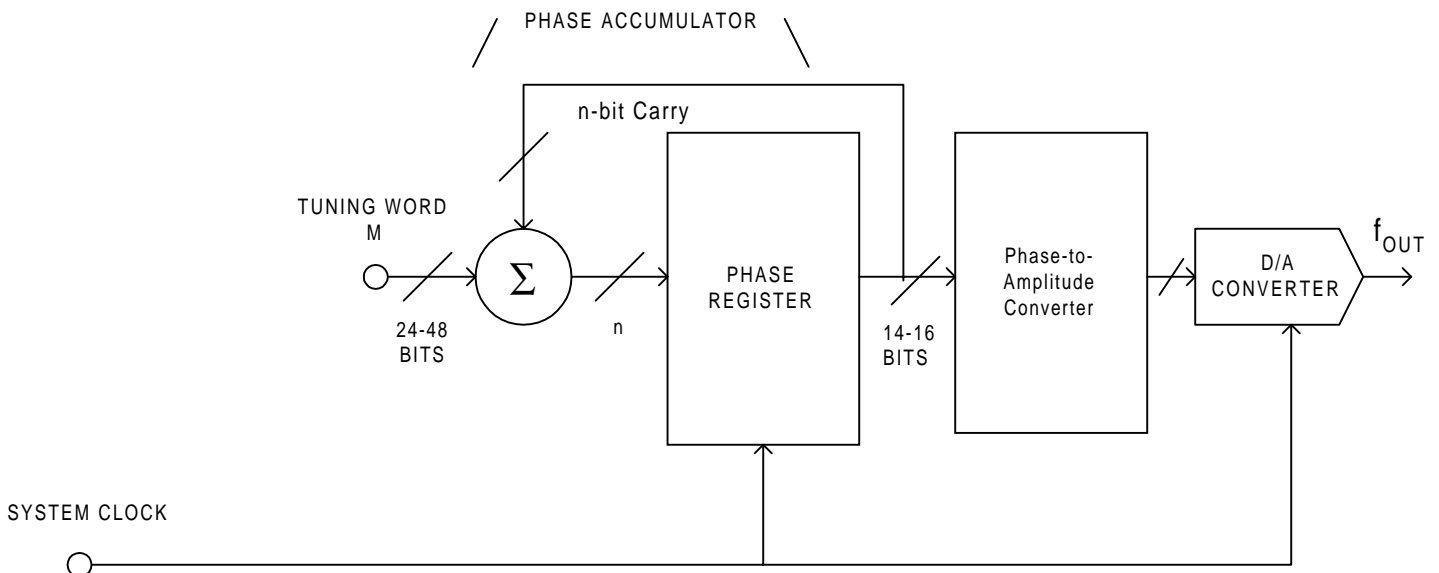


Figure 1-2. Frequency-tunable DDS System

register are implemented in the circuit before the sine lookup table, as a replacement for the address counter. The carry function allows this function as a “phase wheel” in the DDS architecture. To understand this basic function, visualize the sine wave oscillation as a vector

rotating around a phase circle (see Figure 1-3). Each designated point on the phase wheel corresponds to the equivalent point on a

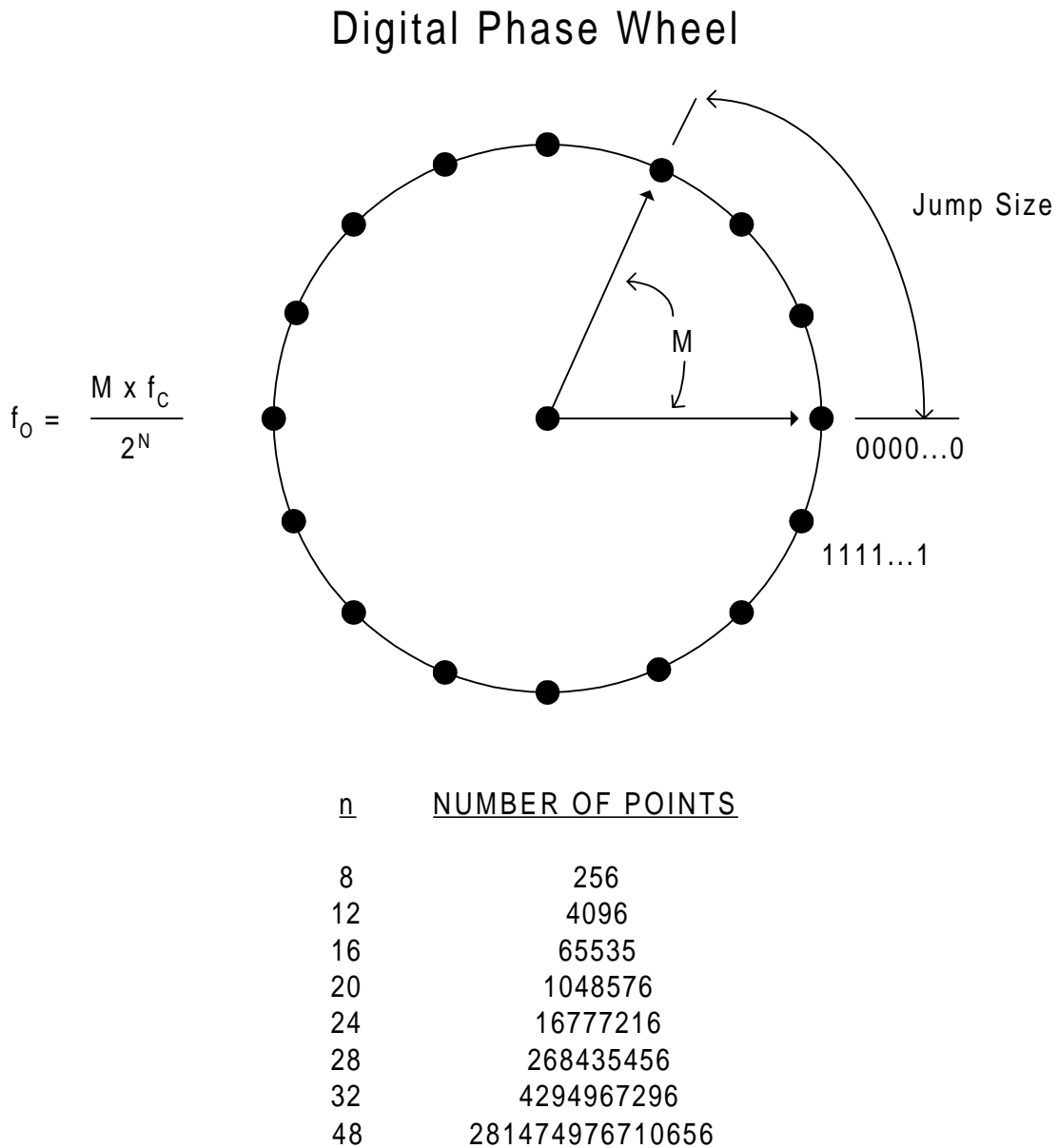


Figure 1-3. Digital Phase Wheel

cycle of a sine waveform. As the vector rotates around the wheel, visualize that a corresponding output sinewave is being generated. One revolution of the vector around the phase wheel, at a constant speed, results in one complete cycle of the output sinewave. The phase accumulator is utilized to provide the equivalent of the vector's linear rotation around the phase wheel. The contents of the phase accumulator correspond to the points on the cycle of the output sinewave. The number of discrete phase points contained in the "wheel" is determined by the resolution, N, of the phase accumulator. The output of the phase accumulator is linear and cannot directly be

used to generate a sine wave or any other waveform except a ramp. Therefore, a phase-to-amplitude lookup table is used to convert a truncated version of the phase accumulator's instantaneous output value into the sine wave amplitude information that is presented to the D/A converter. Most DDS architectures exploit the symmetrical nature of a sine wave and utilize mapping logic to synthesize a complete sine wave cycle from 1/4 cycle of data from the phase accumulator. The phase-to-amplitude lookup table generates all the necessary data by reading forward then back through the lookup table.

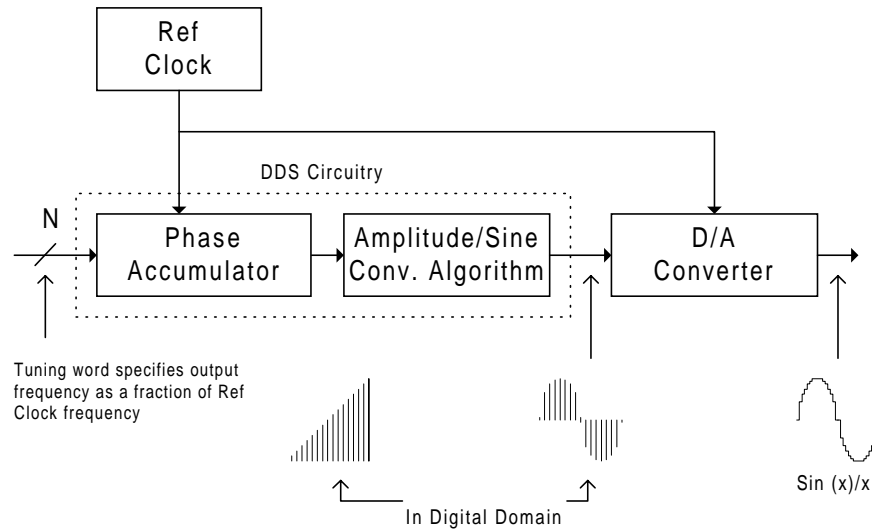


Figure 1-4. Signal flow through the DDS architecture

The phase accumulator is actually a modulus M counter that increments its stored number each time it receives a clock pulse. The magnitude of the increment is determined by a digital word M contained in a “delta phase register” that is summed with the overflow of the counter. The word in the delta phase register forms the phase step size between reference clock updates; it effectively sets how many points to skip around the phase wheel. The larger the jump size, the faster the phase accumulator overflows and completes its equivalent of a sine wave cycle. For a N=32-bit phase accumulator, an M value of 0000...0001(one) would result in the phase accumulator overflowing after  $2^{32}$  reference clock cycles (increments). If the M value is changed to 0111...1111, the phase accumulator will overflow after only  $2^1$  clock cycles, or two reference clock cycles. This control of the jump size constitutes the frequency tuning resolution of the DDS architecture.

The relationship of the phase accumulator and delta phase accumulator form the basic tuning equation for DDS architecture:

$$F_{OUT} = (M (REFCLK)) / 2^N$$

Where:  $F_{OUT}$  = the output frequency of the DDS

M = the binary tuning word

REFCLK = the internal reference clock frequency (system clock)

N = The length in bits of the phase accumulator

Changes to the value of M in the DDS architecture result in immediate and phase-continuous changes in the output frequency. In practical application, the M value, or frequency tuning word, is loaded into an internal serial or byte-loaded register which precedes the parallel-output delta phase register. This is generally done to minimize the package pin count of the DDS device. Once the buffer register is loaded, the parallel-output delta phase register is clocked and the DDS output frequency changes. Generally, the only speed limitation to changing the output frequency of a DDS is the maximum rate at which the buffer register can be loaded and executed. Obviously, a parallel byte load control interface enhances frequency hopping capability.

### Trends in Functional Integration

One of the advantages to the digital nature of DDS architecture is that digital functional blocks can readily be added to the core blocks to enhance the capability and feature set of a given device. For general purpose use, a DDS device will include an integrated D/A converter function to provide an analog output signal. This “complete-DDS” approach greatly enhances the overall usefulness and “user-friendliness” associated with the basic DDS devices. DDS devices are readily available with integrated 10-bit D/A converters supporting internal REFCLK speeds to 180 MHz. The present state of the art for a complete-DDS solution is at 300 MHz clock speeds with an integrated 12-bit D/A converter.

Along with the integrated D/A converter, DDS solutions normally contain additional digital blocks that perform various operations on the signal path. These blocks provide a higher level of functionality in the DDS solution and provide an expanded set of user-controlled features. The block diagram of an expanded-feature DDS device is shown in Figure 1-5.

The individual functional blocks are described below:

- (A) A programmable REFCLK Multiplier function include at the clock input, multiplies the frequency of the external reference clock, thereby reducing the speed requirement on the precision reference clock. The REFCLK Multiplier function also enhances the ability of the DDS device to utilize available system clock sources.
- (B) The addition of an adder after the phase accumulator enables the output sinewave to be phase-delayed in correspondence with a phase tuning word. The length of the adder circuit determines the number of bits in the phase tuning word, and therefore, the resolution of the delay. In this architecture, the phase tuning word is 14-bits.
- (C) An Inverse SINC block inserted before the D/A converter compensates for the  $\text{SIN}(X)/X$  response of the quantized D/A converter output, and thereby provides a constant amplitude output over the Nyquist range of the DDS device
- (D) A digital multiplier inserted between the Sine look-up table and the D/A converter enables amplitude modulation of the output sinewave. The width of the digital multiplier word determines the resolution of the output amplitude step size.

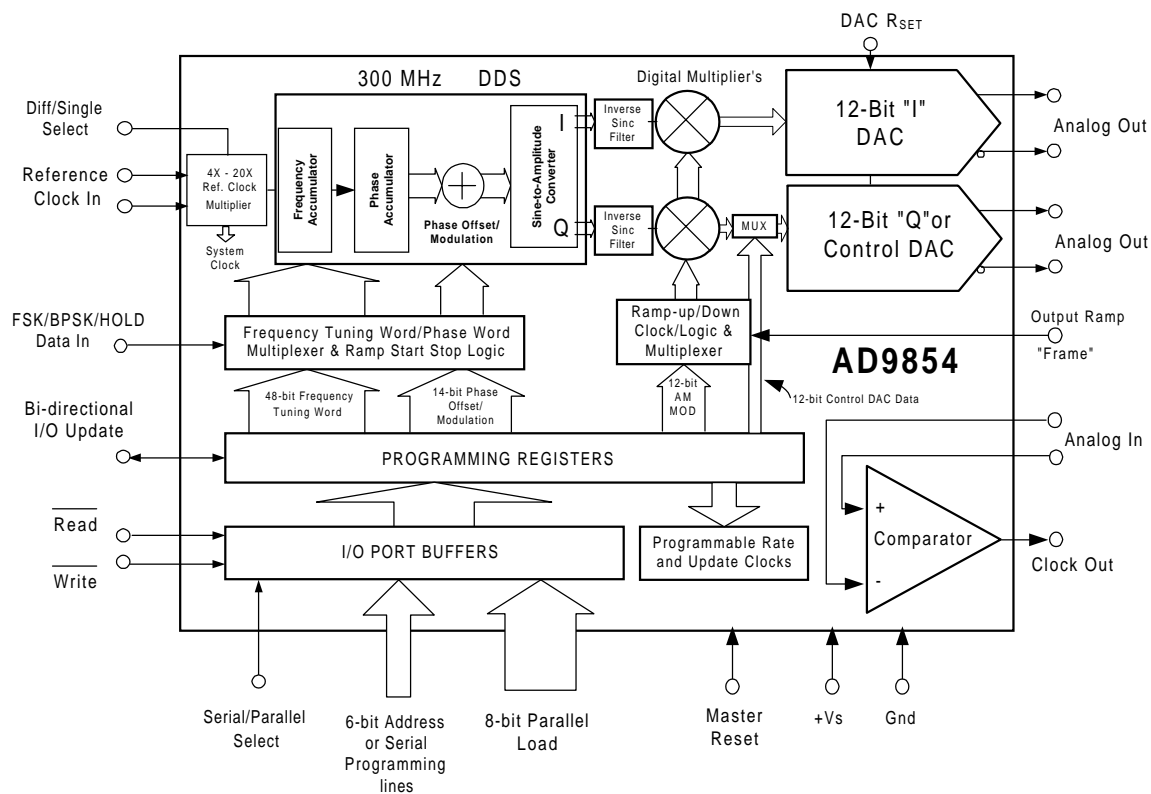


Figure 1-5. Full-featured 12-bit/300 MHz DDS Architecture

- (E) An additional high-speed D/A converter can be included to provide the cosine output from the DDS. This allows the DDS device to provide I and Q outputs which are precisely matched in frequency, quadrature phase, and amplitude. The additional D/A converter may also be driven from the control interface and used as a control DAC for various applications.
- (F) A high-speed comparator function can be integrated which facilitates use of the DDS device as a clock generator. The comparator is configured to convert the sinewave output from the DDS D/A converter into a square wave.
- (G) Frequency/phase registers can be added which allow frequency and phase words to be pre-programmed and their contents executed via a single control pin. This configuration also supports frequency-shift keying (FSK) modulation with the single-pin input programmed for the desired “mark” and “space” frequencies.

DDS devices are available that incorporate all of this functionality (and more) and support internal clock rates up to 300 MHz. The growing popularity in DDS solutions is due to the fact that all of this performance and functionality is available at a reasonable price and in a comparatively small package.

The following is a general guideline for the level of performance available from the dual 12-bit/300 MHz complete-DDS solution described in Figure 1-4. (Conditions assume 30 MHz external reference clock multiplied internally by 10 to yield an internal clock rate of 300 MHz):

-Frequency tuning word length = 48 bits which gives an output frequency tuning resolution of 1  $\mu$ Hz.

-Phase tuning word length = 14 bits which provides .022 degrees of phase delay control resolution.

-REFCLK Multiplier range = programmable in integer increments over the range of 4 $\times$  to 20 $\times$

-Output frequency bandwidth (assuming one-third of REFCLK rate) = 100 MHz

-Frequency tuning rate = 100 MHz with 8-bit byte parallel load

-Output amplitude control = zero output to fullscale in 8128 steps (12-bit control word)

-Output spurious performance = 50 dB worst case wideband spurs at 80 MHz output.

-I/Q output matching = .01 Degree

-Output flatness DC to Nyquist = .01 dB