

A Technical Tutorial **on Digital Signal Synthesis**



Outline

Section 1. Fundamentals of DDS technology

- Theory of operation
- Circuit architecture
- Tuning equation
- Elements of DDS circuit functionality and capabilities
- DAC integration
- Trends in functional integration

Section 2. Understanding the Sampled Output of a DDS Output

- Implications of the Nyquist Theorem
- Aliased images in the output
- Source of aliased images
- Calculating the occurrence of aliased images
- Quantization considerations
- Sin(X)/X response
- AC and DC linearity of the output

Section 3. Frequency/phase-hopping Capability of DDS

- Calculating the output tuning word
- Determining maximum tuning resolution
- Determining maximum tuning speed
- Understanding the DDS control interface
- Pre-programming profile registers

Section 4. The DDS Output Spectrum

- The effect of DAC resolution on spurious performance
- The effect of oversampling on spurious performance
- The effect of truncating the phase accumulator on spurious performance
- Additional DDS Spur sources
- Wideband spur performance
- Narrowband spur performance
- Predicting and exploiting spur "sweet spots" in a DDS' tuning range
- Jitter and phase noise considerations in a DDS system
- Output filtering considerations

Section 5. High-speed Reference Clock Considerations

- Implications of jitter and phase noise in the reference clock
- Reference clock multipliers
- SFDR performance vs. the REFCLK Multiplier function

Section 6. Interfacing to the DDS Output

Output power considerations
FS output current range and tradeoffs vs. spur performance
Single-ended vs. differential DAC output
Driving an output amplifier

Section 7. DDS as a Clock Generator

Definition of clock generator application for a DDS
Squaring the DDS output with an LP filter and comparator
Managing jitter in the clock generator application

Section 8. Replacing/Integrating a PLL with a DDS Solution

Traditional analog synthesizer vs. the DDS implementation
How DDS can eliminate analog upconverter stages
Example of implementation of DDS as an LO

Section 9. Digital Modulator Application of DDS

Basic digital modulator theory
System architecture and requirements
Digital filters
Multirate DSP
Clock and input data synchronization considerations
Data encoding methodologies and DDS implementations

Section 10. Using Aliased Images to Generate Nyquist + Frequencies from a DDS

Creating and isolating aliased images in the DDS output spectrum
SFDR performance expectations of the aliased image
Amplitude prediction of the aliased image
Frequency hopping considerations in the aliased image application

Section 11. Ancillary DDS Techniques, Features, and Functions

Improving SFDR with the addition of phase dither in the phase accumulator
Understanding DDS frequency “chirp” functionality
Achieving output amplitude control/modulation within a DDS device
Synchronization multiple DDS devices

Section 12. Techniques for Bench Evaluation of a DDS Solution

PC-based evaluation platforms and reference designs

Section 13. Integrating DDS-based Hardware into a System Environment

Analog/digital ground considerations

Power supply considerations

High-speed PCB layout techniques

Section 14. DDS Product Selection Guide

Appendix A – Glossary of Related Electronic Terms

Appendix B – Common Communications Acronyms

Appendix C – An FM Modulator using DDS

Appendix D – Pseudo-Random Generator

Appendix E - Jitter Reduction in DDS Clock Generator Systems