Appendix A - Glossary of Digital Communications Systems-Related Terms

A/D Converter	(also A/D or ADC) Short for analog-to-digital converter. This device convertes real-world analog signals into a digital format that can be processed by a computer. Video-speed A/D converters are those able to digitize video bandwidth signals (greater than 1MHz): some are capable of sampling at rates up to 500 million-samples-per-second (Msps) and beyond. The most common architectures for video-speed A/D converters are "flash" and "subranging."
AC Linearity	A dynamic measurement of how well an A/D performs. In an ideal A/D converter, a pure sine wave on the analog input appears at the digital output as a pure (sampled) sine wave. In the real world, however, spurious signals due to nonlinear distortion within the A/D appear in the digital output. These anomalies are usually combinations of harmonics of the fundamental and intermodulation products, produced when the fundamental and its harmonics beat with the sampling frequency. Only the spurious and harmonically-related signals that fall within the A/D's input bandwidth (half the sampling rate) are generally considered important. AC linearity is usually characterized in terms of harmonic disortion, signal-to-noise ratio, and intermodulation distortion performance.
Acquisition Time	This term relates to sampling A/D's which utilize a track/hold amplifer on the input to acquire and hold (to a specified tolerance) the analog input signal. Acquisition time is the time required by the T/H amp to settle to its final value after it is placed in the track mode.
Active Filter	An active filter is one that uses active devices such as operational amplifiers to synthesize the filter response function. This technique has an advantage at high speeds because the need for inductors (with their poor high-frequency characteristics) is eliminated.
Aliased Imaging	This is a technique, commonly applied to **Direct Digital Synthesis** (DDS), for using intentional aliasing as a source of high-frequency signals. The following spectral plot illustrates a DDS output with a clock frequency of 51MHz and fundamental output of 25.5MHz. Aliased images appear at 32MHz, 70MHz, 83MHz, etc., which can be used as signal sources when isolated with a bandpass filter.

Aliasing	In a sampled data system, the analog input must be sampled at a rate of $F_S > 2F_A$ in order to avoid loss of data (Nyquist Theorem). Adhereing to the Nyquist Theorem prevents in-band "alias" signals, which are beat frequencies between the analog signal and the sampling clock that inherently occur at $F_S \pm F_A$. As the Nyquist limit is exceeded, the aliased signals move within the band of the analog input (DC - $F_S/2$) and create distortion. Likewise, high-frequency noise can also be aliased into the input signal range which mandates low-pass filtering, or anti-alias filtering, on the input of a sampled system. See also **Aliased Imaging**.
Analog Ground	In high-speed data acquisition applications, system ground is generally physically separated into "analog" and "digital" grounds in an attempt to supress digital switching noise and minimize its effect on noise-sensitive analog signal processing circuitry. Input signal conditioners, amplifiers, references, and A/D converters are usually connected to analog ground.
Aperture Delay Time	This term applies to A/D converters and Track/hold amplifiers and defines the time elaspsed from the application of the "hold" (or "encode") command until the sampling switch opens fully and the device actually takes the sample. Aperture delay time is a fixed delay time and is normally not in itself an error source since the "hold" clock edge can be advanced to compensate for it.
Aperture Jitter	Uncertainty, or sample-to-sample of variation, in the aperture delay time. Aperture jitter is a source of error in a sampling system and it determines the maximum slew rate limitation of the sampled analog input signal for a given system resolution.
Asymmetrical Digital	A digital communications application that allows for up to 7MBPS of Subscriber Line data transmission capacity over conventional twisted pair telephone lines. ADSL is a contender for a major piece of the "information highway" pie and it promises to deliver telephone, TV, and data services to your home over the exisiting telephone line.
Asynchronous Transfer Mode	A multiplexing and switching technique that organizes information into fixed-length cells consisting of an identification header field and an information field. The tranfer rate is asynchronous in that the recurrence of cells depends on the instantaneously required bit rate.

Autocorrelation	Multiplication of a signal with a time-delayed replica of itself.
Baseband	The frequency bandwidth of the fundamental signal of interest i.e., the voice, audio, or video signal bandwidth, within a communication system.
Base Station	The central transmitter in a communications system that acts as the cell hub for communicating with handsets and/or mobile units.
Baud Rate	The speed at which data is transmitted measured in symbols-per-second.
Bit Rate	The rate of transfer of information necessary to insure satisfactory reproduction of the information at the receiver.
Buffer Amplifier	A unity gain amplifier used to isolate the loading effect of one circuit from another. Buffer amplifiers are almost always used between the signal source and the input of a high-speed A/D converter.
Cable Telephony	This is the idea of using digital communications techniques to provide enhanced home telephone service via the exisiting home cable-TV connections. The bandwidth of cable is high enough to simultaneously support interactive cable-TV, telephone communications, and on-line data services. In this scenario, the cable connection becomes the primary link to the information highway vs. twisted pair telephone wire or a wireless connection.
Chip	A single frequency output from a frequency hopping signal source.
Chip Rate	In spread spectrum systems, this is the rate at which the pseudo-random noise code is applied. In frequency hopping systems, chip rate is the inverse of the dwell time which the output frequency occupies a single carrier frequency. Also called "chipping rate".
Chirp	Pulsed frequency modulation scheme in which a carrier is swept over a wide frequency band during a given pulse interval.
Cross-correlation	The degree of agreement between two unlike signals.
D/A Converter	(also D/A or DAC). Short for digital-to-analog converter, this is a device that changes a digitally-coded word into its "equivalent" quantized analog voltage or current. Just like the A/D device, there are very high-speed D/A's available, capable of converting at data rates up to 1GHz.

Differential Nonlinearity	(also DNL) In an ideal D/A and A/D converter, any two adjacent digital codes should result in measured ouput (or input) values that are exactly one LSB apart. Any positive or negative deviation in the measured "step" from the ideal differences is called differential non-linearity. It's expressed in (sub) multiples of 1 LSB. DNL errors more negative than -1 LSB can result in a non-monotonic response in a D/A and missing codes in an A/D.
Digital Downconversion	(also direct-IF-to-digital conversion) This refers to a demodulation technique for sampling an intermediate frequency (IF) signal with a wide-bandwidth A/D whose sampling rate is equivalent to the local oscillator frequency (<IF frequency). In this super-Nyquist application the A/D serves as the mixer stage and its digital output data is a beat frequency; the modulation data can be recovered with a DSP stage.
Digital Filtering	The process of smoothing, spectrally shaping, or removing noise from a signal has traditionally been accomplished with analog components. With the advent of high-speed DSP products, now filtering can effectively and economically be accomplished in the digital domain. Digital filters are basically mathematical functions that are performed on the digital data stream and their characteristics can be altered under software control which adds to their overall flexibility. Finite Impulse Response (FIR) and Infinite Inpulse Response (IIR) are examples of digital filter functions.
Direct Digital Synthesis	(DDS) A process by which you can digitally generate a frequency-agile, highly-pure sinewave, or arbitrary waveform, from an accurate reference clock. The digital output waveform is typically tuned by a 32-bit digital word which allows sub-Hz frequency agility. The DDS's frequency output is normally reconstructed with a high-speed, high- performance D/A to generate an analog output signal. The ability to add internal functions such as phase modulation, amplitude modulation, digital filtering, and I&Q outputs, are making DDS devices attractive for digital communication applications. They serve in capacities such as modulators, local oscillators, and clock detect/recovery circuits.
Dither	The technique of adding controlled amounts of noise to a signal to improve overall system loop control, or to smear quantizing error in an A/D converter application.

Dynamic Range	The ratio of the maximum output signal to the smallest output signal that can be processed in a system, usually expressed logarithmically in dB. Dynamic range can be specified in terms of harmonic distortion, signal-to-noise ratio, spurious-free dynamic range, or other AC input-based performance criteria
ENOBs	Stands for "Effective Number of Bits". ENOB's are a measure of an A/D's dynamic performance as compared to that of a theoretically perfect A/D transfer function. ENOB's are calcluated by the formula: (ENOB=SNR Actual- 1.76dB)/6.02. An high-speed A/D with 10-bits of resolution typically will <9 ENOBS of dynamic performance at a Nyquist analog input bandwidth.
FFT	Fast Fourier Transform. A computationally efficient mathematical technique which converts digital information from the time domain to the frequency domain for rapid spectral analysis. FFT's generally utilize a "time weighting" function to compensate for data records with a non-integer number of samples; some poplular weighting functions are Hanning Window and 4-term Blackman-Harris, which are presented in Appendix 4 of this glossary.
Frequency Hopping System	Carrier frequency shifting in discrete increments in a pattern dictated by a code sequence. The transmitter jumps from frequency-to-frequency within some predetermined set: the order of frequency hops is determined by a code sequence which, in turn, is detetected and followed by the receiver.
Frequency Shift Keying	A modulation scheme that shifts between two frequencies to represent a "1" or "0" state of data transmission.
Glitch	A spike caused by the skew (difference in turn-on/turn-off time) of switches or logic. Glitches are a troublesome source of error in high-speed D/A converters and they are most prevalent at the mid-scale switching location, when all digital input bits are switching. Glitch energy is specified in picovolt-seconds which describes the area under the voltage-time curve at its worst case occurence.
Group Delay	Distortion resulting from nonuniform speed of transmission of the various frequency components of a signal through a transmission medium, specifically, the propagation delay of a lower frequency is different from that of a higher frequency. This creates a time-related "delay distortion" error.

Heterodyne	A process by which two signals are mixed for the purpose of cross-frequency translation. Integral Nonlinearity (INL) This term describes the absolute accuracy of a converter. It is the maximum deviation, at any point in the transfer function, of the converter's output from its ideal value.
I&Q	In-phase and Quadrature - A modulation technique whereby signal information is derived from a carrier frequency at its 0° and 90° phase angles.
Jitter	Unwanted variations in the frequency or phase of a digital or analog signal.
Mixer	Circuit block used to translate signals from one frequency to another.
Multipath Propagation	A transmission path anomaly that acts as a time-varying source of signal non-linearity. Multipath can distort or reduce a received signal to the point of unreliable reception. In television, multipath is manifested as image "ghosting".
Nyquist Theorum	This theorum says that if a continuous bandwidth-limited signal contains no frequency components higher than f_C then the original signal can be recovered without distortion if its is sampled at a rate of at least 2 f_C.. This theorum applies to A/D converter applications as well as data transmission density over limited-bandwidth channels.
Orthogonal	Term used to signify that two signals (or signal attributes) are mutually transparent and non-interfering with each other. Frequency and amplitude modulation are orthogonal signal attributes.
Packet	A digital communications technique involving the transmission of short bursts of data in a protocol format that contain addressing, control, and error-checking information, along with the field information, in each transmission burst.
Phase Locked Loop	(PLL) A circuit containing a voltage-controlled oscillator whose output phase or frequency can be "steered" to keep it in sync with a reference source. A PLL circuit is generally used to lock onto and "up-convert" the frequency of a stable source.

Phase Noise	The amount of phase noise energy contained in a frequency carrier. Specified in dB/Hz, phase noise amplitude is usually characterized and plotted in 1Hz increments, offset from the carrier. The following illustrates phase noise from various frequencies synthesized by a DDS device clocked at 50MHz. [Insert phase noise plot]
Programmable Gain	(PGA) An amplifier with an analog- or digitally-controlled gain Amplifier function. A PGA can be used in front of an A/D converter to effectively increase its dynamic range.
Pulse Code Modulation	A method of quantizing audio-range analog signals into a digital form for transmission in digital communications systems, or for processing in DSP. Effectively the same as Analog-to-Digital conversion.
Pseudo-noise	Any group of code sequences that exhibit a noise-like characteristic.
Phase Shift Keying	(PSK) A digital modulation technique whereby the phase of a carrier frequency is shifted to represent a digital "1" or "0" state. In "Quadri-phase-shift keying" systems, the phase angle locations of 0°, ±90°, and 180°, are used as reference points to represent sixteen possible digital states (2^4).
Quadrature Amplitude	(QAM) This communication scheme involves the modulation of a carrier by two different signals. One signal modulates the carrier (I) and the other signal modulates the carrier shifted by 90° (Q). The two modulated carriers are then summed and transmitted as a single I&Q modulated carrier. The receiver decodes the I&Q channels and demodulates them 90° apart. QAM lends itself to the transmission of data in a digital format by assigning discrete levels to the two signal inputs which creates a "constellation" of possible digital word combinations on the I&Q graph. The following illustrates a 16-QAM constellation (4 levels of input on the I channel/4 levels of input on the Q channel).
Sin(X)/X	The output of a D/A converter is a series of quantized levels that represent an analog signal whose amplitude is determined by the sin (X)/X response. At higher output frequencies, a D/A converter application may require a sin(X)/X compensation filter to normalize its output amplitude.

Spread Spectrum	This communications technique has been used in secure military systems for a number of years and is now becoming popular in commercial systems. This format involves transmitting information which has been multiplied by a pseudo-random noise (PN) sequence which essentially "spreads" it over a relatively wide frequency bandwidth. The receiver detects and uses the same PN sequence to "despread" the frequency bandwidth and decode the transmitted information. This communications technique allows greater signal density within a given transmission bandwidth and provides a high degree of signal encrytion and security in the process.
Spurious-free Dynamic	(SFDR) This refers to the range between the highest level of the fundamental Range frequency and the highest level of any spurious, or harmonically- related, signal. SFDR is expressed in dB.
Wavelet	A mathematical algorithm that is used to efficiently compress and decompress the phase & frequency information that is contained in a transmitted signal.
Wireless Telephony	The idea of replacing the conventional twisted pair telephone service to the home with a wireless RF connection. High-speed digital communications techniques would be utilized to allow enhanced telephone, multimedia, and data services to be transmitted over the airwaves to the home subscriber. In this scenario, the link to the information highway will be wireless.

Appendix B - Digital Communications Systems-Related Acronyms

ADC	Analog-to-Digital Converter
ADSL	Asynchronous Digital Subscriber Loop
AGC	Automatic Gain Control
AM	Amplitude Modulation
AM-PSK	Amplitude Modulation with Phase-Shift Keying
AMPS	Advanced Mobile Phone System
ASK	Amplitude-Shift Keying
ATM	Asynchronous Transfer Mode
BER	Bit Error Rate (Ratio)
BPSK	Binary-Phase-Shift-Keying
CCITT	International Telephone and Telegraph Consultive Commitee
CDMA	Code-Division Multiple Access
CDPD	Cellular Digital Packet Data
CMOS	Coated Metal Oxide Semiconductor
CODEC	Coder/decoder
CSMA	Carrier-Sense Multiple Access
CSMA/CD	Carrier-Sense Multiple Access with Collision Detection
CT-2	Cordless Telephone 2
DAC	Digital-to-Analog Converter
DBS	Direct Broadcast Satellite
DCPSK	Differentially Coherent Phase Shift Keying
DDS	Direct Digital Synthesis

DECT	Digital European Cordless Telephone
DFT	Discrete Fourier Transform
DM	Delay Modulation
DNL	Differential Non-Linearity
DPCM	Differential Pulse-Code Modulation
DPSK	Differential Phase-Shift Keying
DSL	Asymmetrical Digital Subscriber Line
DSK	Downstream Keyer
DSMS	Direct Sequence Modulated System
DSX	Digital Signal Cross-Connect
DQPSK	Differential Quadrature-Phase-Shift-Keying
DWT	Discrete Wavelet Tone
DSP	Digital Signal Processing
DWMT	Discrete Wavelet Multi-tone
ENOB	Effective Number of Bits
ESMR	Enhanced Specialized Mobile Radio
FDD	Frequency-Division Duplex
FDMA	Frequency-Division Multiple Access
FDX	Full Duplex
FFT	Fast Fourier Transform
FIR	Finite-Impulse-Response Filter
FM	Frequency Modulation
FSK	Frequency Shift Keying

GFSK	Gaussian Frequency-Shift-Keying
GMSK	Gaussian Minimum Shift-Keying
GPS	Global Positioning Satellite
GRI	Group Repetition Interval
GSM	Global System for Mobile Communications
HDSL	Highspeed Digital Subscriber Line
HDX	Half Duplex
HFC	Hybrid Fiber Coax
HSDS	High-speed FM Subcarrier Data System
IIR	Infinite Impulse Response
IMD	Intermodulation Distortion
INL	Integral Non-Linearity
I&Q	In-phase and Quadrature
ISI	Intersymbol Interference
JCT	Japanese Cordless Telephone
JDC	Japanese Digital Cellular (now PDC)
LAN	Local Area Network
LAP	Link Access Protocol
LNA	Low-Noise-Amplifier
LOS	Line-of-Sight
MAC	Medium Access Control
MAS	Multiple-Address-Services
MFM	Modified Frequency Modulation

Modem	Abbreviation for modulator-demodulator
MQPSK	Modified Quadri-Phase-Shift-Keying
MSS	Mobile Satellite Services
NADC	North American Digital Cellular (IS-136)
NRZ	Non-return-to-zero
OFDM	Orthoganol Frequency Division Modulation
OOK	On-Off Keying
OQPSK	Offset Quadri-Phase-Shift-Keying
PAM	Pulse Amplitude Modulation
PBX	Private-Branch-Exchange
PCN	Personal Communications Network
PCM	Pulse Code Modulation
PCS	Personal Communications Services
PCIA	Personal Communcations Industry Association
PDC	Personal Digital Cellular (formerly JDC)
PDM	Pulse Duration (Density) Modulation
PFM	Pulse Frequency Modulation
PGA	Programmable Gain Amplifier
PHS	Personal Handy Phone System
PLL	Phase Locked Loop
PN	Pseudo-Random Noise
PM	Phase (Pulse) Modulation
PRBS	Pseudo-Random Bit Stream

PSK	Phase-shift-Keying
PSTN	Public Switched Telephone Network
QAM	Quadrature Amplitude Modulation
QPSK	Quadri-Phase-Shift-Keying
RF	Radio Frequency
RFI	Radio Frequency Interference
RFID	RF Identification.
RSSI	Received Signal Strength Indication
Rx	Receiver
RZ	Return to Zero
SAW	Surface Acoustic Wave
SCPDM	Suppressed Clock Pulse Duration Modulation
SDLIC	Synchronous Data Link Control
SFDR	Spurious-Free Dynamic Range
SINAD	Signal-to-Noise and Distortion
SMR	Specialized Mobile Radio
SMT	Surface Mount Technology
SNR	Signal-to-Noise Ratio
SONET	Synchronous Optical Network
SPP	Sequenced Packet Protocol
SS	Spread Spectrum
SSB	Single Sideband
SSHE	Spread Spectrum Headend

SQPSK	Staggered Quadriphase Shift Keying
SWR	Standing Wave Ratio
TACS	Total Access Communication System
TDD	Time-Division Duplex
TDM	Time Division Multiplexing
TDMA	Time-Division Multiple Access
TTL	Transistor-to-Transistor Logic
Tx	Transmitter
UPS	Uninterruptible Power Supply
UTC	Universal Time Code (Coordinated Universal Time)
VHF	Very High Frequency
VLF	Very Low Frequency
VSWR	Voltage Standing Wave Ratio
WAN	Wide Area Network
WAFU	Wireless Fixed Access Unit
WDM	Wavelength Division Multiplexing
WLAN	Wireless Local Area Network
WLL	Wireless Local Loop
WWW	World Wide Web
Z	Impedance

Appendix C - An FM Modulator using DDS

Appendix D - Pseudo - Random Generator

Pseudorandom Binary Sequence (PRBS) Generator Basics

The problem at hand is to devise a simple and efficient means to randomly generate a sequence of random bits (i.e., a sequence of 1's and 0's). The method behind generating random bits is based on the theory of *modulo 2 primitive polynomials*.

In general, an n^{th} degree polynomial takes the form:

$$a_n x^n + a_{n-1} x^{n-1} + a_{n-2} x^{n-2} + \ldots + a_2 x^2 + a_1 x + a_0$$

Or, in more compact form:

$$\sum_{k=0}^{n} a_k \, x^k$$

where a_k are the coefficients of the polynomial. A modulo 2 polynomial is simply a polynomial in which the coefficients are constrained to two possible values: 0 and 1. An example of a modulo 2 polynomial (4^{th} degree) is shown below.

$$x^4 + x^3 + x^1 + 1$$

Note that it is not necessary to explicitly display the coefficients. Since the coefficients are constrained to 0 or 1, a polynomial term is either present (coefficient of 1) or absent (coefficient of 0). In the example above, all coefficients are 1 except for the 2^{nd} degree term; hence its absence.

In the opening paragraph reference was made to *primitive* polynomials. A modulo 2 polynomial is *primitive* if it cannot be factored. It should be noted that the polynomial example shown earlier is <u>not</u> primitive. It can be factored as follows:

$$x^4 + x^3 + x^1 + 1 = (x^3 + 1)(x + 1)$$

An example of a *primitive* 4^{th} degree polynomial is shown below. Notice that it cannot be factored.

$$x^4 + x^1 + 1$$

It is interesting to note that the coefficient of the 0^{th} term of a modulo 2 *primitive* polynomial is always 1. That is, a modulo 2 primitive polynomial will always end with "… + 1". The reason should be clear. If the polynomial does not end with a 1, then it must end with some k^{th} degree term ($k < n$). Since the k^{th} degree term is the lowest term in the polynomial, then x^k can be factored out of the polynomial. This makes the polynomial factorable by x^k, thus rendering it *non*-primitive.

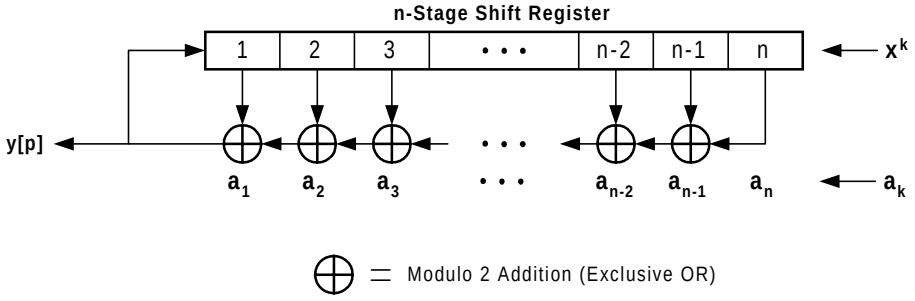
One of the properties of PRBS generators is that the "random" sequence eventually repeats. Hence the term, "pseudorandom". The number of bits that a PRBS can generate before repeating defines the *length*, L, of the PRBS generator. It turns out that there is a relationship between the length, L, of a PRBS generator and degree, n, of the primitive polynomial used to define it. That relationship is shown below:

$$L = 2^n - 1.$$

The first step in designing a PRBS generator is to determine the required length, L. This establishes the minimum degree of the primitive polynomial that must be employed in the design.

The second step in designing a PRBS is to select a suitable primitive polynomial of appropriate degree. Finding primitive polynomials of a particular degree can be a challenge, but there is help. Published lists are available from a number sources. For example, in Ref. [2] primitive polynomials for $n \leq 100$ can be found. Also, a nearly inexhaustible supply of primitive polynomials can be found with a search of the Internet.

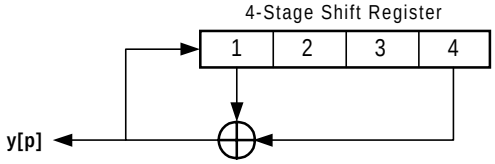
The form of the primitive polynomial relates directly to the design of a *linear feedback shift register* (**LFSR**). The general form of an LFSR is shown below. The output, y[p], is the pseudorandom binary sequence.



n-Stage Linear Feedback Shift Register (LFSR)

Note that each stage of the shift register corresponds to one of the x^k terms of a polynomial, while each associated XOR operation corresponds to one of the a_k coefficients. The coefficients serve as feedback elements. This allows for a direct correlation between the primitive polynomial and the LFSR. It should be noted that for every 0 coefficient of the primitive polynomial, the associated XOR in the feedback path of the LFSR can be removed. The underlying reason is that in modulo 2 addition we have: $0 \oplus q = q$. The implication is that the XOR of 0 with a value yields the same value, rendering the operation superfluous.

With the knowledge of how the primitive polynomial and LFSR are related it is possible to design a PRBS of any desired degree. For example, using the 4^{th} degree primitive polynomial listed previously the corresponding PRBS generator is shown below.



4-th Order PRBS

The above PRBS generator has a pseudorandom sequence of length, $L = 2^4 - 1 = 15$. It should be mentioned at this point that a PRBS fashioned in this manner must be given a non-zero "seed" value in order to guarantee start up. That is, the shift register must be preloaded with a non-zero value. Notice that if the shift register is initialized with all 0's, y[p] will always be 0. Thus, any hardware implementation must ensure that the shift register starts with some non-zero value. It is interesting to note that the choice of the seed value is immaterial. The n-bit initial seed value will not repeat until L bits have been generated at y[p].

A pseudorandom binary sequence generated in the manner just described possesses some interesting properties. Some of these properties are listed below.

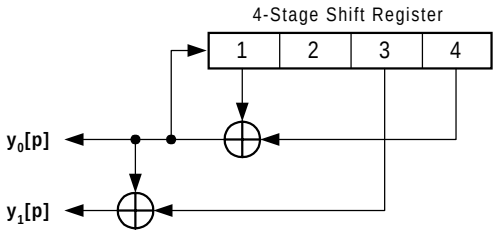
1. Any group of L consecutive bits of y[p] will contain 2^{n-1} ones and $2^{n-1} - 1$ zeroes.

2. In any group of L consecutive bits of y[p], if we slide an n-bit window along the sequence, each n-bit word thus obtained will appear exactly once (excluding the "all zeroes" word, which does not occur at all).

3. The modulo 2 sum of a PRBS and any shifted version of itself, produces another shifted version of itself.

It is important to mention that a PRBS is only useful for generating a random sequence of individual bits. It is not useful for generating random M-bit words. In other words, suppose that it is desired to generate a random sequence of 4-bit numbers. One might be tempted to take groups of 4 bits generated by a PRBS and consider them as a random sequence of 4-bit numbers. Such is not the case. The solution is to generate 4 independent PRBS streams and concatenate their outputs to produce random 4-bit numbers. As a matter of fact, it is preferable that each of the PRBS generators used in a multi-bit random number generator be of a different order.

It turns out, that Property #3 above can be used to generate multi-bit random numbers using a single LFSR. The diagram below is a 2-bit random number generator using a modification of the 4^{th} order PRBS designed earlier.



2-Bit 4^{th} Order Pseudorandom Number Generator

Here, $y_0[p]$ is the original pseudorandom bit sequence. Note that $y_1[p]$ is the modulo 2 sum of $y_0[p]$ (the original) and a tap of the 3rd stage of the shift register. But the 3rd stage of the shift register is simply a replica of $y_0[p]$ delayed by 3. Thus, Property #3 dictates that $y_1[p]$ is a shifted version of $y_0[p]$. Therefore, we can think of $y_0[p]$ and $y_1[p]$ as two separate 4th order pseudorandom sequences but with differing seed values. This makes the two sequences useful for generating the individual bits of a 2-bit number. Hence, we have the makings of a 2-bit random number generator. This concept can be extended to generate pseudorandom numbers with any desired bit width.

References:

[1] Gibson, J. D., 1993, Principles of Digital and Analog Communications, Prentice-Hall, Inc.

[2] Press, H. P., Teukolsky, S. A., Vetterling, W. T., Flannery, B. P., 1992, Numerical Recipes in C: The Art of Scientific Computing, Cambridge University Press.

Appendix E - Jitter

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Jitter Reduction in DDS Clock Generator Systems

by: Rick Cushing, HSC Applications Engineer

One of the most frequently asked questions regarding DDS clock generator applications is how to minimize clock edge jitter. Here are some basic steps in assuring best jitter performance:

1. Use a stable reference clock for the DDS
2. Filter the DDS output to reduce all non-harmonic spurs to at least –65 dBc.
3. Drive the comparator inputs differentially.
4. Provide plenty of comparator over-drive (at least 1 volt p-p).
5. Provide low Z inputs to the comparator to suppress high Z noise sources.
6. Use an external comparator or divider for very demanding applications.
7. Avoid using slow slew rate signals.
8. Use spur reduction techniques.

Using a stable reference clock to the DDS is obvious since jitter in = jitter out. Filtering of the DDS output requires some elaboration. Bandpass filtering is best since spurs may reside well below and above the fundamental output. If wideband output is required, then a low pass filter is the only choice, but jitter performance will be compromised. To make filtering easier, keep the system clock frequency as high as possible to distance the image spurs as far as possible from the fundamental.

Driving the comparator inputs with a low impedance, differential, 1 V p-p input signal is “as good as it gets”. The low impedance input discourages extraneous noise and comparator “kick-back”. The merits of differential inputs include common-mode noise rejection and 2X the input slew rate. A passive broadband 1:1 RF transformer is useful in changing from single-ended to differential configuration; however, it will not pass dc so some means of biasing to the comparator input range may be needed. Sufficient comparator input overdrive keeps output dispersion (variation in propagation delay) to a minimum and promotes decisive switching.

Use of an off-chip comparator is recommended since the hostile (noisy) DDS environment degrades jitter performance. In choosing an external high-speed comparator, look for good PSRR specifications, proper output logic levels, low dispersion and single supply operation.

5 MHz and above: These are the easiest signals to handle due to their fast slew rates. A reason-able jitter figure for these frequencies is about 75 ps p-p using the above techniques. Higher frequency signals have higher harmonic distortion. This is not bad until the harmonic is “aliased” back into the passband to the comparator where it becomes a non-harmonically related product that will increase jitter.

Aliased harmonics can be reduced by passing the filtered fundamental and spurs to a passive frequency mixer, upconverting to a much higher frequency and then dividing down (example VHF divider is a Mitel SP8402) to your desired output frequency. The frequency division process does two very desirable things:

1. Reduces spurious components by 20LOG(N) – where N is the division ratio.
2. Gives you a square wave output which may eliminate the need for a comparator if the divider has suitable logic levels.

Below 5 MHz: *Much more difficult to get good jitter performance due to the slow slew rate of the fundamental. Best results are obtained by outputting a much higher frequency than needed and then dividing down to your desired output. The same benefits as 1 and 2 above will apply. This method of spur reduction is especially useful when extremely low frequencies with low jitter are needed. Depending on external frequency division ratios, jitter levels approaching 75 ps p-p seem obtainable. Without frequency division, a 1 kHz sine wave could produce 10 ns p-p jitter just due to the slow slew to the comparator.*