Practical Power Solutions

SECTION 4
HARDWARE DESIGN TECHNIQUES

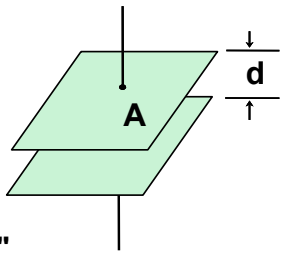
Passive Components

Passive components play a significant role in the operation of switch mode power supplies (SMPS). Inductors are the primary energy storage device in most SMPS. Capacitors are used for filtering, decoupling, energy storage, and affect the design of the compensation network since the SMPS is a closed-loop feedback system. Resistor dividers are often used to set the output voltage, and low value resistors are often used in current sense applications.

Capacitors

- A capacitor is an energy storage element constructed of 2 conductors separated by an insulating material

$$C = \varepsilon \cdot \varepsilon_0 \cdot \frac{A}{d} \qquad E_{STORED} = \frac{1}{2} \cdot C \cdot V^2$$



- Where
  - ε_0 is the dielectric constant of free space
  - ε is the relative dielectric constant of insulator
  - ε is sometimes called the "k-factor" or simply "k"
  - A is area of conductive plates
  - d is distance between plates
  - V is the voltage potential across plates
- Larger capacitors have larger capacitance, and therefore better energy storage.
- Different capacitors use different dielectric material. This changes capacitance and their characteristics (ESR, Current Rating, DC Bias, etc) in power designs

This figure shows the basics of capacitors.

Capacitors come in a wide variety of sizes, both in capacitance value and physical size. Choosing the right capacitor for a specific application can be crucial to the proper operation of the circuit. Choosing the right capacitor means not only choosing the correct value but also the right dielectric material as well. As we will see in the following pages, real world capacitors are far from ideal, especially over a wide frequency range.

The capacitance can be calculated from the information in this figure. It is dependant on the dimensions of parallel conductors, the separation of the conductors, and the dielectric constant of the insulator. The capacitive impedance can be calculated from:

$$Z_C = 1/j\omega C$$

where:

$$j = \sqrt{(-1)}$$

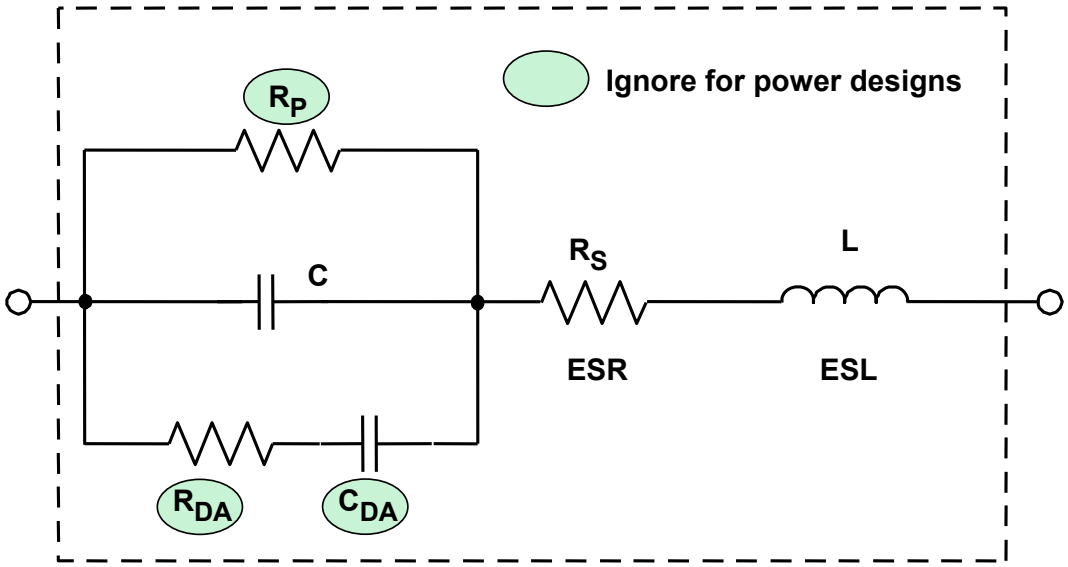
and

$$\omega = \text{radian frequency} = 2\pi \cdot \text{frequency in Hertz.}$$

The energy stored in the capacitor which is charged to a voltage, V, is given by the formula:

$$E = 0.5CV^2$$

A Real Capacitor Equivalent Circuit Includes Parasitic Elements

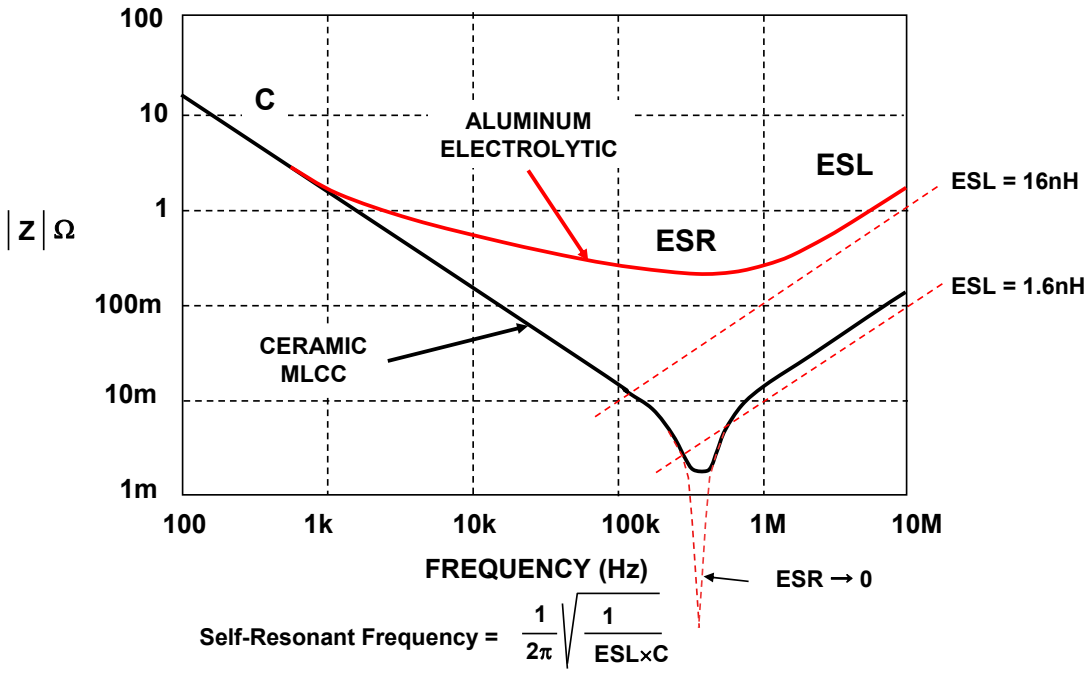


This is a workable model of a non-ideal capacitor. The nominal capacitance, C, is shunted by a resistance, R_P, which represents insulation resistance or leakage. A second resistance, R_S, (equivalent series resistance, or ESR), appears in series with the capacitor and represents the resistance of the capacitor leads and plates.

Note that elements in the capacitor equivalent circuit aren't that easy to separate. The model is for convenience in explanation. Inductance, L (equivalent series inductance, or ESL), models the inductance of the leads and plates. Finally, resistance R_{DA} and capacitance C_{DA} together form a simplified model of a phenomenon known as *dielectric absorption*, or DA. This can degrade fast and slow circuit dynamic performance. In a real capacitor, R_{DA} and C_{DA} may actually consist of multiple parallel sets.

In most cases the values of R_P, R_{DA}, and C_{DA} are more important in high frequency (RF) applications. We will neglect them in most power supply applications and focus on C, ESR, and ESL.

"Bathtub" Impedance of 100µF Capacitors



Theory tells us that the impedance of a capacitor will decrease monotonically as frequency is increased. Practice tells us that at some frequency the ESR will dominate, and the impedance plot will flatten out. In fact, as we continue up in frequency, the impedance will start to rise. This is where the ESL starts to dominate. Where these "knee" points occur will vary with capacitor construction, dielectric, and value.

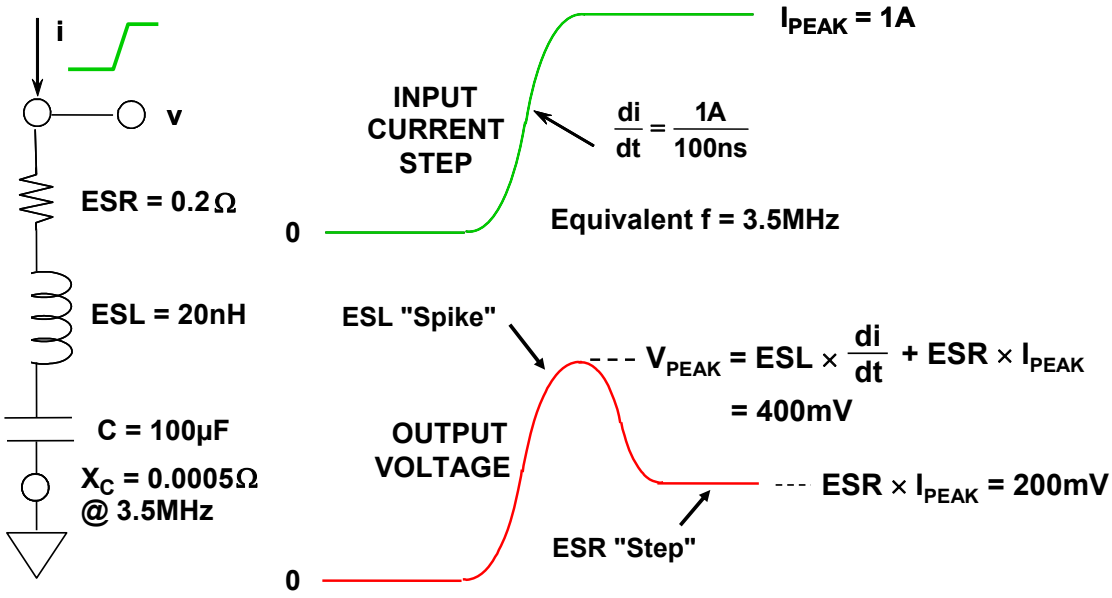
This is why we often see larger value capacitors paralleled with smaller values. The smaller value capacitor will typically have lower ESL and continue to "look" like a capacitor higher in frequency. This improves the overall performance of the parallel combination over a wider frequency range.

The self-resonant frequency of the capacitor is the frequency at which the reactance of the capacitor, $1/\omega C$, is equal to the reactance of the ESL, $\omega \times ESL$.

This figure compares the impedance of a 100 µF aluminum electrolytic capacitor with a 100 µF multi-layer ceramic capacitor (MLCC). Note that the ceramic capacitor has a much lower ESL and ESR than the aluminum electrolytic. Therefore the "dip" at the ceramic capacitor's self resonant frequency is much more pronounced than the dip in the aluminum electrolytic.

An ideal capacitor with ESR = 0 has an infinite "dip" at the self-resonant frequency as shown in the figure.

Response of a Capacitor to a Current Step



The complex impedance of a "real" capacitor will also cause non-ideal response to a current step. The assumption here is that we are stepping from a steady state current of 0 A to a steady state of 1 A. We also assume that the rise time of the current step is about 100 ns, which corresponds to a frequency of about 3.5 MHz. A "perfect" 100 µF capacitor has an impedance of 0.5 mΩ at 3.5 MHz.

We would expect to see the capacitor voltage start at zero (the voltage across an ideal capacitor cannot change instantaneously) and then slew at a rate equal to I_{PEAK}/C (which in this case works out to be 10,000 V/s, or 10 mV/µs). The ideal capacitor should have only a small voltage change during the 100 ns rise time of the current step. (Approximately 1 A × 0.0005 Ω = 500 µV).

The actual response of the non-ideal capacitor (ESR = 0.2 Ω, ESL = 20 µH) is shown in the figure.

The fast-rising edge of the current waveform shown results in an initial voltage peak across the capacitor, which is proportional to the ESL. The current through the inductor cannot change instantaneously. After the initial inductive transient, the voltage settles down to a longer duration level which is proportional to the ESR of the capacitor. Thus the ESL determines how effective a filter the capacitor is for the fastest components of the current signal, and the ESR is important for longer time frame components.

Note that an overall time frame of a few microseconds (or even less) is relevant here. As things turn out, this means switching frequencies in the 100 kHz to 1 MHz range. Unfortunately this happens to be the region where many switching supplies operate, and the ESR and ESL effects become critical.

Capacitor Data Sheet : What Do Specs Mean ?

Size code	SANYO Part number	Rated Voltage (V)	Rated Temperature (℃)	Rated Capacitance (μF)	D.F. (%max.)	L.C. (μA) max./5min.	E.S.R. (mΩmax.) 100kHz/20℃	Maximum allowable ripple current (mArms) 100kHz※1
	10TPB47M	10.0	105	47	8.0	47.0	70	1100
	10TPB33M	10.0	105	33	8.0	33.0	70	1100

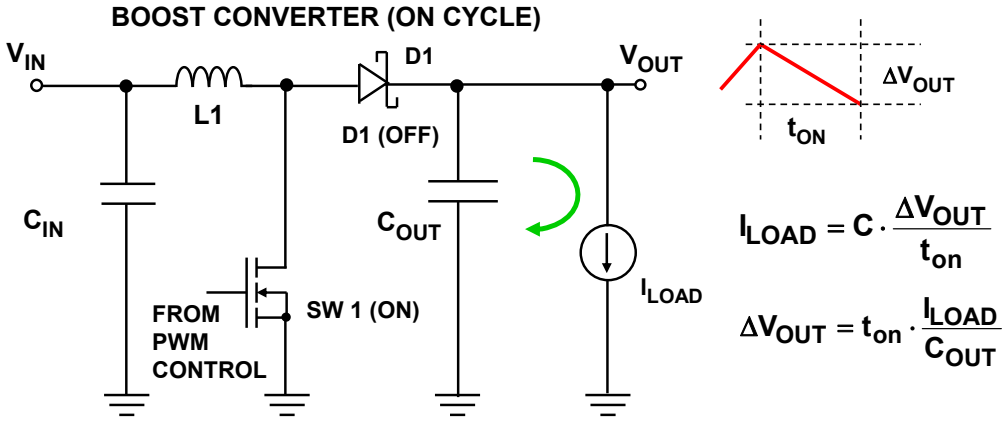
- *Rated Voltage*: Maximum voltage for which the capacitor is guaranteed to function. Often there is no guarantee of actual capacitance at this voltage.
- *Rated Temperature*: Maximum operating temperature. Temperature rise of capacitor based on ripple current should be included.
- *Rated Capacitance*: Usually specified to ±20% or ±30%. Note this is the capacitance at no dc bias and at low frequency. Always look at data sheet plots to check predicted capacitance at your design conditions (especially dc bias).
- *Dissipation Factor, DF*: This is a measure of the power loss of the capacitor expressed as a %. DF = $2\pi fRC \times 100\%$, where R = ESR, f = frequency (Hz)
- *Leakage Current, LC*: The amount of leakage current after a specified amount of continuous operation (5 to 10 minutes). Leakage current will cause the capacitor to discharge itself with no load attached.
- *Equivalent Series Resistance, ESR*: Includes conductor resistance, dielectric loss, and leakage. This is a very important specification, as it will affect load transient, ripple voltage at input and output, and maximum current capability.
- *Maximum Ripple Current*: The maximum allowed RMS current in a dc-to-dc converter application. The frequency is usually specified at 100kHz.

This figure defines the terms that you may find in a specification page for a capacitor.

Different value ranges of capacitors may have different specifications—the one shown is for a large value electrolytic. Small value capacitors may emphasize different specifications. Also you may find that capacitors targeted at different frequency applications may have ESR, etc., specified at frequencies other than 100 kHz.

We will now examine the functions of capacitors in switch mode power supplies.

Capacitors for Power Designs: Energy Storage



- **Energy stored in a capacitor increases as voltage is applied across it.**
- **It can provide energy quickly as required—acts as an energy reservoir.**
- **If load changes, capacitor will supply energy until loop can react. Larger capacitor will give better regulation.**
- **Larger output capacitor = less voltage ripple, neglecting ESR effects**

This figure shows how the C_{OUT} output capacitor acts as an energy storage device in a boost converter.

During the time SW1 is on and D1 is off, C_{OUT} must supply all of the current to the load. The voltage will "droop" at a rate equal to I_{LOAD}/C_{OUT} until the next charge cycle (SW1 off, D1 on) replenishes this charge.

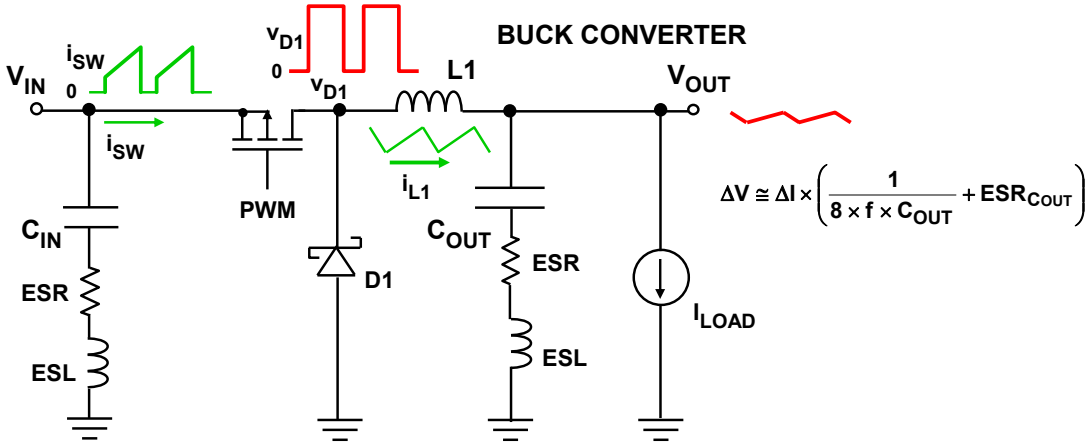
The choice of the value for C_{OUT} is a tradeoff—trying to balance capacitor (physical size), cost, and ripple current.

Since the output ripple of a boost converter current is high, C_{OUT} needs to be rated to handle the required ripple current. This generally means that the ESR will be low.

A good starting point for C_{OUT} size is to use the next standard value up from the value calculated from:

$$C_{OUT} = t_{ON} \frac{I_{LOAD}}{\Delta V_{OUT}}$$

Capacitors for Power Designs: Filtering



- **The LC filter at the output of the buck converter filters the square wave at the switch node, v_{D1}.**
- **The amount of voltage ripple seen at V_{OUT} is inversely proportional to the capacitor value and proportional to ESR.**
- **We can make C very large, so the ultimate limit is the ESR.**
- **The input filter capacitor will reduce the noise injected onto the V_{IN} line which can interfere with other parts of the system.**

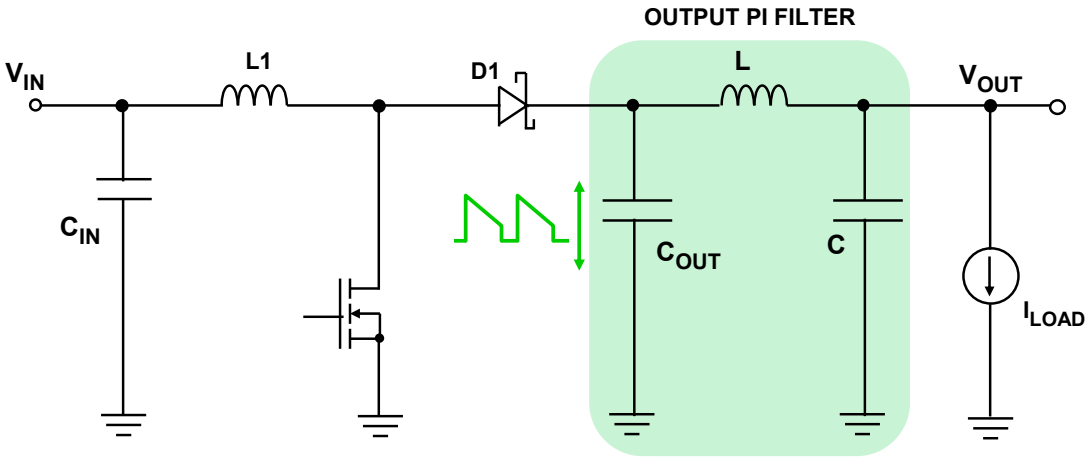
The second function of capacitors in switch mode power supplies is filtering. This shows how the C_{OUT} capacitor in a buck converter is used to reduce the output ripple voltage.

In this instance the inductor will smooth out the ripple, since the current in an inductor can't change instantaneously. While that may seem like a good thing, it should be remembered that low ripple and good transient response are mutually opposed to each other. Also the regulator is a closed loop negative feedback system, so the laws governing stability must be obeyed. The Bode plot of the system needs to be examined for adequate phase margin.

The input current of a buck converter is discontinuous, therefore the input filter capacitors must reduce the noise injected onto the V_{IN} line which can interfere with other parts of the system. The peak source impedance should be about three times lower than V_{IN}/I_{IN}.

This is generally achieved by keeping the input capacitor ESL small and C_{IN} large. Sometimes the C_{IN} ESR has to be decreased to lower the input impedance, or two capacitors in parallel are used for C_{IN}— one with small capacitance and low ESR/ESL and one with large capacitance and higher ESR/ESL.

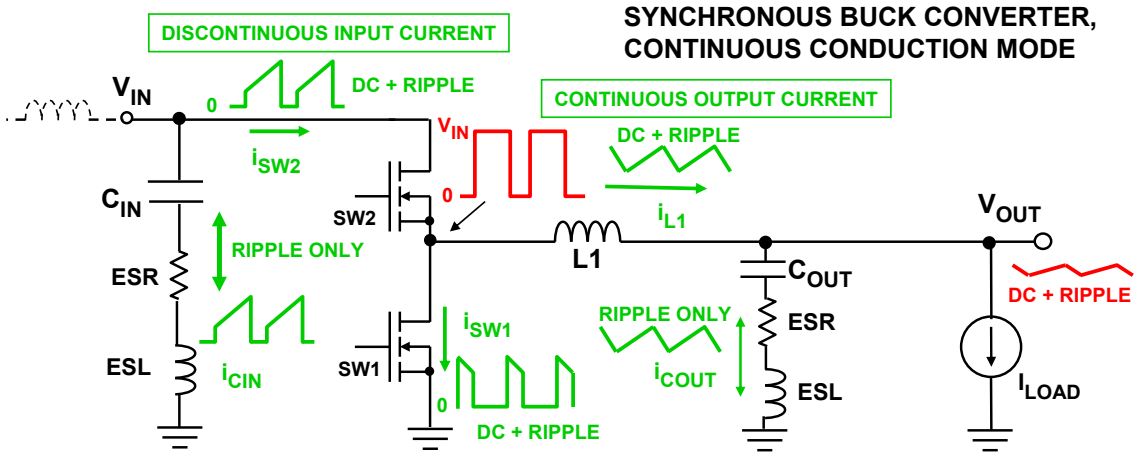
Boost Converter with Output Pi Filter



The boost converter has a discontinuous pulsed output current which is more difficult to filter than the buck converter output. Rather than try and reduce the ripple with a single output capacitor C_{OUT}, it is often more efficient to use an output pi filter as shown in shaded area of the figure. The output noise filter inductor, L, reduces output ripple voltage by attenuating the ac current passing through the output noise filter capacitor, C. The output inductor, L, is subjected to low ac voltage and very low ac current. It is generally safe to use an inexpensive drum core or "open field" type inductor in this application. The output noise filter capacitor, C, should have low ESL and ESR but does not handle much ac ripple current.

Be careful in applying pi output filters as they generally degrade output load transient response. If the filter is placed inside the feedback loop, compensation will be tricky. The pi filter can be equally effective when used on the output of a buck-boost converter.

Capacitor Functions in Buck Converter



- C_{IN} must handle high discontinuous ripple current. ESR, ESL should be low.
- C_{OUT} has continuous ripple current and must minimize output ripple voltage. ESR should be low.
- C_{OUT} affects loop stability and load step transient response.

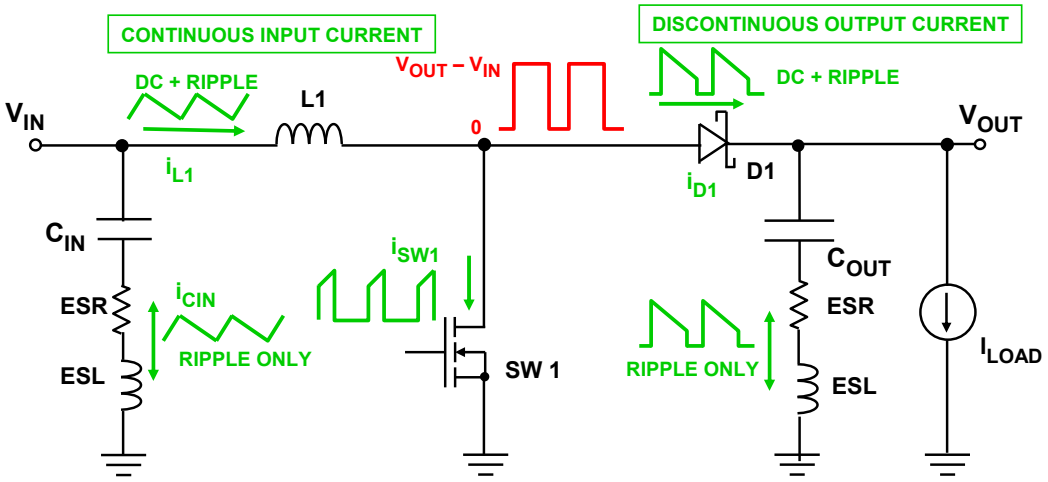
The input ripple current waveform of a buck converter is discontinuous with high di/dt and peak-to-peak amplitude. The input capacitor supplies pulse currents to the upper MOSFET. The input capacitor must therefore have high ripple current handling capability and low inductance. It is usually unwise to allow this input ripple current to be handled by other, uncontrolled bypass capacitors in the system. An inductor is sometimes placed in series with the input supply line capacitor to provide further filtering.

Output ripple current in a buck converter is continuous and usually low, so capacitor ripple current ratings are not usually an issue. However, buck regulators are commonly used to power loads such as processor cores and FPGAs which can impose severe dynamic load regulation requirements. When processor core output voltages approach 1 volt, the allowed error band is proportionately small (50 mV for 5% error), so a controlled low impedance over a broad frequency range is required.

The output capacitor is an integral part of closed loop stability of the buck converter. It smoothes the ripple current coming out of the converter, reducing the ripple voltage. The output capacitor supplies current during transient conditions until the feedback loop acts to increase the inductor current.

A good design tool, such as ADIsimPower, calculates the ripple current in the capacitors and inductors and makes the appropriate parts selection.

Capacitor Functions in a Boost Converter



- C_{IN} filters continuous ripple current and stabilizes feedback loop.
- C_{OUT} filters discontinuous output ripple current and must minimize output ripple voltage. ESR should be low.
- Pi-Filter on output often less costly than optimizing C_{OUT}.
- C_{OUT} affects loop stability and load step transient response.

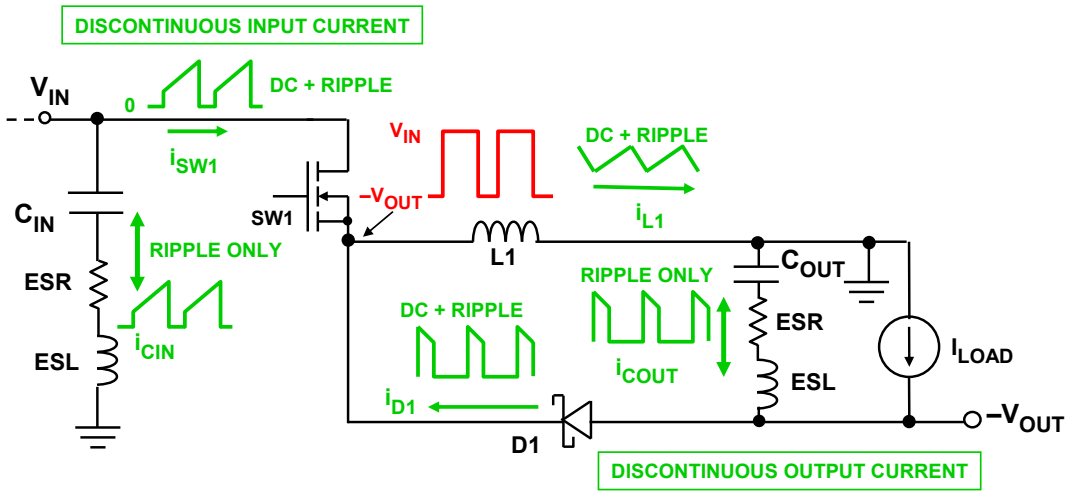
As previously discussed, the boost converter has continuous input current and discontinuous output current. The input capacitor smoothes the ripple current going into the converter, reducing the ripple voltage on the input. The input capacitor also provides low impedance on the input to ensure stability.

The output capacitor is an integral part of closed loop stability of the boost converter. It must supply the load current when the MOSFET is on and the diode is off.

Output capacitor also supplies current during load transient conditions until the feedback loop responds and increases the inductor current.

Depending upon the capacitor technology, an output filter that is designed to handle the high ripple current will tend to produce high output ripple voltage. An output filter that is designed to produce the desired ripple voltage is likely to be significantly larger and more expensive. So boost converters often use a pi filter in the output to more efficiently filter the output ripple voltage.

Capacitor Functions in Buck-Boost Regulators

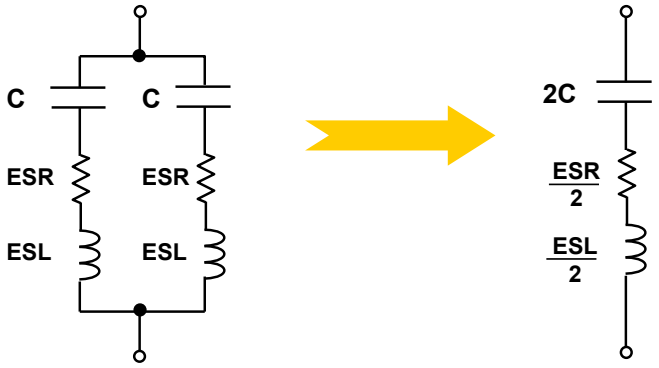


- **Large discontinuous input and output ripple current with high di/dt.**
- **Often requires a pi filter on the output to control ripple.**

In terms of input/output ripple current, the buck boost converter offers the worst of both worlds—large discontinuous ripple current with high di/dt on both the input and output, both must be handled by their respective filter capacitors.

Like the boost converter, the buck-boost converter is often used with a pi filter on the output, instead of the simple “L” section shown here.

Parallel Capacitors



- **Twice the capacitance, half the ESR, half the ESL**
- **Sometimes more cost effective than trying to do it with a single capacitor**
- **Sometimes the only way to get required C and ESR to meet ripple requirements**
- **May increase real estate, but depends highly on type of capacitor**
- **Bulk capacitors may be composed of several parallel capacitors, sometimes of different values**

Output capacitors are often used in parallel combinations of multiple individual capacitors. Parallel capacitors have a total capacitance equal to the sum of all their individual values.

An added benefit is that the effective ESR and ESL is reduced since the impedance of paralleled resistors goes according to the formula:

$$\frac{1}{Z_T} = \frac{1}{Z_1} + \frac{1}{Z_2} + \cdots + \frac{1}{Z_X}$$

In some cases parallel capacitors provide a more cost effective solution than trying to use a single capacitor. Sometimes parallel capacitors are the only way to get the required C and ESR to meet the ripple requirements.

It is a common practice to parallel different types and values of capacitors to take advantage of the low ESR and ESL of ceramic capacitors, while having the benefit of large capacitance values of aluminum or "bulk" capacitors. However, when you parallel different types of capacitors, you can't simply add the C value and parallel the ESR and ESL values. The resulting impedance must be calculated based on the complex impedance model.

Popular Capacitor Types

TECHNOLOGY	ADVANTAGES	DISADVANTAGES	APPLICATIONS
Aluminum Electrolytic (Switching Type)	•High CV product/cost •Large energy storage •Best for 100V to 400V	•Temperature related wearout •High ESR/size •High ESR @ low temp	•Consumer products •Large bulk storage
Solid Tantalum	•High CV product/size •Stable @ cold temp •No wearout	•Fire hazard with reverse voltage •Expensive •Only rated up to 50V	•Popular in military •Concern for tantalum raw material supply
Aluminum-Polymer, Special-Polymer, Poscap, OsCon	•Low ESR •Z stable over temp •Relatively small case	•Rapid degradation above 105°C •Relatively high cost	•Newest technology •CPU core regulators
Ceramic	•Lowest ESR, ESL •High ripple current •X7R good over wide temp	•CV product limited •Microphonics •C decreases with increasing voltage	•Excellent for HF decoupling •Good to 1GHz
Film (Polyester, Teflon, polypropylene, polystyrene, etc.	•Hi Q in large sizes •No wearout •High voltage	•CV product limited •Not popular in SMT •High cost	•High voltage, current •AC •Audio

This is a survey of some of the more popular capacitor types. Note that not all values are available in all types, and the physical size can vary widely for the same value of capacitance.

Aluminum Electrolytic Capacitors

- **Aluminum electrolytic capacitors provide large capacitance (100µF to > 1mF) in relatively small size at very low cost**
- **Represent the best µF/cost of all options**
- **Achieve this with high dielectric constant (ε) due to oxide film, and thin layers, (d is small)**
- **High ESR: can be several ohms**
- **Aging due to dry-out must be taken into account in long lifetime designs**
- **Surface mount available, but some reliability issues. Other technologies better for lower capacitance values**
- **Poor high frequency performance**
- **Use "switching" types, not "general purpose" in switcher designs**

Switching type aluminum electrolytic capacitor are designed and constructed for use in SMPS. They have lower ESR and ESL than general purpose aluminum capacitors, generally meaning higher ripple current. "General purpose" aluminum electrolytic capacitors should not be used in switcher designs.

Aluminum electrolytics are available in large values and in relatively small size and low cost. This is accomplished by using an oxide film with high dielectric constant and thin layers.

The chief disadvantage of aluminum electrolytics is the high ESR, which can be several ohms.

Because of their poor high frequency performance, they are often paralleled with other types of capacitors to achieve the desired filtering characteristic.

Solid Tantalum Capacitors

- **A type of solid electrolytic capacitor, using tantalum powder as dielectric**
- **Size efficient for 10's of µF range**
- **Capacitance is temperature stable**
- **ESR is in the range of 100's of mΩ, lower than aluminum electrolytics**
- **Must be designed for 2 × voltage rating**
- **Safety is a concern (e.g. reverse polarity, overvoltage rating): as failure is seen as burn out of capacitor with flame**
- **Popular in high-rel military applications**
- **However, becoming less popular, as ceramic capacitors can achieve same capacitance with lower ESR, and ESL, and less safety issues without cost penalty**

Solid tantalum capacitors have traditionally been popular in small hand held devices and in servers, but recent polymer and ceramic capacitor improvements have made tantalum less attractive.

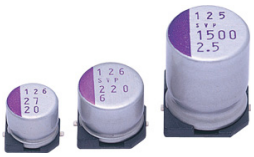
Raw material sourcing issues have also reduced tantalum's market share (increased price).

Extreme care must be taken with tantalum capacitors to avoid reverse voltage or overvoltage, as these conditions can cause the capacitor to burn out.

In spite of these concerns, tantalum capacitors are highly reliable and have been very popular in military applications. However, modern ceramic capacitors can achieve nearly the same capacitance with lower ESR and ESL and are replacing tantalums in many applications.

Only solid tantalum capacitors should be considered in modern applications. The "wet slug" type tantalum capacitors are not suitable in today's designs.

OS-CON (Sanyo)



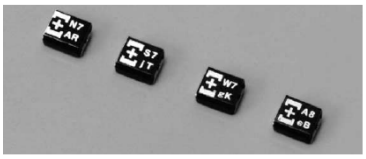
- Offers large capacitance and very low ESR in relatively small package with > 16V rating
- Useful for generating 100µF or more capacitance, and maintaining ESR of < 50 mΩ (5 mΩ available)
- Can handle 0.5 to 4A of RMS ripple current
- Suitable for high current designs requiring very low voltage ripple
- > 5000 hours at 105°C with capacitance remaining within ±20%, with some ESR increase
- Suitable for long lifetime products
- Lowest Height 4mm
  - Not suitable for portable designs
  - Used a great deal in servers, CPU voltage regulators
- Cost $0.50 to $1.00/100k piece price

OS-CON capacitors are attractive due to their reduced ESR and ESL. "OS-CON" is a trademark of Sanyo and stands for "organic semiconductor."

OS-CON is an aluminum solid capacitor with high conductive polymer or organic semiconductor electrolyte material. OS-CON achieves low Equivalent Series Resistance (ESR), excellent noise reduction capability and frequency characteristics. In addition, OS-CON has a long life span, and its ESR has little change even at low temperatures since the electrolyte is solid.

Other companies such as United Chemi-con have come out with similar products based on an aluminum polymer technology that may have slightly lower lifetime but are more cost effective for the same capacitance and similar ESR.

POSCAP (Polymer Organic Semiconductor Capacitor)



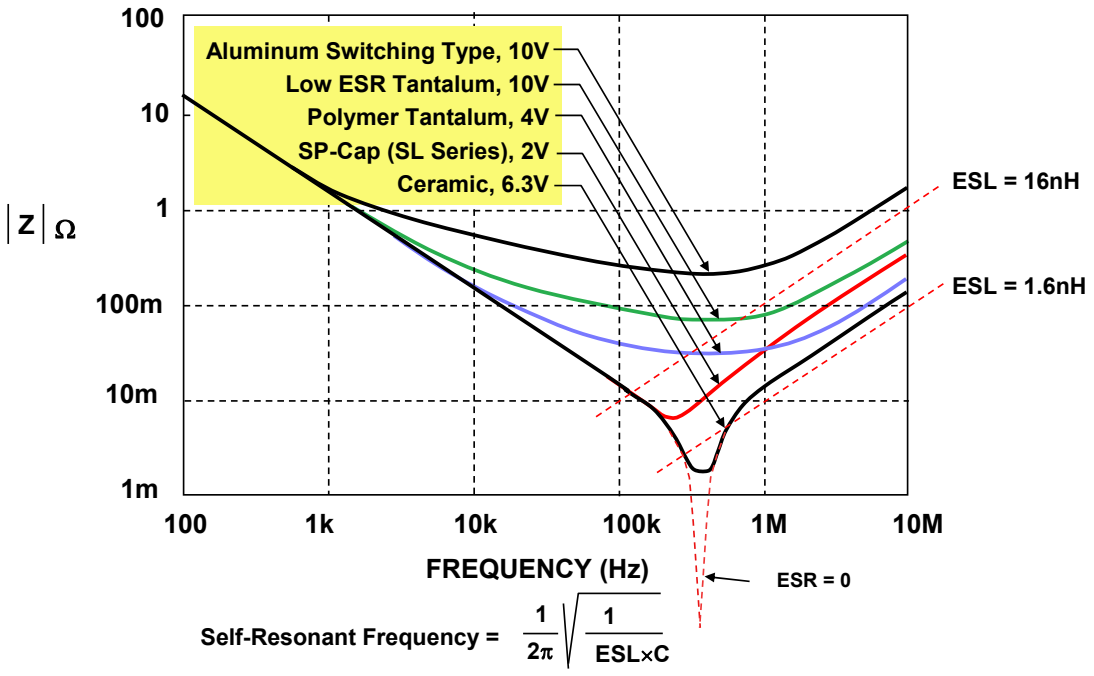
- **Solid electrolytic capacitor with Sanyo-specific organic compound**
- **Offers reasonably low ESR (50mΩ down to 5mΩ)**
- **Small Size and Height**
- **Values up to 1000µF available**
- **Generally low voltage (up up to 25V but limited capacitance)**
- **Cost 47µF, 6.3V: $0.40 to $1.50 at 100k piece price**
  - **Less expensive than similar specified ceramic**
  - **More expensive than similar standard electrolytic or tantalum**

This capacitor type is similar to the OS-CON and also made by Sanyo.

"POSCAP" is a solid electrolytic chip capacitor. The anode is sintered tantalum, and the cathode is a highly conductive polymer. "POSCAP" has a low ESR and excellent performance at high frequency with a low profile and high capacitance. In addition, it has high reliability and high heat resistance.

Panasonic also has a “Special Polymer” cap that has similar specifications in the same footprint as the "POSCAP." The cost is also comparable for similar values.

Impedance of Various 100µF Capacitors

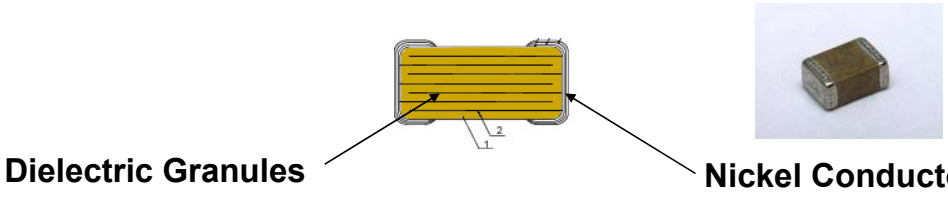


This is a graph adapted from Panasonic's "S-P Capacitor Technical Guide" showcasing their “Special Polymer” capacitor technology. It may cast a slightly unfavorable light on their competitor’s product (namely Polymer Tantalum) but it shows the general trend of various capacitor types.

General purpose aluminum electrolytics have slightly higher ESR than the switching type. However, they are not recommended for switching supply applications.

As you can see here, the ceramic capacitor has the lowest ESR at the switching frequency and the lowest ESL.

Ceramic Capacitors



- **Multilayer ceramic capacitors (MLCC) offer extremely low ESR (<10mΩ) and ESL (<1nH) in a small thin package**
- **"0603" is 1.6mm (l) × 0.8mm (w) × 0.8mm (h)**
- **Best cost for performance from 1pF to 40µF**
  - **Most suitable capacitor for portable power, decoupling supplies**
  - **Available up to 100µF, but become larger and more expensive above 10µF**
  - **Cost is dependent on value, with lower values being cheaper due to less layers being printed. More popular values cheaper.**
  - **1µF 16V, 0603 is < $0.01 in 100k pieces**
- **Resilient to fault conditions – voltage surges etc.**
- **Capacitance value decreases with increasing voltage (stick with X7R types for best results)**

Due to low ESR, ceramic capacitors can handle very high ripple currents for their size. They are exclusively used in compensation and small signal circuits, and are very good for reducing ripple voltage on the input and output of switching supplies. Their ESL is also low, making them good choices at high frequencies.

Due to their limitation in upper capacitance value, they are often paralleled with other capacitor types on the input and output of switching supplies.

The ESL of a standard multilayer ceramic capacitor in an 0603 case is approximately 1 nH.

Other more expensive ceramic technologies are available which can reduce the ESL to less than 100 pH.

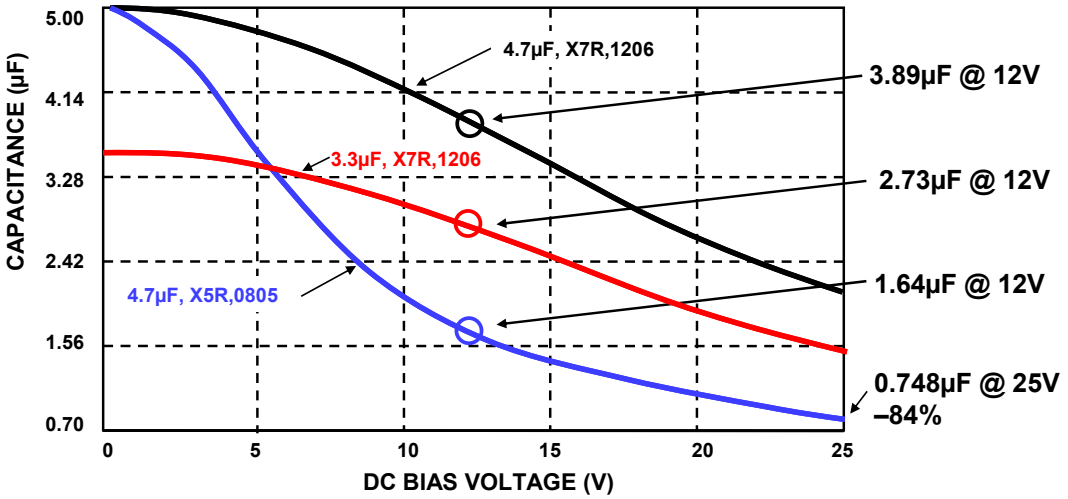
One type is the low inductance chip capacitor (LICC) which has a reverse-geometry where the terminations are located on the long sides rather than the short sides of the rectangular package.

Other low inductance types are the inter-digitated capacitors (IDC), land grid array (LGA) capacitors, and low-inductance capacitor arrays (LICA).

Details of these low inductance capacitors can be found at the AVX website, www.avxcorp.com, and in the following reference:

Tim Sullivan, "Choosing Decoupling Capacitors," *Electronic Products*, December 2007, available at www.electronicproducts.com/ShowPage.asp?FileName=farr_avx_dec2007.html.

Which Ceramic Capacitor Provides More Capacitance?



- **Generally more temperature stable parts (X7R) have less variation due to applied voltage**

A potential problem with ceramic capacitors is their capacitance change with dc bias voltage. This may or may not be a problem in decoupling applications, but it can be a real issue if the capacitor is used in a critical compensation network, for example. Another place where the voltage coefficient is a problem is where the capacitor is used in the signal path, and the signal modulates the voltage. This can produce unwanted harmonics because of the signal-dependent capacitance.

These plots show capacitance versus applied dc bias voltage for three types of ceramic capacitors:

4.7 µF, 25V, X7R, 1206 case style

4.7 µF, 25 V, X5R, 0805 case style (higher K, smaller case)

3.3 µF, 25 V, X7R, 1206 case style

It is interesting that the 3.3 µF (at zero bias) X7R capacitor actually has a larger capacitance at 12 V bias than the 4.7 µF X5R type. At full rated voltage, the X5R capacitor is down 84% from its zero bias value.

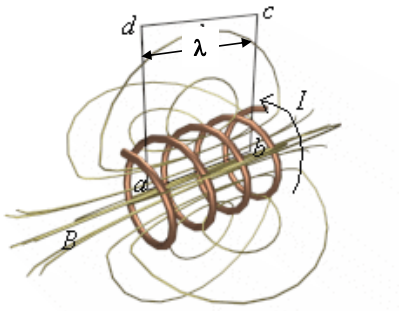
Note that the X7R capacitors (which have a slightly lower dielectric constant) maintain their capacitance better with dc bias voltage than the X5R type.

In addition, the X7R types perform better over temperature and should be used in preference to the X5R.

Avoid using Z5U and Y5V types which are worse.

Inductor Basics

- **An inductor is a magnetic energy storage element which consists of a conducting coil surrounding a core, usually made of ferrite material or powdered iron**



- **Air: μ = 1.257x10^{-6} H/m**
- **Ferrite U M33: μ = 9.42x10^{-4} H/m**
- **Nickel: μ = 7.54x10^{-4} H/m**
- **Iron: μ = 6.28x10^{-3} H/m**
- **Ferrite T38: μ = 1.26x10^{-2} H/m**
- **Silicon GO steel: μ = 5.03x10^{-2} H/m**
- **Supermalloy: μ = 1.26 H/m**

$$\mathbf{L(Henries) = \frac{\mu \cdot n^2 \cdot A}{\lambda}}$$

μ = permeability of core,
n = number of turns,
A = cross-sectional area of core,
λ = effective length of core

- **Larger core cross-sectional area, coil turns and/or core permeability increase inductance**

The practical inductor consists of a conductor coil wound on a ferromagnetic core. This combination yields an inductance (L) that offers a reluctance to a change in current, and therefore the current through an inductor cannot change instantaneously.

The rate of change of current through an inductor (di/dt) is determined by the inductance and the voltage dropped across the inductor, given by the expression:

$$v = L \times di/dt.$$

The use of ferromagnetic material as the inductor core allows energy to be stored in the inductor. When a positive voltage is applied to the inductor, the current increases, and energy is added to the inductor magnetic field.

The inductive impedance can be calculated from:

$$Z_L = j\omega L$$

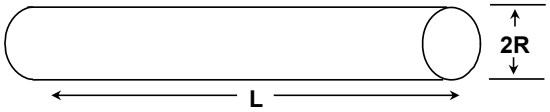
where:

$$j = \sqrt{(-1)}$$

and

$$\omega = \text{radian frequency} = 2\pi \times \text{frequency in Hertz}$$

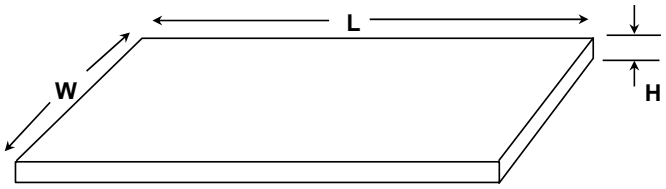
Wire and Strip Inductance Calculations



L, R in mm

$$\text{WIRE INDUCTANCE} = 0.0002L\left[\ln\left(\frac{2L}{R}\right) - 0.75\right]\ \mu H$$

EXAMPLE: 1cm of 0.5mm o.d. wire has an inductance of 7.26nH
(2R = 0.5mm, L = 1cm)



$$\text{STRIP INDUCTANCE} = 0.0002L\left[\ln\left(\frac{2L}{W+H}\right) + 0.2235\left(\frac{W+H}{L}\right) + 0.5\right]\ \mu H$$

EXAMPLE: 1cm of 0.25 mm PC track has an inductance of 9.59 nH
(H = 0.038mm, W = 0.25mm, L = 1cm)

A piece of wire or a PCB trace will have inductance, even though it is not a coil.

In addition to the resistance (basically a dc spec), a trace (wire or ground plane) will have a frequency dependent impedance component (known as inductance).

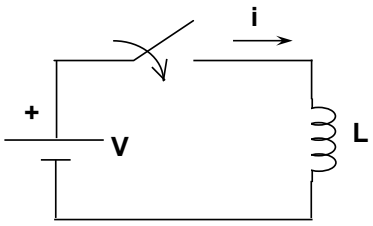
Inductive impedance increases linearly with frequency. This can become significant at higher frequencies.

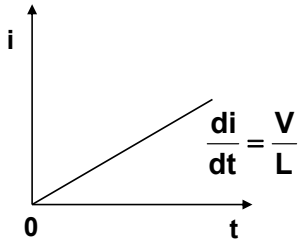
The above figure shows simple equations to calculate the inductance of a length of wire or a rectangular strip conductor. The assumption is that the return current path is a fairly long distance away from the wire or strip—the wire or strip is treated as a circuit element.

However, on a PCB the actual inductance also depends on the loop area which includes the current return path, and the above equations are no longer valid. There are modeling packages available to determine the actual trace impedance in these cases.

For example, the effective inductance of a gate drive trace may be as much as a factor of 10 lower than predicted by the above equation if it runs directly over a ground plane.

Inductor Basic Current/Voltage Relationship





$$E(\text{joules}) = \frac{1}{2} \cdot L \cdot i^2$$

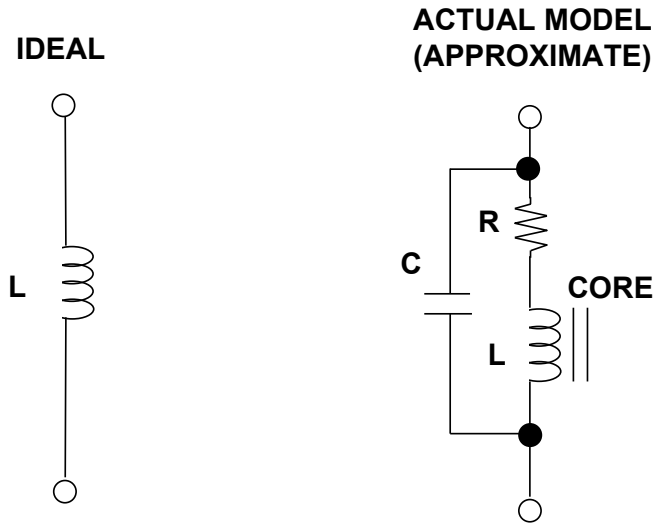
- **Inductor current increases at rate of V/L**
- **If inductor current tries to change rapidly (switch opened), a large voltage will be generated as the magnetic field collapses**
- **Energy stored is proportional to the inductance and the square of the current.**

You cannot change the current through an inductor instantaneously. When a voltage is applied to the inductor, the current increases, and energy is added to the inductor magnetic field. When the switch is opened, the inductor current goes to zero, and a large voltage is generated as the magnetic field collapses.

The inductor magnetic field can only hold a finite amount of energy before the ferromagnetic material will saturate. Saturation causes the inductance to decrease and ripple current to increase in a switching supply. When making an inductor selection, it is important to check that the core saturation current (I_{SAT}) is greater than the application's peak inductor current,

$$(I_{PEAK} = I_{OUT} + I_{RIPPLE}/2).$$

Inductor Model



Just as with the capacitor, a real inductor will have a more complex model.

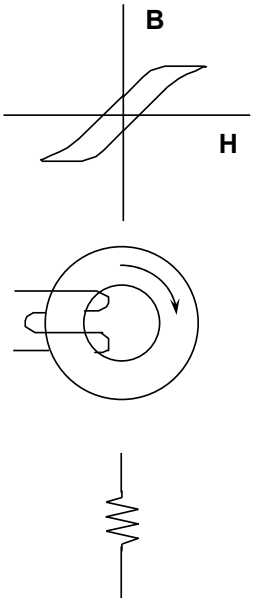
The inductor will have series resistance (called DCR for dc resistance) just as in a capacitor. There is also a small amount of parallel parasitic capacitance which can be relevant in RF applications.

Another consideration is the inductor self-resonant frequency. A practical example would be an inductor of 10 µH which has an equivalent distributed capacitance of 5 pF. The self-resonant frequency can be calculated as follows:

$$f_{resonance} = \frac{1}{2\pi}\sqrt{\frac{1}{LC}} \qquad = 22.5 \text{ MHz}$$

The switching frequency of the regulator should be at least ten times less than the inductor self-resonant frequency. In most practical designs with switching frequencies less than 2 MHz this will be the case, but a quick calculation is a good idea.

Inductor Power Losses



LOSS	FUNCTION OF
Magnetic Hysteresis	◆ Core Material ◆ Core Volume ◆ Flux Density ◆ Frequency
Eddy Currents	◆ Core Material ◆ Core Volume ◆ Flux Density ◆ Frequency
Winding Resistance	◆ Wire Size ◆ Number of Turns ◆ Core Volume

◆ Figure of Merit: "Q" = $\frac{2\pi fL}{R}$

Another important consideration is that the temperature of the inductor will rise due to internal power losses. The designer needs to consider winding resistance loss (sometimes referred to a copper loss) and core losses from eddy currents (often referred to a core loss).

Winding resistance power loss is due to the effective current (I_{RMS}) flowing through the resistance (R_{DC}) of the conductor winding, simply expressed as:

$$P_{CU} = R_{DC} \times I_{RMS}^2.$$

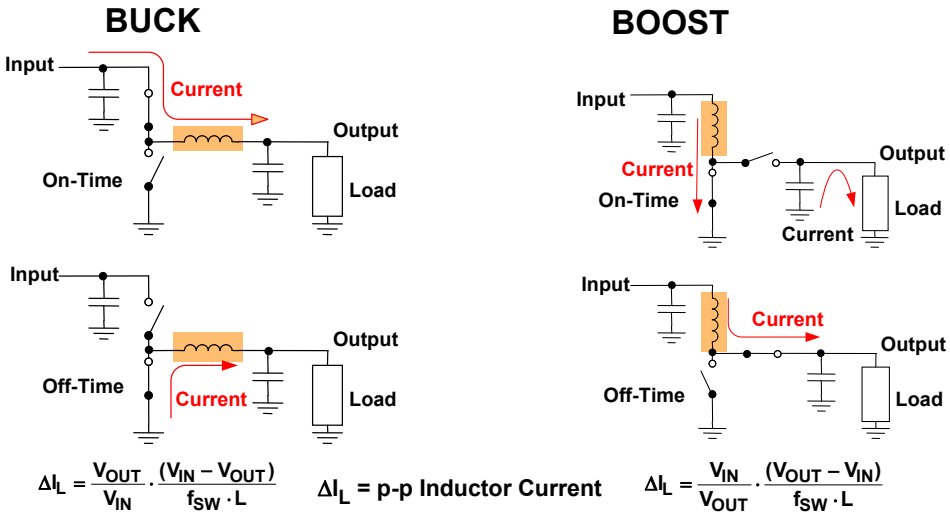
Inductor data sheets typically specify a temperature rise at a given current—for example, the equivalent dc current yielding a 40°C temperature rise. The lower value of the temperature rise and saturation current is called the "rated" current of the inductor.

The mechanism of core loss is more complex. Recall that current flowing through an inductor winding induces a magnetic flux in the ferromagnetic material, or the core. So the changing current in the power inductor generates a changing flux density (B_{AC}) and the reluctance of the core material tends to oppose this B_{AC}.

Just like the current flowing through the conductor results in copper losses due to the conductor's resistance to the flow of current, the core's reluctance to a changing flux generates a core loss. The core loss is determined by the type of core material, the amount of material, the B_{AC}, and the frequency of change, that is, the switching frequency (F). A good power inductor data sheet will simplify this equation based on a calculated B_{AC} for the operating condition of the inductor and the core material and size.

While the data sheet may specify a temperature rise current, it is important to note that where the core losses are significant, the inductor will reach the specified temperature rise at lower rms current because of the additional temperature rise caused by the core loss.

Inductor Functions in Switching Converters



$\Delta I_L = \frac{V_{OUT}}{V_{IN}} \cdot \frac{(V_{IN} - V_{OUT})}{f_{SW} \cdot L}$ ΔI_L = p-p Inductor Current $\Delta I_L = \frac{V_{IN}}{V_{OUT}} \cdot \frac{(V_{OUT} - V_{IN})}{f_{SW} \cdot L}$

- Increasing f_{SW}, reduces ripple current for same V_{IN}/V_{OUT} conditions
- Higher f_{SW} = smaller value inductor = smaller physical inductor, and lower DCR
- However switching losses degrade efficiency at higher frequency
- Use $\Delta I \approx 0.3\ I_{DC}$ (Buck I_{load}, Boost I_{in}) as starting point for inductance value
- Choosing L is a size/efficiency tradeoff

The primary function of an inductor in a switch mode power supply is to act as an energy storage device. Another function of the inductor is to act as a filter—either on the input or output or both.

This figure reviews the basic operation of a buck and boost converter and how the inductor acts to step down (buck) or step up (boost) the input voltage.

The calculation of the required inductor value begins by determining the maximum peak-to-peak ripple current, ΔI_L. This value is typically chosen to be about 30% of the output dc load current for a buck converter, and 30% of the input dc current for a boost converter.

The inductor value itself can then be found by solving the above equations for L, given the value of ΔI_L, V_{IN}, V_{OUT}, and f_{SW}.

Note that increasing the switching frequency reduces the value of the inductor required for the same ripple current.

The ADIsimPower design tool calculates the proper value for the inductor based on the customer requirements as well as determines the exact part and manufacturer for use in the bill of materials.

The ADIsimPower vendor database contains over 4000 individual parts. The inductor core loss data has been included in the inductor model and is not generally published by the manufacturer.

Inductor Specifications

Part number	L[1] (µH)	Percent tol	DCR[2] max (Ohms)	SRF[3] typ (MHz)	Isat[4] (A)	Irms[5] (A)
DO3316P-682_L_	6.8	20,10	0.027	38	4.6	4.4
DO3316P-103_L_	10	20,10 20	0.038	30	3.8	3.9

1. **Inductances may vary 20 to 30% from the nominal inductor value! Current ripple could be increased 43%. Coilcraft offers 10% and 20% tolerance.**
2. **DCR: DC resistance. Physically smaller inductors (for same L) will have larger DCR due to reduced wire thickness and increased efficiency losses.**
3. **SRF: Resonant frequency of inductor and parasitic capacitance of inductor—typically not a concern for design.**
4. **Isat: Inductor current level for which the inductance falls 10% using coilcraft, for others it is –30%! You don't want to operate at –30% (–10% is OK)**
5. **Irms (Also called Imax): At this RMS current level the temperature of the inductor will rise 40°C. Inductors are usually rated to 125°C. Typically you don't want to have inductor rising much more than 40°C, because saturation current level is further decreased.**

This figure shows specifications for a particular inductor taken from the manufacturer's data sheet (in this case, Coilcraft).

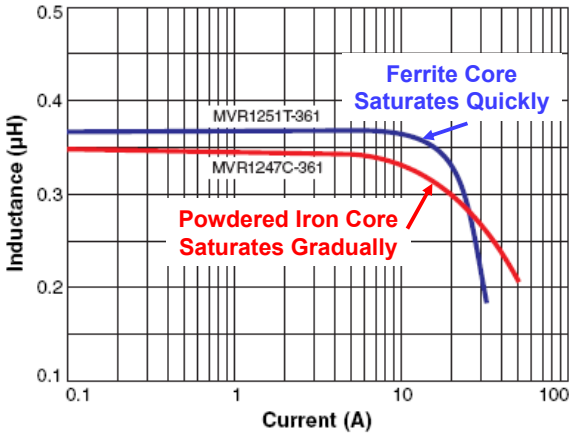
The inductance value can vary 20% to 30% from the nominal value, however, Coilcraft offers 10% and 20% tolerances. Since inductor ripple current is inversely proportional to L, inductances less than nominal will cause an increase in ripple current.

Another important specification is the saturation current, Isat, which is the inductor current level for which the inductance falls 10% (Coilcraft inductors). For other manufacturers, it is –30%.

Operation at 10% saturation is acceptable provided it represents the maximum load and worst case conditions. Knowing this is valuable in selecting the right inductor value. Inductors which are larger than necessary take up more real estate and are more expensive.

The specification Irms (or Imax) is the rms current level at which the temperature of the inductor will rise 40°C. The maximum allowable temperature is usually 125°C. If you allow the inductor temperature to rise more than 40°C the saturation current level will probably be further decreased.

Inductor Cores and Their Characteristics



- **Natural air gaps in powdered iron core cause a more gradual saturation curve for same physical size.**
- **Powdered iron cores suited to applications requiring large instantaneous current (i.e., camera flash, VRM power supplies).**
- **Powdered iron cores more expensive and have higher core losses.**

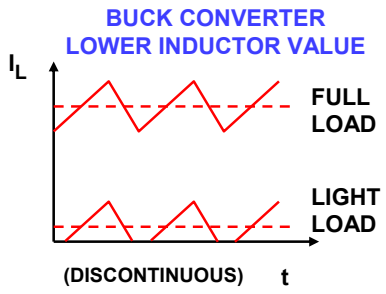
There are two basic types of cores commonly used for inductors: powdered iron and solid ferrite.

The powdered iron core has natural air gaps which cause a more gradual saturation curve for the same physical size (compared to solid ferrite cores). Because of the gradual saturation, powdered iron cores are more suited to applications requiring large instantaneous currents such as camera flash and VRM power supplies.

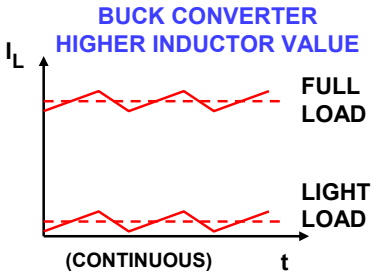
Ferrite core inductors saturate quickly but are lower cost and have lower core losses. They are therefore more suited for standard POL switching supplies.

Inductor Selection Considerations

- **Benefits of low value inductors**
  - Lower DCR
  - Higher saturation current
  - Higher di/dt
  - Faster switching frequencies
  - Improved transient response
  - Less output capacitance required for given transient performance



- **Benefits of high value inductors**
  - Lower ripple current
  - Lower AC loss (skin effect, hysteresis)
  - Lower RMS current in switches
  - Lower RMS capacitor current (mainly output)
  - Continuous inductor current over wider load range
  - Less capacitance required for an equivalent output ripple

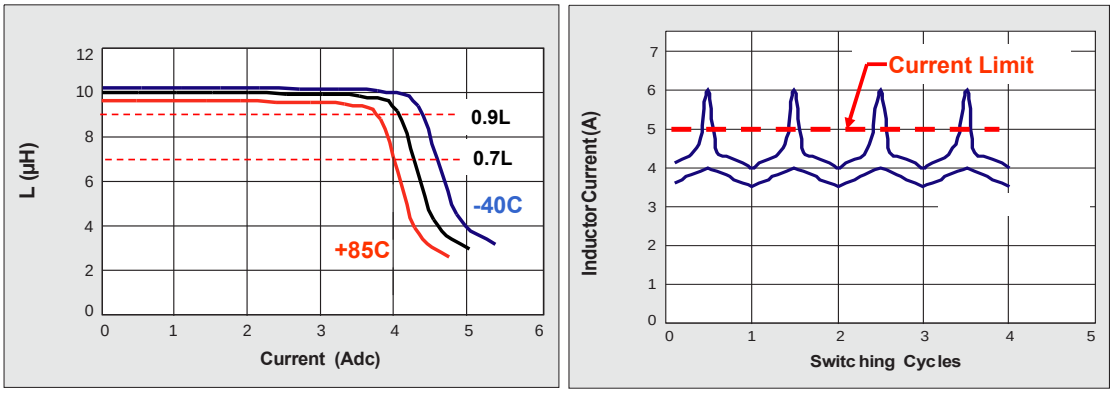


This figure examines the tradeoffs between low and high value inductors. The ultimate choice depends on the particular design.

The ADIsimPower design tool strives to achieve the desired performance with the lowest practical inductor. This philosophy is the proper one for most modern portable systems.

On the other hand, higher value inductors do have certain advantages as shown in the figure. Under certain conditions they may be the desirable choice.

Saturation of Inductors



- **The inductor core can become biased with too much current resulting in a sudden drop in inductance.**
- **Operating with I_{DC} + ΔI / 2 equal to a current I_{SAT} which causes a 30% drop in L will cause issues:**
  - **Ripple current increase > 40%**
  - **May hit current limit for lower DC current than desired**
  - **Core saturation results in core efficiency loss**
  - **Greater di / dt results in increased EMI leakage**
- **Over designing will result in physically large inductors**
  - **10% saturation for peak current at maximum load and worst case conditions is a reasonable compromise. For the above example, this would be about 4A.**
  - **Check Inductor saturation curves vs. temperature—Don't just read spec!**

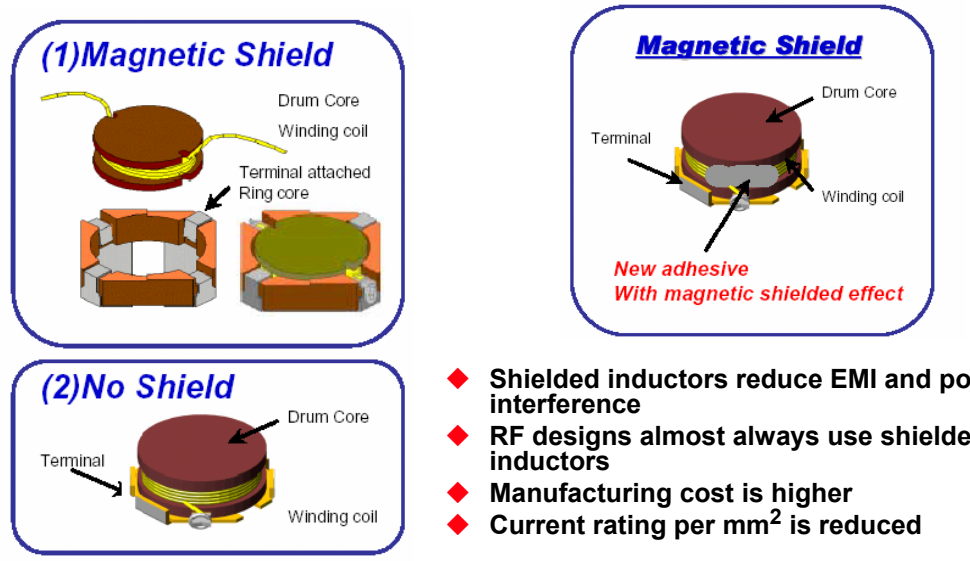
This figure shows what happens to the inductor ripple current when the saturation current (Isat) is exceeded. Exceeding the saturation current causes a sudden drop in inductance and a corresponding rise in the inductor current.

The saturation current (Isat) is the current at which the inductance drops by a maximum of 10% below the lower limit of its value specified at 0 A dc bias. This is the definition Coilcraft uses. Other manufactures use different percentages.

The inductance at Isat is measured at the specified ambient temperature by applying dc bias for a short period of time to minimize self-heating.

Selecting the inductor such that it will reach 10% saturation for peak current at maximum load and worst case conditions is a good compromise. For the example shown in the figure, this would be about 4 A.

Shielded or Unshielded?



- Shielded inductors reduce EMI and potential interference
- RF designs almost always use shielded inductors
- Manufacturing cost is higher
- Current rating per mm^2 is reduced

Model	L, µH	DCR, Ω	SRF, MHz	ISAT, A	IRMS, A	Shielded	Size, mm	Price, $ 1k
DO5022P-103ML	10	0.031	30	10	4.3	No	18 x 15	0.73
DS5022P-103ML_	10	0.04	30	8	3.9	Yes	18 x 15	1.11

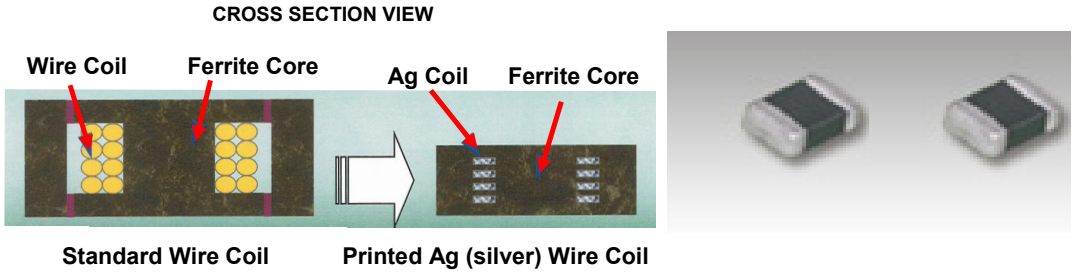
To shield or not to shield, that is the question.

Shielding will reduce EMI. Although the cost will increase slightly, as is shown in the figure. Shielding will tend to lower the saturation current, which in turn lowers the maximum allowable rms current.

Shielded inductors are very common in RF applications.

The above figure compares two similar inductors from Coilcraft. Both are the same size and value, but the shielded version has slightly lower Isat and Irms currents.

New Inductor Technology: Multilayer Ceramic Inductors for Power



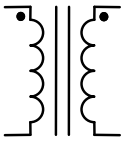
- **Characteristics of Ceramic Inductors**
  - **Low cost (about 50% to 65% of coil types with similar specifications)**
  - **Small size (2.5mm x 2.0mm x 1mm(h), 1.5µH, I_{SAT} = 1.5A)**
  - **Lower DCR improves efficiency**
  - **Useful < 2.2µH (drives IC manufacturers to higher switching frequencies)**
  - **Imax = 1.5A due to small printed Ag (silver) wire coils**
  - **Usable to about 1.0A due to saturation**
- **Manufacturers: FDK, Murata, TDK, Toko (in development)**

Multilayer ceramic inductors lower cost, smaller size, lower DCR than standard wire coil inductors. The only disadvantage is that the saturation current is typically limited to about 1.5 A because of the small printed silver wire coils.

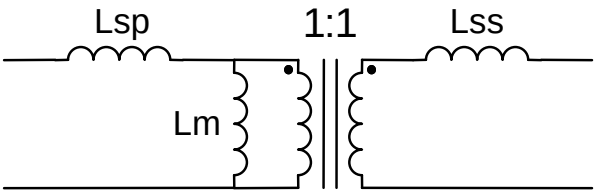
The upper range of inductance is limited to a few microhenries.

Coupled inductors

- **A coupled inductor is an inductor with multiple windings on the same core**
- **Coupled inductors are basically transformers with poor coupling and low magnetizing inductance**
- **A flyback transformer could be considered a coupled inductor with good coupling**



Ideal Transformer



Coupled Inductor Model

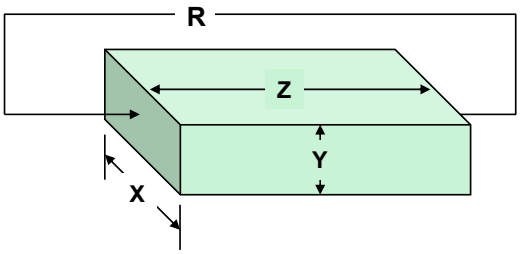
A coupled inductor is an inductor with multiple windings on the same core. It is similar to a transformer but has more losses and a more complex model. It can be viewed as a transformer with poor coupling and low magnetizing inductance.

This figure shows the relationship between the ideal transformer and a coupled inductor. The 1:1 transformer in the model is an ideal transformer (all it does is offer isolation)

The coupled inductor is more complex, since no simplifications can be made to the circuit model. Coupled inductors generally have a 1:1 turns ratio, so Lsp = Lss.

Often Lm is of the same order of magnitude as Lsp and Lss.

Calculation of Sheet Resistance and Linear Resistance



$$R = \frac{\rho Z}{XY}$$

ρ = RESISTIVITY

SHEET RESISTANCE CALCULATION FOR 1 OZ. COPPER CONDUCTOR:

$\rho = 1.724 \times 10^{-6}\ \Omega$ cm, Y = 0.0036cm

$$R = 0.491\frac{Z}{X}\ m\Omega$$

$\frac{Z}{X}$ = NUMBER OF SQUARES

R = SHEET RESISTANCE OF 1 SQUARE (Z = X)
= 0.491mΩ/SQUARE

We will now examine the resistor, another passive component.

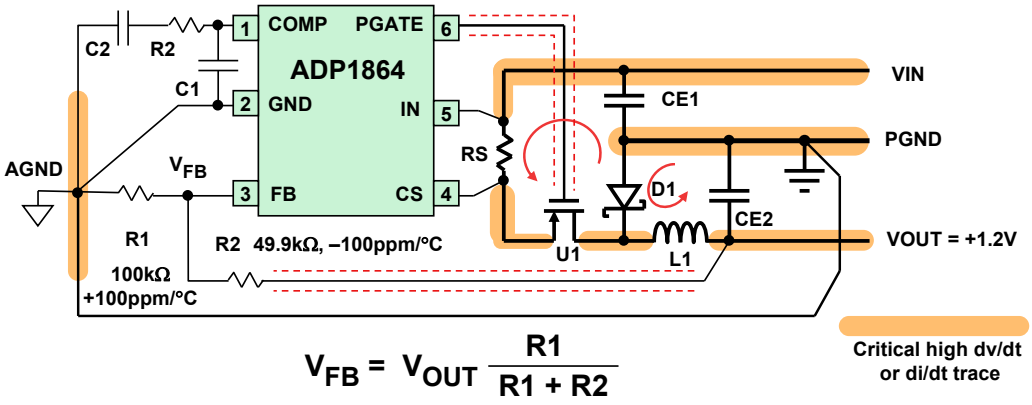
All conductors have some resistance (at least when operating above 0°K).

Using large area ground planes decreases the resistance, but cannot eliminate it. And from ohm's law we know that a current flowing through a resistance will cause a voltage drop across the resistance.

The resistance of a trace (or a ground plane) can be calculated by taking the resistivity of the material, which will typically be given in a resistance per unit volume (squares) of the conductor material, and multiplying by the number of the squares.

In the above example, the sheet resistance of 1 oz. copper, which is a typical PC board material, is calculated as 0.491 mΩ/square.

Mismatched Resistor TCs Can Induce Temperature-related Gain Errors



$$V_{FB} = V_{OUT} \frac{R1}{R1 + R2}$$

- R1/R2 divider sets output voltage (internal reference is 0.8V)
- Assume TC of R1 is +100ppm/°C and TC of R2 is –100ppm/°C
- Temperature change of 100°C causes gain error of +0.66%
- This translates into an error of +8mV at the buck output
- Avoid further mismatch errors by keeping R1 and R2 away from heat generating components such as D1 and L1
- 1% surface mount chip resistors available in TCs to 25ppm/°C

As we have seen, processors with lower core voltages, such as FPGAs, are placing tighter tolerances on power supply voltages. The accuracy of the feedback network in this circuit must be considered as part of the overall error budget in the final output voltage. The following example illustrates the point.

For nominal resistor values R1 = 100kΩ, R2 = 49.9kΩ, gain = 0.6666666

Assume that R1 and R2 have temperature coefficients of +100 ppm/°C and –100 ppm/°C, respectively.

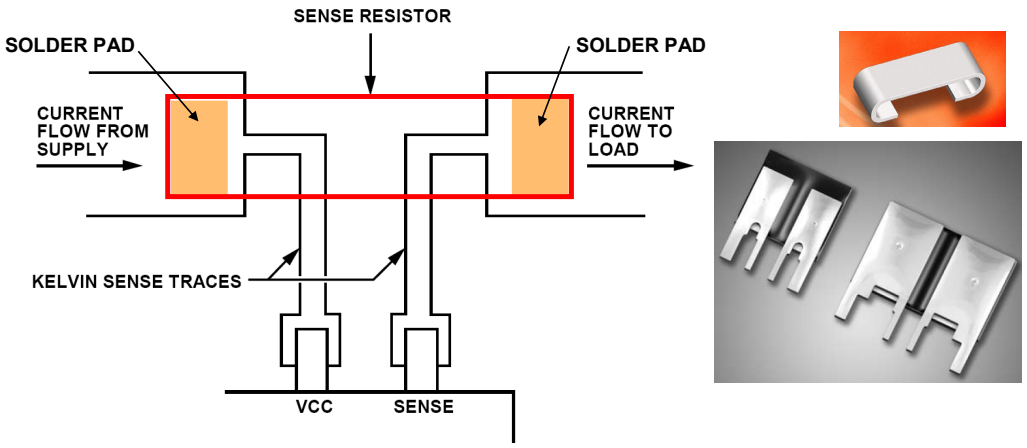
For a 100°C temperature change, R1 goes from 100 kΩ to 101 kΩ, and R2 goes from 49.9 kΩ to 49.4 kΩ. The new gain is 0.671096, which is 0.66% higher than the nominal gain. This becomes part of the overall error budget which must also include the initial resistor ratio accuracy, line/load regulation, reference accuracy, transient response, etc. Although 0.66% may seem small, the overall error budget may be less than 5% for FPGA applications.

The use of 1% surface mount chip resistors for the gain setting resistors is recommended (such as Vishay CRCW-series). TCs are available as low as 25 ppm/°C if required.

In the above diagram the red dotted line around the gate drive and feedback trace note that it should be protected from interference for external signals.

Details of layout requirements regarding switching supplies follow later in this section.

Current Sense Resistors Require Kelvin Sensing



- **If using a two pin/pad sense resistor, layout is critical to accuracy**
- **Kelvin sense tracks should be used at equal locations on each pad to optimize voltage drop measurement**
- **It is also advisable not to place the sense resistor too close to heat sources such as the MOSFET or catch diode in order to minimize temperature rise**

If the current sense resistance value is low, the lead resistance may be a significant source of error. To compensate for this error it is common to use "Kelvin" (4-wire) connections, where the current flows through one pair of leads and the voltage across the resistor is sensed with a second set in which no significant current will flow. No current means no voltage drop. Such devices are, of course, more complex and so more expensive.

This figure shows how careful board layout can often make them unnecessary. The current flowing through the sense line to the V_{CC} pin is small (assuming a switching controller with external switches), and the voltage drop is usually insignificant. The load current flows through the sense resistor to the load. If the V_{CC} current is significant, then this sense trace must be made wide enough so that the voltage drop is small with respect to the drop across the sense resistor.

Medium accuracy current sense resistors often use thick film or wire-wound technology, with resistance accuracy of 1% to 5% and temperature coefficient of 20 ppm/°C to 80 ppm/°C. High precision sense resistors use metal foil resistors and can meet specifications as high as 0.1% accuracy and 5 ppm/°C temperature coefficient.

Sense resistors should not be placed close to heat sources such as MOSFET switches or catch diodes.

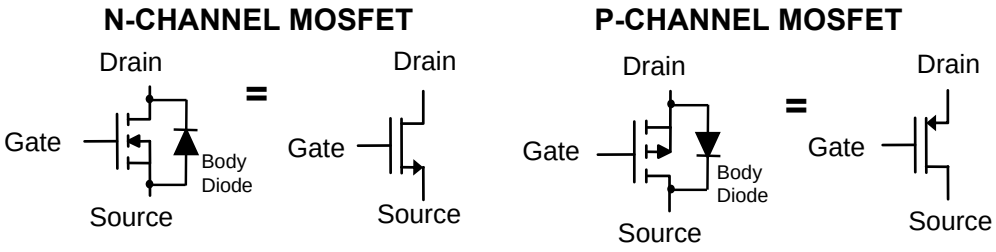
Sense Resistor Considerations

- **Choose maximum current limit, Imax**
  - Select the max operating current limit. This value can be obtained from the data sheet of the controller
- **Calculate sense resistor value**
  - Using the maximum sense voltage of the controller, the sense resistor can be calculated as follows: **Rsense = Vsense / Imax**
- **Calculate the sense resistor power**
  - The power is calculated simply as follows: **P = Vsense × Imax**
- **Determine what accuracy you will require**
  - Once all this data is determined you can choose the sense resistor. Often it is not possible to use just one resistor due to power and/or value constraints. In these case multiple resistors are used in parallel / series
- **Follow recommendations on the controller manufacturer's data sheet!!**
- **Sense resistors also used with hot swap controllers, etc.**

This figure shows some considerations regarding the selection of the sense resistor.

Active Components

MOSFET Basics



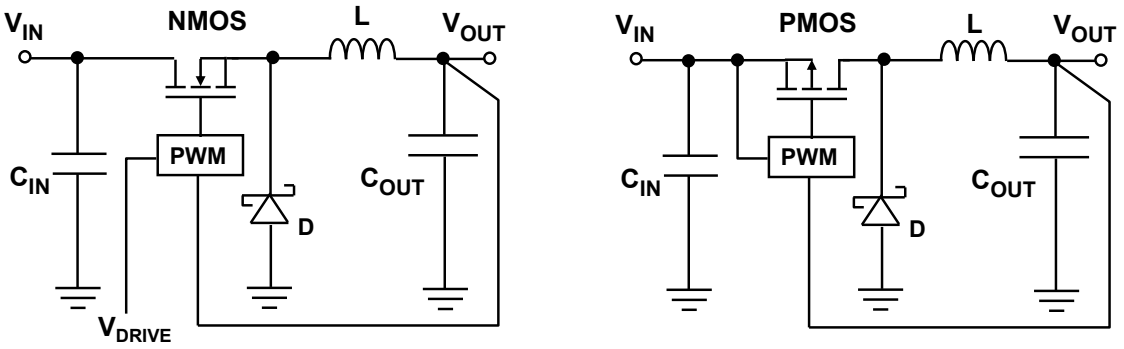
- **Three Terminal Device**
  - **Gate**
  - **Source**
  - **Drain**
- **Two classical varieties: NMOS, PMOS**
- **Electrically isolated gate**
- **High input impedance**
- **Voltage-controlled device**
- **Internal parasitic body diode from drain to source**

MOSFETs are the dominant switch technology for switch mode power supplies. Bipolar transitors are sometimes used as switches, but suffer from a number of disadvantages compared to MOSFETs.

The figure shows two common schematic representations of the NMOS and PMOS FETs. The internal parasitic body diode from drain to source is omitted in many schematics for simplification. The body diode is unavoidable due to the way MOSFETS are constructed.

MOSFETs are easy to drive since they have high impedance inputs and are voltage-controlled devices. The only current required is to charge/discharge the parasitic gate capacitance.

N-Channel vs. P-Channel



N-Channel MOSFET

- More difficult to drive
- Gate must be $V_{IN} + V_{GS(ON)}$ to turn NMOS on
- Drive voltage needed ≥ $V_{IN} + V_{GS(ON)}$
- Lower $R_{DS(ON)}$
- Lower cost

P-Channel MOSFET

- Easier to drive
- Gate driven below V_{IN} by at least $V_{GS(ON)}$ to turn PMOS on
- Gate can be driven between V_{IN} and ground
- Can be run at 100% duty cycle for portable applications
- Higher $R_{DS(ON)}$
- Higher cost

This figure summarizes the basic differences between the N-Channel and the P-Channel MOSFET. Both are shown in a typical asynchronous switching supply application.

N-Channel devices are more difficult to drive because the gate drive voltage (V_{DRIVE}) has to be taken to a more positive voltage than the source to turn on the device. If this voltage is not available it must be generated, usually with a simple bootstrap circuit consisting of an external diode and a capacitor (the current requirement is very low). P-channel devices require drive voltages which are less than the source and therefore do not require an additional drive voltage supply. The gate of a P-Channel device can be driven between V_{IN} and ground.

P-Channel devices have intrinsically higher on resistance (R_{ON}) due to the deceased mobility of the carriers in the P-type material. In addition, P-Channel devices are usually slightly more expensive than N-channel devices.

MOSFET current handling capability can be increased by paralleling two or more similar devices. The temperature coefficient of R_{ON} is positive which prevents current hogging. Diodes, on the other hand, have a negative TC which makes paralleling difficult.

Parallel MOSFETs reduce the effective R_{ON}, but increase the gate capacitance and the resulting switching losses.

MOSFET Parameters of Interest for Switching Converters

- Threshold voltage $V_{GS(TH)}$
  - Minimum gate bias which enables the formation of the channel between source and drain
  - Decreases with temperature
- On resistance $R_{DS(ON)}$
  - Total resistance between source and drain during on state
  - Important parameter in determining current rating and power dissipation
  - Increases with temperature due to hole and electron mobility decreasing with temperature
  - Decreases with increased gate to source voltage
- $R_{DS(ON)}$ has positive TC (0.7%/°C to 1%/°C)
  - Ideal for parallel operation
  - Parallel MOSFETs tend to share current evenly
- Drain-source breakdown voltage BV_{DSS}
  - Maximum drain-to-source voltage device can endure without avalanche breakdown in off state.

This figure summarizes the parameters of interest when selecting MOSFETs for switching converters.

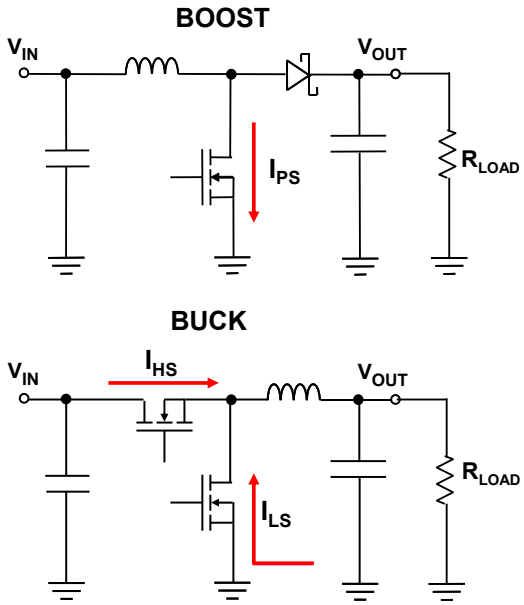
The gate threshold voltage determines the drive voltage required to turn the MOSFET on and off. It is important that this voltage does not exceed the input voltage. Otherwise, an additional supply will be needed for the drive voltage.

The on resistance determines the current rating and the power dissipation of the MOSFET. It has a positive temperature coefficient which allows multiple FETs to be paralleled without current hogging.

The drain-to-source breakdown voltage must include any transient voltage which may be generated due to the inductor switching.

Calculating Power in MOSFETs: Conduction Loss

- The first of two primary mechanisms of loss in a power FET is conduction loss
- Conduction loss = $(I_{RMS})^2 \times R_{DS(ON)}$
- RMS current in Boost MOSFET
  - $I_{PS(RMS)} \approx V_{IN} \sqrt{D} \times 1/((1-D)^2 \times R_{LOAD})$
  - $D = t_{ON}/(t_{ON} + t_{OFF})$
  - $V_{OUT}/V_{IN} = 1/(1-D)$
- RMS current in Buck MOSFET
  - $I_{HS(RMS)} \approx I_{OUT} \times \sqrt{D}$
  - $I_{LS(RMS)} \approx I_{OUT} \times \sqrt{(1-D)}$
  - $V_{OUT}/V_{IN} = D$
- Use $R_{DS(ON)}$ *max* value from data sheet at the appropriate V_{GS} drive voltage



When the FET is conducting it will be in series with an inductor for a period of the switching cycle. Knowing that inductor's dc current and ripple current values will allow you to calculate the rms current through the FET during that cycle via the following equations.

Boost (CCM) (ΔI_L is defined as peak-to-peak inductor current):

$$I_{PS(RMS)} = \left(\frac{V_{IN}}{(1-D)^2 \cdot R_{LOAD}}\right)\sqrt{D\left[1+\left[\Delta I_L(1-D)^2 \cdot \frac{R_{LOAD}}{2 \cdot V_{IN}}\right]^2 \frac{1}{3}\right]} \approx \frac{V_{IN} \cdot \sqrt{D}}{(1-D)^2 R_{LOAD}}$$

Buck (CCM) (ΔI_L is defined as peak-to-peak inductor current):

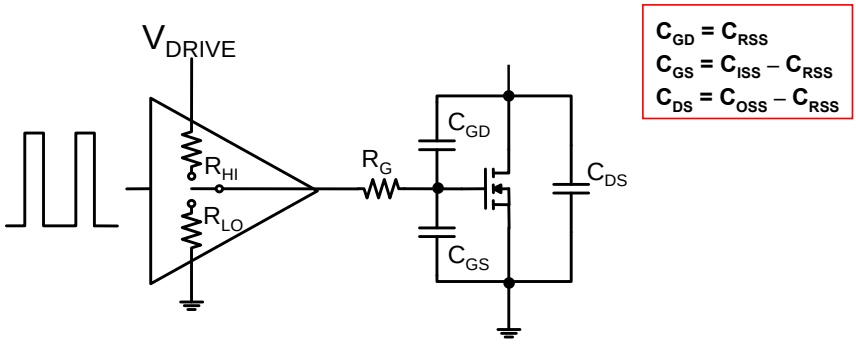
$$I_{HS(RMS)} = I_{OUT}\sqrt{D\left[1+\frac{1}{3}\left(\frac{\Delta I_L}{2 \cdot I_{OUT}}\right)^2\right]} \approx I_{OUT} \cdot \sqrt{D}$$

$$I_{LS(RMS)} = I_{OUT}\sqrt{(1-D)\left[1+\frac{1}{3}\left(\frac{\Delta I_L}{2 \cdot I_{OUT}}\right)^2\right]} \approx I_{OUT} \cdot \sqrt{(1-D)}$$

For a first order approximation, use the $R_{DS(ON)}$ max value from the data sheet for the appropriate V_{GS} drive voltage. Be aware that $R_{DS(ON)}$ increases with temperature, so calculating power dissipation due to conduction losses is actually an iterative process. However, when doing a "Will this FET work?" check, the first order approximations shown above will likely answer that question for you.

Calculating Power in MOSFETs: Switching Loss

- **The second of two primary mechanisms of loss in a power FET is switching loss**
- **Goal is to switch between highest resistance state and lowest resistance state as quickly as possible.**
- **Parasitic capacitances C_{GS} and C_{GD} slow down these transitions and thus cause power dissipation proportional to frequency.**



The second source of power loss in a power FET is switching loss. Ideally, the FET switches from its highest resistance to its lowest resistance state in zero time. In practice, the finite switching time will cause switching loss.

The parasitic capacitances C_{GS} and C_{GD} slow down the transition times and cause power dissipation associated with the switching frequency.

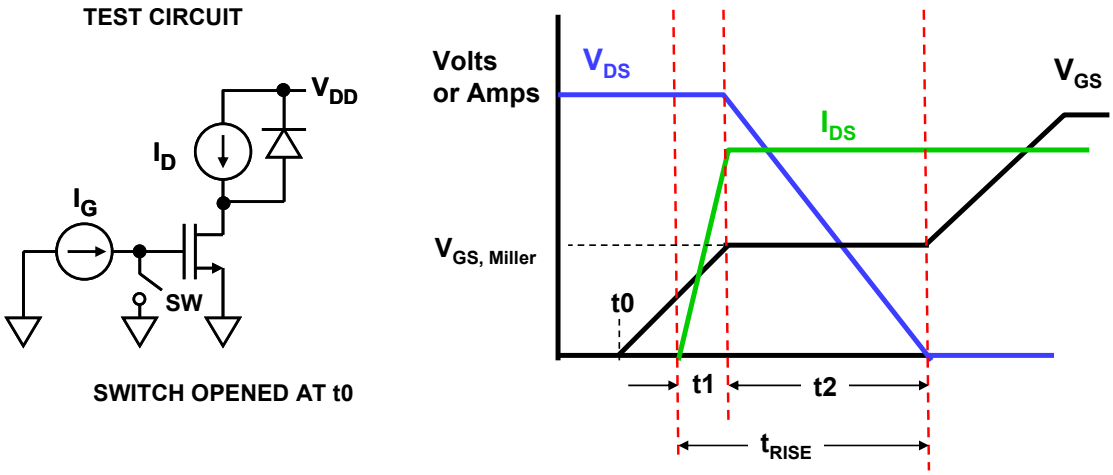
As a reminder:

$$C_{GD} = C_{RSS}$$
$$C_{GS} = C_{ISS} - C_{RSS}$$
$$C_{DS} = C_{OSS} - C_{RSS}$$

Note that the parasitic capacitances are voltage dependent. Therefore the values in the table of the data sheet are not very helpful. Use the capacitance versus V_{DS} curves on data sheet to determine the value of capacitance to use.

MOSFET Switching Loss (Continued)

- The product of the current through and voltage across the inductor is a triangle wave shape. The area of this triangle is the switching transition loss.
- $P_{SW} \approx (V_{IN} \times I_{OUT}) \times F_{SW} \times (t_{RISE} + t_{FALL})/2$



This figure represents the turn on waveforms of a MOSFET.

Time period t1 is primarily due to the C_{GS} capacitance and current drive capability of the driver.

Time period t2 is the main component in slowing switching and transitions and increasing power loss. t2 is primarily due to the C_{GD} or Miller capacitance and the current drive capability of the driver.

During switching transitions (time periods t1 and t2) there is both voltage across drain to source and current flowing from drain to source. The presence of both current and voltage suggests there will be power dissipation in the device.

The turn off waveforms follow the same signatures. The falling waveforms would be rising and the rising waveforms falling in the turn off transition.

These losses are a function of how often the transitions occur, so switching losses increase with switching frequency.

Many other factors take this analysis beyond 1st order approximations seen here. MOSFET transconductance, reverse recovery of synchronous FETs, parasitic inductances.

$$I_{GT1} = V_{DRIVE} - 0.5 \times (V_{GS,Miller} + V_{TH}) / (R_{HI} + R_{GATE})$$

$$I_{GT2} = (V_{DRIVE} - V_{GS,Miller}) / (R_{HI} + R_{GATE})$$

$$t1 = C_{ISS} \times (V_{GS,Miller} - V_{TH}) / I_{GT1}$$

$$t2 = C_{RSS} \times V_{DS(OFF)} / I_{GT2}$$

$$t_{RISE} = t1 + t2$$

$$I_{GT3} = V_{GS,Miller} / (R_{LO} + R_{GATE})$$

$$t_{FALL} = Q_{G(SW)} / I_{GT3}$$

Fsw= switching frequency

Is MOSFET Power Dissipation Too High?

- **The total loss (nearly) in the FET is the sum of the switching loss and conduction loss**
  - $P_{TOTAL} = P_{CONDUCTION} + P_{SWITCH}$
- **Now that we have the total loss, we can determine if it is too high for thermal stability. The answer will be (as with most things) "it depends."**
- **MOSFET manufacturers will specify a maximum junction temperature (T_{JMAX}) as well as a junction to ambient thermal resistance (θ_{JA}) on their data sheets.**
- **One can roughly calculate the approximate junction temperature (T_J) knowing θ_{JA}, estimated ambient temperature (T_A), and total power (P_{TOTAL}) as follows:**
  - $T_J = T_A + \theta_{JA} \times P_{TOTAL}$
  - **If $T_J > T_{JMAX}$, the FET you selected will not work. (for long)**
- **Because MOSFET $R_{DS(ON)}$ has a positive TC (0.7%/°C to 1%/°C), parallel MOSFETs share current fairly evenly, so parallel connections are often used in lieu of larger single FETs. Dual FETs are often connected in parallel, for example**

It should be noted that Θ_{JA} is generally specified with a given type and area of copper. Chances are your design may have different copper and area. Additional analysis must be done to get a precise T_J. However, this 1st order approximation will likely answer the "Will this FET work?" question. There is also a linear derating factor associated with increased ambient temperature. If the design pushes the upper thermal limit, it might or might not work. Proceed with caution.

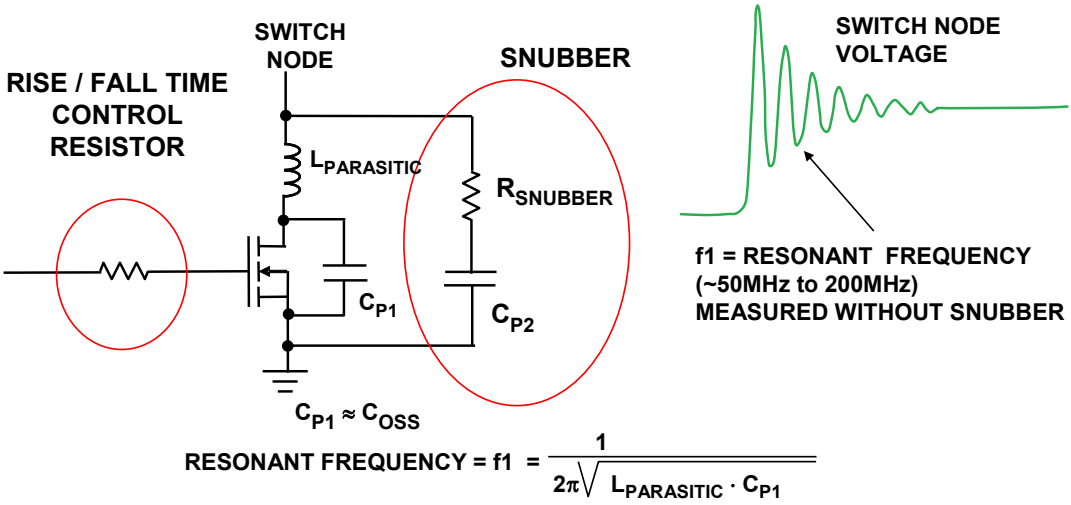
The failure mechanism in the FET is the heat itself. There is no inherent limit to the amount of current a FET can pass, so if you were running a FET with a good heat sink, the amount of power it dissipated could be significantly increased.

As indicated previously, MOSFETs can be paralleled in order to increase the total current capability at the expense of more drive current.

See the thermal design discussion later in this section.

Snubber Selection for Buck Converters

- Not generally required for <3A applications with good layout
- Add series RC to each switching FET
- Check each switch node
- Design will have less EMI and less component stress
- Gate resistance can control rise / fall time



A *snubber* is sometimes required to protect the FET from overshoot, undershoot, and ringing at the switch node. This is caused by fast edges exciting the switch node capacitance and parasitic inductances of parts and traces. Most of the time we do not care much about this unless the spikes exceed device breakdown ratings, or the resulting EMI exceeds limits.

There is no good rule for the use of snubbers, other than use them when needed. If layout is bad, a snubber may improve EMI at most any current; but with good layout we seldom use snubbers in buck regulators under 3 A . As the current rises to >10 A snubbers are often used.

Snubbers are good at damping the ringing, but they consume power and have little effect on initial overshoot. Rise time and fall time control can be used to limit this spike—sometimes a gate resistor is used—but this method is lossy. Both methods reduce overall efficiency. A conservative approach is to initially lay out the PCB with a place for a snubber network also rise time limiting resistors, realizing that these may not be required after testing.

The figure shows an approximate equivalent circuit for designing the snubber network. When the FET current changes rapidly, ringing can occur at the resonant frequency of the FET output capacitance (C_{OSS}) and the parasitic inductance in the loop ($L_{PARASITIC}$). The frequency of this ringing is generally between 50 MHz and 200 MHz depending on circuit conditions.

Assume a resonant frequency of 100 MHz, and C_{OSS} = 300 pF, then $L_{PARASITIC}$ = 8 nH.

Snubber Selection for Buck Converters

- **Apply Load to a Buck converter and measure resonant frequency (f1) on switch node transition**

$$f1 = \frac{1}{2\pi \bullet \sqrt{C_{P1} \bullet L_P}}$$

- **Add a reasonable amount of capacitance (C_{P2}) whose value is somewhere between C_{OSS} of the low side FET and $2\times C_{OSS}$ to the switch node to ground and measure the resonant frequency again (f2).**

$$f2 = \frac{1}{2\pi \bullet \sqrt{(C_{P1} + C_{P2}) \bullet L_P}}$$

- **The result is two equations and two unknowns (C_{P1} and L_P)**
- **The next step is to find an R_S value which will slightly over-damp the LRC resonance by setting Q roughly equal to 0.9**

$$Q = \sqrt{L_P / (C_{P1} + C_{P2})} / R_S$$

- **The power dissipated in the snubber resistor will be ½ CV^2 for turn on and ½ CV^2 for turn off:**

$$P = C_{P2} \bullet V_{IN}^2 \bullet f_{SWITCHING}$$

This is the first order approximation process for finding snubber values for a buck converter. Proper measurement techniques to reduce parasitics are necessary when measurement switch node resonant frequencies.

The first step is to measure the ringing frequency on the switch node, f1. Then add an external capacitor from the switch node to ground, C_{P2}, with a value between C_{OSS} (from the FET data sheet) and $2 \cdot C_{OSS}$. Measure the new resonant frequency, f2.

The resulting two equations can then be solved for the two unknowns, L_P and C_{P1}.

The next step is to determine the approximate value of R_S which will slightly over-damp the LRC resonance by setting Q equal to 0.9. The equation for Q can then be solved for R_S.

One can see that the added capacitance is directly proportional to the total loss in the snubber. There may be an iterative process required to find a value that minimizes losses and provides adequate damping of the ringing on the switch node.

R_S and C_{P2} can be further optimized by experimentation—increase C_{P2} slightly and decrease R_S.

Snubbers are more effective the closer you can physically get them to the die voltage which you trying to snub, so the RC should be placed as close to the drain-to-source on the low side FET in a buck as possible. Make sure to adequately size the resistor to handle the power dissipation. The capacitor will not dissipate any notable amount power.

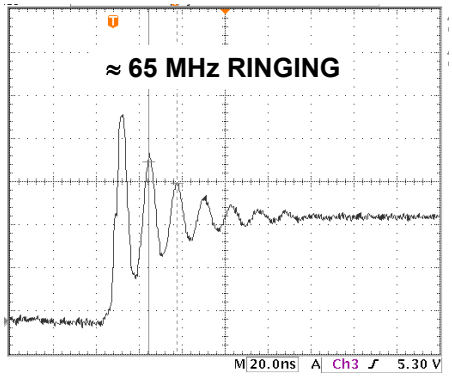
The power dissipated in the snubber resistor is approximately

$$P = C_{P2} \cdot V_{INPUT}^2 \cdot F_{SWITCHING} \cdot$$

For an example power calculation, assume C_{P2} = 600 pF, V_{INPUT} = 12 V, $F_{SWITCHING}$ = 1 MHz, then P = 86 mW.

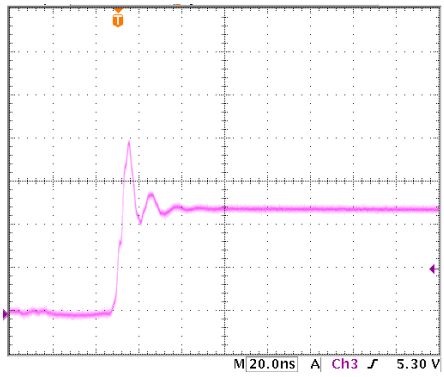
Effect of Snubber on the Switch Node for a Buck Converter

NO SNUBBER



VERTICAL: 5V/div
HORIZONTAL: 20ns/div

WITH SNUBBER



VERTICAL: 5V/div
HORIZONTAL: 20ns/div

Here we show the effect of the snubber on the switched waveform. Note the reduction (although not elimination) of the initial overshoot and ringing.

Diode Rectifiers

- Standard Recovery Silicon (not recommended)
- Fast Recovery Silicon (not recommended)
  - 50V to 1000V breakdown
  - 100ns to 500ns recovery time
- "Ultrafast" Recover Silicon (only for high voltage applications)
  - 50V to 1000V breakdown
  - 20ns to 75ns recovery time
- Standard Schottky
  - 20V to 100V breakdown
  - Switcher "Workhorse"
  - 0ns recovery time
- Low Forward Voltage Schottky
  - 10V to 40V breakdown
  - 0ns recovery time

This figure lists diode rectifiers starting with the oldest technology, standard recovery silicon diodes. These were the first type of rectifiers, such as the 1N4004 and 1N5404. Reverse breakdowns were high, but recovery time was not specified.

The addition of gold doping yielded "fast recovery" silicon diodes of 100 ns to 500 ns recovery, such as the 1N4936.

These were followed by "ultrafast" recovery silicon diodes with 20 ns to 75 ns recovery time and up to 1000 V reverse breakdown, such as the MUR140 and ES1D.

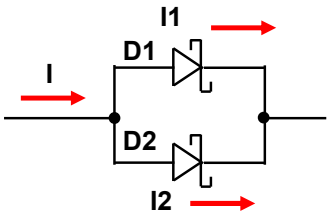
Today, the standard Schottky diode is the workhorse diode of asynchronous switchers. Certain varieties are available with breakdowns up to 200 V.

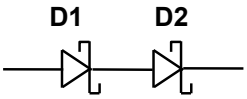
A variety of Schottky diodes are optimized for low forward voltage drop with breakdowns up to 40 V.

None of the Schottky diodes have measurable reverse recovery time.

Modern switching regulators use Schottky diodes in 99% of applications rather than the older silicon varieties.

Diode Parallel and Series Connections





- **Diodes have a negative TC, therefore one will "hog" most of the current in parallel connection. Use synchronous rectification.**
- **This may be useful in reducing overall parasitic inductance at the expense of additional capacitance. Cannot assume currents will share equally, however. Each diode must be rated for full current load.**
- **Series connection of diodes to increase effective breakdown voltage is risky and should be avoided.**

The power dissipated in the diode in an asynchronous switching converter often becomes a limiting factor at high currents. Unfortunately, diodes can't be paralleled to share the current, because they have a negative forward voltage temperature coefficient.

With two diodes in parallel, one will always have a slightly lower voltage drop, and this diode will carry slightly more current than the other one, the voltage drop will decrease, it will carry even more current, and eventually it will carry all the current.

Parallel diodes can be useful in reducing the overall parasitic inductance (at the expense of increased capacitance) but will not work in current-sharing applications.

It is not advisable to connect diodes in series to increase the effective reverse breakdown.

The basic point here is that it is not advisable to try to use multiple diodes in place of one correctly sized diode in either the parallel or series connection.

Power Supply Layout and Grounding

Parasitics to Deal with in PCB Layout

- **Trace Resistance**
  - **DC and AC errors due to voltage drop**
  - **Sheet resistance of 1 ounce copper = 0.491mΩ / square**
- **Board Capacitance**
  - **Coupling into high impedances and noise-sensitive circuits**
  - **Coupling between planes and to component pads**
  - **Trace capacitance = 2.8 pF/cm² for 1.5mm glass epoxy (ε_r = 4.7)**
- **Wiring Inductance**
  - **Especially in low impedance circuits and filters**
  - **Use wide conductors and ground planes to minimize**
- **Magnetic Coupling**
  - **Inductor-to-inductor, especially toroids. Consider alternate mounting directions**
  - **Loop-to-loop, minimize loop areas, use ground planes**

Besides the components loaded on a PC board, there are also many others parasitic elements that contribute to the performance of the circuit.

Trace resistance of the copper is approximately 0.491 mΩ / square for 1 ounce copper. For 2 ounce copper, it is one-half this value, or 0.246 mΩ / square, etc.

Trace capacitance is about 2.8 pF/cm² for 1.5 mm thick glass epoxy (ε_r = 4.7).

Trace inductance is given by the equation on p. 4.23 in this book.

Magnetic coupling between inductors, especially toroids, is also a consideration. This effect can be reduced by alternate mounting directions, minimizing loop areas, and the use of ground planes.

Printed Circuit Board Resistance

Copper Thickness	Resistance Coefficient, milliohms/inch/w (trace width w in inches)	Reference 0.1 inch wide trace, milliohms/inch
1/2 oz/ft ^{2}	0.983/w	9.83
1 oz/ft ^{2}	0.491/w	4.91
2 oz/ft ^{2}	0.246/w	2.46
3 oz/ft ^{2}	0.163/w	1.63

Sheet resistance of 1 ounce copper = 0.491mΩ/square

Common values for resistance of traces for various weights of copper commonly used in PCB manufacture.

Note that not all layers of a multilayer board need to be the same weight of copper. Thinner copper can be used for signal layers, especially when using fine pitch components which require very narrow traces.

Power planes can benefit from heavier copper by lowering trace resistance and helping dissipate more heat.

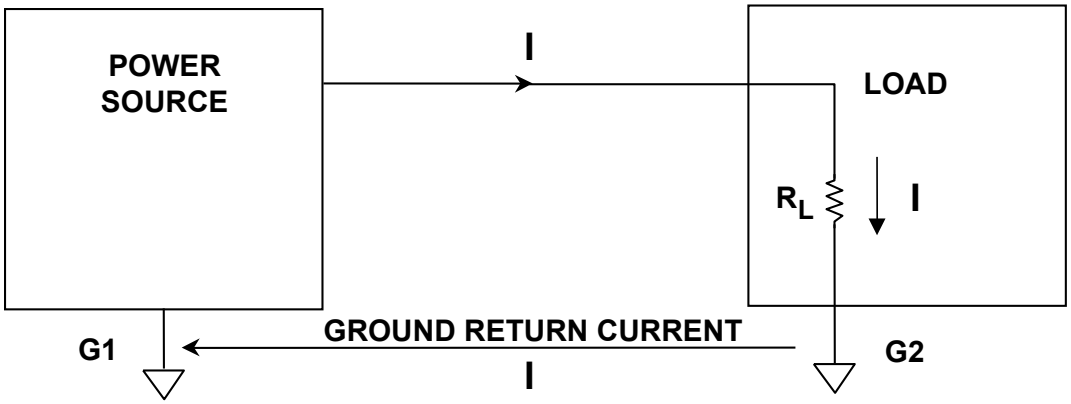
Relative Dielectric Constant, ε_r ,for Common PCB Materials

	Test Frequency	
Laminate	1kHz	1MHz
FR4 Glass Epoxy	4.4	4.7
FR5 Glass Epoxy	4.4	4.7
G9 Glass Melamine	7.2	7.5
G3 Glass Phenolic	5.5	
G7 Glass Silicon	4.2	4.7
Epoxy Thermount	3.9	
BT Epoxy	4.1	
Epoxy/Polymide	4.4	
Cyanide Ester	3.5	

This table shows the approximate dielectric constants of a variety of materials used in PCB dielectrics. These are rough averages of numbers from several handbooks and various manufacturers' literature, which often disagree significantly. Most are for 25°C ambient conditions, but some are measured at 20°C.

If this is an issue for your design, it is best to check with the PCB manufacturer.

Kirchoff's Law Helps Analyze Voltage Drops Around a Complete Circuit



AT ANY POINT IN A CIRCUIT
THE ALGEBRAIC SUM OF THE CURRENTS IS ZERO
OR
WHAT GOES OUT MUST COME BACK
WHICH LEADS TO THE CONCLUSION THAT
ALL VOLTAGES ARE DIFFERENTIAL
(EVEN IF THEY'RE GROUNDED)

One of the biggest problems in system design is how to handle grounding. There are several competing requirements that are dependent on the frequency and system complexity.

Unfortunately, there is no magic "cookbook" approach to grounding that will always guarantee success. What we will do here is present some of the effects that must be considered when designing the system.

The main thing is to look at how and where the dc and ac currents flow in a PCB.

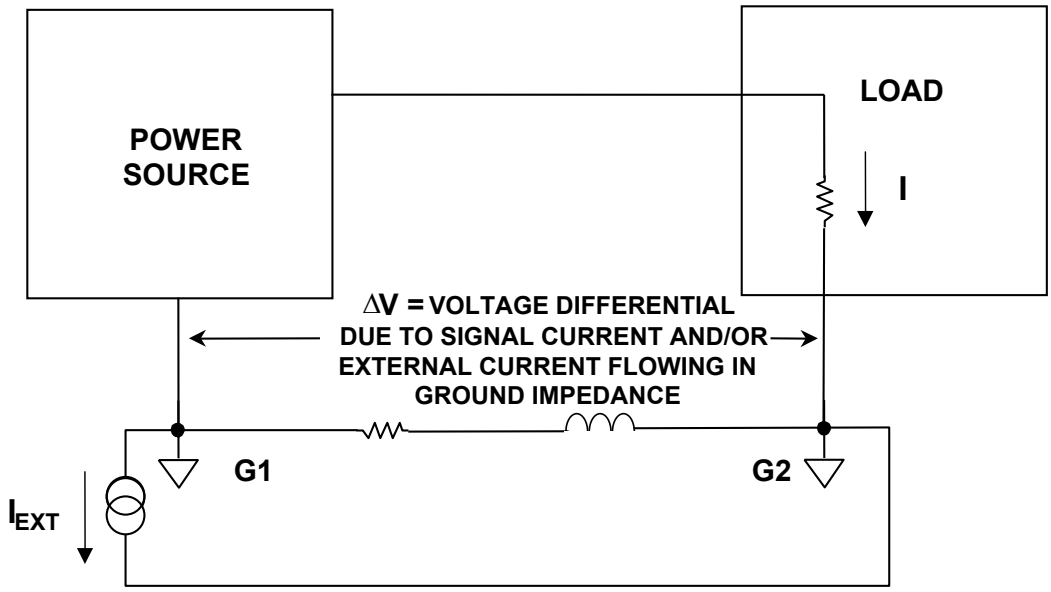
We reviewed the procedures for proper mixed-signal circuit grounding in Section 3. In this section we will look at grounding issues associated with switching power supplies.

When we draw the ground symbol on a schematic, we assume that all ground points are at the same potential. This is rarely the case, unfortunately.

Historically, "ground" was the reference level with which we measured various voltage levels in the circuit. However, ground has also become the power return not only for digital signals but for analog signals as well.

All signals that flow in a circuit must have a return path to complete the loop. Often we consider the forward path only, but there always must be a return to close the loop or current cannot flow. This return path is often through the ground plane.

A More Realistic View of the Impedance Between Grounds



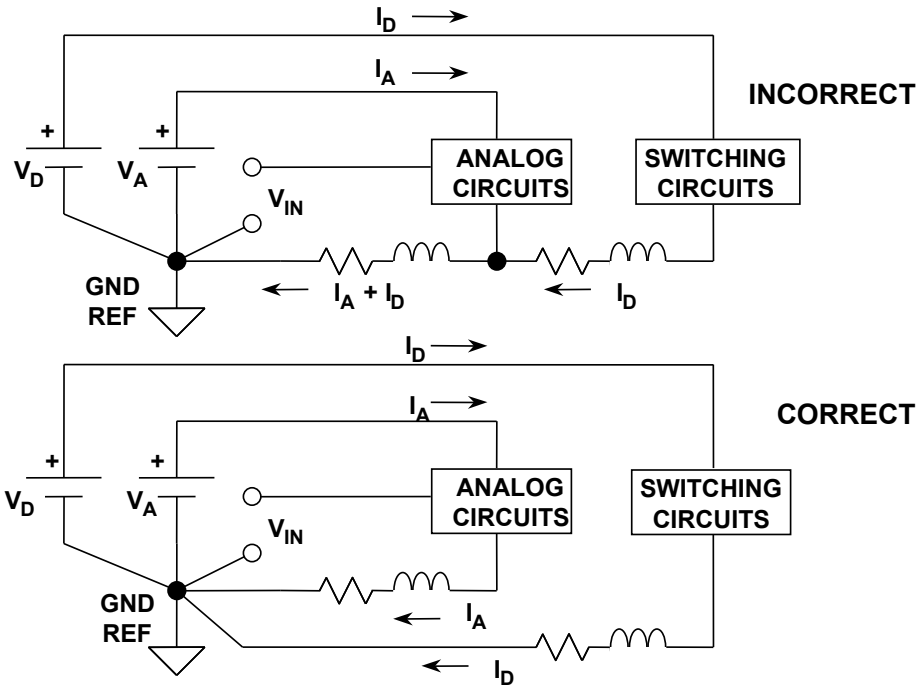
The connection between two points on the ground plane is never zero impedance. There is always some resistance and inductance, even in a large area heavy ground plane.

The magnitude of the impedance may be small, but it is not zero. And a current flowing through an impedance causes a voltage drop.

This means that the two grounds in the diagram above will not be at the same potential.

It is important to consider the inductance of the ground as well as the resistance, especially as the frequency increases.

Switching Currents Flowing in Analog Return Path Create Error Voltages



Because ground is the power return for all digital circuits, as well as many analog circuits, one of the most basic design philosophies is to separate digital ground returns from analog ground returns.

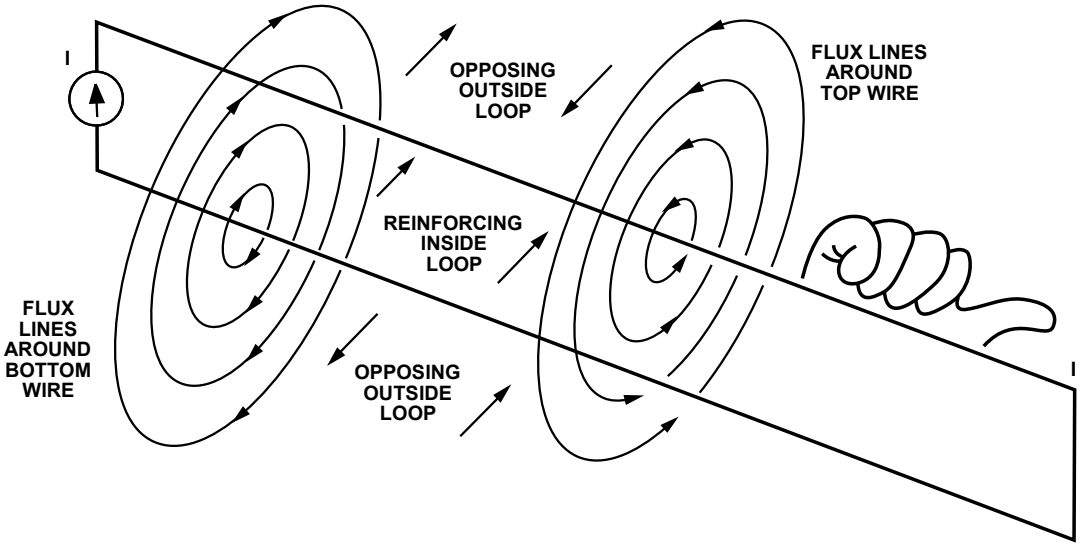
If the grounds are not separated, not only does the return from the analog circuitry flow through the analog ground impedance, but the digital ground current also flows through the analog ground, and the digital ground current is typically much greater than the analog ground current.

As the frequency of digital circuits increases, the noise generated on the ground increases dramatically. TTL and CMOS logic families are of the saturating types. This means that the logic transitions cause large transient currents on the power supply and ground. CMOS outputs basically connect the power to ground through a low impedance during the logic transitions.

And it's not just the basic clock rate that is a problem. Digital logic waveforms are basically rectangular waves, which implies many higher frequency harmonic components.

The same holds true for switching power supplies.

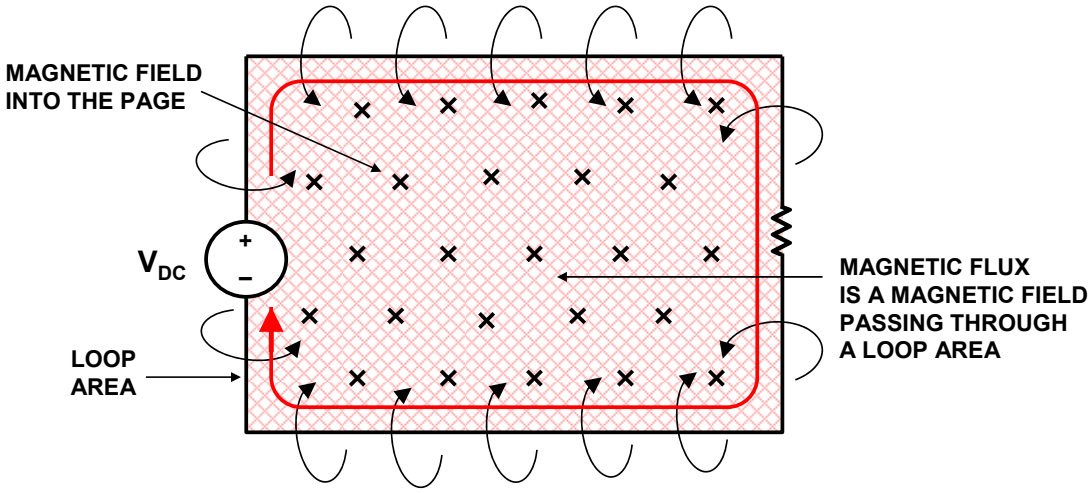
Magnetic Field Lines and Inductive Loop (Right Hand Rule)



The right hand rule is useful in predicting the direction of the magnetic field lines produced by a current flowing in a conductor.

If you point the fingers of your right hand in the direction of the flux density, the induced signal will flow in the direction that your thumb is pointing.

Magnetic Field Passing Through a Loop Area Creates Magnetic Flux



A loop of wire carrying current is essentially an electromagnet whose field strength is proportional to the current. Magnetic flux is proportional to the magnetic field passing through the loop area,

$$\text{Magnetic Flux} \propto \text{Magnetic Field} \times \text{Loop Area}$$

or more precisely,

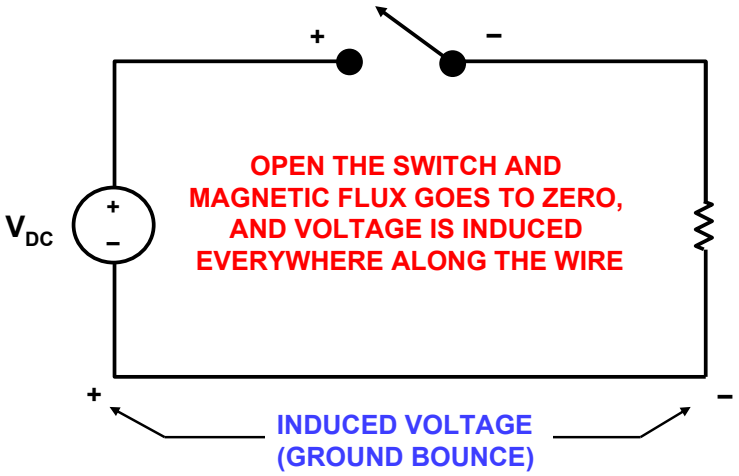
$$\Phi_B = BA\cos\varphi$$

Where the magnetic flux, Φ_B, is the magnetic field, B, passing through a surface loop area, A, at an angle, φ, to the area's unit vector.

A look at the figure gives meaning to the magnetic flux associated with an electric current. A voltage source pushes current through a resistor and around a loop of wire. This current generates a *magnetic field* which encircles the wire. To relate the different quantities, think of grabbing the wire with your right hand (applying the *right-hand rule*). If you point your thumb in the direction of current flow, your fingers will wrap around the wire in the direction of the magnetic field lines. As those field lines pass through the loop, their product is *magnetic flux*, directed in this case into the page.

Change either the magnetic field strength or the loop area, and the magnetic flux will change. As the flux changes, a voltage is induced in the wire, proportional to the rate of change of the flux, $d\Phi_B/dt$. Notice that either a fixed loop and changing current or a constant current and a changing loop area—or both—will the change the flux.

Effects of Opening a Switch

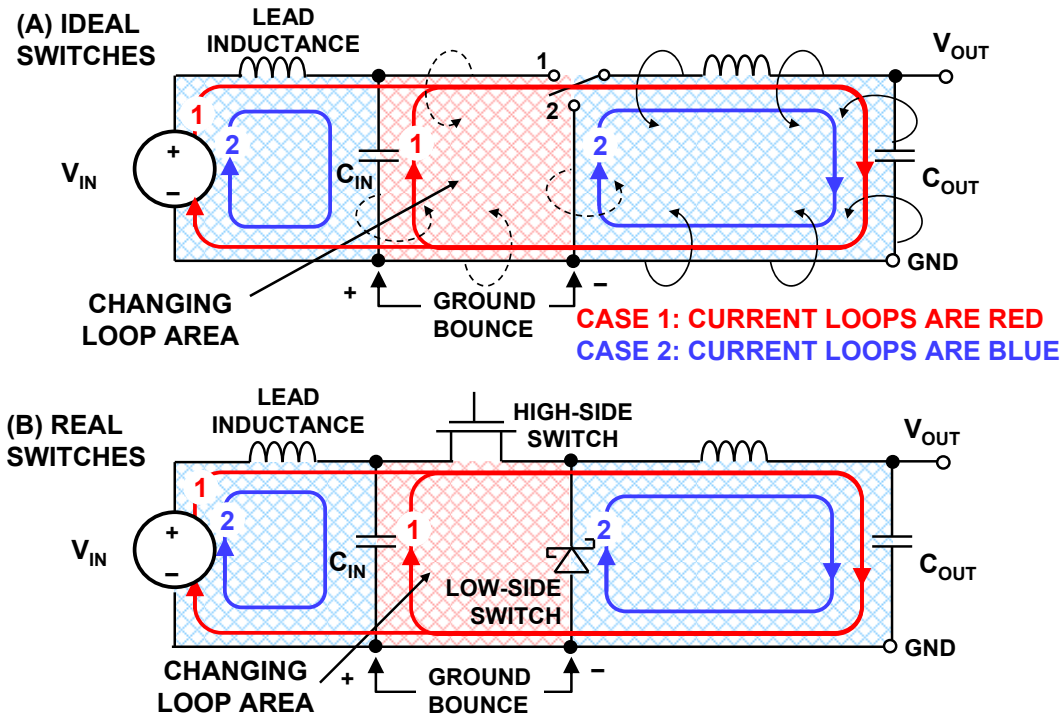


Suppose, for example, that the switch in the figure is suddenly opened. When current stops flowing, the magnetic flux collapses, which induces a momentarily large voltage everywhere along the wire.

If part of the wire is a ground return lead, voltage that is supposed to be at ground will spike, thus producing false signals in any circuitry using it as a ground reference.

Generally, voltage drops in printed-circuit-board sheet resistance are not a major source of ground bounce. 1-oz copper has a resistivity of about 500 mΩ/square, so a 1 A change in current produces a bounce of 500 mV/square—a problem only for thin, long, or daisy-chained grounds, or precision electronics.

The Effects of Switching on Loop Area for Buck Converters



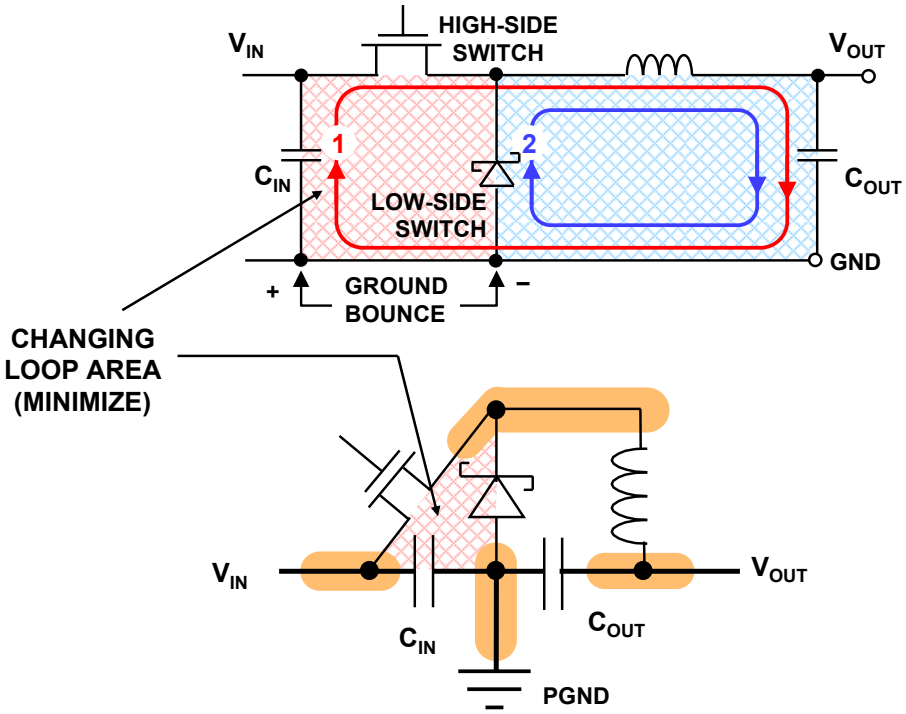
The best way to reduce ground bounce in a switching dc-to-dc converter is to control changes in magnetic flux—by minimizing both current loop *areas* and *changes* in loop area. This is illustrated in (A) which uses ideal switches. Although the input and output currents are roughly constant, as the switch moves from Position 1 to Position 2, the total loop area rapidly changes in the middle portion of the circuit. That change means a rapid change in magnetic flux, which in turn induces ground bounce along the return wire. In some cases, as in the figure, the current remains constant, but the switching produces a change of loop *area*, hence a change of flux. In (A) an ideal voltage source is connected by ideal wires to an ideal current source (the inductor represents the ideal current source). Current flows in a loop that includes a ground return. When the switch changes position, the same current flows in a different path. The current source is dc and does not change, but loop area does change. The change in loop area means a change in magnetic flux, so voltage is induced. Since a ground return is part of that changing loop, its voltage will bounce. The circuit in (B) shows the same principle implemented with real switches.

The fact that a change in magnetic flux will induce voltage everywhere along a ground return brings up the interesting question: where is true ground? Because ground bounce means a voltage on the ground return trace is bouncing with respect to some ideal point called *ground*, that point needs to be identified.

In the case of power-regulating circuits, true ground needs to be at the low end of the load. After all, a dc-to-dc converter's purpose is to deliver quality voltage and current to the load. All other points along the current return are not ground, just part of the ground return, subject to losses due to inductance and resistance.

In the following discussions, we will ignore the loop composed of V_{IN} and the lead inductance, because the current through this loop remains constant for each cycle.

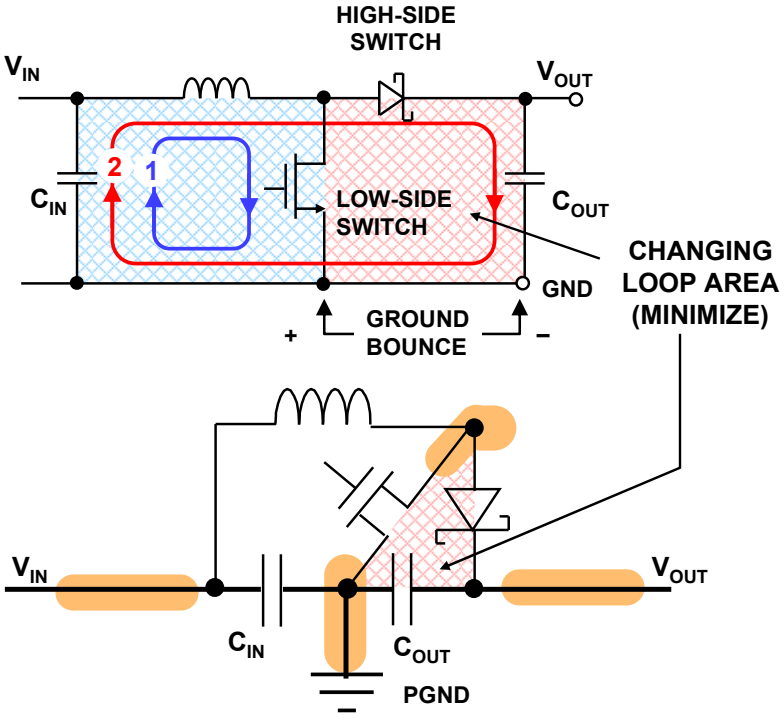
Buck Converter Layout



This shows how the currents and loop areas change in a buck converter. A good way to minimize the ground bounce is to minimize the *changing* loop area by careful placement of the components, primarily the C_{IN} capacitor. The critical loop is comprised of the high-side switch, the diode, and C_{IN}. Capacitor C_{IN} bypasses the top of the high-side switch directly to the bottom of the low side switch. thereby shrinking the changing loop area and isolating it from the ground return. From the bottom of V_{IN} to the bottom of the load, there is only a small loop-area change from one case to the next. Consequently, the ground return bounce is minimized.

As shown in the lower diagram, both C_{IN}, C_{OUT}, and the diode should be connected together with short leads to the power ground, designated "PGND" and shown by a triangle comprised of line segments rather than a solid triangle.

Boost Converter Layout

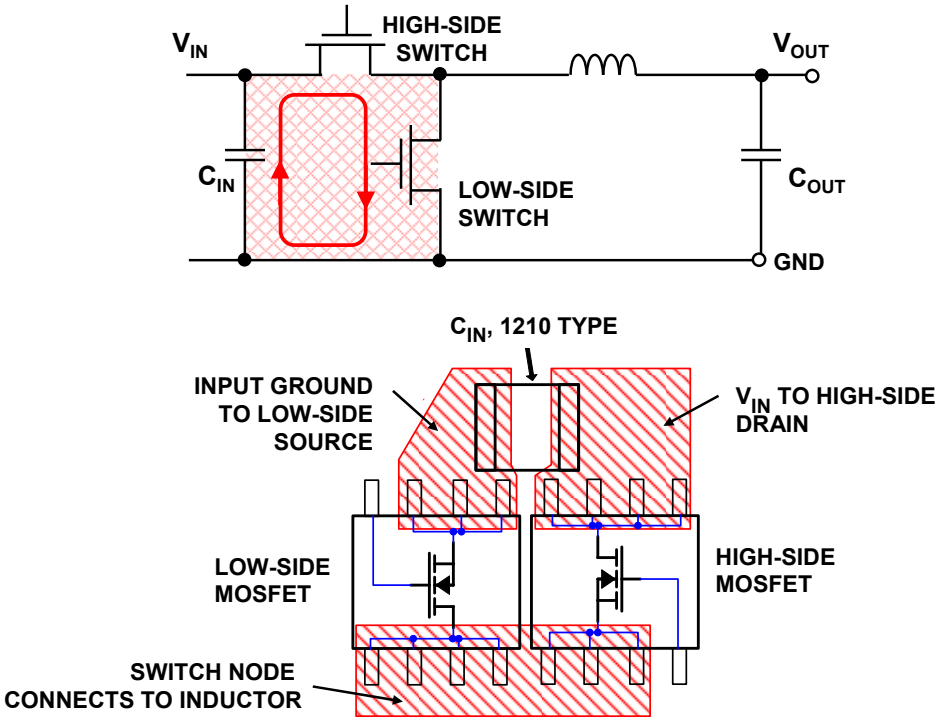


A boost converter is essentially a reflection of a buck converter, so it is the *output* capacitor that must be placed between the top of the high-side switch and the bottom of the low-side switch to minimize the change in loop area. Here the critical loop to be minimized is comprised of the low-side switch, the diode, and C_{OUT}.

Note that C_{IN}, C_{OUT}, and the bottom of the low-side switch are connected through short leads to the PGND.

This figure and the previous one illustrate the basic principle of identifying the critical loops and minimizing their areas. This will now be applied to several actual SMPS layouts.

Synchronous Buck Converter Layout

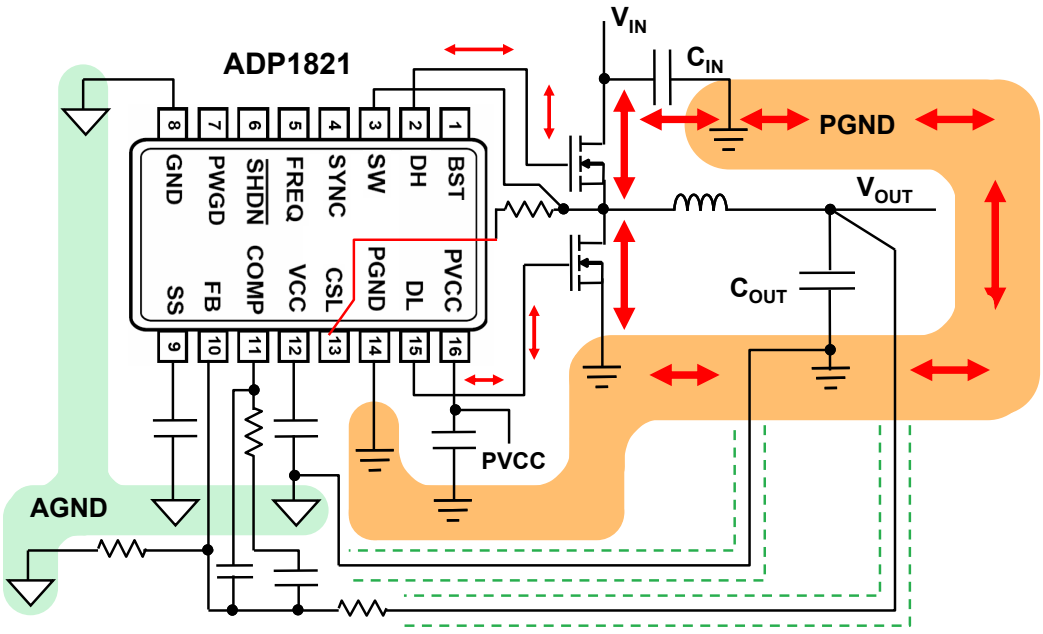


This figure shows the layout of the critical loop area in a synchronous buck converter.

Although the inductor has "continuous" high current, this current is switched alternately thru the top (control) and bottom (synchronous rectifier) FETs. The current waveform in each FET is a pulse with very high di/dt. This high di/dt flows in alternating directions in a loop comprised by the two FETs and the input bypass capacitor. Any inductance in this loop causes voltage spikes on the switch node and high-side drain with respect to the low side source, which can result in a variety of problems. To minimize this inductance, the current loop between the input bypass capacitor and thru the two FETs should be as short, fat, and tight as possible.

This example illustrates one way to get low inductance in the input ac current loop. Here, the SO-8 FETs are counter-rotated to allow shorter connections to the high current paths. The high-side drain and low-side source fit closely against the ceramic input bypass. The switch node connections fit to one compact power plane. This arrangement effectively minimizes the critical loop area composed of the switches and the input capacitor.

ADP1821 Synchronous Buck Layout



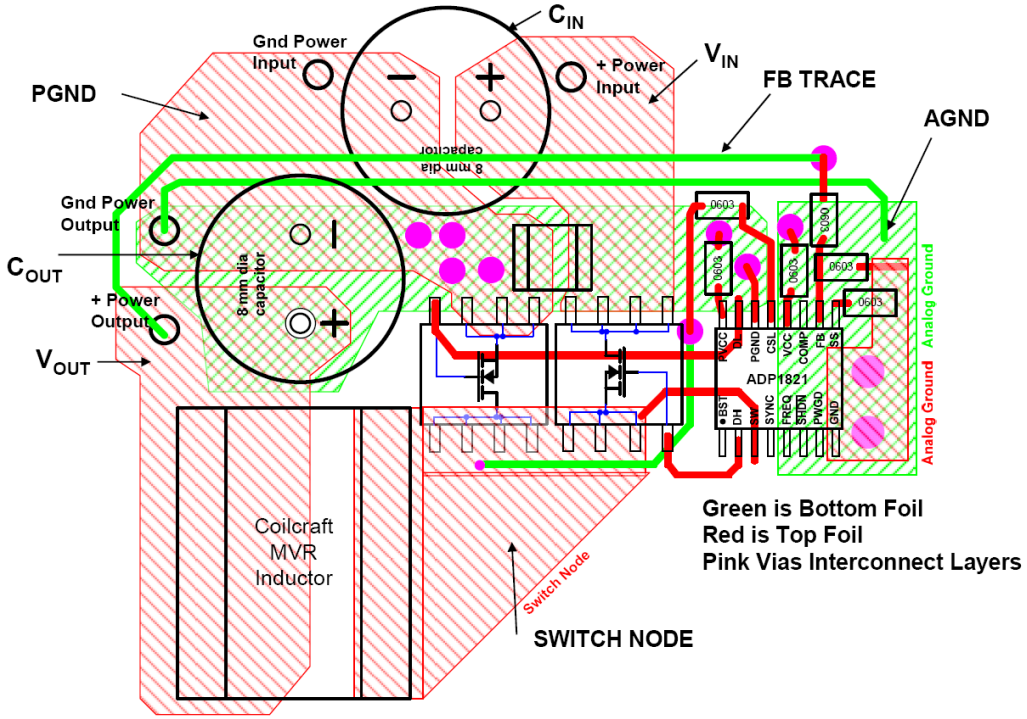
After minimizing inductance and impedance in the critical high current power paths, the second key concept is to prevent power and gate drive noise sources from interfering with the sensitive analog connections. You want to keep noise current out of traces that are noise sensitive; some of the approaches to doing this are based on Kelvin voltage sensing

ADI's design of controllers such as the ADP1821 allows significant noise voltage differential between PGND (current return path for the gate driver) and AGND (ground reference for analog circuitry). This permits a useful degree of separation of these two, which makes it easier to accomplish the desired isolation. Some competitor's ICs do not allow this separation and the layout can suffer as a result.

This figure shows schematically where the critical loop is located. All connections to the PGND island should be as short as possible. The PGND island is connected to the AGND island using a separate trace. The feedback resistors, soft-start capacitor, and the feedback compensation network should be connected to the AGND island.

Note that the output voltage is Kelvin sensed and connected to the feedback network using a separate trace. This trace should be isolated from any noisy traces.

ADP1821 Synchronous Buck Layout Details-1



This shows details of the layout of the critical components in the ADP1821 synchronous buck layout. Note that C_{IN} and C_{OUT} are both grounded to the PGND island. The high-side and low-side FETs are rotated as previously described to minimize the critical loop area.

PGND connects directly to PGND foil. PVCC is bypassed to PGND foil with a short trace to a capacitor very close to the chip.

The AGND island is located under the ADP1821 and is connected to the PGND by a separate trace. This trace carries very little current. The FB divider, V_{CC} bypass, soft-start capacitor, and control signals are grounded to the AGND island.

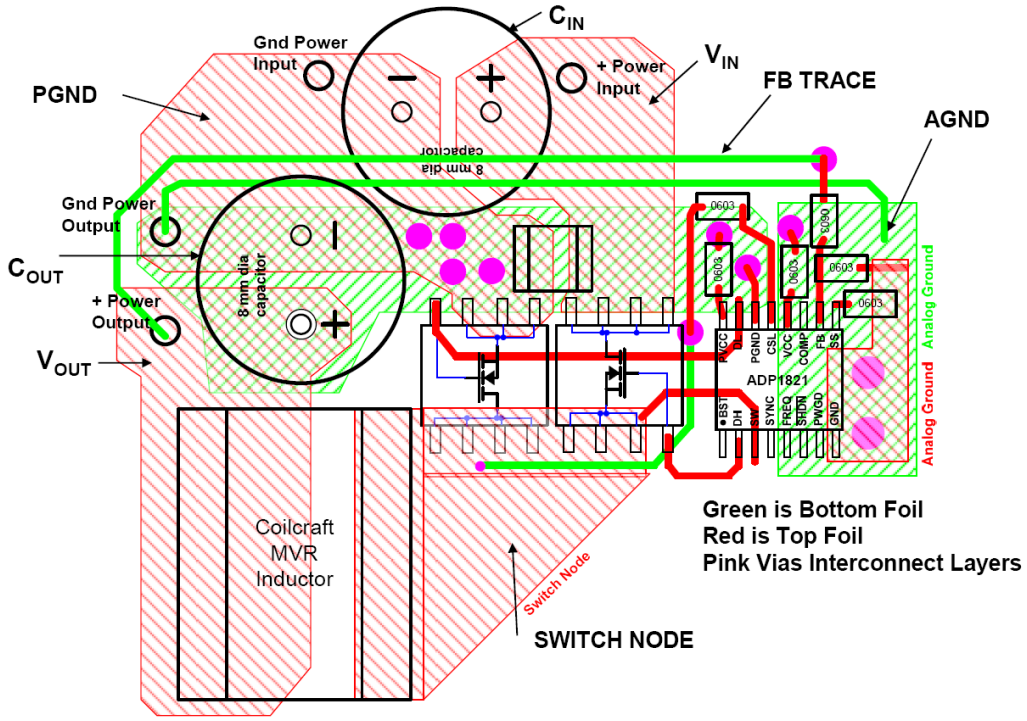
This arrangement provides the most accurate ground return sense for the converter. Place components close to the IC and make connections as short as possible.

This rotation of the ADP1821 allows direct connections from the driver outputs to the FET gates. Neat, huh?

The CSL resistor connection to switch node is separate from that of SW pin for best accuracy in sensing V_{DS} on the low-side FET.

Short, fat power ground foil connects ADP1821 PGND to source leads of low side FET thru multiple vias. This provides a low impedance ground return path for gate drive current. This path is separate from analog ground.

ADP1821 Synchronous Buck Layout Details-2

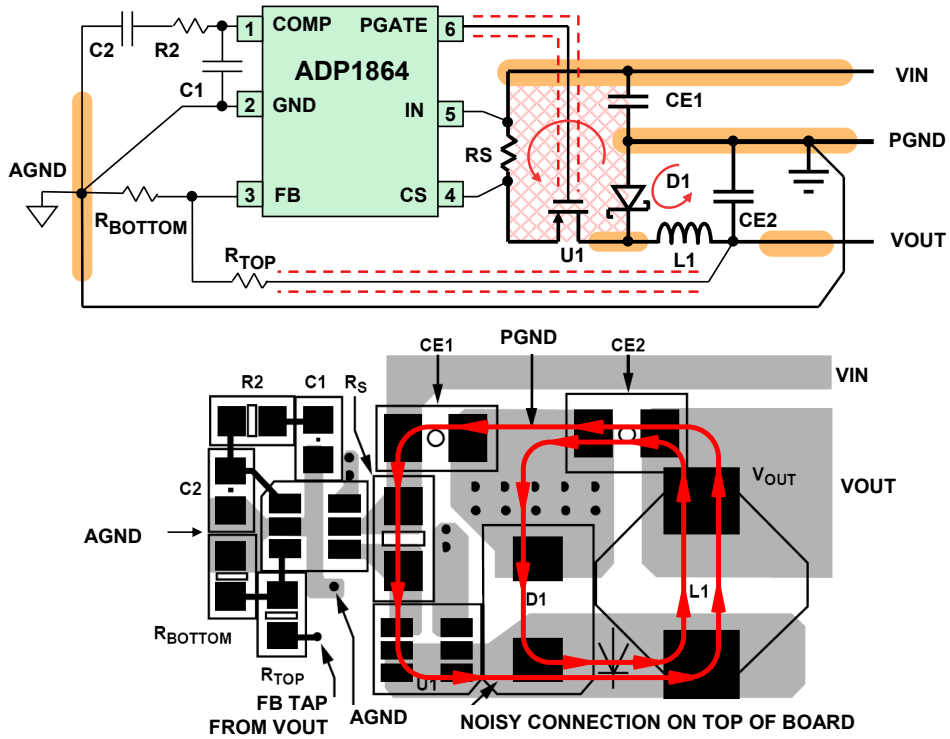


Do not run sensitive traces (such as FB, Soft Start, and Compensation) close to and parallel with noise generators such as gate drive (DH and DL) and the switch node. Parallel traces encourage inductive coupling, while mutual surface area can encourage capacitive noise coupling. Close proximity can make both worse. Where additional copper layers are available, a ground plane (placed between noise generating and noise sensitive nodes) can provide significant and helpful decoupling.

Gate drive traces (DH and DL) handle high di/dt so tend to produce noise and ringing. It is imperative that they should be as short and direct as possible. If at all possible, avoid using feedthru vias in the gate drive traces. If vias are needed, it is best to use two relatively large ones in parallel to reduce the peak current density and the current in each via.

The switch node connects the source of the high-side FET to the drain of the low-side FET and the inductor. This is the noisiest node in the switcher circuit with large ac and dc voltage and current (high dv/dt and di/dt). This node should be wide to keep resistive voltage drop down. But to minimize the generation of capacitively coupled noise, the total area should be small. The best layout will generally place the FETs and inductor all close together on a small copper plane in order to minimize series resistance and keep the copper area small.

Asynchronous Buck Switching Controller Layout



Here we show another example of a double-sided PCB layout for a switching supply. This is the layout of the evaluation board for the ADP1864 asynchronous buck switching controller.

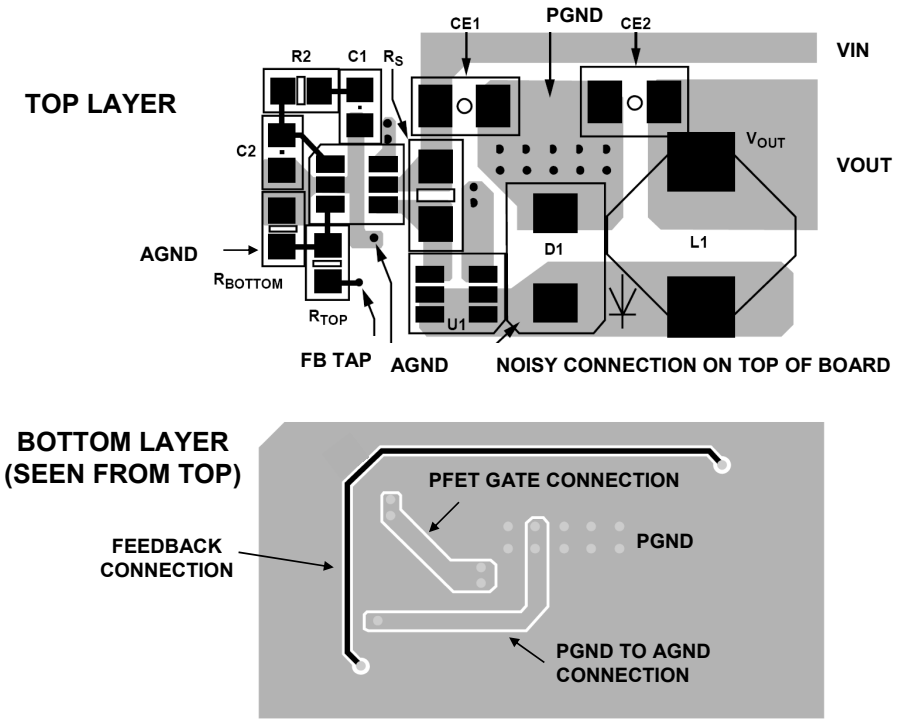
This layout follows the guidelines previously presented. The critical loop area to be minimized is comprised of the high-side FET (U1), the current sense resistor (RS), the input capacitor (CE1), and the diode (D1).

Note that high dv/dt and di/dt traces and the changing loop area have been minimized.

Ground islands are used for PGND and AGND.

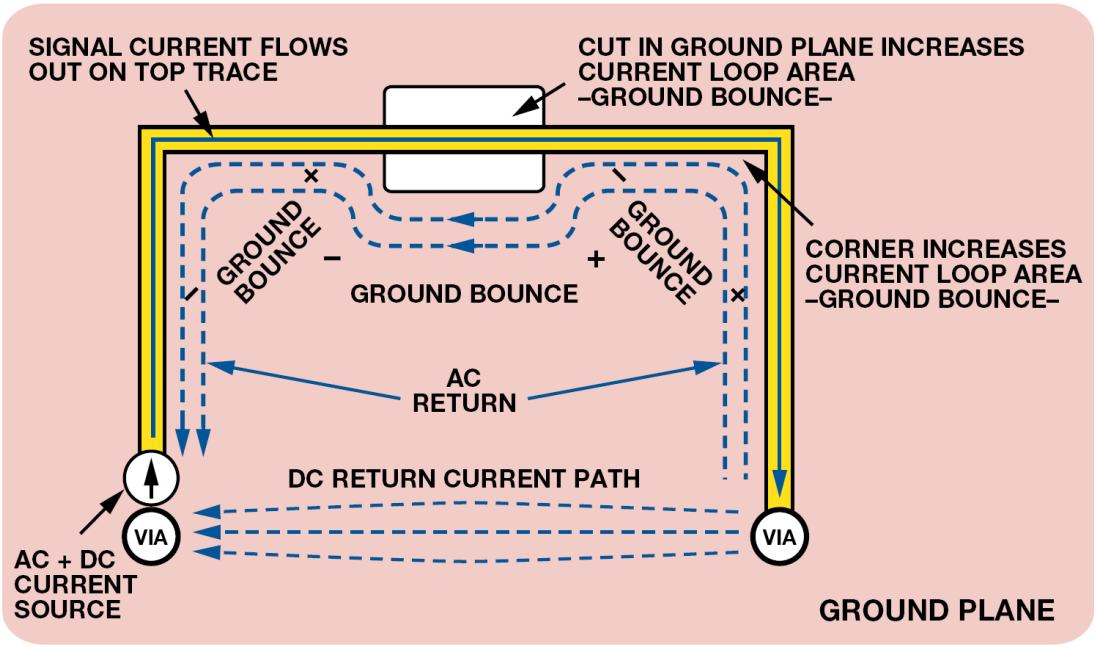
The output voltage is sensed and routed to the feedback network using a separate trace on the bottom layer of the board.

Details of ADP1864 Double-Sided Board Layout



This figure shows the top and bottom layers of the PCB in order to see the feedback connection, and the PGND to AGND connection.

Return Current Takes the Path of Least Impedance



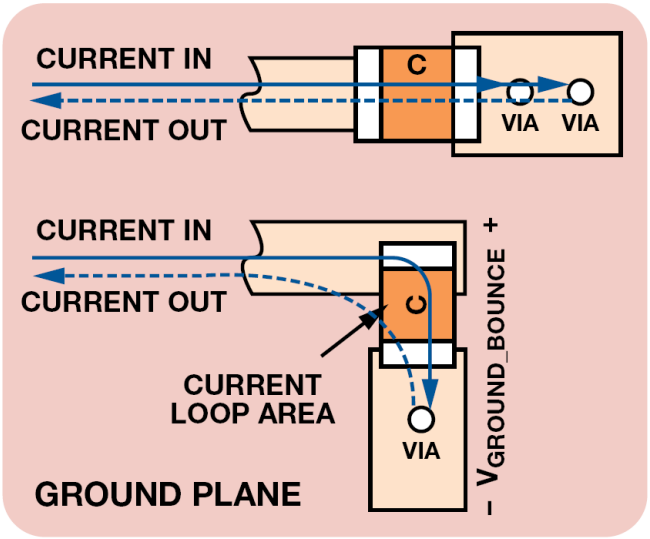
Interruptions to the ground plane under conductors carrying current can increase loop area by diverting the return current, thus increasing loop size and facilitating ground bounce. This is especially troublesome in a double-sided board.

The same thing applies for signal traces where the increased inductance and loop area can lead to increased inductive coupling of unwanted interference signals. This obviously should be avoided.

Note that the dc path is more direct than the ac path. As frequency increases the path of *least resistance* becomes the path of *least impedance*. At high frequencies return path currents tend to concentrate under the forward path (remember that all signals are really loops) to reduce inductance and therefore impedance.

Multilayer boards are almost always used in modern high-density layouts, and the ground plane breaks are much less than with simple double-sided boards.

Effects of Component Orientation



GOOD LAYOUT—
CAPACITOR IN LINE
WITH CURRENT FLOW
—SMALL LOOP AREA

BAD LAYOUT—
CAPACITOR AT RIGHT
ANGLE TO CURRENT FLOW

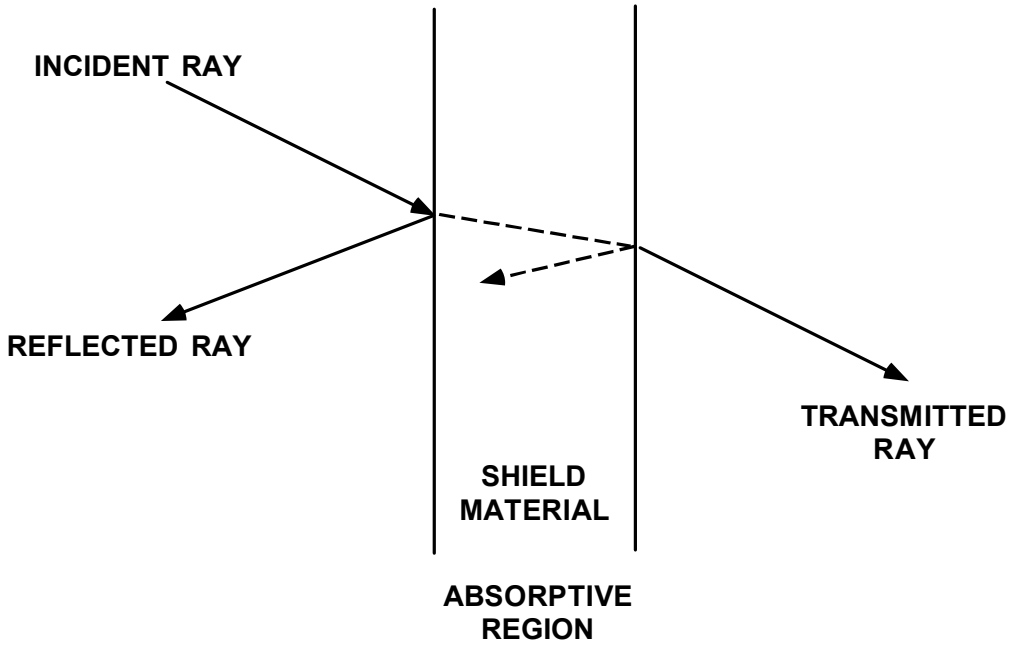
BOTTOM LAYOUT CAUSES
GROUND BOUNCE

In this example, a two-layer PCB is constructed so that a bypass capacitor is attached at right angles or in-line to a top-layer supply line. In the example, the ground plane is solid and uncut. Power trace current (on the top side) flows through the capacitor, down the via, and out the ground plane.

Because ac current always takes the path of least impedance, ground return current on the lower example rounds the corner on its way back to the source. So the current's magnetic field and the associated loop area change when either magnitude or frequency of the current changes, hence the changing flux. The tendency of current to flow along the easiest path means that even a solid-sheet ground plane can have ground bounce—irrespective of its conductivity.

Shielding

Reflection and Absorption Are the Two Principal Shielding Mechanisms



Applying the concepts of shielding requires an understanding of the source of the interference, the environment surrounding the source, and the distance between the source and point of observation (the receptor or victim). If the circuit is operating close to the source (in the near-, or induction-field), then the field characteristics are determined by the source. If the circuit is remotely located (in the far-, or radiation-field), then the field characteristics are determined by the transmission medium.

A circuit operates in a near-field if its distance from the source of the interference is less than the wavelength (λ) of the interference divided by 2π, or $\pi/2\lambda$. If the distance between the circuit and the source of the interference is larger than this quantity, then the circuit operates in the far field. For instance, the interference caused by a 1 ns pulse edge has an upper bandwidth of approximately 350 MHz. The wavelength of a 350 MHz signal is approximately 34 inches (the speed of light is approximately 12"/ns). Dividing the wavelength by 2π yields a distance of approximately 5 inches, the boundary between near- and far-field. If a circuit is within 5 inches of a 350 MHz interference source, then the circuit operates in the near-field of the interference. If the distance is greater than 5 inches, the circuit operates in the far-field of the interference.

Conductivity and Permeability for Various Shielding Materials

MATERIAL	RELATIVE CONDUCTIVITY	RELATIVE PERMEABILITY
Copper	1	1
Aluminum	1	0.61
Steel	0.1	1,000
Mu-Metal	0.03	20,000

Conductivity: Ability to Conduct Electricity

Permeability: Ability to Absorb Magnetic Energy

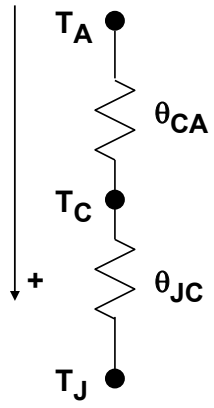
For electric fields the primary shielding mechanism is reflection loss, and at high frequencies, the mechanism is absorption loss. For these types of interference, high conductivity materials, such as copper or aluminum, provide adequate shielding.

At low frequencies, both reflection and absorption loss to magnetic fields is low; thus, it is very difficult to shield circuits from low-frequency magnetic fields. In these applications, high-permeability materials that exhibit low reluctance provide the best protection. These low-reluctance materials provide a magnetic shunt path that diverts the magnetic field away from the protected circuit.

Thermal Design

Thermal Design Basics

- θ = Thermal Resistance (°C/W)
- $\Delta T = P \times \theta$
- θ_{JA} = Junction-to-Ambient Thermal Resistance
- θ_{JC} = Junction-to-Case Thermal Resistance
- θ_{CA} = Case-to-Ambient Thermal Resistance
- $\theta_{JA} = \theta_{JC} + \theta_{CA}$
- $T_J = T_A + (P \times \theta_{JA})$, P = Total Device Power Dissipation
- $T_{J\,(Max)}$ = Data sheet parameter. Varies device to device.



The basic concept of thermal design is to keep the junction temperature of the chip below its rated maximum junction temperature. The maximum rated junction temperature varies from device to device, but is generally between 125°C and 150°C.

The change in temperature is analogous to a resistance. The amount of power times the thermal resistance equals the temperature rise. The power is analogous to a current, and the thermal resistance is analogous to a resistance (obviously).

The thermal resistance is typically divided up into two components. The first is the thermal resistance from the junction to the case (θ_{JC}) and the thermal resistance from the case to the ambient (θ_{CA}). The θ_{JC} is determined primarily by the package. It is typically higher for smaller packages. The θ_{CA} can be reduced by the addition of heatsinks. The θ_{JA} number is generally given in still air (i.e. no fans). Adding airflow will further reduce the thermal resistance somewhat.

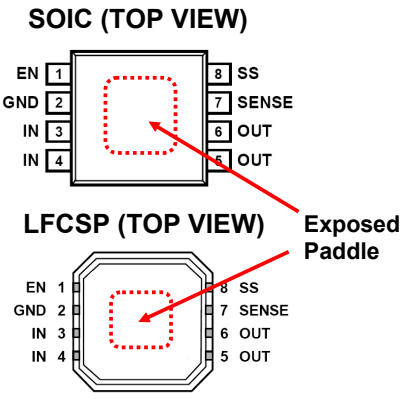
θ_{JA} is very dependent on PCB area, copper volume, and the dissipation of components around it. It is not incredibly useful because the data sheet will specify this number at one or possibly two points, which are very unlikely to be exactly like many other applications. While using θ_{JC} to predict die temperature is not perfect, it is significantly better than using θ_{JA}. One simply measures the temperature of the component using thermocouples or a thermal imaging device, adds that to $\theta_{JC} \times P$ (estimated power dissipation of the IC) to find the junction temperature or $\theta_{JC} \times P + T_C = T_J$, where T_C is the case temperature. Note that even on a small IC, there can be “hot spots,” so it is advisable to "hunt" around that IC using thermocouples for the “hot spot.” A thermal imaging device should clearly define that spot.

ADI has an online tool to help with this calculation:

www.analog.com/Analog_Root/static/techSupport/designTools/interactiveTools/powertemp/powertemp.html

This tool can be accessed form the Design Center tab on the ADI website.

ADP1706 1A LDO Power Dissipation



Both packages have an exposed paddle on the bottom which should be soldered to the copper ground plane

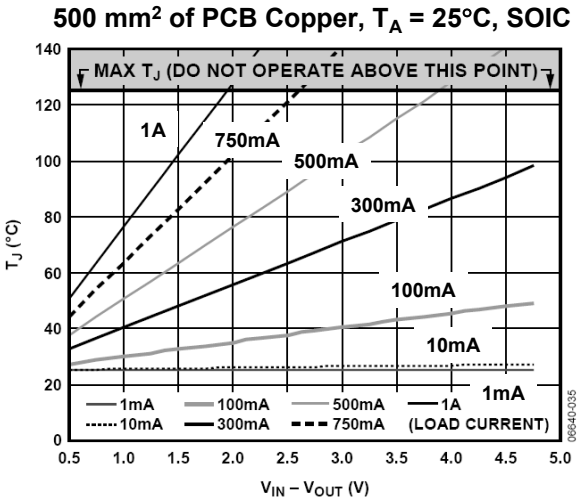


Table 5. Typical θ_{JA} Values

Copper Size (mm²)	θ_{JA} (°C/W), SOIC	θ_{JA} (°C/W), LFCSP
0[1]	57.6	65.9
50	53.1	62.3
100	52.3	61.2
300	51.3	59.7
500	51.3	59.4

[1] Device soldered to minimum size pin traces.

In some packages there is a lug or paddle that is meant to be soldered to the PCB. This is a means of decreasing the thermal resistance from the die to the PCB. The lug or paddle is typically the pad to which the chip is bonded and is in direct thermal contact with the die. The larger the copper land area that this lug is soldered to, the better the PCB behaves as a heatsink. Increasing copper thickness and area also increases the ability of the PCB to extract heat out of the IC.

This figure shows the thermal derating curves for the ADP1706, a 1 A LDO regulator. It is available in two packages, both of which have an exposed paddle on the bottom which should be soldered to a copper ground plane (1 ounce copper thickness). The data in the plot assumes a 500 mm² copper area and an ambient temperature of 25°C. The plot shows the junction temperature as a function of the difference between the input and output voltage for various load currents. The maximum allowable junction temperature for this device is 125°C.

A good reference for dealing with exposed paddle packages can be found at *www.analog.com*:

Gary Griffin, "A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)," Application Note AN-772, Analog Devices, 2006.

Thermal Resistance of Popular Packages

PACKAGE	θ_{JA} (°C/W)	COMMENTS
3-lead SOT-23	300	
5-lead SOT-23	190	
6-lead SOT-23	165	
6-lead TSOT	186	ADP1864 SW Controller
8-lead SOIC	160	
16-lead QSOP	105	ADP1821 SW Controller
8-lead MSOP	75	ADP1715/ADP1716 LDOs (500mm^2 copper)
8-lead LFCSP (*EP)	60	ADP1706/ADP1707/ADP1708 LDOs (500mm^2 copper)
8-lead SOIC (*EP)	51	ADP1706/ADP1707/ADP1708 LDOs (500mm^2 copper)
16-lead LFCSP (*EP)	20-40	ADP2105/ADP2106/ADP2107 SW Regulators ADP1740/ADP1741 LDOs
SOT-223	65	ADP3338/ADP3339 LDOs (1 in^2 copper), θ_{JC} = 27°C/W
TO-220	35	(1 in^2 copper), θ_{JC} = 3°C/W
TO-263 (D2PAK)	35	(1 in^2 copper), θ_{JC} = 3°C/W

***EP = Exposed Paddle**

Above values are typical, consult product data sheet for exact value

Here are some example θ_{JA} numbers for some popular IC packages, especially those commonly used for power circuits.

It should be noted that there can be some variation in these numbers between different manufacturers depending upon the method of measurement, PCB mounting, etc.

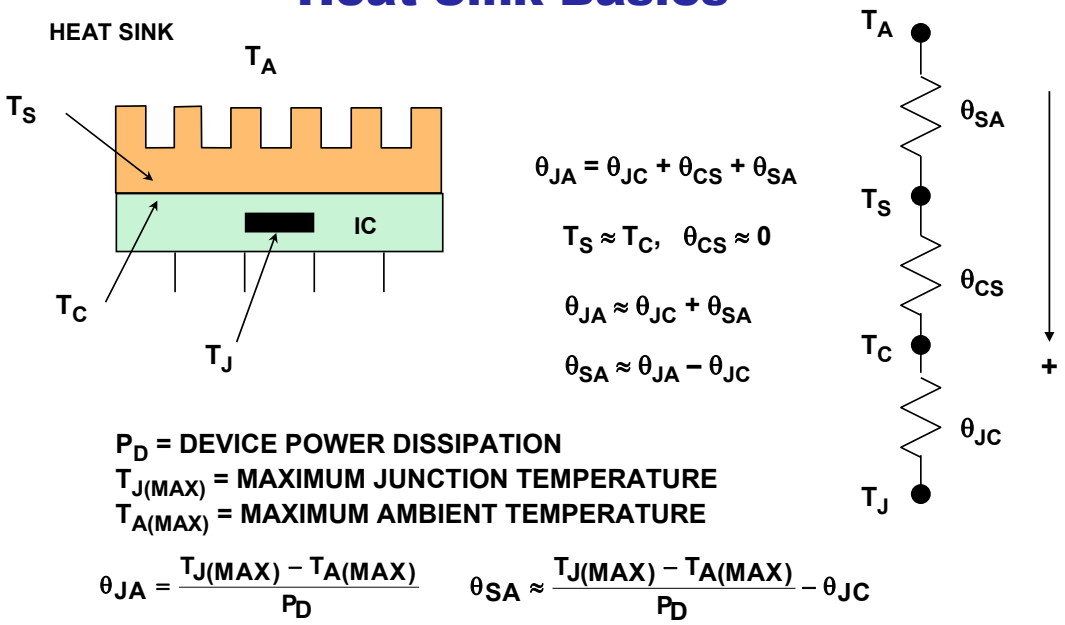
See also:

www.analog.com/Analog_Root/static/Packages/ThermalDataWP.pdf

This can also be accessed form the Package Thermal Characteristics tab on the heat sink design tool.

www.analog.com/Analog_Root/static/techSupport/designTools/interactiveTools/powertemp/powertemp.html

Heat Sink Basics



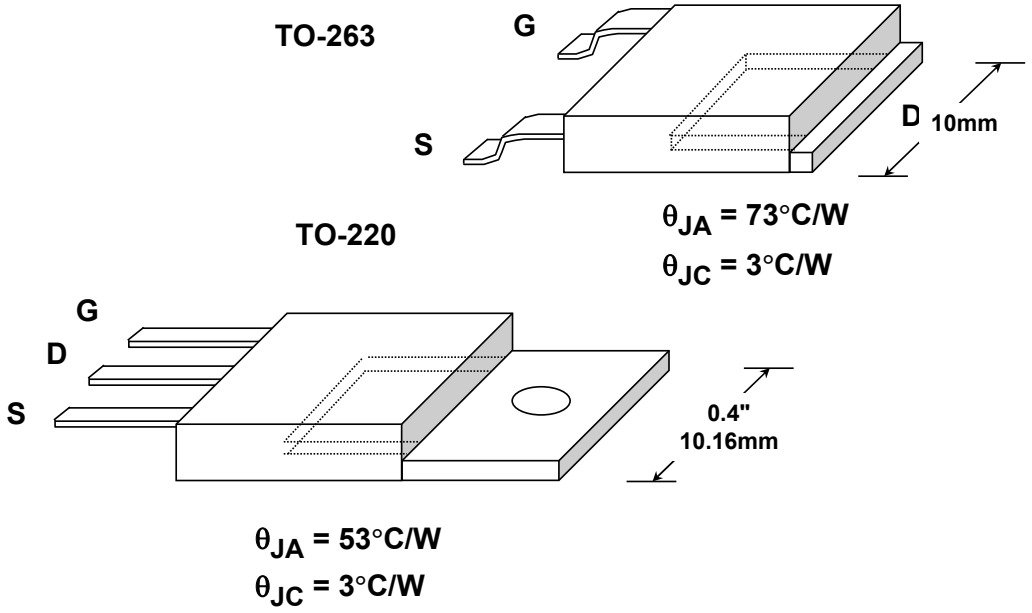
P_D = DEVICE POWER DISSIPATION
$T_{J(MAX)}$ = MAXIMUM JUNCTION TEMPERATURE
$T_{A(MAX)}$ = MAXIMUM AMBIENT TEMPERATURE

$$\theta_{JA} = \frac{T_{J(MAX)} - T_{A(MAX)}}{P_D} \qquad \theta_{SA} \approx \frac{T_{J(MAX)} - T_{A(MAX)}}{P_D} - \theta_{JC}$$

The fundamental purpose of heat sinks and airflow is to allow high power dissipation levels while maintaining safe junction temperatures. There are many tradeoffs which can be made between airflow and heat sink area, and this section examines some of them.

A thermal model of an IC and a heat sink is shown in this figure. The critical parameter is the junction temperature, T_J, which must be kept below 150ºC for most ICs. The model shows the various thermal resistances and temperatures at various parts of the system. T_A is the ambient temperature, T_S is the heat sink temperature, T_C is the IC case temperature, and T_J is the junction temperature. The heat sink is usually attached to the IC in such a manner as to minimize the difference between the IC case temperature and the heat sink temperature. This is accomplished by a variety of means, including thermal grease, machined surface contact area, etc. In any case, the thermal resistance between the heat sink and the IC case can usually be made less than 1ºC/W to 5°C/W.

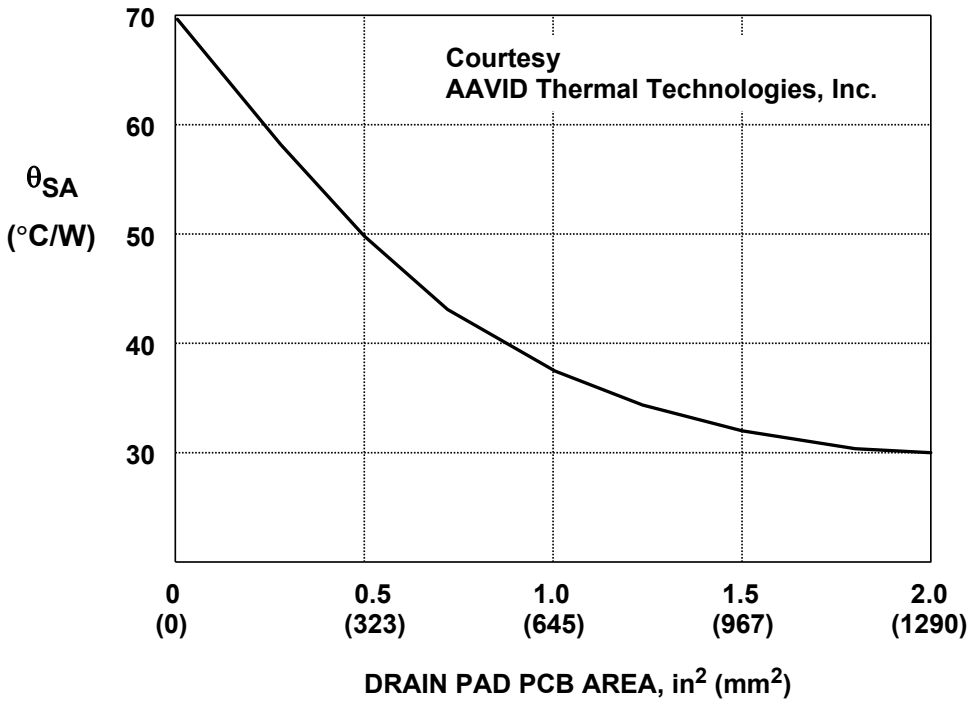
TO-220 and TO-263 (D^2PAK) Packages



This figure shows two standard packages which are capable of dissipating considerable power

Also note that the drain (D) connection for the TO-263 package is electrically connected to the slug. This means that electric isolation from the heatsink is required for safety.

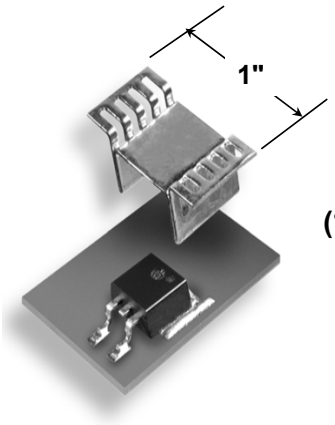
Thermal Resistance of TO-263 (D^2PAK) vs. Drain Pad Area—No Airflow



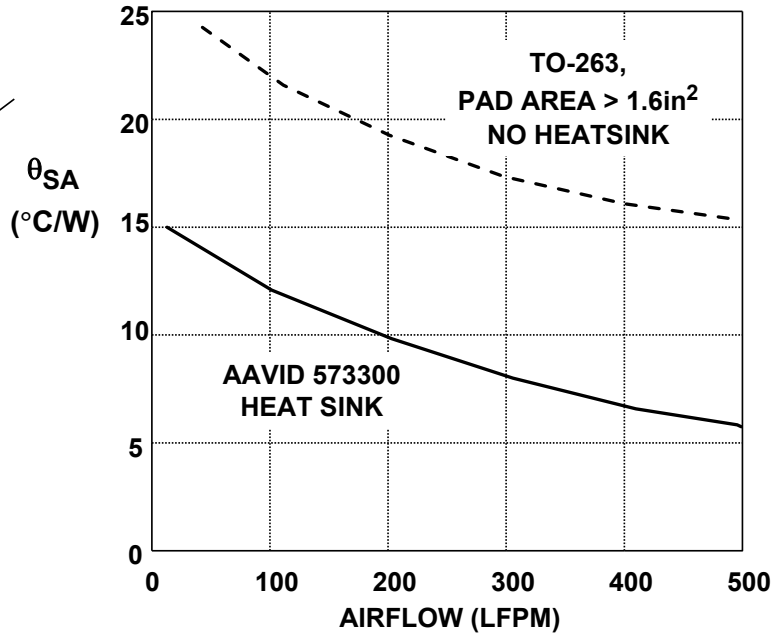
The thermal resistance of a TO-263 package soldered to a PCB land area. Obviously, a larger PCB land area will make a better heatsink. Copper is a fairly effective conductor of heat (as well as electricity). Again, this is in still air. Airflow will help some (see next page).

This figure shows the thermal resistance of the TO-263 package as a function of PC board drain pad area which is acting as the heat sink. Note that even with 2 square inches of pad area, the thermal resistance is still 30ºC/W.

Thermal Resistance of AAVID 573300 Surface Mount Heat Sink vs. Airflow



Courtesy
AAVID Thermal
Technologies, Inc.



The situation can be improved by the addition of a surface-mount heat sink as shown in this figure (AAVID part number 573300). This heat sink solders to two pads on the PC board which are extensions of the drain pad connecting area. The thermal resistance of this combination as a function of airflow is shown in this figure.

Note that with the addition of the surface-mount heat sink, the thermal resistance of the combination is reduced to approximately 10ºC/W with a reasonable amount of airflow (200 linear feet per minute). The curve also shows the thermal resistance with no heat sink as a function of airflow, clearly indicating that a heat sink definitely is effective for high power dissipation.

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9. Stephen H. Hall, *High-Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices*, Wiley-IEEE Press, 2000, ISBN-10: 0471360902, ISBN-13: 978-0471360902.

Notes: