

Practical Power Solutions

1. Point-of-Load Power
2. System Power Management and Portable Power
3. Power for Mixed Analog/Digital Systems
4. Hardware Design Techniques

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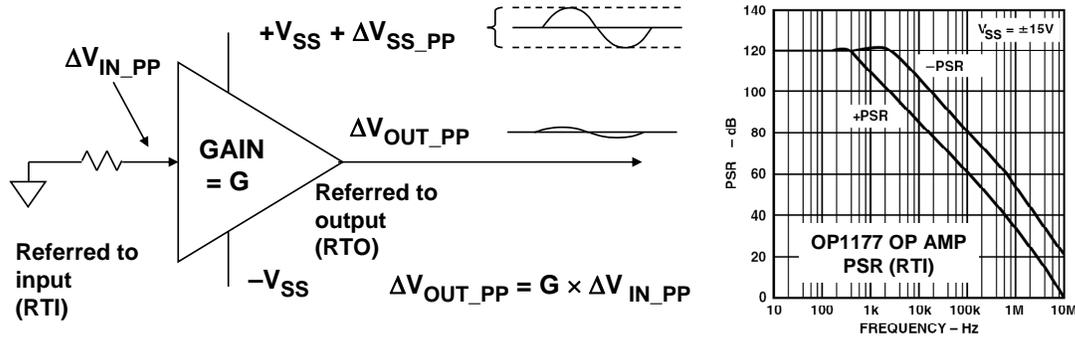
SECTION 3

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General Guidelines for Powering Analog Circuits

Power Supply Rejection (PSR) vs. Frequency Is a Key Specification



- ◆ $PSRR = \frac{\Delta V_{SS_PP}}{\Delta V_{OUT_PP}}$ We will use this convention which gives a positive value for PSR in dB
- ◆ $PSR (dB) = 20 \log_{10} PSRR$
- ◆ PSRR and PSR are often used interchangeably, and the value in dB can be + or -
- ◆ Dual supply devices have separate specifications for + and - supplies, +PSR, -PSR
- ◆ PSRR and PSR are often used interchangeably,

The ability of an electronic device to reject power supply ripple and noise is key to determining the ripple and noise allowable on its power inputs. Ripple and noise rejection ability is specified as the PSRR (Power Supply Rejection Ratio). We will use an op amp as an initial example.

If the supply of an op amp changes, its output should not, but it typically does. If a change of X volts in the supply produces an output voltage change of Y volts, then the PSRR on that supply (referred to the output, RTO) is X/Y. The dimensionless ratio is generally called the power supply rejection ratio (PSRR), and Power Supply Rejection (PSR) if it is expressed in dB. However, PSRR and PSR are almost always used interchangeably.

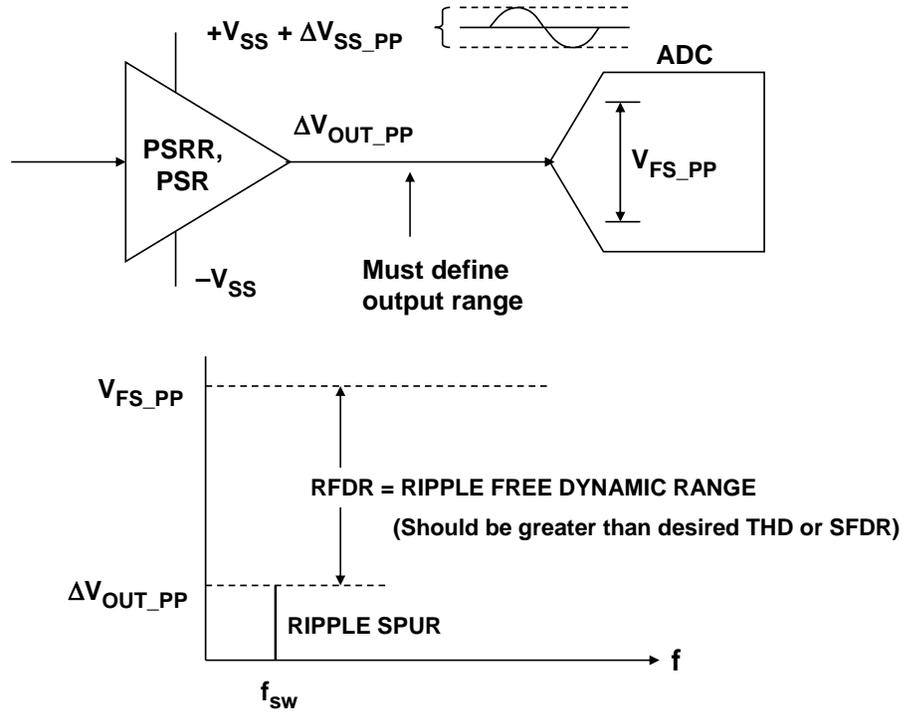
PSRR or PSR can be referred either to the output (RTO) or the input (RTI). The RTI value can be obtained by dividing the RTO value by the amplifier gain. In the case of the traditional op amp, this would be the noise gain. The data sheet should be read carefully, because PSR can be expressed either as an RTO or RTI value.

PSR can be expressed as a positive or negative value in dB, depending on whether the PSRR is defined as the power supply change divided by the output voltage change, or vice-versa. There is no accepted standard for this, and both conventions are in use.

If the amplifier has dual supplies, it is customary to express PSR separately for each.

It is extremely important to remember that PSR is very much a function of ripple or noise frequency as shown in the plot for the OP1177 op amp. In most cases, the roll-off follows that of the open-loop gain, and the slope is approximately 6 dB per octave (20 dB per decade).

Definition of Ripple Free Dynamic Range

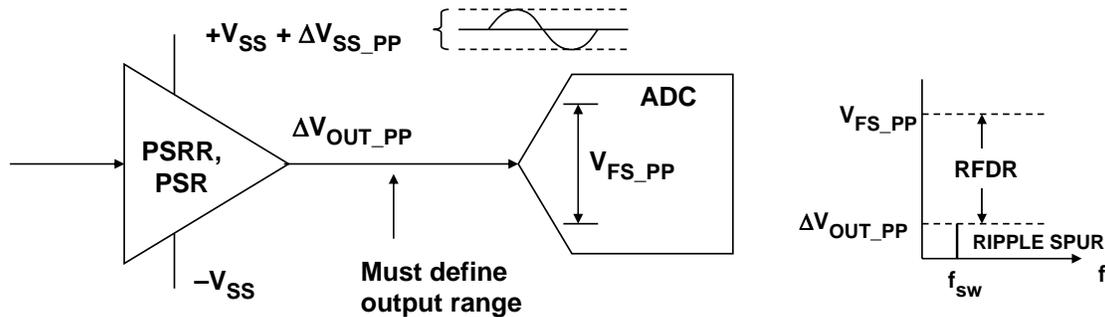


The amplifier output ripple voltage is not very useful unless it is compared to the dynamic range of the signal. If the amplifier drives an ADC, then the full-scale input voltage, V_{FS_PP} , or the ADC defines the signal range. If the amplifier drives another amplifier, then the signal range is defined by the output range of the second amplifier divided by the gain of the second amplifier.

The Ripple Free Dynamic Range, RFDR, is defined as the ratio of the full-scale signal range to the output ripple spur, expressed in dB.

Many systems have requirements on harmonic distortion, or spurious free dynamic range (SFDR). It is therefore important that the ripple-free-dynamic-range be greater than the desired harmonic distortion or SFDR.

Determine the Device's Sensitivity to Ripple by Calculating the RFDR at the Switching Frequency



$$\blacklozenge \text{ PSRR} = \frac{\Delta V_{SS_PP}}{\Delta V_{OUT_PP}} \quad \blacklozenge \text{ PSR (dB)} = 20 \log_{10} \text{ PSRR}$$

$$\blacklozenge \Delta V_{OUT_PP} = \Delta V_{SS_PP} / \text{PSRR}$$

$$\blacklozenge \text{ "RIPPLE FREE" DYNAMIC RANGE (RFDR)} = 20 \log \frac{V_{FS_PP}}{\Delta V_{OUT_PP}}$$

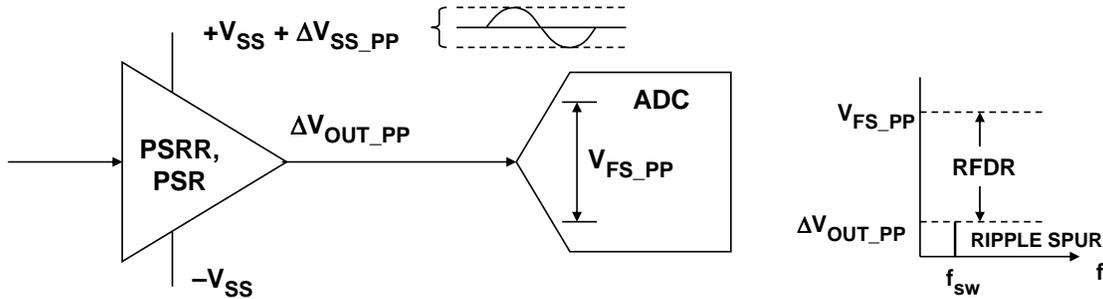
$$\blacklozenge \text{ RFDR} = \text{PSR} + 20 \log \frac{V_{FS_PP}}{\Delta V_{SS_PP}}$$

The PSR specification can be used to calculate the amplifier output ripple, and the output ripple amplitude can then be compared to the signal range. The signal range must be specified in order for the calculated output ripple to be meaningful.

In most cases, an ADC will determine the signal range. In some cases it is determined by the compression point of an amplifier further downstream in the signal path.

Once the dynamic range is defined, the ripple-free-dynamic-range is easily calculated as shown in the figure.

Example Calculation of Maximum Allowable Power Supply Ripple Voltage



$$\diamond \Delta V_{SS_PP} \leq V_{FS_PP} \times 10^{-\left[\frac{RFDR - PSR}{20}\right]}$$

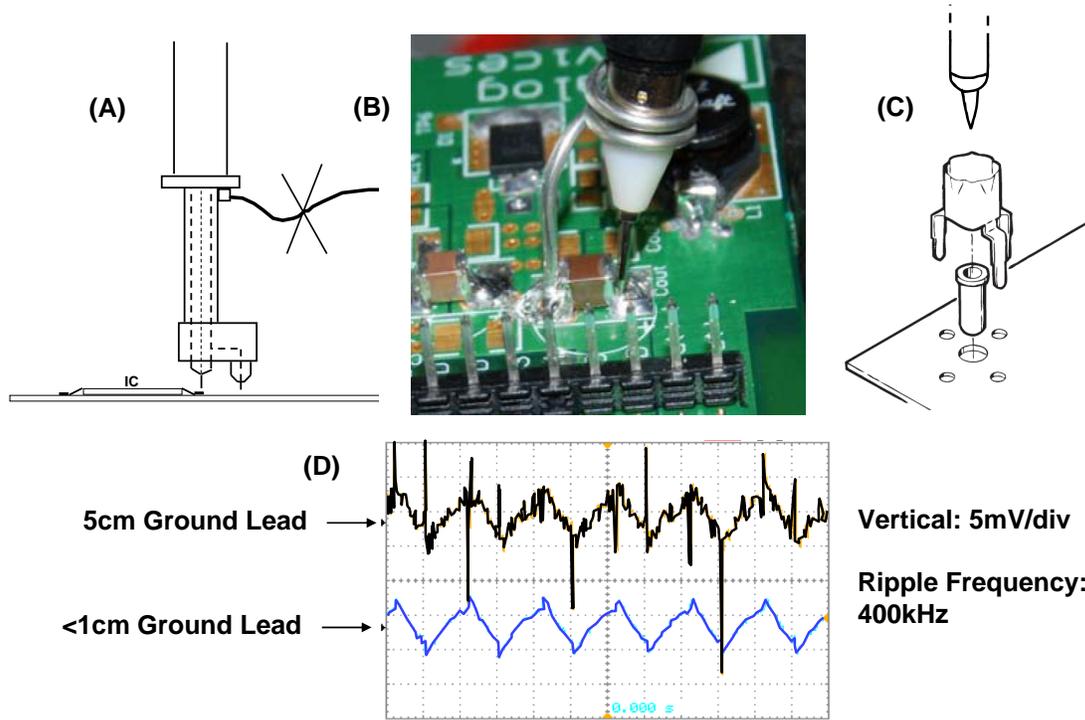
◆ Example: $V_{FS_PP} = 2.0V$, $RFDR = 100dB$, $PSR = 60dB$

Then $\Delta V_{SS_PP} \leq 20mV$

The equation for RFDR in the previous figure can be rearranged and solved for the maximum allowable power supply ripple, ΔV_{SS_PP} , for a required RFDR and a given PSR.

The example shows that for a full-scale range of $V_{FS_PP} = 2 V$, a ripple free dynamic range of 100 dB, and a PSR of 60 dB, the peak-to-peak power supply ripple must be less than 20 mV.

Measuring Ripple



Simply obtaining an accurate measurement of power supply ripple can be a difficult task, especially due to switching noise.

Power supply ripple must be measured directly at the IC power pin. This can be difficult to do with an oscilloscope, because a standard probe ground clip lead of a few cm creates an effective antenna which picks up magnetic switching noise from the power supply as well as noise from other sources and translates it into voltage spikes as shown in (D).

The "bayonet" clip used in (A) reduces the ground probe length to less than 1 cm. A wire loop soldered to ground as in (B) is also an effective way to maintain a short connection to the ground plane.

The ideal method is to use a special probe tip adapter which solders directly to the PC board as shown in (C), but this technique is generally reserved for prototypes or test boards where frequent measurements are required.

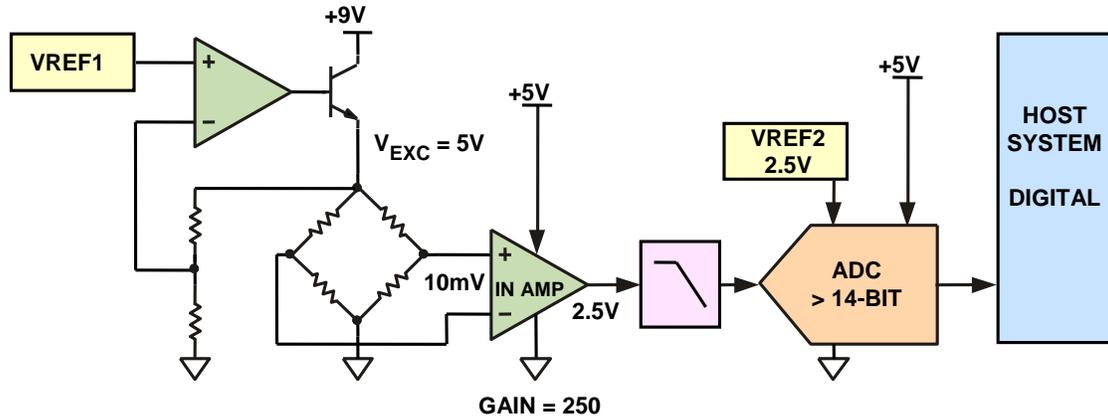
The scope trace capture in (D) shows the effect of reducing the ground lead from 5 cm to less than 1 cm. Note the dramatic reduction in the 400 kHz "spikes" which ride on the ripple voltage.

Powering Amplifiers

www.analog.com/amplifiers

In this section, we examine the PSR of various amplifiers to determine their sensitivity to power supply ripple.

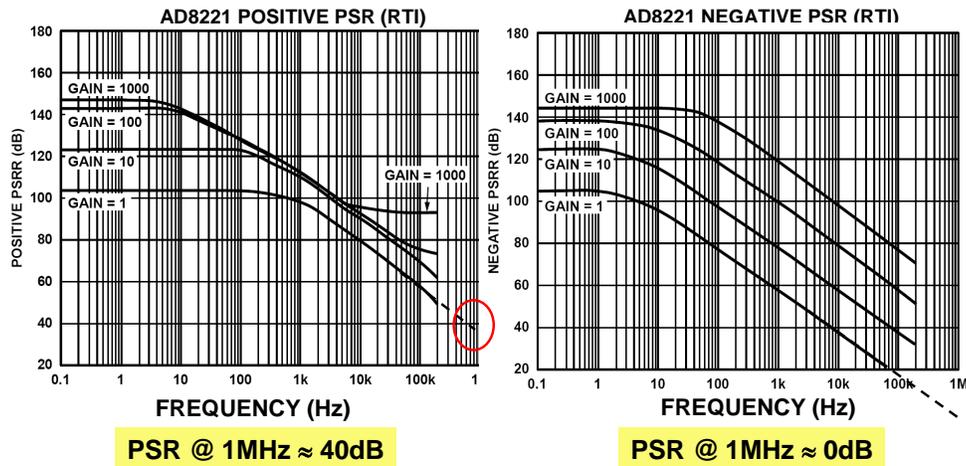
Typical Weigh Scale Application of Instrumentation Amplifier



The instrumentation amplifier (in-amp) is a fundamental building block in practically all industrial measurement systems. This shows a typical application in a weigh scale signal processor.

The in-amp is set for a gain of 250 to amplify the full-scale load cell bridge output of 10 mV to "fill" the 2.5 V input range of the ADC.

PSR for Representative In-Amps



OTHER POPULAR IN-AMPS:

AD623 SINGLE SUPPLY PSR @ 1MHz \approx 0dB, G = 1

AD627 SINGLE SUPPLY PSR @ 1MHz \approx 0dB, G = 5

This shows the PSR of the industry-standard AD8221 in-amp as well as two newer single-supply devices. Note that the graph shows the PSR reflected to the input (RTI).

The PSR for the positive supply at 1 MHz is extrapolated to be approximately 40 dB, and the PSR of the negative supply is approximately 0 dB.

This poor PSR performance of in-amps is typical, and must be dealt with in all application circuits which use them. The following pages will discuss this critical issue in more detail.

Instrumentation Amplifier Characteristics

- ◆ Instrumentation amplifiers are optimized for CMR and PSR at AC power line frequencies of 50Hz and 60Hz
- ◆ Gain, CMR, PSR falls off at 6dB/Octave above 100Hz
- ◆ Must assume 0dB PSR at switching frequencies above 500kHz
- ◆ Out-of-band signals on power or input will be rectified by internal junctions and create unwanted DC offsets (RFI Rectification)
- ◆ Must have excellent localized decoupling to filter noise and ripple frequencies if power supply is not clean

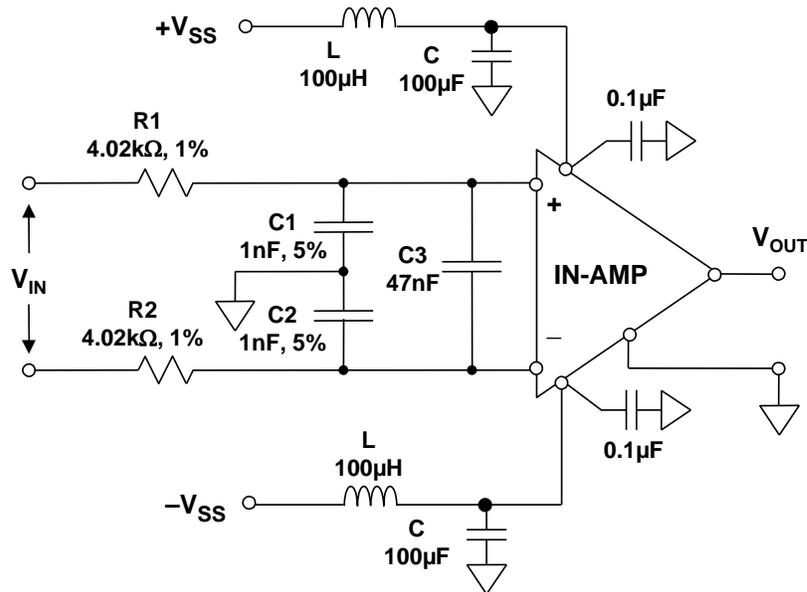
The in-amp is optimized for common-mode rejection (CMR) and PSR at ac power line frequencies of 50 Hz and 60 Hz.

The gain, CMR, and PSR generally drop off at 6 dB/octave above about 100 Hz.

High frequency ripple or noise outside this bandwidth which appears on the power supply or the input is rectified by internal junctions and creates unwanted dc offsets at the output. This process is called "RFI rectification."

For this reason, excellent localized decoupling must be applied to the in-amp power supply pins. The in-amp inputs usually require additional common-mode input filtering to prevent RFI rectification.

In-Amp Input and Power Supply Filtering



$$\text{DIFFERENTIAL FILTER BANDWIDTH} = \frac{1}{2\pi (R1 + R2) \left[\frac{C1 \cdot C2}{C1 + C2} + C3 \right]} = 417\text{Hz}$$

This shows a typical filtering network for the power supply and signal input of an in-amp. Let's look at the power supply networks first.

The input LC filter is designed to remove the ripple component of the power supply noise. The 100 µF electrolytic capacitors should be located within a couple of inches of the in-amp power pins. The ESR of the capacitors should be low, depending on the amount of ripple attenuation required. There is a detailed discussion later in this section regarding the design of the LC network.

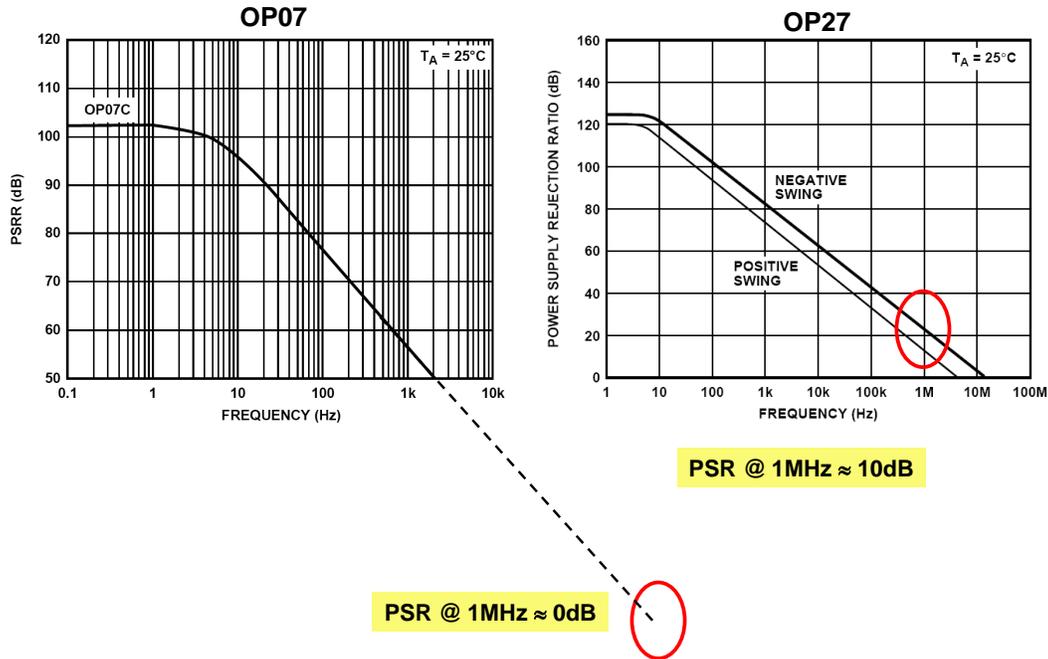
The 0.1 µF ceramic capacitors are for high frequency decoupling. They should be located as close to the actual power pins as is physically possible, and the connection to the power pin and the ground plane should be as short as possible.

The input filter network is designed to reduce RFI rectification by rejecting common-mode signals outside the signal bandwidth.

The R1/C1 and R2/C2 networks filter the common-mode noise. The time constants should be well matched to prevent common-mode-to-differential mode conversion. For this reason, the resistors (R1, R2) should be 1%, and the capacitors (C1, C2) 5% or better. With the values shown, the common-mode filter bandwidth due to R1/C1 is approximately 40 kHz.

Because of the potential slight mismatch between the two time constants, C3 is added as a differential-mode filter. The resulting differential filter bandwidth is approximately 417 Hz.

Industry-Standard OP07 and OP27 Precision Bipolar Op Amps PSR (RTI)

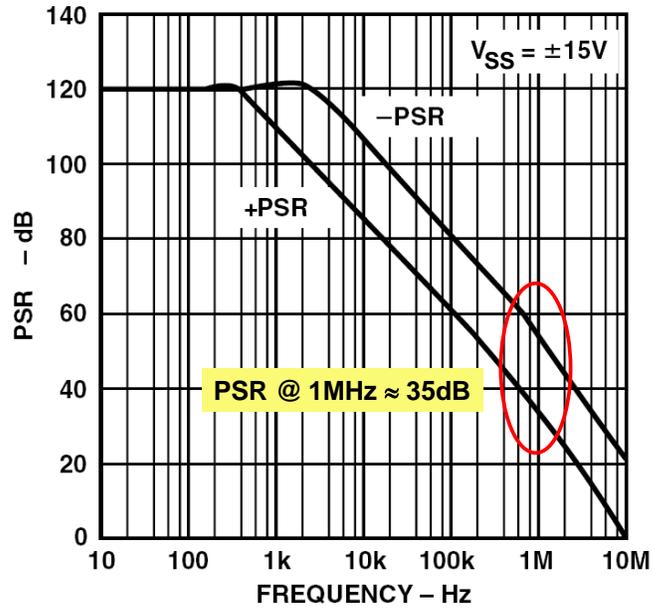


We now look at a couple of industry-standard precision bipolar op amps, the OP07 and the OP27. The OP07, designed by George Erdi and first introduced by PMI in 1975, became the "741" of precision op amps. It is still widely second-sourced today. The OP07 uses a trim technique called "zener zapping" to obtain offset voltages as low as 25 μ V and drift rates of 0.6 μ V/°C. The unity gain bandwidth product of the OP07 is about 0.6 MHz.

Both the OP07 and OP27 use input bias current cancellation to achieve a low input bias current of less than ± 10 nA.

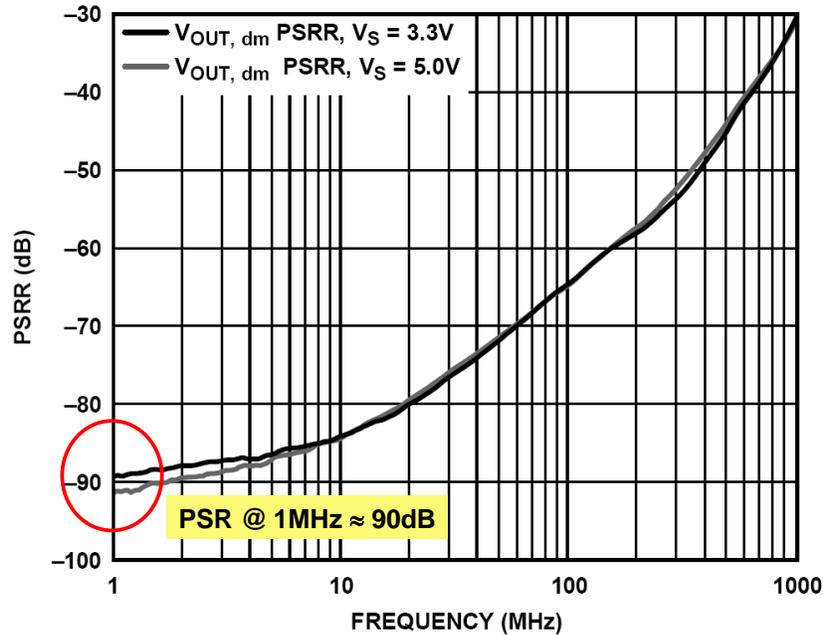
However, from a PSR standpoint these parts fall in about the same category as the in-amps previously discussed.

OP1177 Modern Precision Bipolar Op Amp PSR (RTI)



The OP1177 is a modern version of a precision bipolar op amp and has a unity gain-bandwidth product of 1.3 MHz. It has approximately 25 dB better PSR than the OP07 or OP27.

ADA4937-1, 1.9GHz, Low Distortion, 16-Bit, SiGe Differential ADC Driver (RTO)



The trend in most high performance ADCs is to use differential inputs and differential techniques throughout the circuit as well as the digital outputs.

The differential input drivers for these converters have both high bandwidth and relatively good PSR as shown here for the ADA4937-1 differential driver.

The differential wideband nature of these parts gives them excellent CMR at high frequencies which helps the PSR.

Amplifier PSR Summary

- 
- BETTER
PSR
- ◆ **Instrumentation Amplifiers**
 - Very low, 0dB to 10dB
 - Require RFI filtering on input and power supplies
 - ◆ **CMOS Auto-Zero Precision Op Amps**
 - Very low, \approx 10dB
 - ◆ **CMOS General Purpose Op Amps**
 - Very low, \approx 5dB
 - ◆ **Precision Low Frequency Bipolar Op Amps**
 - Very low, \approx 0dB to 10dB
 - ◆ **High Frequency Single-Ended Op Amps**
 - Good, \approx 35dB to 60dB
 - ◆ **Precision Differential Amplifiers**
 - Very good, \approx 45dB to 60dB
 - ◆ **High Frequency Differential Amplifiers**
 - Very good, \approx 55dB to 90dB

This summarizes the PSR of typical amplifiers.

Within a particular family, amplifiers with higher loop gain and bandwidth generally have better PSR.

In most cases, the higher speed amplifiers typically have better PSR, and the differential amplifiers have the highest.

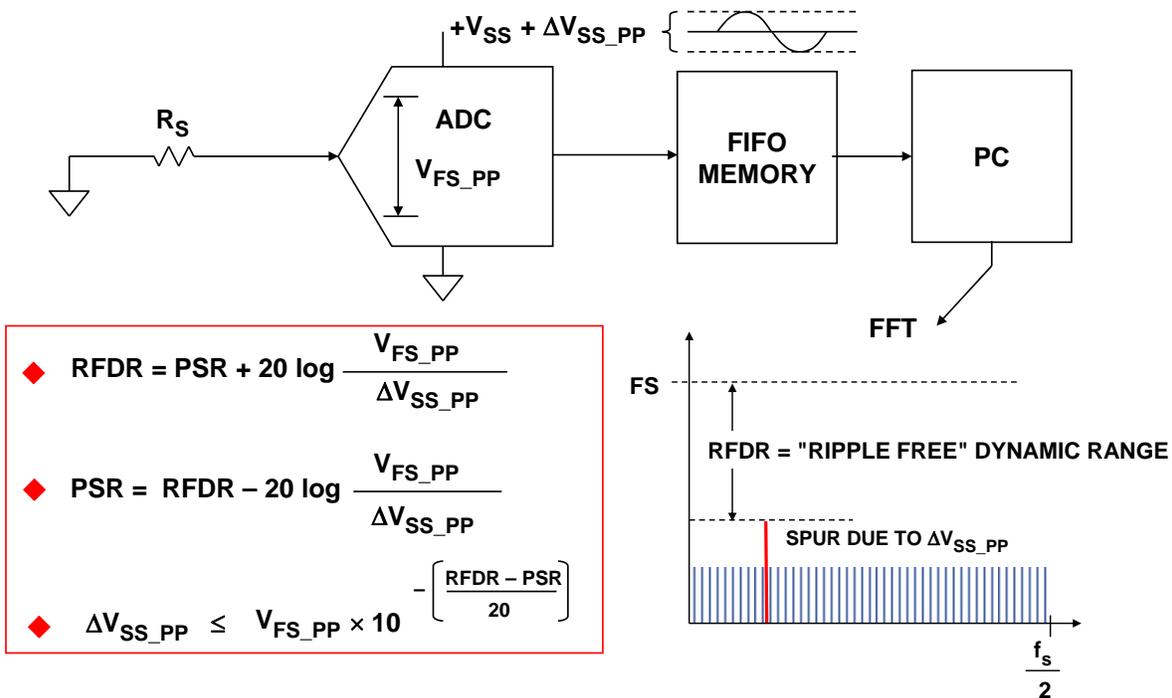
The bottom line is that while there seem to be some general trends, you must always consult the individual amplifier data sheet for specific PSR numbers.

The PSR at the maximum power supply switching frequency is a good measure of the sensitivity of amplifiers to ripple and noise.

Powering ADCs

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Defining the PSR of an ADC in Terms of its Spectral Output



Defining the PSR for an ADC is somewhat more difficult than for an op amp. Because most ADCs are used in signal processing applications, the effects of power supply ripple on the output frequency spectrum are more important than the effects on static parameters such as offset or gain.

This figure shows a standard method for measuring the PSR of an ADC. The input to the ADC is grounded through a resistor, and the ripple free dynamic range (RFDR) is measured using standard FFT techniques. In the figure, the spur of interest is the spur that occurs at the power supply switching frequency.

The next step is to measure the peak-to-peak ripple on the ADC power supply pin, ΔV_{SS_PP} . The PSR is then calculated by the equation:

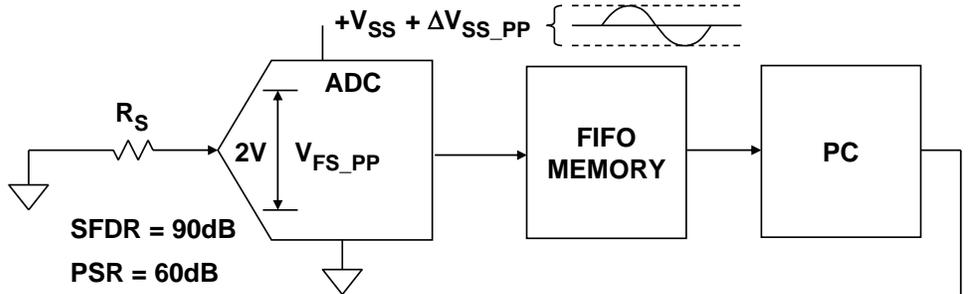
$$PSR = RFDR - 20 \log \frac{V_{FS_PP}}{\Delta V_{SS_PP}}$$

The second term in the equation normalizes the PSR with respect to the ADC full-scale input range.

If the ADC PSR specification and the RFDR requirement are known, the equation can be re-arranged to solve for the maximum allowable peak-to-peak ripple voltage:

$$\Delta V_{SS_PP} \leq V_{FS_PP} \times 10^{-\left(\frac{RFDR - PSR}{20}\right)}$$

Example Calculation of Maximum Allowable Power Supply Ripple

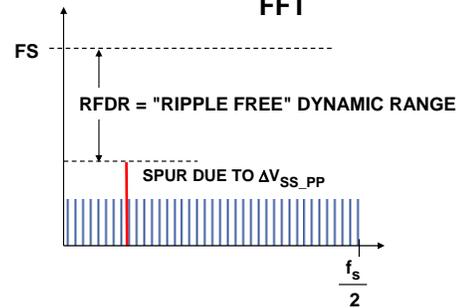


- ◆ The ADC Spurious Free Dynamic Range (SFDR) is 90dB
- ◆ The Ripple Free Dynamic Range (RFDR) should be at least 100dB
- ◆ The ADC PSR @ switching frequency is 60dB
- ◆ The ADC full scale voltage is $V_{FS_PP} = 2V$

$$\Delta V_{SS_PP} \leq V_{FS_PP} \times 10^{-\left[\frac{RFDR - PSR}{20}\right]}$$

- ◆ Substitute in above equation, solve for ΔV_{SS_PP}

$$\Delta V_{SS_PP} \leq 20mV$$



This example shows how the maximum allowable power supply ripple is determined based on the ADC specifications and desired frequency-domain performance.

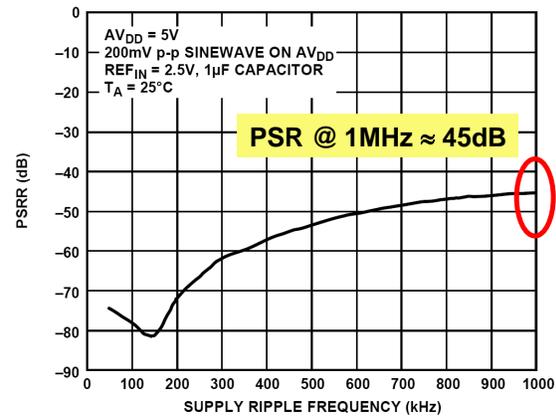
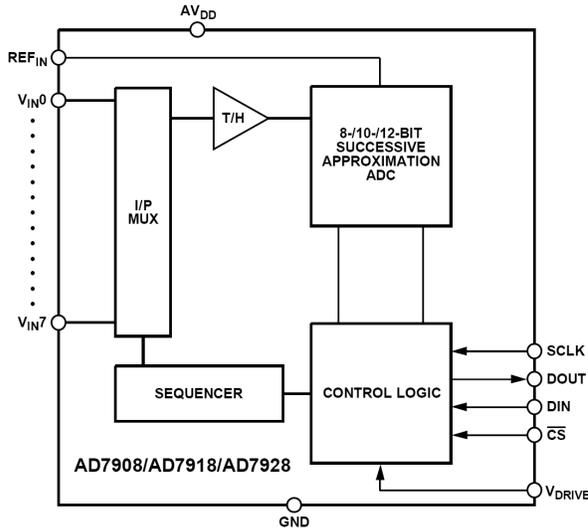
This ADC has an SFDR of 90 dB. The RFDR should be greater than this by at least 10 dB, so the RFDR requirement is 100 dB.

The PSR at the switching frequency is obtained from the ADC data sheet and is 60 dB (at the switching frequency).

The full-scale input range of the ADC is 2 V peak-to-peak.

The equation is solved for the maximum allowable ripple voltage, which in this case is 20 mV.

Multichannel Data Acquisition System on a Chip

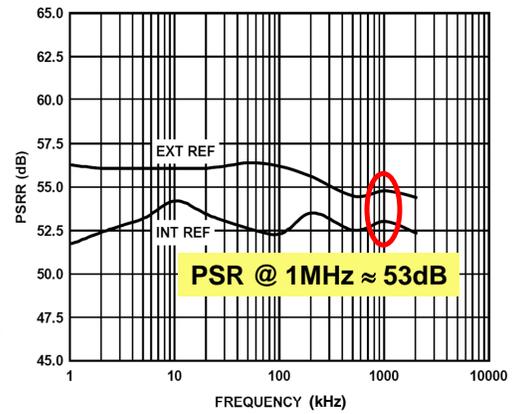
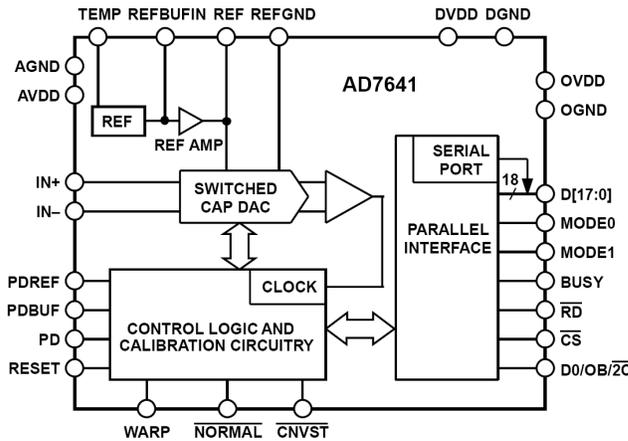


Now let's look at the PSR of several popular families of ADCs. There is little consistency between manufacturers regarding this specification, but the numbers presented here will give an idea of what to expect in an actual design.

This shows the PSR of a complete data acquisition system on a chip, the AD7908 (8-bit), AD7918 (10-bit), and AD7928 (12-bit) family. The architecture is typical of such systems and consists of an 8-channel input multiplexer, sample-and-hold, and a successive approximation (SAR) ADC.

The PSR of the device at 1 MHz is approximately 45 dB. This assumes an external 2.5 V reference with a 1 μF decoupling capacitor on the REF_{IN} pin.

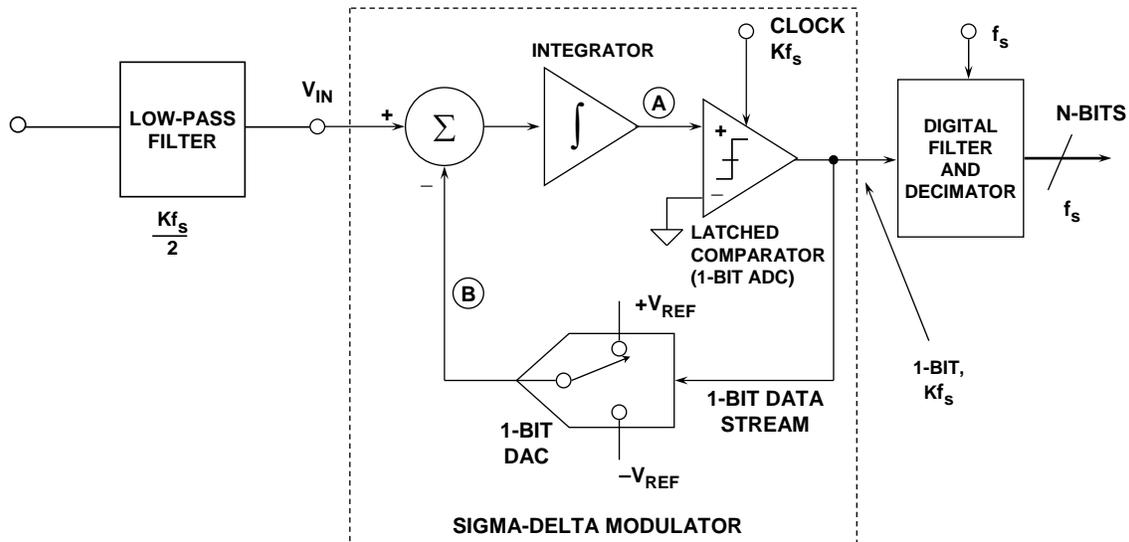
AD7641 18-Bit, 2 MSPS, PuLSAR® ADC



The PuLSAR family of high performance successive approximation (SAR) ADCs all use differential techniques throughout the design, so the PSR is maintained across a fairly wide range of ripple frequencies.

This shows the AD7641 18-bit, 2 MSPS ADC PSR as approximately 53 dB at 1 MHz using the internal reference. Slightly better PSR can be obtained using an external reference.

Integrator and Digital Filter Reduce the Effects of Power Supply Ripple in Σ - Δ ADCs



Sigma-delta ADCs use a combination of oversampling, quantization noise shaping, and digital filtering in order to achieve up to 24 bits of resolution at sampling rates of up to 1 kSPS. These high resolution ADCs have virtually replaced the dual-slope type.

This is a block diagram of a sigma-delta ADC which shows the key functional blocks. The averaging nature of the sigma-delta modulator and the digital filter make this type of converter relatively insensitive to power supply ripple. DC power supply rejection as well as 50 Hz or 60 Hz rejection is typically 70 dB to 90 dB, but data sheets rarely specify the ac PSR for these devices.

Sigma-Delta Power Considerations

- ◆ Typical throughput rates are less than a few kSPS for high resolutions (18+ bits)
- ◆ DC PSR is typically 70dB to 90dB
- ◆ AC PSR is not usually specified except at 50Hz and 60Hz power line frequencies
- ◆ Internal digital filter removes most ripple frequency components.
- ◆ Don't depend on the averaging effect of the digital filter to remove all the ripple components. Aliasing can still occur and put the ripple frequency into the signal bandwidth
- ◆ Broadband and ripple noise should be minimized with good localized decoupling of power pins at the IC, especially important for 20+ bit devices
- ◆ Consider using localized low power LDOs or references as power sources for 16+ bit ADCs in measurement or audio applications

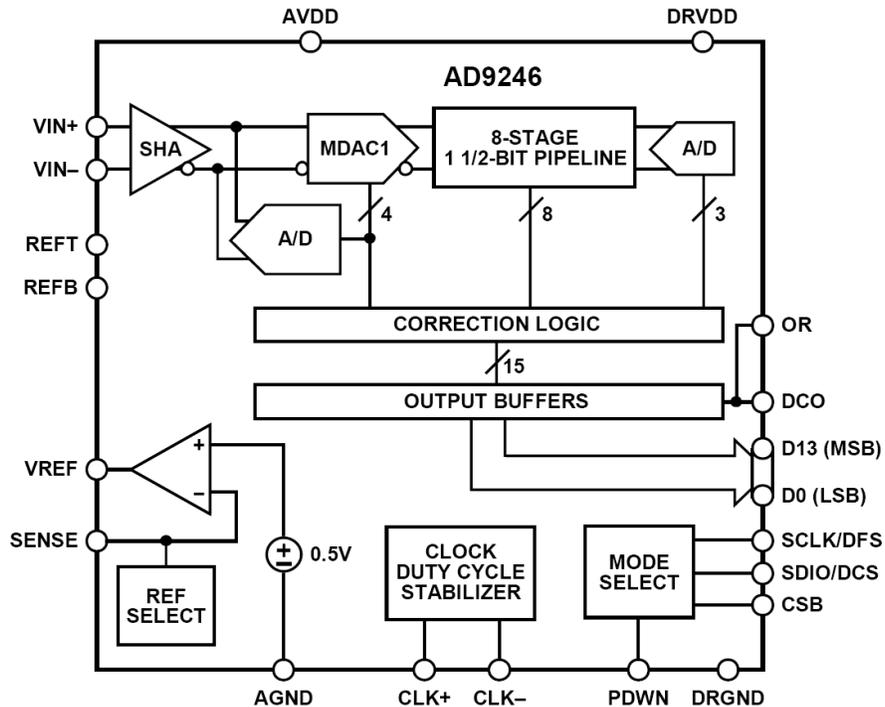
Although dc and 50 Hz or 60 Hz PSR is generally quite good, ac PSR is generally not specified in sigma-delta ADC data sheets.

Because of the high resolution of these devices (up to 24 bits), they should be powered from LDOs rather than risk power supply ripple increasing the overall noise of the converter. This does not usually present a power dissipation problem, because sigma-delta ADCs are typically low power devices.

For audio applications, LDOs should definitely be used to power sigma-delta ADCs in order to minimize the possibility of the ripple frequency mixing with the sampling clock and producing undesirable frequency components within the audio bandwidth.

It should be noted that the addition of LDOs does not eliminate the need for good localized decoupling at the IC power pins. Decoupling is covered in Section 4 of this book.

AD9246 14-Bit, 125MSPS Pipelined ADC



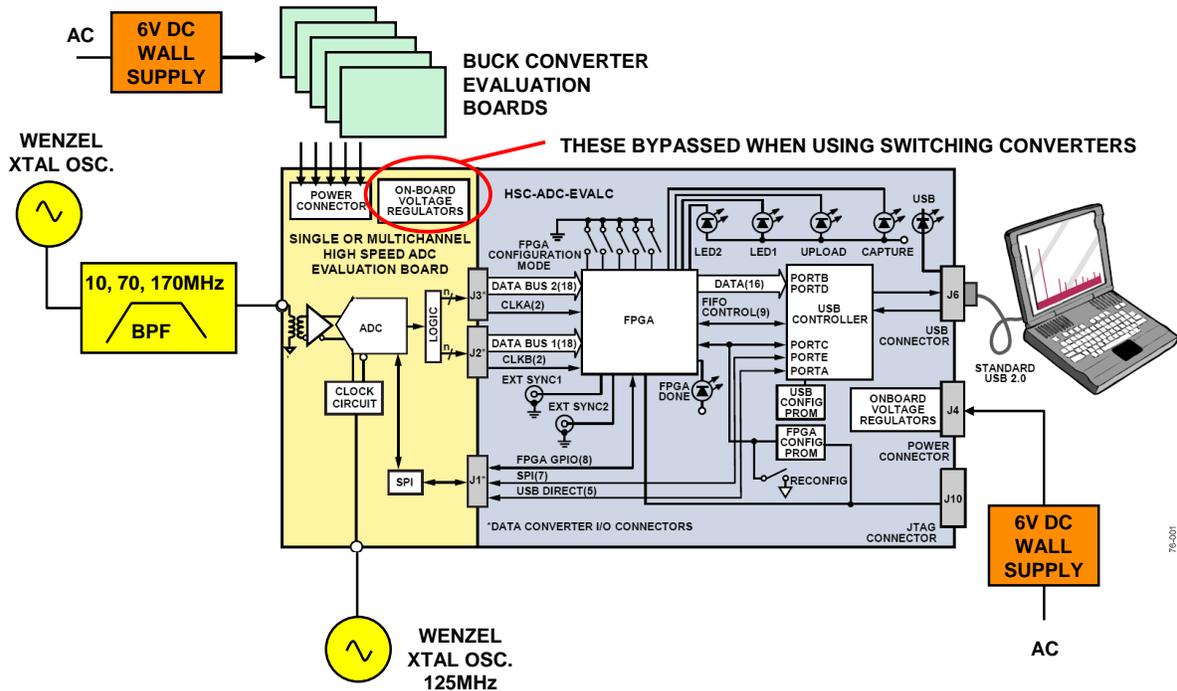
We now look at the PSR characteristics of high speed wide dynamic range pipelined ADCs. This class of ADCs is designed for wide input bandwidth and high SFDR and SNR over a wide range of input frequencies. These converters are often used in IF sampling applications where the input signal is much higher than $f_s/2$. Because PSR is rarely specified for this type of ADC, the data must be obtained experimentally.

In order to evaluate the effects of switching supplies on the SFDR and SNR, some experiments were conducted using the AD9246 14-bit, 125MSPS ADC. This is a CMOS ADC with fully differential inputs for both the analog input and the sampling clock input. The part operates on a single 1.8 V analog supply, and a 1.8 V to 3.3 V I/O supply. Power is only 395 mW at a 125 MSPS sampling rate. Outputs are CMOS compatible.

The SFDR is at least 85 dBc and the SNR 71.7 dB for up to 70 MHz inputs. This type of ADC is very sensitive to noise due to layout and power supply and therefore makes a good choice for these experiments.

Most modern high performance pipelined and SAR ADCs have fully differential inputs.

Test Setup to Evaluate Switching Supply Effect on AD9246 14-Bit, 125MSPS ADC



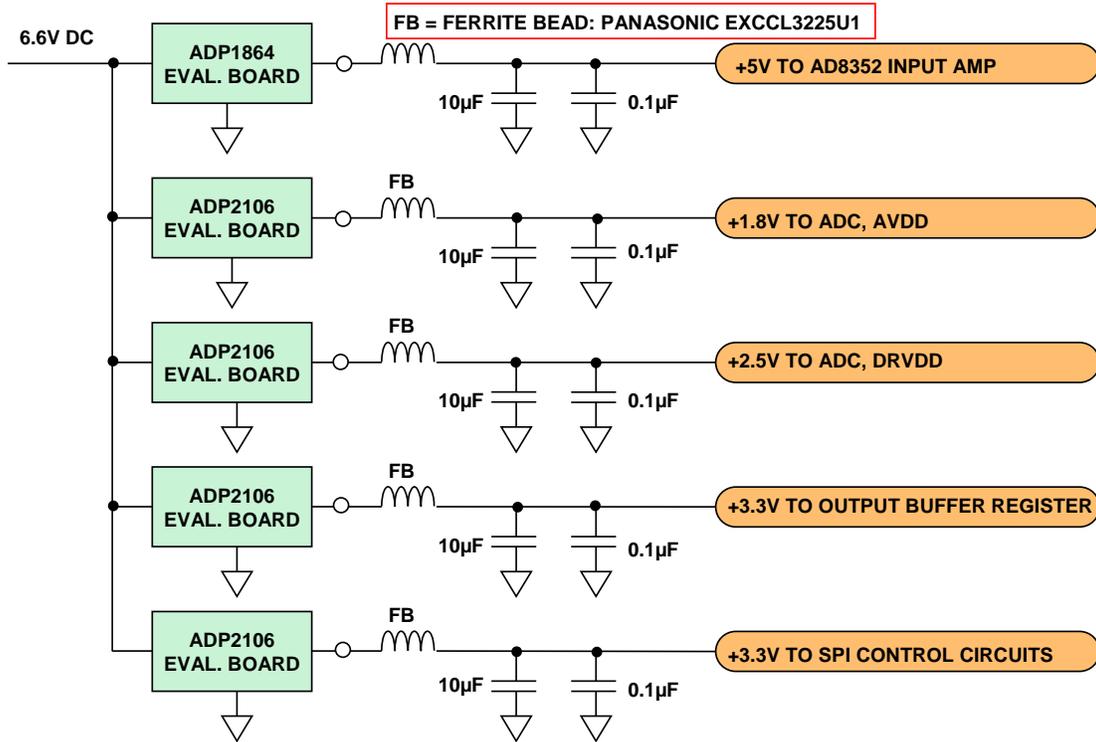
The test setup used for the experiments was a standard ADC evaluation board interfaced to a FIFO (buffer memory) board. The FIFO board interfaces to a computer using the USB port.

This figure shows the standard configuration. The ADC evaluation board is product-specific and contains an input transformer, amplifier, the ADC, clock driver, output buffer logic, and SPI port control logic.

Separate wall mount ac supplies provide the 6 V dc voltage for each board. The ADC evaluation board uses LDO point-of-load regulators to supply the voltages to the ADC and the control logic. The FIFO board uses a combination of LDOs and switching converters for its point-of-load power.

The baseline data on SFDR and SNR was first taken using the standard LDOs on the ADC evaluation board. They were then replaced with switching converter evaluation boards, and the experiments were repeated.

Switching Power Supply Details

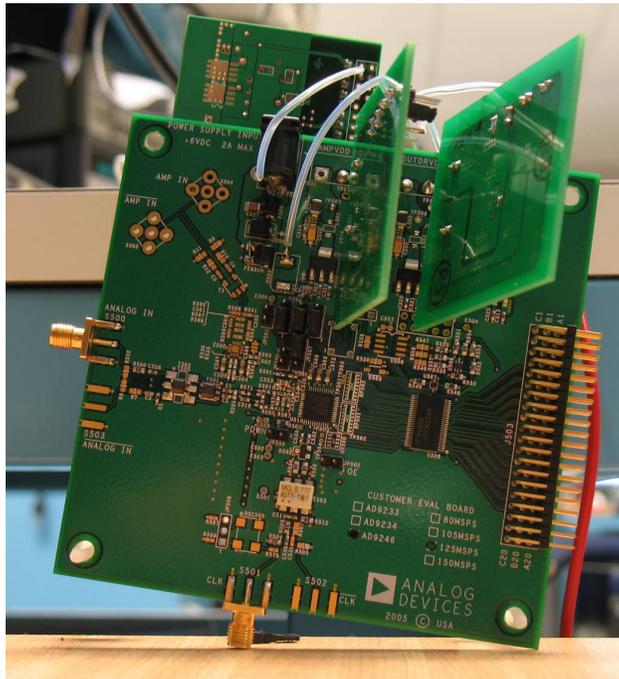


This figure shows how the switching converter evaluation boards were interfaced to the ADC evaluation board voltages. The ferrite beads, 10 µF capacitors, and the 0.1 µF capacitors were part of the ADC evaluation board and located close to the LDOs. In addition, there were the standard recommended localized decoupling capacitors connected close to the power pins of the ADC. The ADC evaluation board external power connector provided a convenient place to connect the switching converter boards and effectively disable the LDOs.

The ferrite bead is a Panasonic EXCCL3225U1 which has an impedance of about 50 Ω from 100 MHz to 1 GHz.

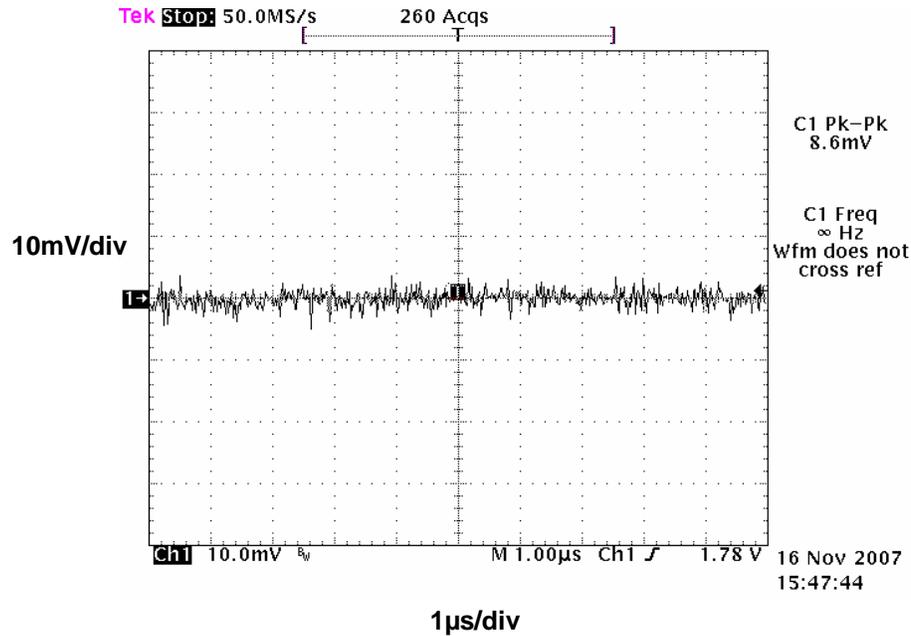
The switching converters were not synchronized to each other.

Modified AD9246 Evaluation Board Showing Switching Supply Boards



This shows a photo of the additional switching supply evaluation boards connected to the ADC evaluation board. No particular care was taken in the interconnections between the supplies and the board in terms of their orientation, although leads were kept as short as practical.

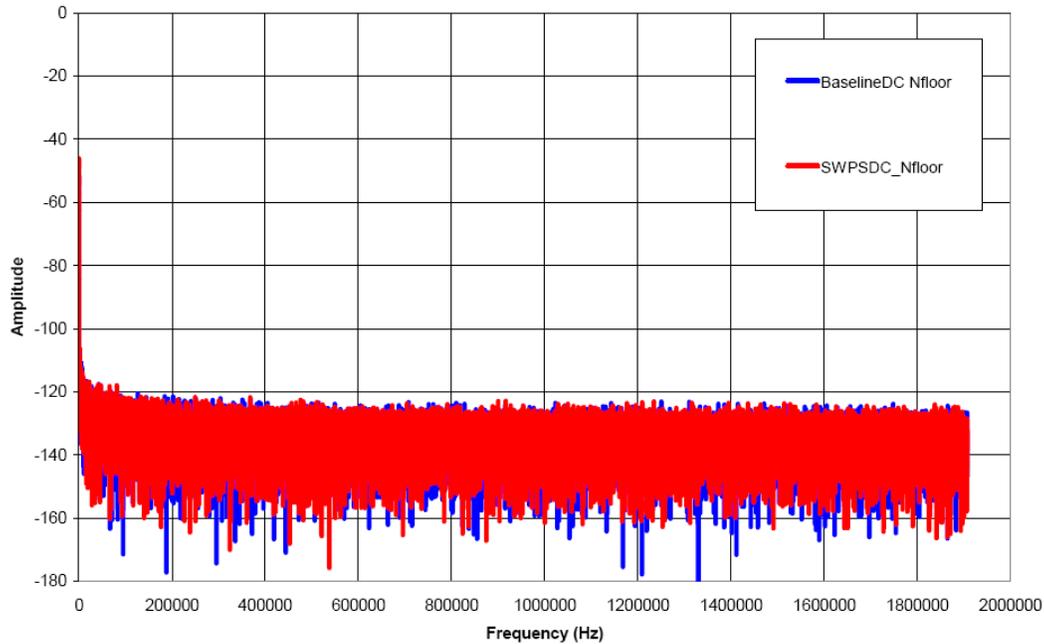
ADP2106 Switching Regulator Output Measured at AVDD of AD9246



The peak-to-peak ripple was measured at the AVDD pin of the AD9246 and was approximately 10 mV. This measurement was made using all five of the switching regulators connected to the evaluation board. The AVDD pin supplies the power to the analog portion of the AD9246, and is therefore the most sensitive one.

It is difficult to distinguish the ripple components from the noise spikes. The oscilloscope's 20 MHz internal filter was used to remove as much high frequency noise as possible.

Noise Floor of ADC for Linear and Switching Supplies with Input Grounded FFT Data Shows Spurs to 2MHz



This shows an FFT output with the ADC input grounded and the switching supplies connected in place of the LDOs. The sampling rate was 125 MSPS, but the FFT is expanded here to show only the portion up to 2 MHz.

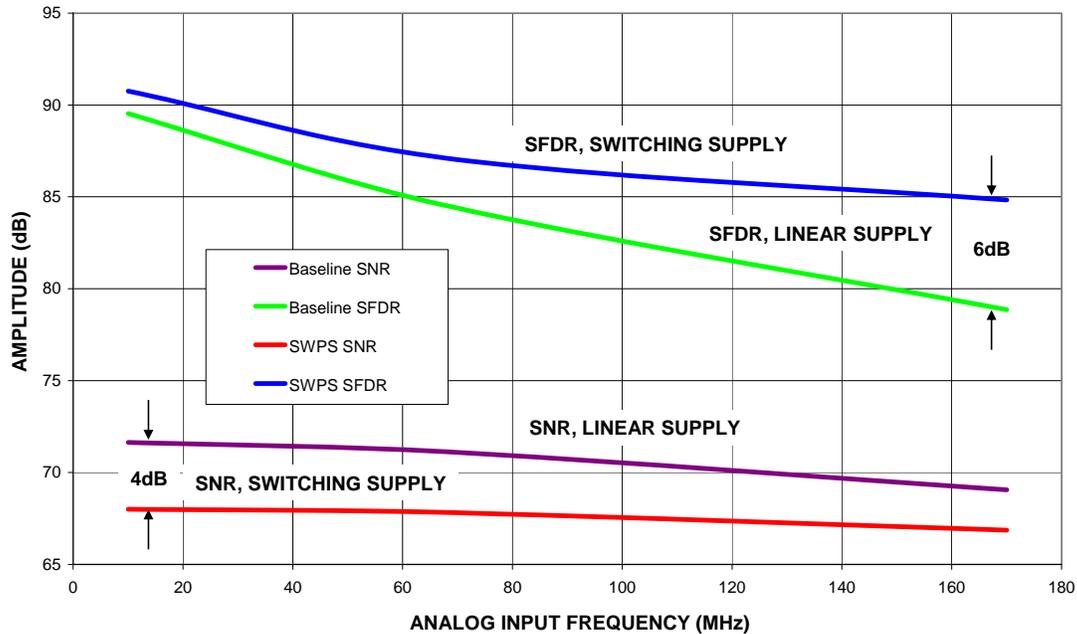
There was little difference between the noise floor using the LDOs or the switching supplies. The overall spur level was approximately 120 dB below full scale.

Analysis of AD9246 ADC PSR

- ◆ Ripple Free Dynamic Range, RFDR = 120dB from grounded-input FFT plots.
- ◆ $V_{FS_PP} = 2.0V$
- ◆ $\Delta V_{SS_PP} = 10mV$
- ◆ $20 \log (2.0/0.01) = 46dB$
- ◆ $PSR = RFDR - 46 = 120 - 46 = 74dB$

We can calculate the approximate PSR of the ADC based on the method previously developed. In this case it works out to be 74 dB.

SNR and SFDR of 14-Bit AD9246 for Linear and Switching Supplies, $f_s = 125\text{MSPS}$



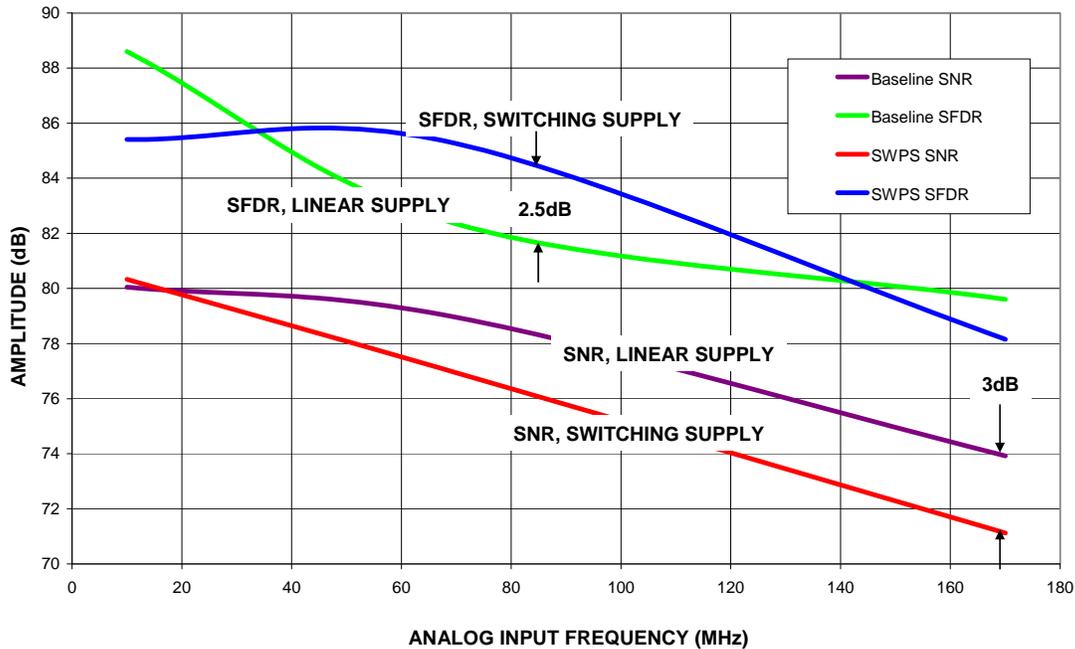
This figure shows the SFDR and the SNR as a function of input frequency for the case of switching supply power and linear supply power.

The SNR was approximately 4 dB worse at low frequencies with the switching supplies. The low frequency (10 MHz) SNR was actually about 68 dB, which does not meet the specified value of 71.9 dB. Although the grounded input FFTs don't indicate significant degradation, the actual SNR of the ADC when stimulated by an ac signal is definitely degraded by the switching supplies.

The effect of power supply noise on SFDR is more difficult to explain, because the switching supply actually improved the SFDR. It has been demonstrated that small amounts of dither noise summed with the analog input signal can improve SFDR in some high performance ADCs. The improvement in SFDR with the switching supply is attributed to this effect. The power supply noise is summed in with the analog signal within the ADC and produces a similar effect. However, under no circumstances should a switching supply be chosen because of the results observed in this particular experiment in anticipation of an SFDR improvement.

It should be noted that you may obtain slightly different results if you conduct these same experiments. The purpose of the experiments is mainly to show the general trend you can expect.

SNR and SFDR of AD9446 16-Bit, 80MSPS ADC for Linear and Switching Supplies, $f_s = 80\text{MSPS}$



This shows results for a similar experiment conducted with the AD9446 16-bit 80 MSPS pipelined ADC. The ADC has LVDS outputs, and the SNR @ 10 MHz is specified at 79.6 dB.

The vertical scale in this figure is 2 dB/division. The previous figure was 5 dB/division.

In this case, there is no significant change in the SNR for a 10 MHz input signal. The degradation occurs at the higher input frequencies and is approximately 3 dB worse using the switching regulator for a 170 MHz input signal.

The AD9446 16-bit, 80 MSPS ADC appears less sensitive to power supply noise than the 14-bit AD9246 (see previous figure on p. 3.30). This could be because the AD9246 has CMOS outputs, while the AD9446 has LVDS outputs which generate less noise. The digital power supply pins of the CMOS output ADC are more sensitive to noise than those that have LVDS outputs. This is because LVDS logic uses constant current low-level differential switches as opposed to the saturating switches found in CMOS logic.

The maximum variation in the SFDR between the linear and switching supply power is about 2.5 dB, and the curves cross each other. This is within the range of experimental error considering all the variables in the experiment.

Pipelined ADC PSR Summary

- ◆ **No consistency in manufacturer's specifications of PSR for pipelined ADCs. Some specify ripple PSR, but noise rejection may be more important.**
- ◆ **Experiments show that pipelined ADCs have good PSR for ripple frequency.**
- ◆ **However, broadband switching noise can decrease SNR. This must be verified by experimentation.**
- ◆ **Effect of switching noise greater for high input frequencies (IF sampling).**
- ◆ **With proper filtering, switchers probably ok for 12-bit baseband sampling applications.**
- ◆ **ADCs with LVDS outputs appear less sensitive to power supply noise than those with CMOS outputs.**
- ◆ **Experimentation required for 14 or 16 bit applications, or IF sampling.**
- ◆ **Conservative approach is to use LDOs to power ADCs, or verify performance with switchers by experimentation.**

Pipelined ADCs are typically used for sampling rates greater than about 10 MSPS. There are many varieties currently available. Some are designed for baseband operation, and some are designed to handle input signals well above the Nyquist frequency of $f_s/2$.

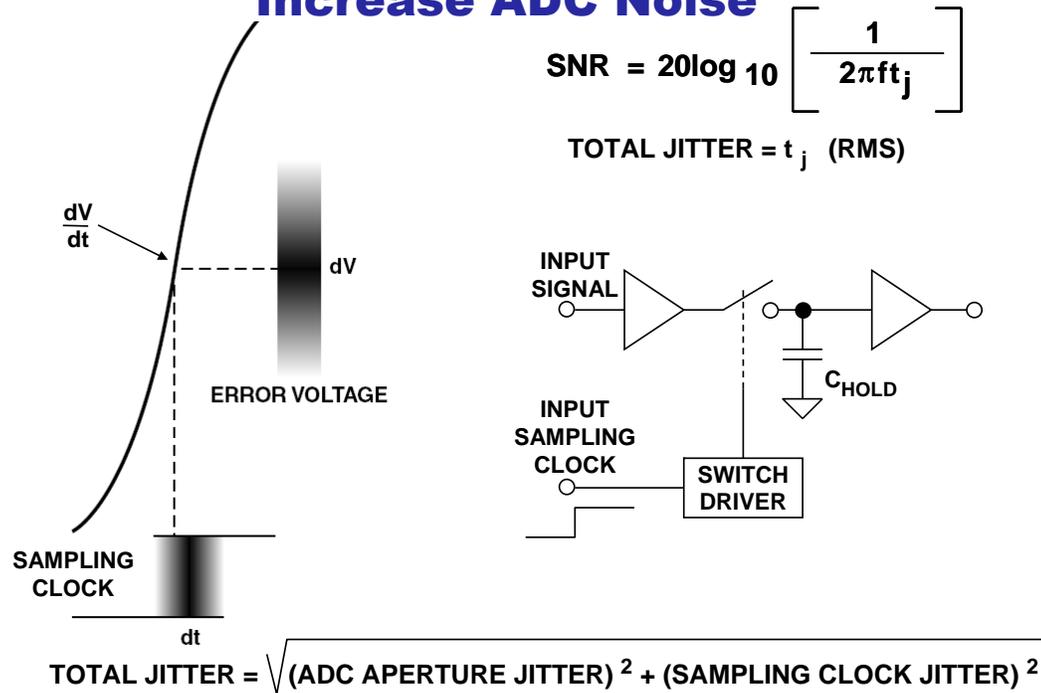
A few have single-ended inputs, but most have differential inputs for both the analog input and sampling clock inputs.

Even though a high speed pipelined ADC may have a PSR specification, it is dangerous to assume that it applies to critical specifications such as SNR or SFDR. The only certain way to determine if a switching supply can be used to power the ADC is to actually run a controlled experiment where the frequency domain results of linear versus switching supplies can be compared.

In some cases, the switching supply noise and ripple may yield acceptable results. The only way to be certain is to try it.

The conservative approach is to use LDOs to power pipelined ADCs unless system efficiency or real estate requirements make this impossible.

Sampling Clock Jitter and Aperture Jitter Increase ADC Noise



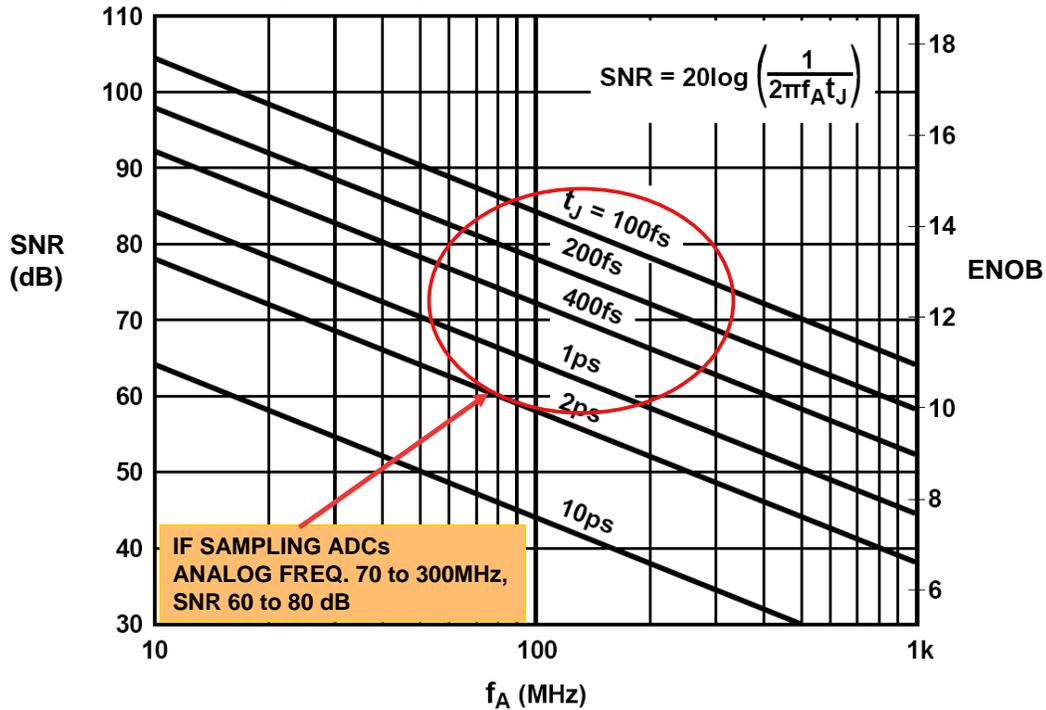
Power supply ripple and noise can affect critical clock generating circuits by increasing the amount of jitter. The ADC sampling clock is especially sensitive. The leading edge determines the instant the ADC takes a sample. The sampling clock jitter translates into a voltage error at the sample-and-hold output as shown here.

The effect is to limit the SNR to a value given by the equation $SNR = 20 \log(1/2\pi f t_j)$, where f is the full-scale analog input frequency, and t_j is the total jitter. This equation describes the SNR for an ideal ADC of infinite resolution where the only error source is the clock jitter. In practice, the SNR will be worse due to additional error sources.

The ADC aperture jitter is created internally in the sample-and-hold circuit. It combines in a root-sum-square manner with the external clock jitter. In most situations, the external clock jitter dominates.

Most high performance ADCs now use differential sampling clock inputs in order to minimize sensitivity to clock jitter.

ADC SNR as a Function of Analog Input Frequency and Clock Jitter



This figure shows the theoretical SNR (left side) due to total jitter versus full-scale analog input frequency. The ADC is assumed to have infinite resolution, and the only noise source is that produced by the jitter.

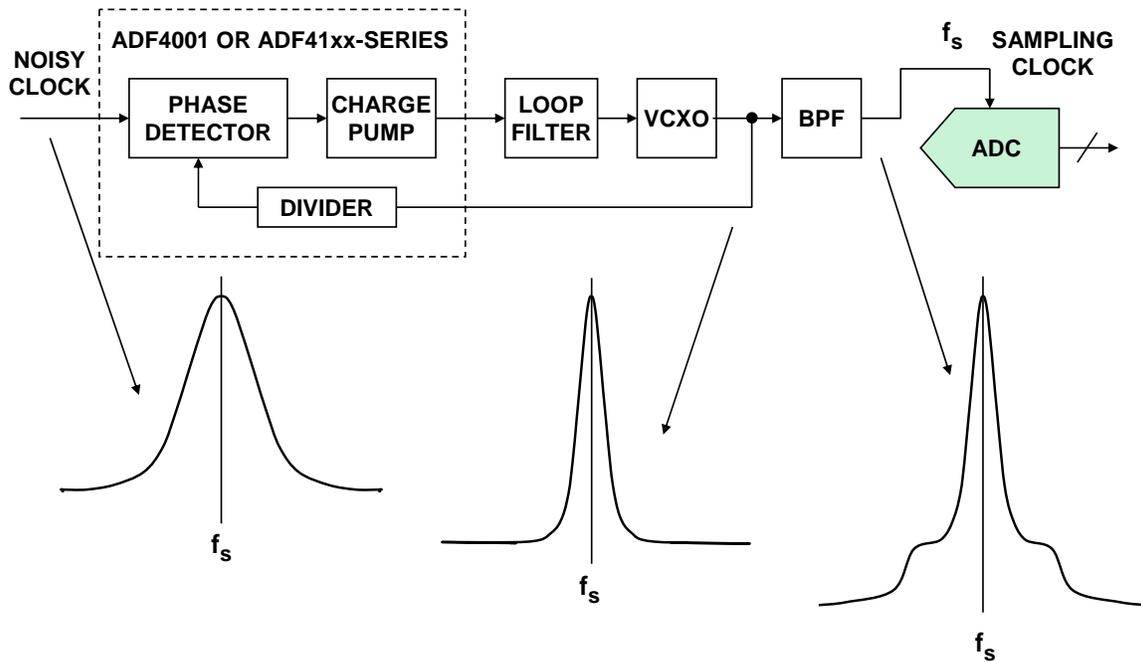
The effective number of bits (ENOB) is shown on the right and is related to SNR by the well known equation, $SNR = 6.02N + 1.76dB$, where $N = ENOB$.

IF-sampling ADCs typically operate with analog frequencies between 70 MHz and 300 MHz, with system SNR requirements of 60 dB to 80 dB (the circled region). The range of allowable sampling clock jitter for this level of performance is from about 0.1 ps to 2 ps, depending upon the IF frequency and the SNR requirement.

These stringent requirements mean that special care must be taken with the ADC sampling clock, which is often derived from other clocks in the system.

Clock jitter less than 2 ps can only be attained using dedicated crystal controlled oscillators or PLLs with VCXOs.

Using a Phase-Locked Loop (PLL) and Bandpass Filter to Condition a Noisy Clock Source



Only the highest end systems can afford the dedicated crystal oscillators.

Many systems therefore use a lower-cost combination of a phase-locked loop (PLL) and a VCXO (voltage-controlled crystal oscillator) followed by a bandpass filter to generate a low jitter sampling clock from a noisy system clock.

Circuits such as the one shown in this figure are capable of generating sampling clocks with less than 1 ps rms jitter.

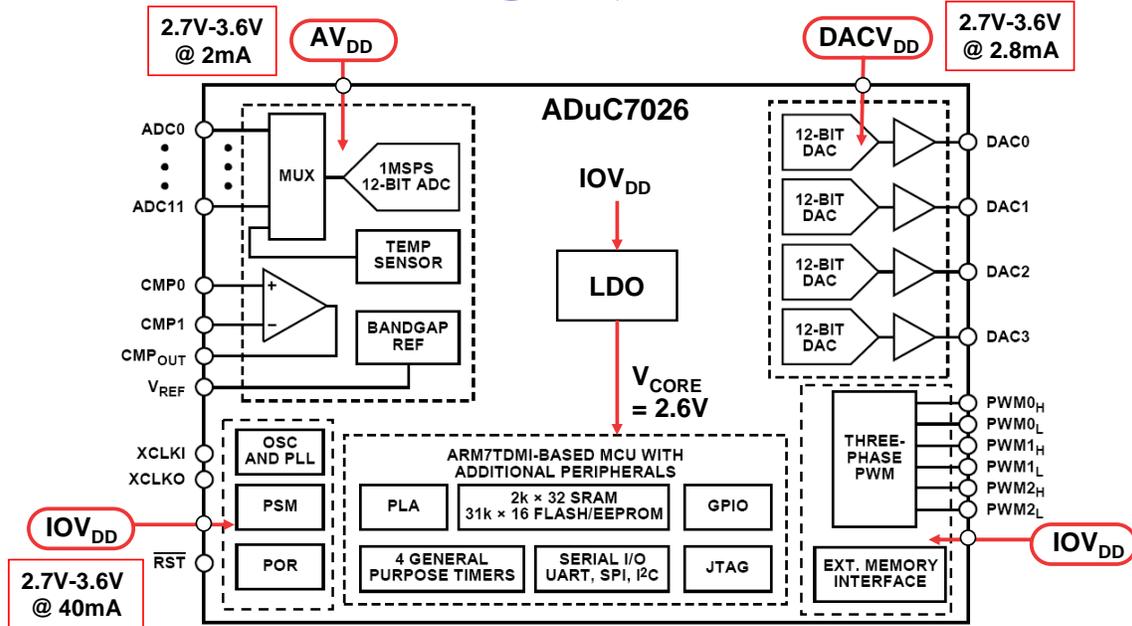
Analog Devices makes a number of PLLs and clock generation and distribution ICs suitable for this function.

See, www.analog.com/pll and www.analog.com/clocks for more information on Analog Device's clock generation products.

Powering Precision Analog Microcontrollers

www.analog.com/microcontrollers

ADuC7026 Precision Analog Microcontroller, with 12-Bit Analog I/O, ARM7TDMI® MCU

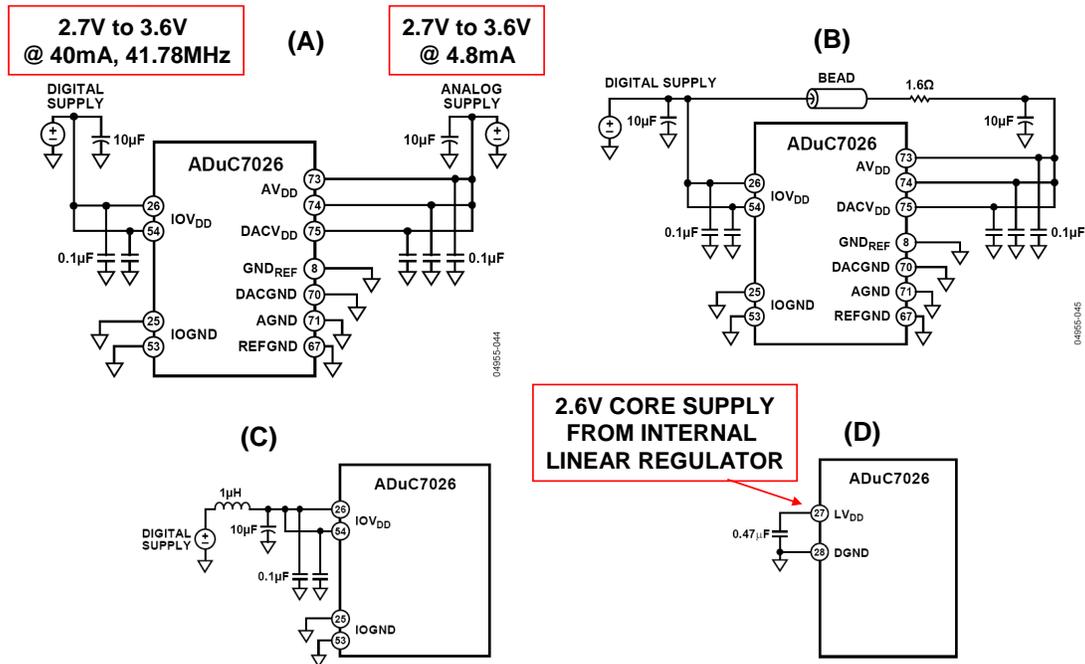


The ADuC7019 to ADuC7028 are fully integrated, 1 MSPS, 12-bit data acquisition systems incorporating high performance multichannel ADCs, 16-bit/32-bit MCUs, and Flash/EE memory on a single chip. The ADC consists of up to 12 single-ended inputs. An additional four inputs are available but are multiplexed with the four DAC output pins. The ADC can operate in single-ended or differential input modes. The ADC input voltage is 0 V to V_{REF} (2.5 V nominal). A low drift band gap reference, temperature sensor, and voltage comparator complete the ADC peripheral set. Depending on the part model, up to four buffered voltage output DACs are available on-chip. The DAC output range is programmable to one of three voltage ranges.

The devices operate from an on-chip oscillator and a PLL generating an internal high frequency clock of 41.78 MHz. This clock is routed through a programmable clock divider from which the MCU core clock operating frequency is generated. The microcontroller core is an ARM7TDMI, 16-bit/32-bit RISC machine, which offers up to 41 MIPS peak performance. Eight kilobytes of SRAM and 62 kilobytes of nonvolatile Flash/EE memory are provided on-chip. The ARM7TDMI core views all memory and registers as a single linear array. On-chip factory firmware supports in-circuit serial download via the UART or I²C serial interface ports, while nonintrusive emulation is also supported via the JTAG interface. These features are incorporated into a low cost QuickStart™ Development System supporting this MicroConverter family. The parts operate from 2.7 V to 3.6 V and are specified over an industrial temperature range of -40°C to +125°C. When operating at 41.78 MHz, the power dissipation is typically 120 mW. The ADuC7019 to ADuC7028 are available in a variety of memory models and packages.

The above block diagram illustrates how power is applied to the part. Analog power is applied to the AV_{DD} and $DACV_{DD}$ inputs. The I/O power is applied on the IOV_{DD} pins, and the internal core voltage of 2.6 V is derived from the IOV_{DD} voltage using an internal LDO.

Powering the Analog Devices' ADuC702x Family of Precision Analog Microcontrollers



The ADuC702x family of precision analog microcontrollers contains high precision 12-bit data conversion circuits as well as the ARM7TDMI core. The analog data conversion circuits are driven from the AV_{DD} and the $DACV_{DD}$ pins. Ideally, these pins should be driven from a low noise analog supply as shown in (A). The supply current is only 4.8 mA and will result in minimum power loss if driven from an LDO.

With proper filtering, the analog supply pins can be driven from the digital supply as shown in (B). However, the IOV_{DD} supply is also sensitive to high frequency noise because it is the supply source for the internal oscillator and PLL circuits. When the internal PLL loses lock, the clock source is removed by a gating circuit from the CPU, and the ARM7TDMI core stops executing code until the PLL regains lock. This feature is to ensure that no flash interface timings or ARM7TDMI timings are violated.

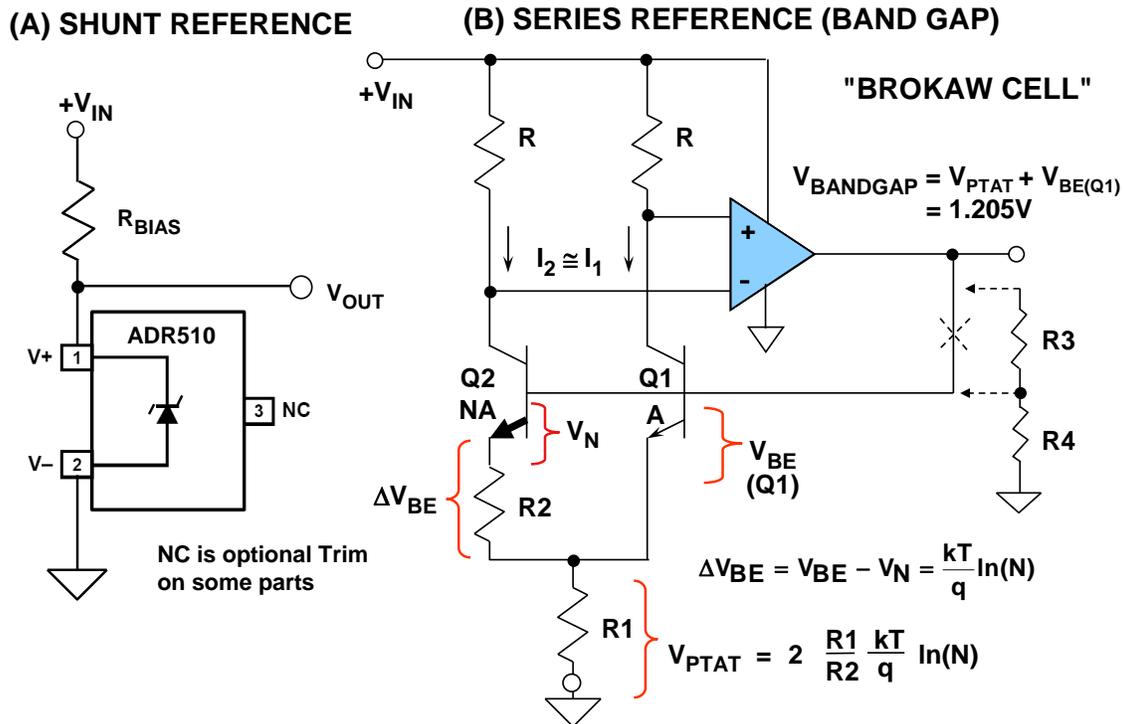
Typically, noise greater than 50 kHz and 50 mV p-p on top of the supply causes the PLL to lose lock and the core to stop working. If the decoupling circuit shown in (B) does not limit the ripple and noise to less than 50 mV on IOV_{DD} , an inductor or ferrite bead as shown in (C) should be added for extra filtering.

Each part in the ADuC7019 to ADuC7028 family requires a single 3.3 V supply, but the core logic requires a 2.6 V supply. An on-chip linear regulator generates the 2.6 V from IOV_{DD} for the core logic. The LV_{DD} pin is the 2.6 V supply for the core logic. An external compensation capacitor of 0.47 µF must be connected between LV_{DD} and $DGND$ (as close as possible to these pins) to act as a charge reservoir as shown in (D). The LV_{DD} pin should not be used for any other chip. It is also recommended to use good power supply decoupling and filtering on IOV_{DD} as discussed above to help improve line regulation performance of the on-chip voltage regulator.

Voltage References

www.analog.com/references

Shunt and Series Voltage References



A voltage reference is a low noise, accurate, and well regulated power supply which is designed specifically for data acquisition applications, such as establishing the full-scale input voltage of an ADC or DAC.

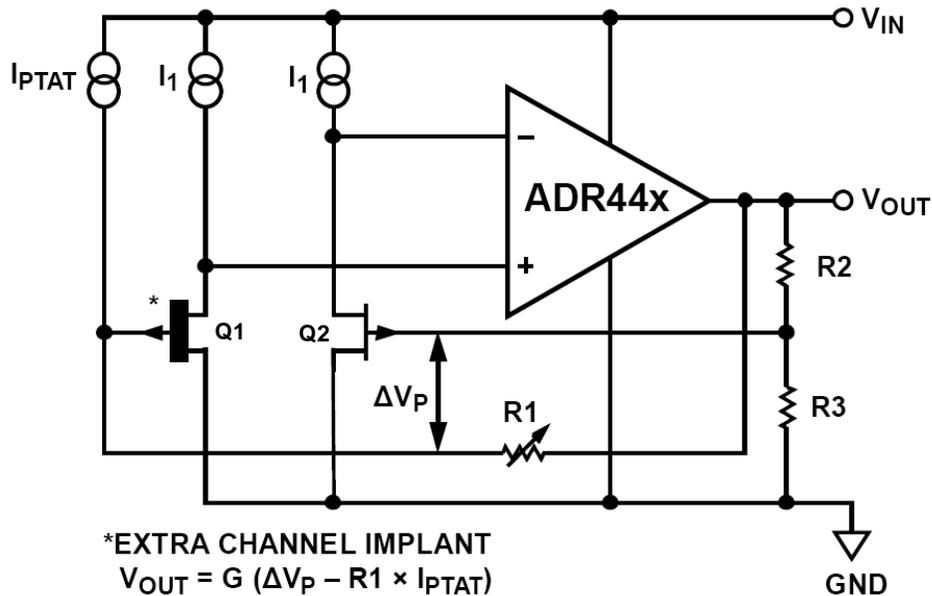
This figure shows two popular types: shunt and series.

The shunt reference in (A) is a two terminal device which essentially acts as a low voltage Zener diode. For example, the ADR510 is a low voltage (1.000 V), precision shunt-mode voltage reference in an ultracompact (3 mm × 3 mm) SOT-23-3 package. The ADR510 features low temperature drift (70 ppm/°C), high accuracy (±0.35%), and ultralow noise (4 μV p-p) performance.

The ADR510 advanced design eliminates the need for an external capacitor, yet it is stable with any capacitive load. The minimum operating current increases from 100 μA to a maximum of 10 mA. This low operating current and ease of use make the ADR510 ideally suited for handheld battery-powered applications.

Both shunt and series references are based on the band gap reference. The circuit in (B) shows a "Brokaw Cell" band gap circuit which forms the basis for many series references. Transistors Q1 and Q2 operate at equal collector currents by virtue of the feedback network. However, the emitter area of Q2 is N times that of Q1. This causes the V_{BE} drop of Q2 (V_{N}) to be less than that of Q1 by an amount equal to $(kT/q)\ln(N)$. The current through R2 is therefore proportional to absolute temperature, PTAT. This current is equal to $(kT/q)\ln(N)/R2$. Since an equal current flows through Q1, the sum of the two transistor currents produces a voltage across R1 which is equal to $2(R1/R2)(kT/q)\ln(N)$. This voltage is PTAT and is summed with $V_{\text{BE(Q1)}}$ which is complementary to absolute temperature (CTAT), to produce the voltage at the output. When the voltages are scaled (trimming R1 and R2) for minimum output TC, the value is approximately equal to the band gap voltage, 1.205 V. Note that the output voltage can then be scaled by simply adding the feedback resistor network shown dotted in the figure.

XFET® Reference Architecture



The ADR44x series of references uses a new reference generation technique known as XFET (eXtra implanted junction FET). This technique yields a reference with low dropout, good thermal hysteresis, and exceptionally low noise. The core of the XFET reference consists of two junction field-effect transistors (JFETs), one of which has an extra channel implant to raise its pinch-off voltage. By running the two JFETs at the same drain current, the difference in pinch-off voltage can be amplified and used to form a highly stable voltage reference.

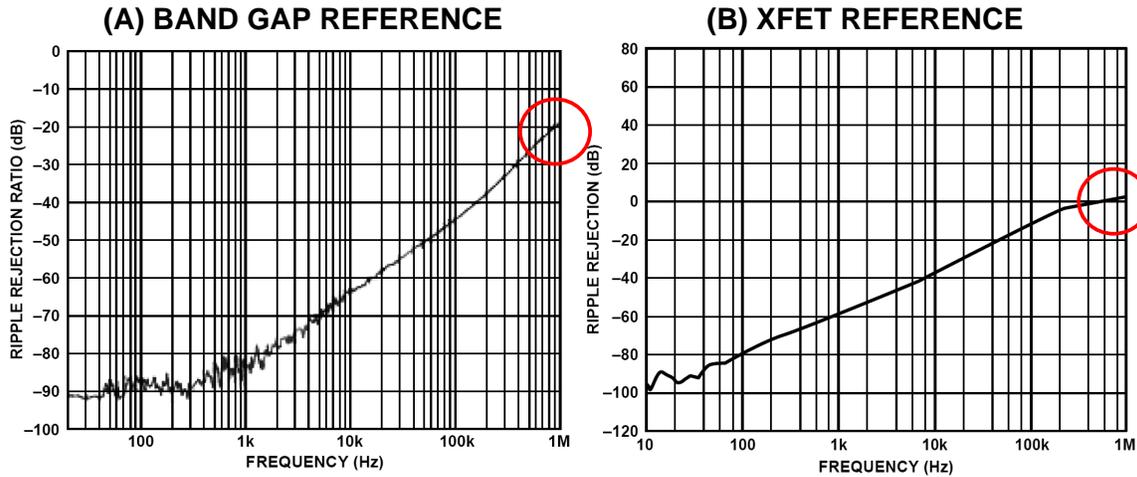
The intrinsic reference voltage is around 0.5 V with a negative temperature coefficient of about $-120 \text{ ppm}/^\circ\text{C}$. This slope is essentially proportional to the dielectric constant of silicon, and it can be compensated by adding a correction term generated in the same fashion as the proportional-to-absolute temperature (PTAT) term used to compensate band gap references. The advantage of an XFET reference is its correction term, which is approximately 20 times lower and requires less correction than that of a band gap reference. Because most of the noise of a band gap reference comes from the temperature compensation circuitry, the XFET results in much lower noise. The temperature correction term is provided by a current source with a value designed to be proportional-to-absolute temperature. The general equation is

$$V_{OUT} = G (\Delta V_P - R1 \times I_{PTAT}),$$

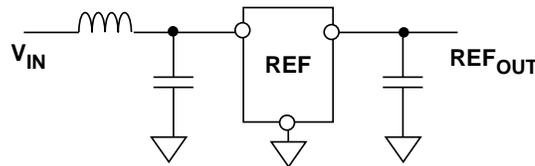
where G is the gain of the reciprocal of the divider ratio. ΔV_P is the difference in pinch-off voltage between the two JFETs. I_{PTAT} is the positive temperature coefficient correction current.

The reference output voltage of the ADR44x devices is scaled by on-chip adjustment of $R2$ and $R3$ to provide different output voltage options.

Band Gap and XFET Reference Ripple Rejection Ratio



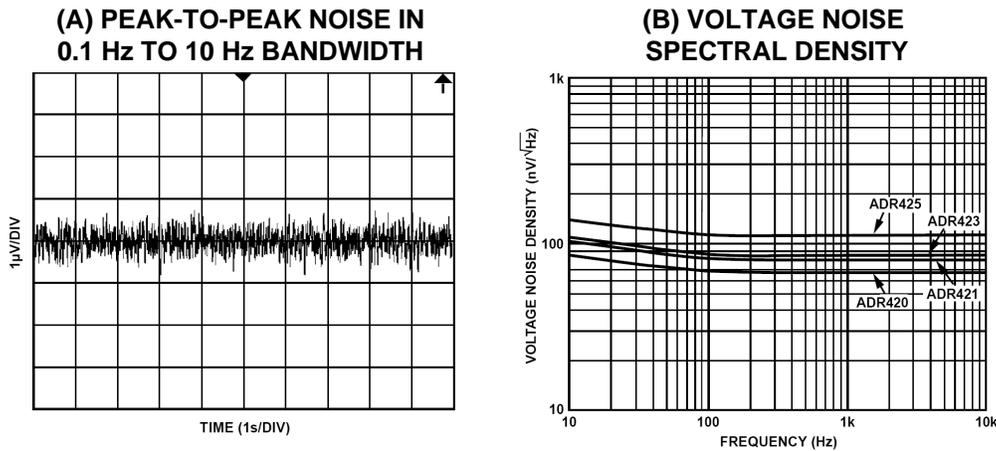
- ◆ Don't count on references to filter power supply ripple!
- ◆ Must use good filtering on the reference input and output



Ripple rejection ratio is shown in this figure for a typical band gap and XFET reference. The 1 MHz ripple rejection of the band gap is 20 dB and the XFET is 0 dB.

For this reason, the input voltage to any reference must be adequately filtered. In most cases, an LC filter is adequate, provided the input capacitor has a low ESR and ESL.

Voltage Reference Noise



OTHER WAYS TO SPECIFY NOISE

- ◆ Noise spectral density @ 1 kHz
- ◆ RMS noise measured over 100 kHz bandwidth
- ◆ Must always specify bandwidth!

Voltage reference noise can be specified in a number of ways. The most common is to specify the noise similarly to that of an op amp.

The scope photo in (A) shows the peak-to-peak noise measured in a 0.1 Hz to 10 Hz bandwidth. This standard measurement is important in low frequency high resolution measurement applications.

The plot in (B) shows the traditional rms voltage noise spectral density as a function of frequency. This plot is sometimes referred to as the "spot noise."

It is important to remember that the 0.1 Hz to 10 Hz noise is specified as a peak-to-peak quantity, while the noise spectral density plot is rms.

Note that a noise specification is meaningless unless the bandwidth is also specified. In some cases, reference noise is measured over a 100 kHz bandwidth, but other bandwidths are often used. Sometimes only the noise spectral density (spot noise) at 1 kHz is specified.

Another point to consider is that both the input and output capacitors must also be specified if the noise specification is to be meaningful.

Reference Noise Requirements for Various System Accuracies (1/2 LSB / 100kHz BW Criteria)

BITS	NOISE DENSITY (nV/ $\sqrt{\text{Hz}}$) FOR 10, 5, AND 2.5V FULL-SCALE RANGES		
	10V	5V	2.5V
12	643	322	161
13	322	161	80
14	161	80	40
15	80	40	20
16	40	20	10

- ◆ Criteria: $V_{N(\text{PP})} < 0.5 \text{ LSB}$, $\text{LSB} = V_{\text{FS}}/2^N$
- ◆ Assume p-p noise $V_{N(\text{P-P})} \approx 6 \times V_{N(\text{RMS})}$, calculate $V_{N(\text{RMS})}$
- ◆ Assume a bandwidth of 100kHz, calculate noise density
- ◆ Noise Density = $V_{N(\text{RMS})}/\sqrt{100\text{kHz}}$
- ◆ Most references are about 100nV/ $\sqrt{\text{Hz}}$

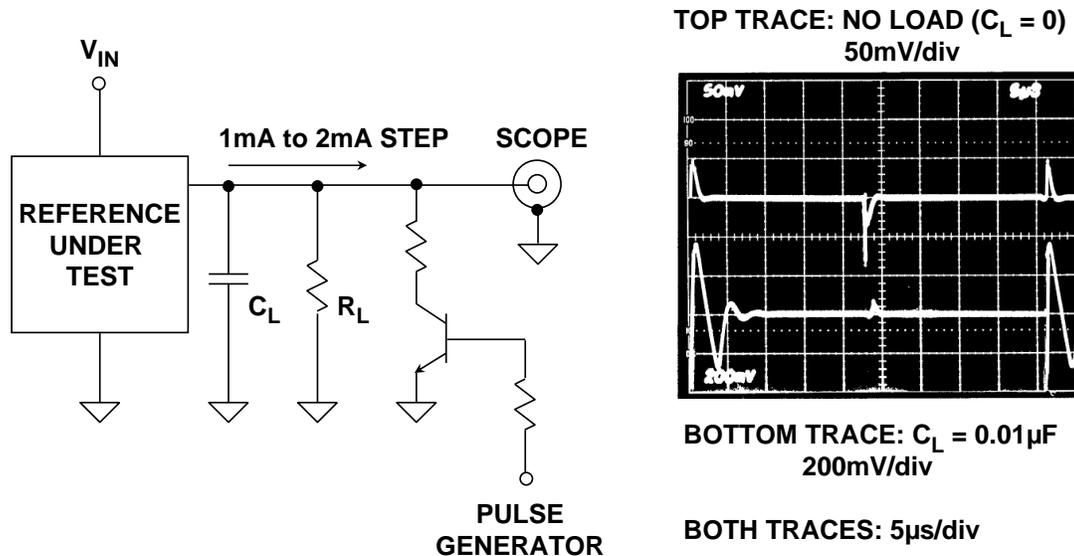
This chart relates noise spectral density to ADC resolution for various signal ranges. It is useful in determining the approximate requirement on the voltage reference noise. It should be noted, however, that further reductions in the rms noise can be achieved with additional filtering. The numbers in the table are calculated as follows:

- The basic criteria is that the peak-to-peak noise should be less than 0.5 least significant bit (LSB).
- An N-bit ADC has 2^N levels. Each level is separated by 1 LSB.
- The LSB value is calculated by dividing the ADC full-scale range, V_{REF} , by 2^N .
- One-half LSB is $2^N \div 2$
- Assume that the peak-to-peak noise is 6 times the rms noise. This is a widely used approximation.
- Divide the LSB value by 12 in order to obtain the approximate rms noise, $V_{\text{REF}}/(12 \times 2^N)$.
- Divide the rms noise by the square root of the bandwidth, BW, to get the noise spectral density:

$$E_n \leq \frac{V_{\text{REF}}}{12 \times 2^N \times \sqrt{\text{BW}}}$$

Most voltage references have a noise spectral density of between 50 nV/ $\sqrt{\text{Hz}}$ and 100 nV/ $\sqrt{\text{Hz}}$. This implies that additional filtering is required for applications requiring greater than approximately 12 bits of resolution.

References Should Be Stable with Capacitive Loads



As previously discussed, the reference input to an ADC must be heavily decoupled. This means that the reference must be stable with capacitive loads in order to be useful as an ADC reference.

This test set is used to test reference stability by applying a current step to the output and checking for ringing and oscillation. The objective is to simulate the current transients produced by switched capacitor inputs.

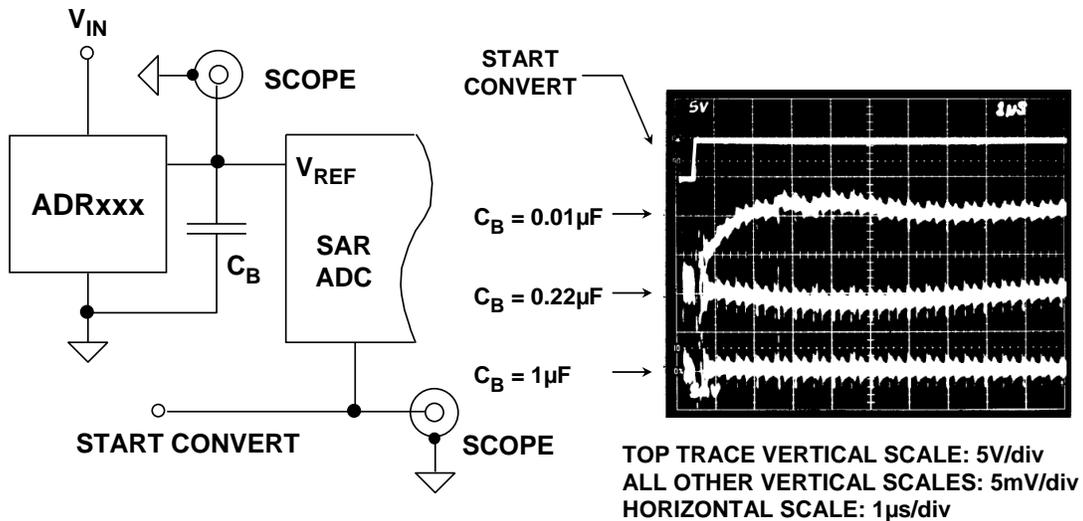
The top trace shows the step response with no capacitive decoupling. The transients are well behaved with no oscillation.

The bottom trace shows the step response with a decoupling capacitor of 0.01 μF . Note the increased transient amplitude (400 mV) and the ringing.

It is clear that this reference is useless as an ADC or DAC reference because a decoupling capacitor such as the 0.01 μF used in this test is almost always required. In fact, a larger value (1 μF or greater) is preferable and would cause even more instability for this reference.

Modern references should be designed for stability under reasonable decoupling loads, and the data sheet should recommend typical minimum and/or maximum values, and show recommended application circuits.

External Reference for SAR ADC Requires Energy Storage Capacitor to Prevent Errors



As noted above, reference bypass capacitors are useful when driving the reference inputs of ADCs. This figure illustrates reference voltage settling behavior immediately following the "Start Convert" command for a successive approximation ADC. This particular SAR ADC requires approximately 10 μs to complete the conversion process. A small capacitor (0.01 μF) does not provide sufficient charge storage to keep the reference voltage stable during conversion, and errors will result. As shown by the bottom trace, decoupling with a 1 μF capacitor maintains the reference stability during the entire conversion cycle for accurate results.

Where voltage references are required to drive large capacitances, it is also critically important to realize that their turn-on time will be prolonged. Experimentation may be needed to determine the delay before the reference output reaches full accuracy, but it will certainly be much longer than the time specified on the data sheet for the same reference in a low capacitance loaded state.

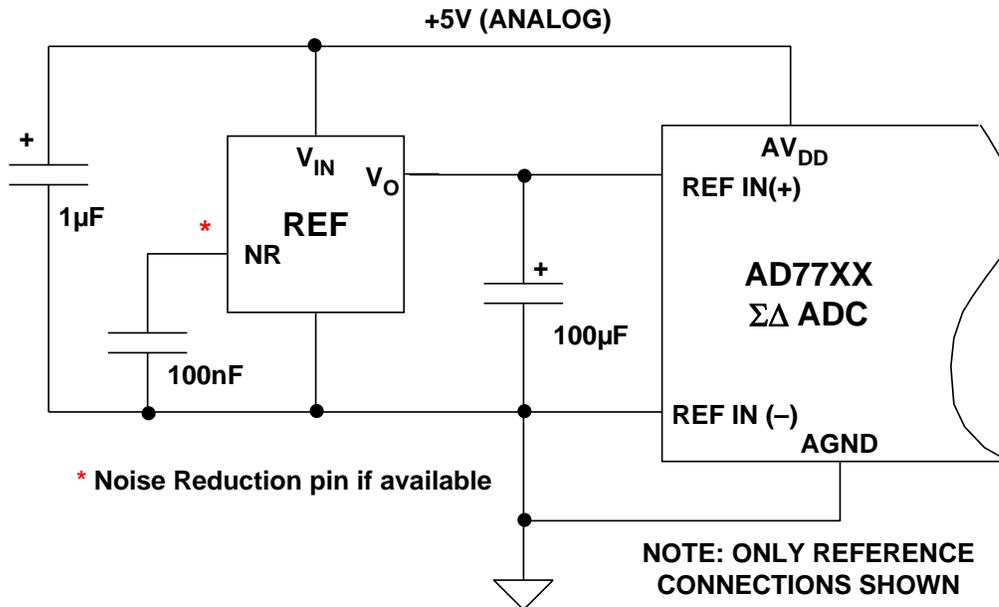
In most cases the data sheet for the SAR ADC gives the required value of the external reference decoupling capacitor for specified performance.

Reference Temperature Drift Requirements for Various System Accuracies (1/2 LSB Criteria, 100°C Span)

BITS	REQUIRED DRIFT (ppm/°C)	½ LSB WEIGHT (mV) 10, 5, AND 2.5V FULL-SCALE RANGES		
		10V	5V	2.5V
8	19.53	19.53	9.77	4.88
9	9.77	9.77	4.88	2.44
10	4.88	4.88	2.44	1.22
11	2.44	2.44	1.22	0.61
12	1.22	1.22	0.61	0.31
13	0.61	0.61	0.31	0.15
14	0.31	0.31	0.15	0.08
15	0.15	0.15	0.08	0.04
16	0.08	0.08	0.04	0.02

The accuracy of an ADC or DAC can be no better than that of its reference. Reference temperature drift affects full-scale accuracy as shown in this figure. This table shows system resolution and the TC required to maintain 1/2 LSB error over an operating temperature range of 100°C. For example, a TC of about 1 ppm/°C is required to maintain 1/2 LSB error at 12 bits. For smaller operating temperature ranges, the drift requirement will be less. The last three columns of the table show the voltage value of 1/2 LSB for popular full-scale ranges.

Low Noise Reference Driving a Sigma-Delta ADC



High resolution converters (both sigma-delta and other types) can benefit from recent improvements in IC references, such as lower noise and the ability to drive capacitive loads. Even though many data converters have internal references, the performance of these references is often compromised because of the limitations of the converter process. In such cases, using an external reference rather than the internal one often yields better overall performance.

This figure shows a low noise reference, such as the ADR4xx series, used as the reference for the AD77xx-series ADCs. These references allow a large decoupling capacitor on their outputs thereby minimizing conversion errors due to transients.

There is one possible but yet quite real problem when replacing the internal reference of a converter with a higher precision external one. The converter in question may have been trimmed during manufacture to deliver its specified performance with a relatively inaccurate internal reference. In such a case, using a more accurate external reference with the converter may actually introduce additional gain error! Therefore the data sheet should be carefully checked regarding the use of external references and their possible effect on gain and offset.

Voltage Reference Summary

BAND GAP	XFET	BURIED ZENER
< 5V Supplies	< 5V Supplies	> 5V Supplies
High Noise @ High Power	Low Noise @ Low Power	Low Noise @ High Power
Fair Drift and Long Term Stability	Excellent Drift and Long Term Stability	Good Drift and Long Term Stability
Fair Thermal Hysteresis	Low Thermal Hysteresis	Fair Thermal Hysteresis

This summarizes the characteristics of the three most popular types of references.

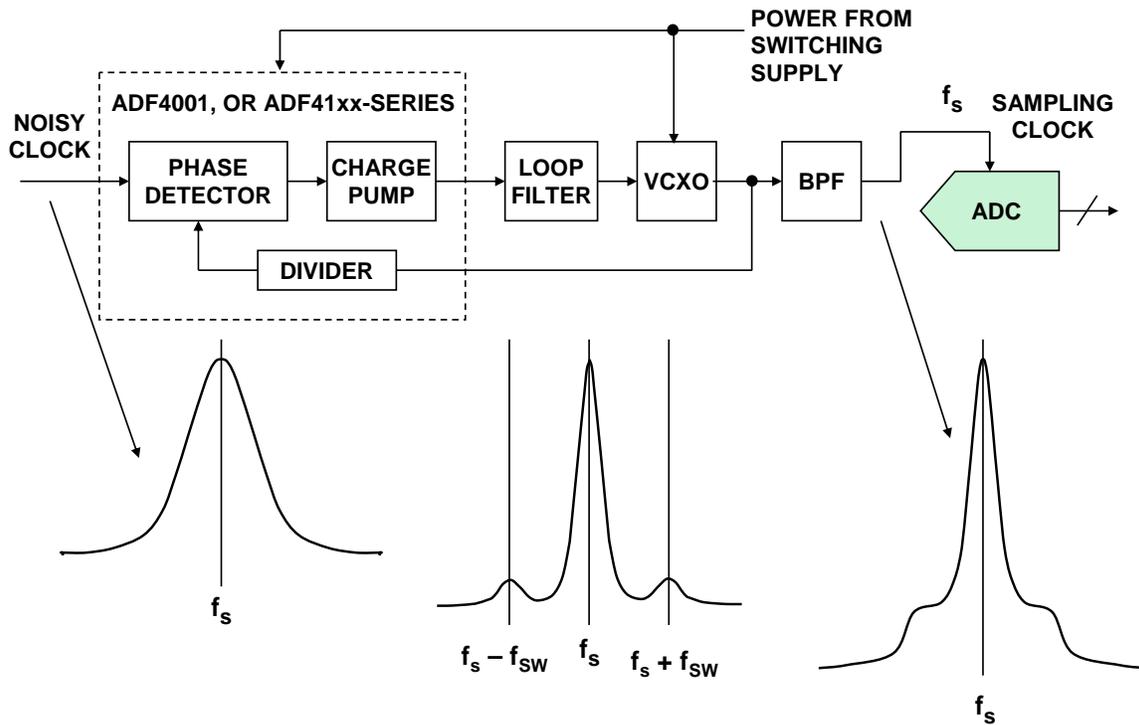
Most modern data converter applications use either the band gap or XFET reference. The buried zener types require supply voltages greater than 5 V and are therefore not relevant to most modern single-supply applications.

The XFET reference series offers the best overall performance for applications greater than 16 bits because of their superior noise and drift characteristics.

Powering Clock Circuits

www.analog.com/pll
www.analog.com/clocks
www.analog.com/dds

Power Supply Ripple Modulates PLL Output



Clock generating circuits are more and more critical to a successful system design. Transmitting digital signals at high data rates (sometimes greater than 1 GHz) using CML, LVDS, or other types of fast logic requires low noise supplies to prevent data corruption. An example of this requirement is the Xilinx Virtex-4 FPGA previously discussed in Section 1, where the manufacturer specifically recommends LDOs for powering the high-speed I/O circuits.

As previously discussed, sampling clocks to ADCs must also be low noise and low jitter in order to achieve the required SNR performance.

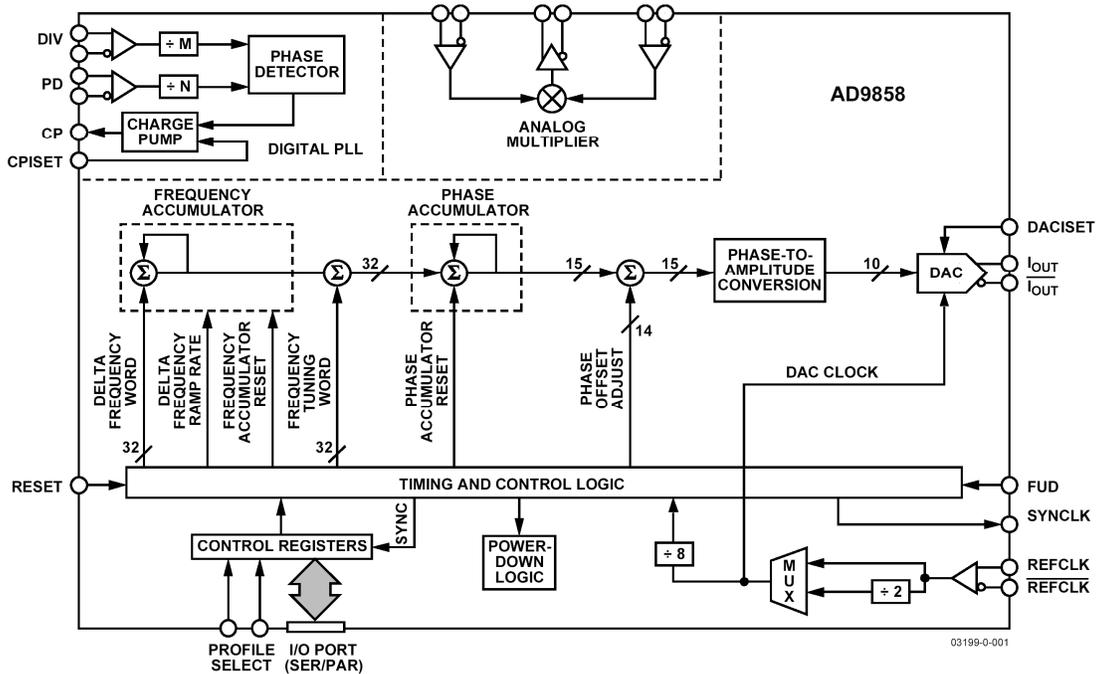
The two most popular methods for frequency synthesis are phase-locked-loops (PLLs) and direct digital synthesis (DDS). In many cases, a combination of the two offers the optimum solution. PLLs can generate frequencies well into the GHz range, but don't have the tuning flexibility of DDS. Since the upper frequency output of DDS systems is limited by the output DAC clock rate, DDSes generally are limited to an output frequency of approximately 500 MHz. It is common for DDSes to drive PLLs, a combination which takes advantage of both techniques.

Dedicated crystal oscillators provide the lowest noise and phase jitter, however they are expensive. Many systems therefore use a lower-cost combination of a phase-locked loop (PLL) and a VCXO (voltage-controlled crystal oscillator) followed by a bandpass filter to generate a low jitter sampling clock from a noisy system clock.

Analog Devices makes a number of PLLs and clock generation and distribution ICs suitable for this function.

Switching supply and noise modulate the fundamental output frequency as shown in the figure. This sensitivity of PLLs and DDSes is rarely specified on data sheets. Experiments were conducted on a representative DDS system to explore this sensitivity.

AD9858 1GSPS DDS with Phase Detector and Analog Multiplier



This figure shows a block diagram of one of Analog Devices' DDS ICs. The AD9858 is a direct digital synthesizer (DDS) featuring a 10-bit DAC operating up to 1 GSPS. The AD9858 uses advanced DDS technology, coupled with an internal high speed, high performance DAC to form a digitally programmable, complete high frequency synthesizer capable of generating a frequency-agile analog output sine wave at up to 400 MHz.

The AD9858 is designed to provide fast frequency hopping and fine tuning resolution (32-bit frequency tuning word). The frequency tuning and control words are loaded into the AD9858 via parallel (8-bit) or serial loading formats.

The AD9858 contains an integrated charge pump (CP) and phase frequency detector (PFD) for synthesis applications requiring the combination of a high speed DDS along with phase-locked loop (PLL) functions.

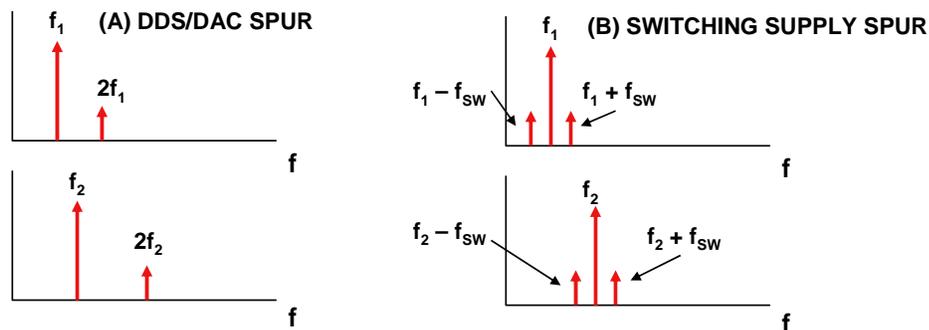
Another benefit of the DDS approach to frequency synthesis is the ability to very accurately and reliably inject phase offsets. 14 bits of phase control allow fine adjustments to ~0.022 degrees as well as supporting phase hopping in the same way that frequency hopping is supported.

Note that a second accumulator has been included in the DDS architecture. Shown here specifically driving the frequency tuning word, this enables a very easy and well controlled method for sweeping across a range of frequencies rather than holding at, or jumping between, specific frequencies. The newest DDS chips allow the second accumulator to drive the phase and amplitude control functions of the DDS as well, so that either of these may be swept instead of the frequency.

An analog mixer is also provided on-chip for applications requiring the combination of a DDS, PLL, and mixer, such as frequency translation loops, tuners, and so on. The AD9858 also features a divide-by-two on the clock input, allowing the external clock to be as high as 2 GHz.

Determining If Spurs Are Coming from Power Supply in DAC/DDS Systems

- ◆ (A) If the frequency offset of a spur relative to the fundamental output frequency changes as the output frequency changes, then the DDS DAC is probably the source of the spur.
- ◆ (B) If frequency offset of spur relative to the fundamental frequency output remains unchanged as the output frequency changes, then the spur is not coming from the DDS DAC. This would be the case of a power supply ripple component modulating the DDS output, or modulation on the reference clock.



Spurious free dynamic range (SFDR) is a key specification for a DDS system output, but determining the source of unwanted spurs can sometimes be a daunting task unless some fundamentals are understood.

The most common source of spurs are those created by the DDS DAC itself. Manufacturers go to great lengths to design low glitch high SFDR DACs, and typically specify SFDR as a function of output frequency, output amplitude, DAC update rate, etc.

Spurs can also occur if the output frequency is an exact submultiple of the DAC update rate. This is a well known effect which is caused when quantization noise becomes correlated with the output frequency rather than remaining randomly distributed over the Nyquist bandwidth.

The most common type of output spur is created by the non-linearity of the DAC and its switches and occurs at harmonics of the fundamental output frequency. This is increasingly true as the output frequency is increased to its upper limit, which is usually about 1/3 the update rate.

The offset of these spurs from the fundamental output frequency changes as the output frequency changes as shown in (A) for the second harmonic.

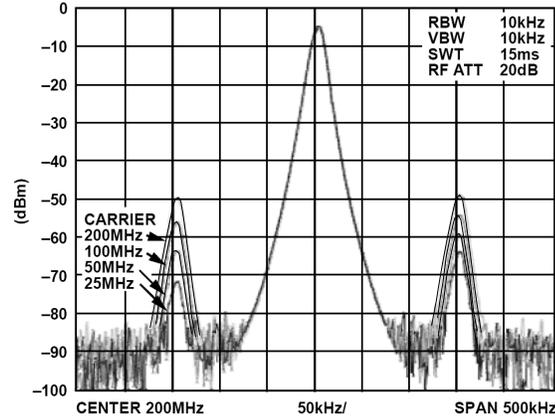
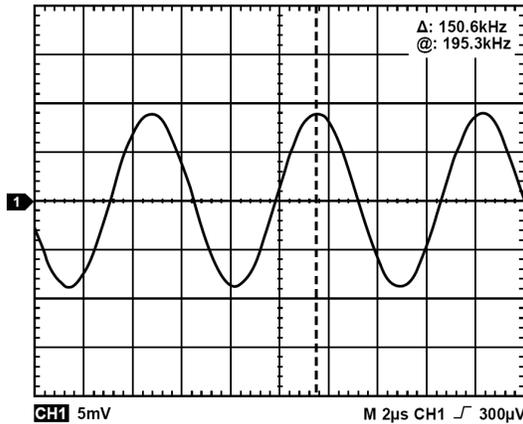
On the other hand, the ripple frequency of a power supply modulates the fundamental output frequency producing spurs which are a constant offset from the fundamental as in (B). The offset remains constant regardless of the fundamental output frequency. The separation of the spurs from the fundamental is equal to the switching frequency, making them fairly easy to identify. There can be other spurs, but these close-in spurs are generally the largest ones.

It should be noted that spurs on the DDS reference clock produce the same effect as ripple spurs on the power supply, so care must be taken that the reference clock is clean. If the internal DDS PLL is enabled, then it can produce spurs which are offset from the carrier frequency by an amount equal to the PLL reference frequency.

Superposition of Four DDS Output Carriers with 150kHz AM Modulation on AVDD Power Supply

+1.8V POWER SUPPLY MODULATION:
16mV (p-p), ($\pm 0.44\%$), 150kHz

AD9959 DDS OUTPUT SPECTRUM:
 $f_s = 500\text{MSPS}$, $f_{\text{OUT}} = 25\text{MHz}, 50\text{MHz}, 100\text{MHz}, 200\text{MHz}$ (Superimposed)



This shows an actual DDS output for four output frequencies, where the 1.8 V power supply is modulated by a 150 kHz, 16 mV p-p sinewave. The DAC update rate is 500 MSPS.

The 25 MHz, 50 MHz, 100 MHz, and 200 MHz outputs are superimposed on each other. In each case the 150 kHz sidebands appear at a constant offset of 150 kHz from the fundamental carrier frequency. (See Reference 1.)

Notice that the frequency offset of the spur on the output remains fixed in frequency offset to all four of the carrier frequencies. However, the amplitude of the spur follows a $20 \log(x)$ change where x is the ratio of the frequency of the DDS carrier output to the reference clock frequency. In other words, each time the carrier frequency is doubled, the spur amplitude increases by 6 dB. (See Reference 2.)

This data was taken with the internal DDS PLL disabled and driving the reference clock input directly from a 500 MHz low noise spectrally pure oscillator.

REFERENCES:

1. David Brandon, "Determining if a Spur is Related to the DDS/DAC or to Some Other Source (For Example, Switching Supplies)," Application Note AN-927, Analog Devices, 2007. Available at www.analog.com.
2. Paul Smith, "Little Known Characteristics of Phase Noise," Application Note AN-741, Analog Devices, 2004. Available at www.analog.com.

DDS RFDR/PSR Analysis (Very Approximate)

- ◆ RFDR = 50 dB from previous photo.
- ◆ $V_{FS_PP} = 1.0V$ (Typical DAC output voltage into resistive load)
- ◆ $\Delta V_{SS_PP} = 16mV$ @ 150kHz (from previous figure)
- ◆ $PSR = RFDR - 20\log(V_{FS_PP}/\Delta V_{SS_PP}) = 50 - 35.9 = 14.1dB$

- ◆ Frequency synthesis ICs (PLLs, DDSes) do not generally have PSR specifications.
- ◆ Power supply ripple frequency spurs can be distinguished from DDS DAC spurs, but it may be too late when you find them.

- ◆ Summary: Should always use well filtered LDO to supply PLLs and DDS unless experimentation and/or manufacturer's data indicates otherwise.

We can perform a very crude calculation which gives the PSR of the DDS system in terms of the spur amplitude.

From the spectral outputs, the worst case spur occurs for a 200 MHz carrier frequency, and its amplitude is approximately 50 dB below full-scale. Therefore, assume that RFDR = 50 dB.

The full-scale voltage output of the DDS DAC is approximately 1 V p-p into a 50 Ω load. Therefore $V_{FS_PP} = 1.0 V$.

The 150 kHz power supply ripple injected onto the 1.8 V supply has an amplitude of approximately 16 mV.

The PSR is then calculated from our previous formula,

$$PSR = RFDR - 20\log(V_{FS_PP} / \Delta V_{SS_PP}) = 14.1 \text{ dB.}$$

To summarize, power supply ripple spurs can be distinguished from DDS DAC spurs, but it may be too late when you find them.

The conservative approach is to always use well filtered LDOs to supply PLLs and DDSes unless experimentation and/or manufacturer's data indicates otherwise.

Reducing Power Supply Noise by Bulk Filtering

We will discuss power supply filtering in two parts. The first is known as bulk filtering, and generally occurs directly at the output of the switching supply. The input and output capacitors are included in this topic, as well as additional filtering components which may be required.

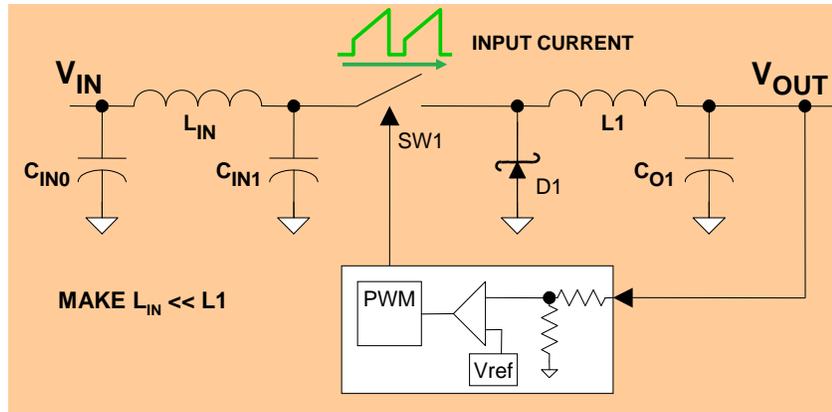
The second type of filtering is the localized decoupling which must be applied to each IC power pin. Proper localized decoupling is mandatory for modern ICs to function properly.

Another method to reduce power supply ripple and noise is to use an LDO following the switching supply. This method must be used with caution, however, because LDOs generally have poor PSR at switching frequencies.

The final method to reduce the effects of power supply ripple and noise is to physically separate the power supply from the rest of the circuits. This can usually be achieved with proper PC board layout.

Buck Converter with Input Filter

- ◆ Buck switchers have discontinuous input current
- ◆ Input filter can be used to reduce conducted noise
- ◆ Input filter can prevent beat frequencies between switchers
- ◆ Typical L_{IN} is much smaller than $L1$

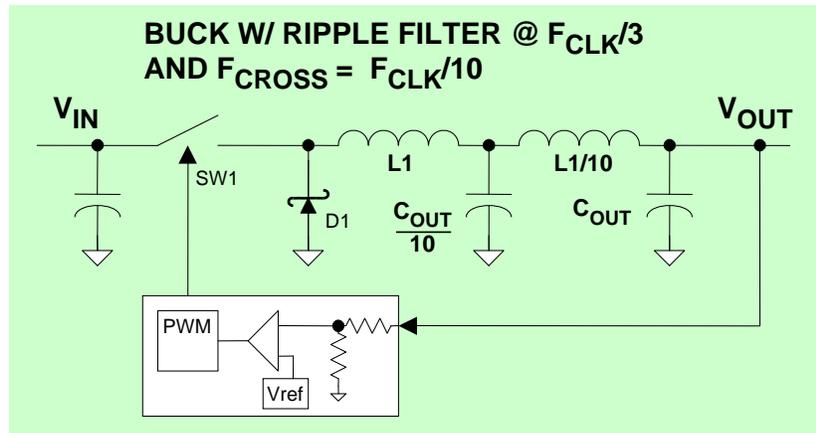


A buck converter has a discontinuous input current which may require additional filtering in order to reduce conducted EMI and prevent crosstalk. In the above circuit, the input filter inductor L_{IN} is generally much smaller than $L1$.

Multiple buck converters used without input filters can produce a beat frequency ripple at the input and output of each converter. For this reason, multiple switchers often use a common synchronized clock.

Buck Converter with Output Ripple Filter

- ◆ Output filter can be added to reduce ripple and spikes
- ◆ Good layout is required to get the full benefit
- ◆ Closing the feedback loop around the filter is tricky
- ◆ Putting the filter outside the feedback loops hurts transient response
- ◆ Ripple out can be reduced to < 1mV p-p



The buck converter has a continuous output ripple current, but further filtering may be required. A single LC filter may be limited by both component and PCB trace ESR and ESL.

Increasing the value of the inductor L1 will reduce the ripple current and the output ripple voltage, but also increases the size and cost of the circuit. Large values for L1 can degrade the step response. In many cases, an additional LC filter as shown in this figure can reduce the output voltage ripple with less performance degradation and at lower cost. However, closing the feedback loop around the filter can be tricky because of the additional poles.

The value for L1 is chosen as a normal part of the design of the buck converter. C_{OUT} and L1 produce a double pole at $1/[2\pi\sqrt{L1 \cdot C_{OUT}}]$. The additional pole created by L1/10 and $C_{OUT}/10$ is positioned at $F_{CLK}/3$. This will attenuate the ripple by 10 dB.

The loop unity gain frequency (F_{CROSS}) should be set $< F_{CLK}/10$ to provide a fast loop that is stable. Details get into compensation methods and loop control modes and some more mathematics.

As an example, assume that $F_{CLK} = 1$ MHz, $L1 = 10$ μ H, $L1/10 = 1$ μ H. We have the following equation:

$$\frac{F_{CLK}}{3} = \frac{1}{2\pi\sqrt{\frac{L1}{10} \times \frac{C_{OUT}}{10}}}$$

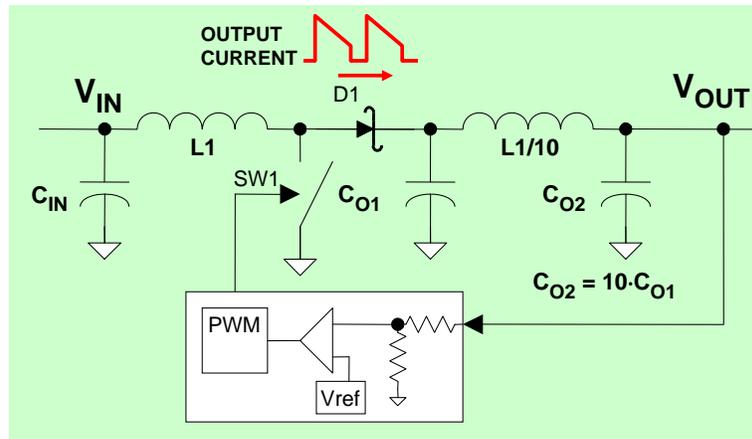
Substituting the above values for F_{CLK} and L1 and solving for C_{OUT} , we obtain $C_{OUT} = 2.3$ μ F and $C_{OUT}/10 = 0.23$ μ F.

Proper layout in conjunction with the use of output filtering as shown here can reduce the peak-to-peak output ripple to less than 1 mV.

Note that simply adding an LC to reduce ripple will affect compensation and step response. Better step response and loop stability fall out of the "big L little C followed by little L big C" implementation described above. If step response is not an issue, then the filter can be placed outside the feedback loop. In this case the voltage dropped across the external ESR of the inductor will not be included in the feedback correction.

Boost Converter with Output Ripple Filter

- ◆ Ripple and switching spikes are often too high, especially when powering analog circuits
- ◆ Output filter reduces capacitance needed for C_{O1}
- ◆ Output filter reduces RMS ripple spec for C_{O2}
- ◆ Total size/cost may actually decrease



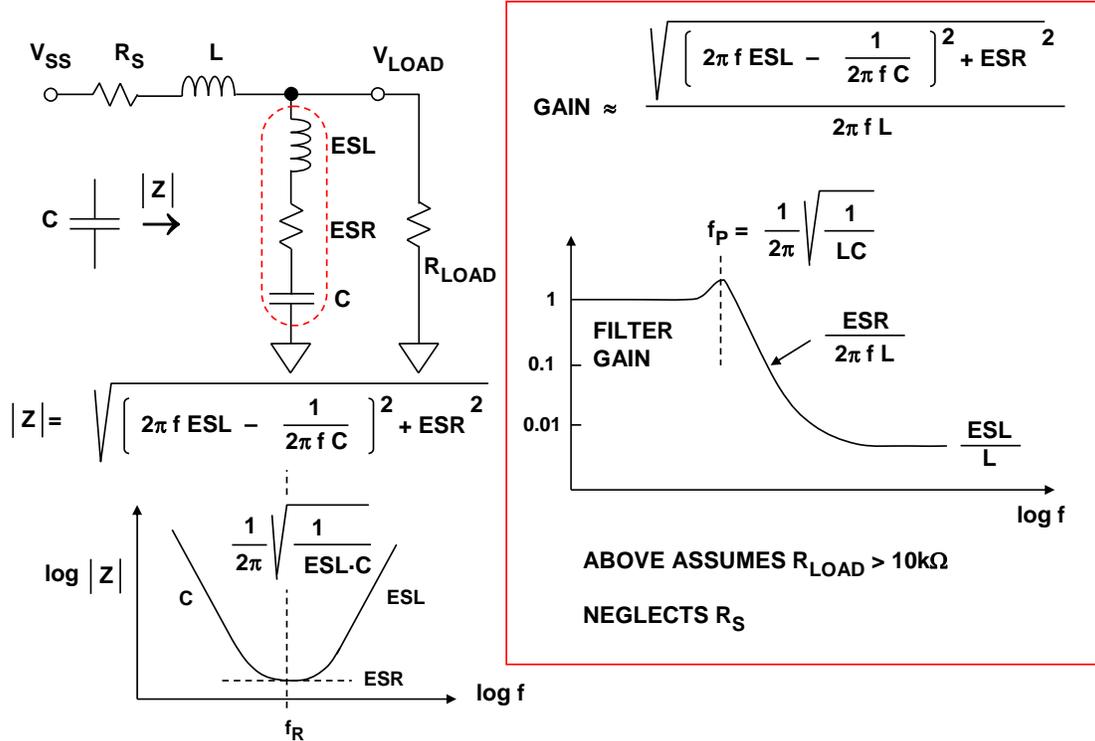
The boost converter has continuous input current, but discontinuous output current. The output ripple and spikes are therefore more troublesome than for the buck converter, especially if powering analog circuits.

Although the output ripple and noise can be reduced by adding more and more low ESR bulk capacitance, an attractive alternative is to add an additional stage of filtering. This shows an additional LC filter on the output, consisting of $L1/10$ and C_{O2} . The additional filter reduces the capacitance required for C_{O1} and reduces the rms ripple requirement for C_{O2} . After optimizing the filter, the total size and cost of the overall circuit may actually decrease than by simply increasing C_{O1} .

C_{O2} is generally $C_{O1} \times 10$ or more. C_{O1} should be low ESR (ceramic) to remove the spikes and limit ripple. C_{O2} is usually much larger to provide the bulk needed for step response and loop stability.

Reversing the capacitor placement will degrade stability and load step response.

LC Filter Attenuation Approximation



Generalized LC filter design can be implemented using a SPICE-based simulation program such as National Instruments Multisim™. Analog Devices offers a special edition of Multisim that is free and can be downloaded. The free version is similar to the full-featured version except for the number of nodes and components allowed.

This simple LC filter model includes the most important parasitics associated with the inductor and the capacitor.

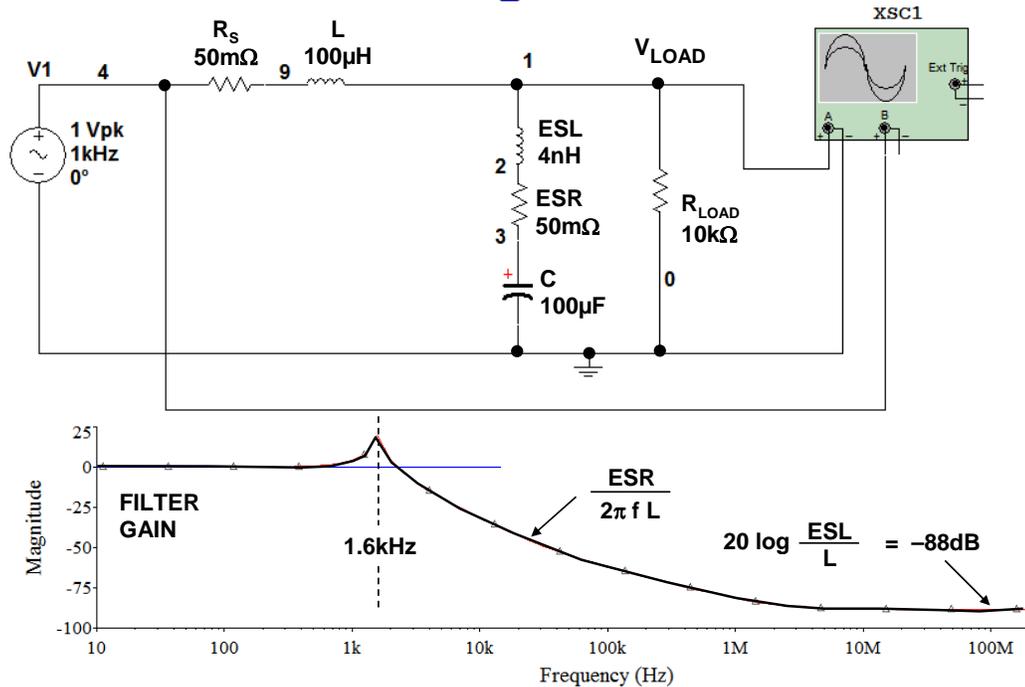
The impedance of the capacitor is shown on the left. At low frequency, the capacitance determines the impedance. As the frequency approaches the self-resonant frequency of the capacitor, the ESR of the capacitor dominates. At higher frequencies, the capacitor ESL dominates.

The "peak" in the overall filter gain plot occurs when the input inductor, L, resonates with the capacitor, C. If desired, the peaking can be eliminated by adding an additional resistance in series with the inductor. The generalized frequency response of this network is shown on the right.

After the resonant peak, the gain drops at a rate of 6 dB/octave due to the inductor, L. It then flattens out at a value approximately equal to ESL/L . This curve neglects the effects of the load resistance and the ESR and parasitic capacitance of the inductor.

The load impedance is chosen to be 10 kΩ, representing that of a single low power IC. In a practical simulation, the load resistance should be chosen so that the load current approximates that of the IC.

Simulated Gain of LC Network Using NI Multisim Analog Devices Edition



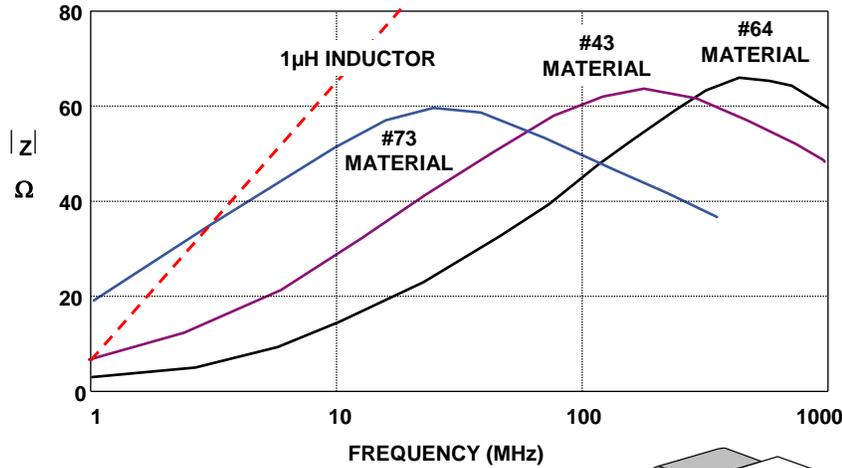
This simple LC filter model includes the most important parasitics associated with the inductor and the capacitor. The Multisim model is shown for an inductor of 100 μH ($\text{ESR} = 50 \text{ m}\Omega$) and a 100 μF capacitor ($\text{ESR} = 50 \text{ m}\Omega$, $\text{ESL} = 4 \text{ nH}$). The ESR and ESL values are typical of an electrolytic capacitor. The load is simulated with a 10 $\text{k}\Omega$ resistor.

The "peak" in the overall filter gain plot occurs at approximately 1.6 kHz when the input 100 μH inductor resonates with the 100 μF capacitor. If desired, the peaking can be eliminated by adding an additional resistance in series with the inductor.

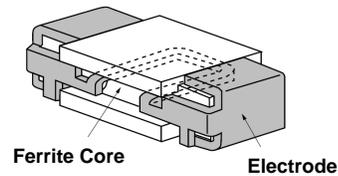
Simple LC filters such as this one can be easily simulated using Multisim. It is important to include the PC board parasitics, especially the parasitic inductance and resistance associated with vias and interconnections. If designed properly, this type of filter should be capable of providing at least 60 dB of attenuation to switching power supply noise and ripple.

More detailed discussions of parasitics associated with inductors and capacitors can be found in Section 4.

Ferrite Bead Impedance Compared to a 1μH Inductor



Courtesy: Fair-Rite Products Corp, Walkill, NY
(www.fair-rite.com)



Ferrite beads are often used in power supply filters, and they are available in small surface mount packages. Unlike inductors, the ferrite bead impedance is mostly resistive at the higher frequencies as shown here for several types of ferrite materials. Ferrite beads are equivalent to lossy inductors. When used in a simple LC filter, the effective Q of the bead is low enough so that there is usually no peaking.

The dc resistance of a ferrite bead is very low (10 to 50 mΩ typical), and care must be taken that the current through the bead does not exceed the maximum specified rated saturation current. If it does, the ferrite bead becomes a short circuit. Beads with maximum currents up to several amps are available in surface mount packages.

The figure shows the impedance of a 1 μH inductor as the dotted line compared to the bead impedances. If high attenuation is required using an LC filter, then the inductor is a better choice.

Reducing Ripple and Noise by Localized Decoupling and Filtering

What Is Proper Localized Decoupling?

- ◆ **A large electrolytic capacitor (typ. 10 μF – 100 μF) no more than 2 in. away from the chip.**
 - **The purpose of this capacitor is to be a reservoir of charge to supply the instantaneous charge requirements of the circuits locally so the charge need not come through the inductance of the power trace.**

- ◆ **A smaller cap (typ. 0.01 μF to 0.1 μF) as physically close to the power pins of the chip as is possible.**
 - **The purpose of this capacitor is to short the high frequency noise away from the chip.**

- ◆ **Optionally a small ferrite bead or inductor in series with the supply pin.**
 - **Localizes the noise in the system.**
 - **Keeps external high frequency noise from the IC.**
 - **Keeps internally generated noise from propagating to the rest of the system.**

As previously stated, the electrolytic type large value capacitors are used as local charge reservoirs. This means that the instantaneous current requirements do not have to be met by the power supply, which may be located an appreciable distance away with a considerable amount of inductance and resistance in the line.

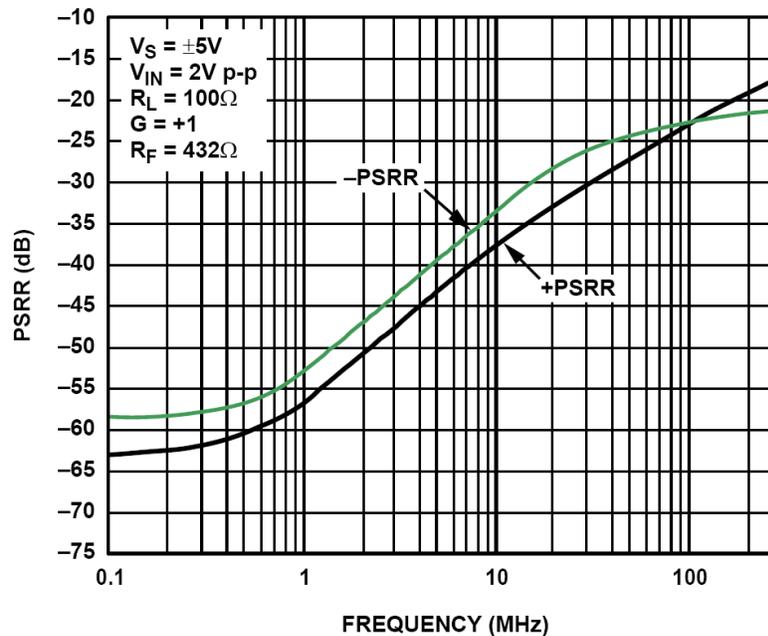
Smaller value capacitors are used to short the high frequency interference away from the chip. Relevant parameters here are low equivalent series inductance (ESL) and equivalent series resistance (ESR). Quite often multilayer ceramics are excellent choices for these applications. At frequencies above the resonant frequency of the capacitor, the ESL dominates, so smaller packages generally give lower inductance at the expense of smaller values of capacitance.

Ferrites (nonconductive ceramics manufactured from the oxides of nickel, zinc, manganese, or other compounds) are useful for decoupling in power supply filters. At low frequencies (<100 kHz), ferrites are inductive; thus they are useful in low-pass LC filters. Above 100 kHz, ferrites becomes resistive, an important characteristic in high-frequency filter designs. Ferrite impedance is a function of material, operating frequency range, dc bias current, number of turns, size, shape, and temperature.

The ferrite beads or inductors may not always be necessary, but they will add extra high frequency noise isolation and decoupling, which is often desirable. Possible caveats here would be to verify that the beads never saturate, especially in circuits that consume high currents. When a ferrite saturates it becomes nonlinear and loses its filtering properties.

Note that some ferrites, even before full saturation occurs, can be nonlinear; so if a power stage is required to operate with a low distortion output, this should also be checked in a prototype.

Power Supply Rejection Ratio vs. Frequency for the AD8000 1.5GHz Op Amp



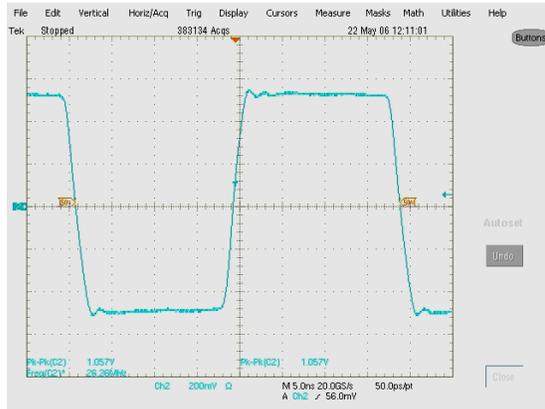
Why is decoupling necessary?

This graph shows how the power supply rejection (PSR) of an amplifier varies with frequency. At high frequencies there is little isolation between the power supply pin and the amplifier output. Therefore, a large portion of any high frequency energy on the power line will couple to the output directly. So it is necessary to keep this high frequency energy from entering the chip in the first place. This is done by using a small ceramic capacitor to short the high frequency signals away from the chip.

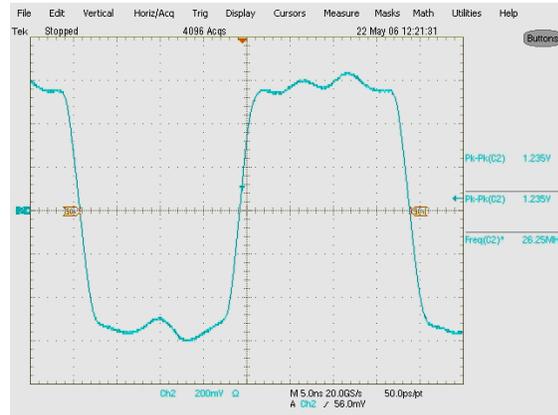
Power supply rejection of data converters has been discussed earlier in this section.

Another aspect to decoupling is the lower frequency interference. Here we use larger electrolytic capacitors.

Effects of Decoupling on Performance of the AD8000 Op Amp



PROPER DECOUPLING



NO DECOUPLING

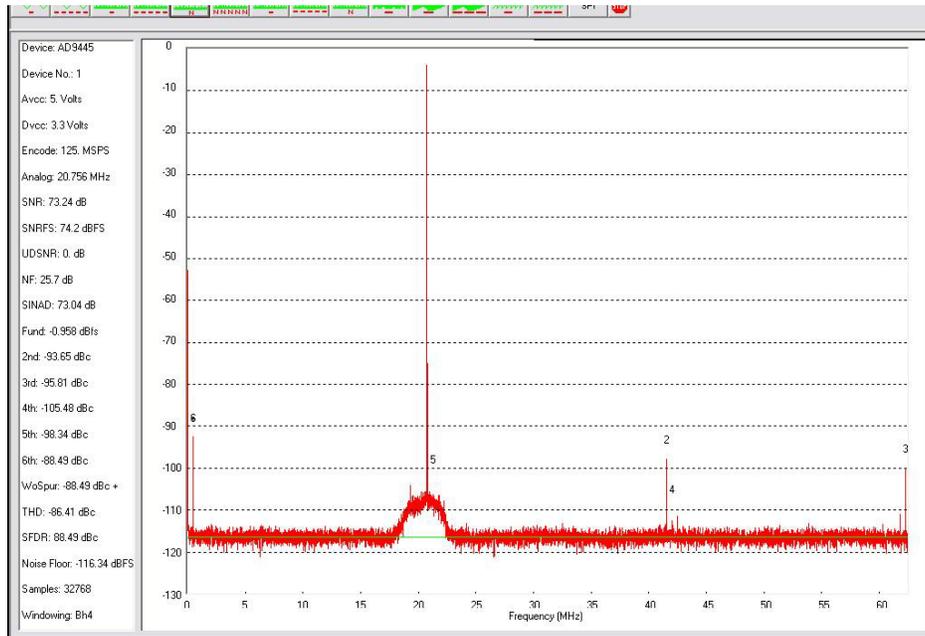
Here is an example of what could happen to the response of an op amp with no decoupling.

Both of the oscilloscope graphs were taken on the same evaluation board.

The difference is that on the right the decoupling capacitors were removed.

Other than that, everything remained the same. In this case the device was an AD8000, a 1.5 GHz high speed current feedback op amp, but the effect will occur in most any high speed IC.

FFT Plot for the AD9445 Evaluation Board with Proper Decoupling

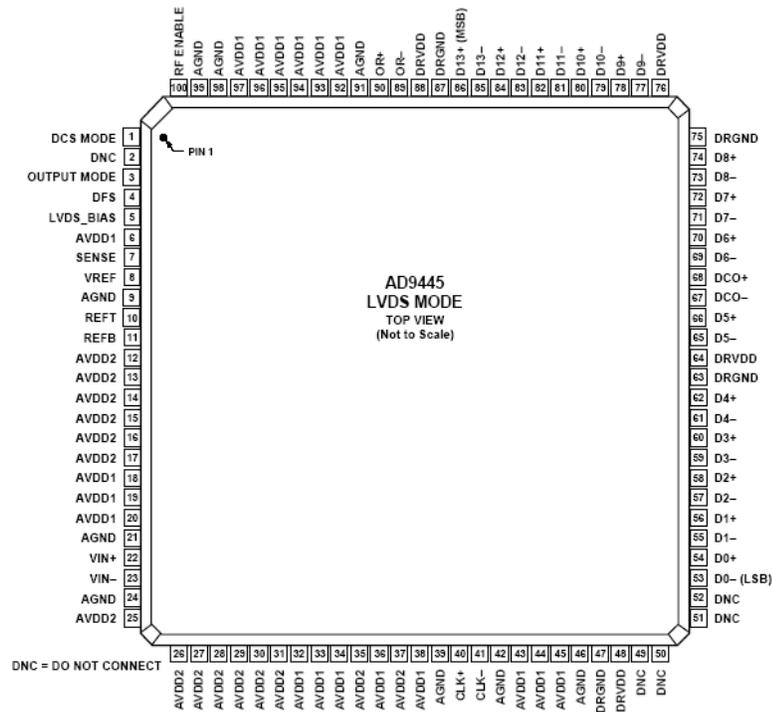


We will now examine the effect of proper and improper decoupling on a high performance data converter, the AD9445 14-bit, 105 MSPS/125 MSPS ADC.

A converter will typically not have a PSR specification, and proper decoupling is very important.

Here is the FFT output of a properly designed circuit. In this case, we are using the evaluation board for the AD9445. Note the clean spectrum.

AD9445 Pinout Diagram



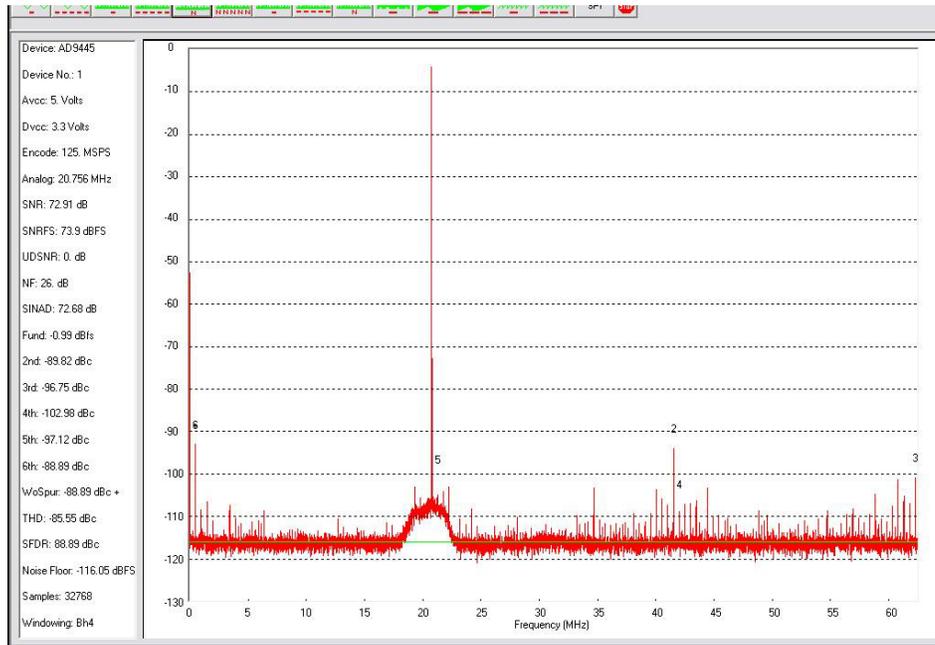
This is the pinout of the AD9445. Note that there are multiple power and ground pins. This is done to lower the impedance of the power supply (pins in parallel).

There are 33 analog power pins. 18 pins are connected to AVDD1 (which is $+3.3\text{ V} \pm 5\%$) and 15 pins are connected to AVDD2 (which is $+5\text{ V} \pm 5\%$). There are four DVDD (which is $+5\text{ V} \pm 5\%$) pins.

On the evaluation board used in this experiment, each power pin has a decoupling cap.

In addition, there are several $10\ \mu\text{F}$ electrolytic capacitors as well.

FFT Plot for an AD9445 Evaluation Board with Caps Removed from the Analog Supply



Here is the spectrum with the decoupling caps removed from the analog supply.

Note the increase in high frequency spurious signals, as well as some intermodulation products (lower frequency components).

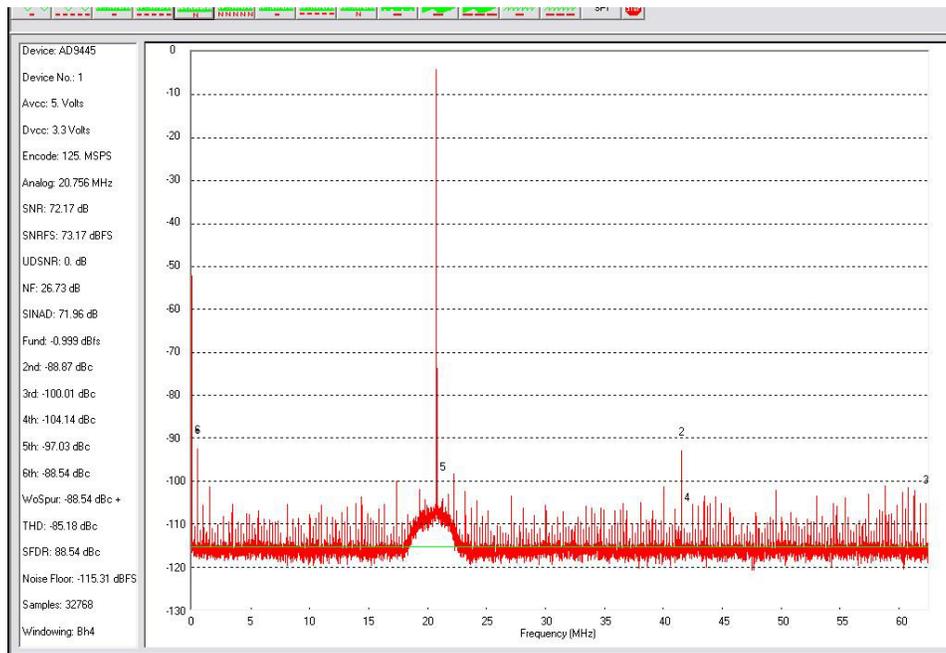
The SNR of the signal has obviously degenerated.

The only difference between this figure and the last is removal of the decoupling capacitors.

Again we used the AD9445 evaluation board as a test vehicle.

In the experiment, the capacitors were removed one at a time. Initially, the SNR degradation was approximately proportional to the number of capacitors removed. With fewer and fewer remaining decoupling capacitors, the SNR curve began to flatten (similar to an amplifier's 1 dB compression point).

FFT Plot for an AD9445 Evaluation Board with Caps Removed from the Digital Supply



Here is the result of removing the decoupling caps from the digital supply. Again note the increase in spurs. Also note the frequency distribution of the spurs.

Not only do these spurs occur at high frequencies, but across the spectrum.

This experiment was run with the LVDS version of the converter.

We can assume that the CMOS version would be worse because non-saturating current mode LVDS logic is less noisy than saturating CMOS logic.

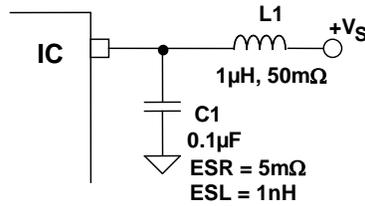
More information on PC board design techniques can be found in the following three references:

Walt Kester, *Analog-Digital Conversion*, Analog Devices, 2004, ISBN: 0916550273 Chapter 9. Also available as *Data Conversion Handbook*, Elsevier-Newnes, 2005, ISBN: 0750678410, Chapter 9.

Walt Jung, *Op Amp Applications*, Analog Devices, 2002, ISBN: 0-916550-26-5, Chapter 7. Also available as *Op Amp Applications Handbook*, Elsevier-Newnes, 2004, ISBN: 0-7506-7844-5, Chapter 7.

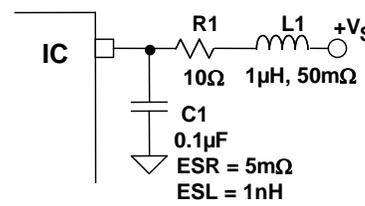
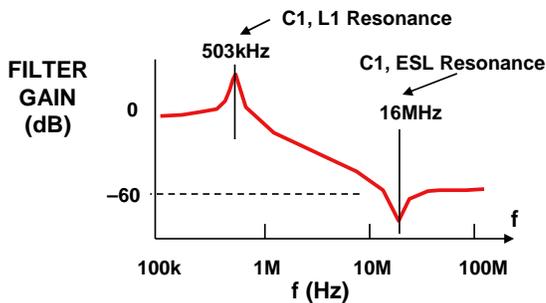
Hank Zumbahlen, *Linear Circuit Design Handbook*, Elsevier-Newnes, 2008, ISBN-10: 0750687037, ISBN-13: 978-0750687034, Chapter 12.

Resonant Circuit Formed by Power Supply Decoupling Network

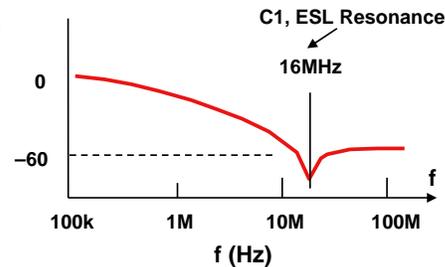


(A) EQUIVALENT DECOUPLED POWER LINE CIRCUIT RESONATES AT:

$$f = \frac{1}{2\pi\sqrt{LC}}$$



(B) SMALL SERIES RESISTANCE CLOSE TO IC REDUCES Q. OR USE FERRITE BEAD INSTEAD OF INDUCTOR



An inductor in series or parallel with a capacitor forms a resonant, or "tuned," circuit, whose key feature is that it shows marked change in impedance over a small range of frequency. Just how sharp the effect is depends on the relative Q (quality factor) of the tuned circuit. The Q of a resonant circuit is a measure of its reactance to its resistance.

$$Q = 2\pi f(L/R)$$

If stray inductance and capacitance in a circuit forms a tuned circuit, then that tuned circuit may be excited by signals in the circuit, and ring at its resonant frequency.

Most ceramic capacitors from 0.01 µF to 0.1 µF will self-resonate well above a few MHz. For example, a 0.1 µF capacitor with an ESL of 1 nH resonates at 16 MHz. However in the circuit shown on the left (A), the 0.1µF capacitor and 1 µH of external inductance resonates at 500 kHz. Left unchecked, this causes a peaking in the filter gain.

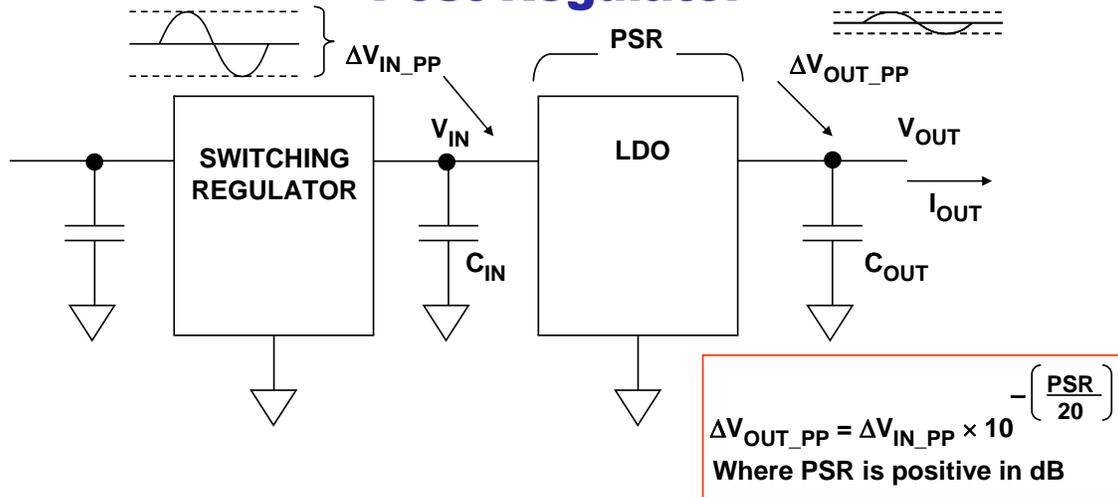
Should an undesired power line resonance be present, the effect may be minimized by lowering the Q of the inductance. This is most easily done by inserting a small resistance (~10 Ω) in the power line close to the IC, as shown in the right case (B).

The resistance should be kept as low as possible to minimize the voltage drop across the resistor. The resistor should be as large as needed, but no larger. An alternative to a resistor is a small ferrite bead which looks primarily resistive at the resonant frequency (see page 3.62).

Reducing Power Supply Noise Using LDO Post Regulators

www.analog.com/lido

Reducing Ripple Using an LDO as a Post Regulator

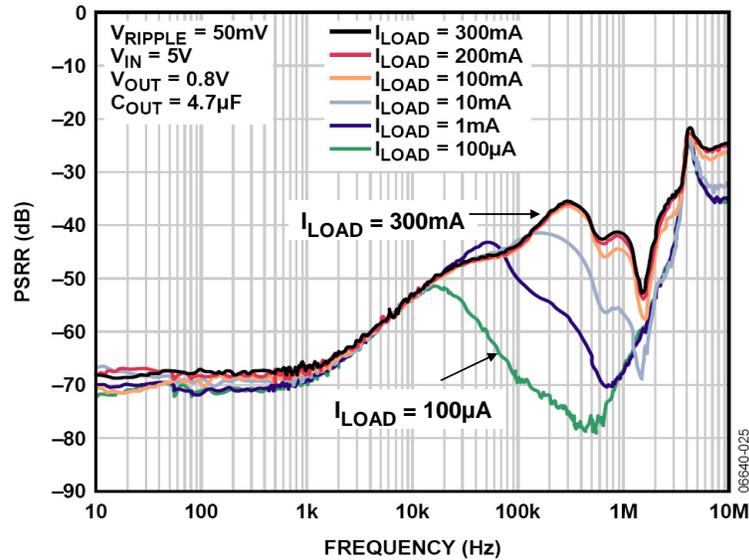


- ◆ Typical PSR @ 1MHz = 35dB to 60dB
- ◆ Specified for a given value of output capacitance, C_{OUT}
- ◆ Adding additional capacitance improves PSR
- ◆ However, LDO must be stable for selected value of C_{OUT}
- ◆ PSR increases for small load currents
- ◆ PSR is a function of $V_{IN} - V_{OUT}$

It is a common misconception that LDO post regulators provide excellent filtering for power supply noise. This is certainly true at low frequencies, but the PSR of many LDOs at typical switching frequencies is surprisingly low—somewhere between about 35 dB and 60 dB at 1 MHz. This PSR is primarily determined by the internal LDO buffer amplifier.

The LDO PSR is a function of output capacitance, load current, and the difference between the input and output voltage, $V_{IN} - V_{OUT}$. These variables must be specified in order for the PSR to be meaningful.

ADP1708 1A CMOS LDO PSR



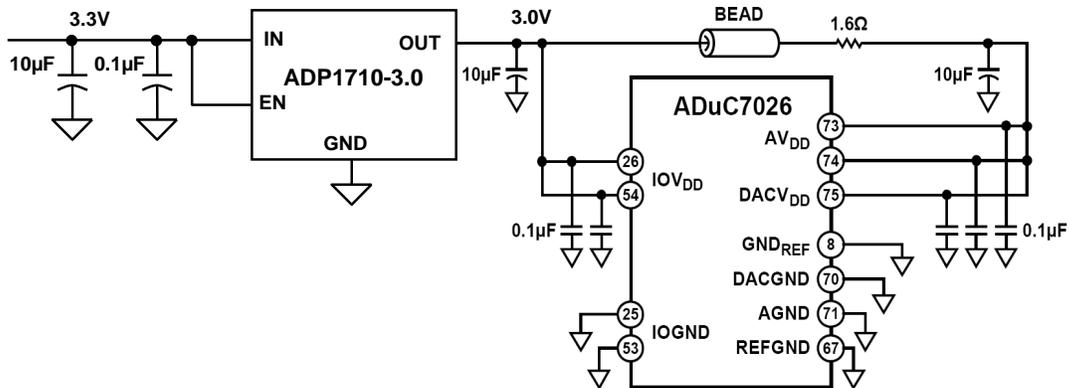
"Dip" in curves due to output capacitance self-resonance

This shows the PSR of the ADP1708 1 A CMOS LDO as a function of frequency and load current. The "dip" in the PSR curves is more pronounced for small load currents, and is due to the output capacitor self-resonance. In the above example, the resonant frequency of the 4.7 μF capacitor and its 50 nH ESL is approximately 300 kHz.

Data sheets for LDOs typically give the PSR for a number of input/output voltages. The data in this graph is for an input voltage of 5 V and an output voltage of 0.8 V. PSR typically decreases as $V_{IN} - V_{OUT}$ decreases and approaches the dropout voltage.

The ADP220/ADP221 low noise, high PSRR LDO has 60 dB PSR at 100 kHz for an input voltage of 3.3 V, an output voltage of 2.8 V, and an output current of 100 mA.

Powering the ADuC7026 MicroConverter with the ADP1710 150mA LDO



In many cases it is wise to power the MicroConverter from an LDO rather than the noisy digital system supply. This figure shows the ADP1710 150 mA LDO supplying the 3.0 V to the ADuC7026 MicroConverter.

The ADP1710 supplies the IOV_{DD} digital power directly, and the AV_{DD} voltage is filtered with the ferrite bead, 1.6 Ω resistor, and 10 µF capacitor. The 0.1 µF capacitors are MLCC types and are placed directly at the IC power pins.

The ADP1710 has approximately 45 dB PSR at 1 MHz in the configuration shown in the figure.

LDO Regulator Noise

- ◆ LDO noise specified in several ways, but usually the RMS noise in a bandwidth of 10Hz to 100kHz
- ◆ Noise specification must give values of input and output capacitors
 - ADP1706-series is 125 μ V rms from 10Hz to 100kHz for $C_{IN} = C_{OUT} = 4.7\mu$ F. This corresponds to a noise spectral density of $125\mu\text{V}/\sqrt{(100\text{kHz})} = 395\text{nV}/\sqrt{\text{Hz}}$
 - ADP220/ADP221-series has 50 μ V rms noise from 10Hz to 100kHz for $C_{IN} = C_{OUT} = 1\mu$ F
- ◆ As with voltage references, a "noise reduction" pin may be available.
 - ADP1710 noise = 330 μ V rms from 10Hz to 100kHz, $C_{IN} = C_{OUT} = 1\mu$ F, no noise reduction pin.
 - ADP1711 noise = 40 μ V rms from 10Hz to 100kHz with 10nF capacitor on noise reduction pin.

LDO noise can be specified in a number of ways. Regardless of the method, it must be specified for given values of input and output capacitors.

In most cases, LDO noise is specified as an rms voltage over a 10 Hz to 100 kHz bandwidth.

The equivalent noise spectral density can be calculated by dividing this rms voltage by the square root of the measurement bandwidth. For the ADP1706 series, the rms noise in the 100 kHz bandwidth is 125 μ V rms, corresponding to a noise spectral density of approximately 395 nV/ $\sqrt{\text{Hz}}$.

For the ADP220/ADP221, the noise is 50 μ V rms from 10 Hz to 100 kHz with an input voltage of 3.3 V, an output voltage of 2.8 V, and an output current of 100 mA.

In some cases, a "noise reduction" pin may be available, as in the case of the ADP1711. Bypassing this pin with a 10 nF capacitor can reduce the rms noise from 125 μ V to 40 μ V rms.

Further LC filtering on the LDO output can reduce the noise even further if system requirements dictate.

Reducing Power Supply Noise by Physical Separation from Analog Circuits

Types of Coupling

- ◆ **Conducted (Most focus on this)**
 - **Noise on Power Supplies**
 - **Remedies**
 - ◆ **Low Impedance Ground Planes**
 - ◆ **Filtering and Decoupling**
 - ◆ **Component Layout**

- ◆ **Radiated (This is important also)**
 - **Primarily from Magnetic Switching Regulators**
 - **Remedies**
 - ◆ **Physical Separation from Analog Circuits**
 - ◆ **Component Layout (Minimize Loops)**
 - ◆ **Shielded Magnetic Devices**
 - ◆ **Add Extra Shielding**

- ◆ **PHYSICAL SEPARATION AVOIDS NOISE!**

Quite a bit of attention is given to conducted noise on power supplies, ground planes, etc. Most designers address these problems with the use of filtering and decoupling techniques.

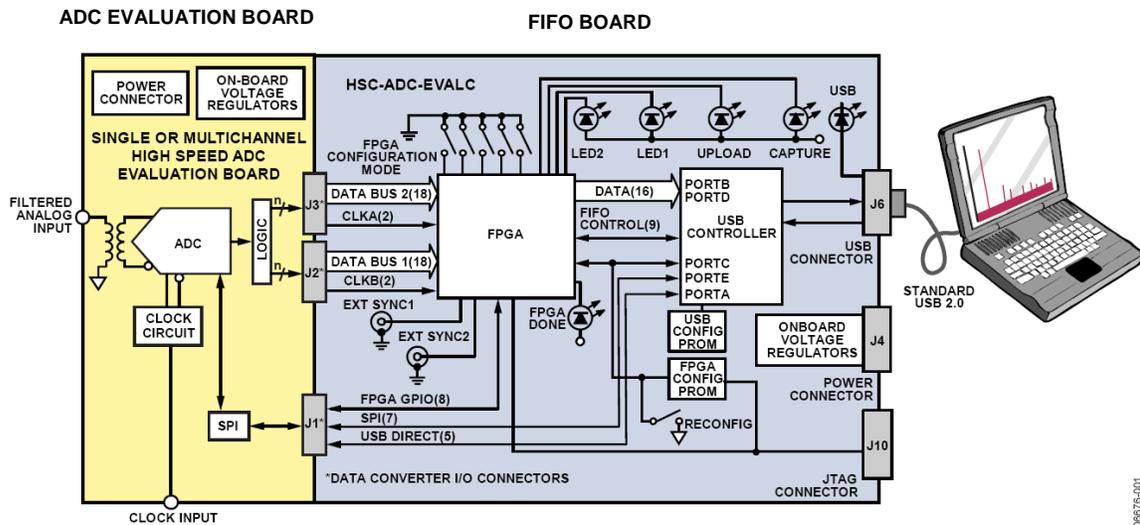
Another often neglected source of noise is that due to radiation, primarily from magnetic elements such as the inductors used in switching regulators. The high dv/dt and di/dt in these circuits often couples into the ground plane and any nearby circuits.

A very effective (and often overlooked) technique for reducing the effect of this type of noise is to simply separate sensitive circuits from the noisy ones. The magnetic field coupling decreases with the square of the distance of separation.

Proper component layout, physical separation, and the addition of extra shielding if required can usually eliminate most noise coupling problems.

ADC/FPGA System Evaluation Board Power Design

(Physical Separation Avoids Noise)



The Analog Devices' high speed ADC evaluation board system is a good example of proper component layout and signal routing. It encompasses several functions commonly found in modern systems:

- High speed, high performance ADC (12 to 16 bits, up to 250 MSPS)
- Clock generation circuits
- High speed FPGA for buffering ADC output data (Xilinx Virtex-4)
- USB and FPGA configuration EPROMs
- Control functions for interfaces and USB
- Point-of-load regulators for supply voltages

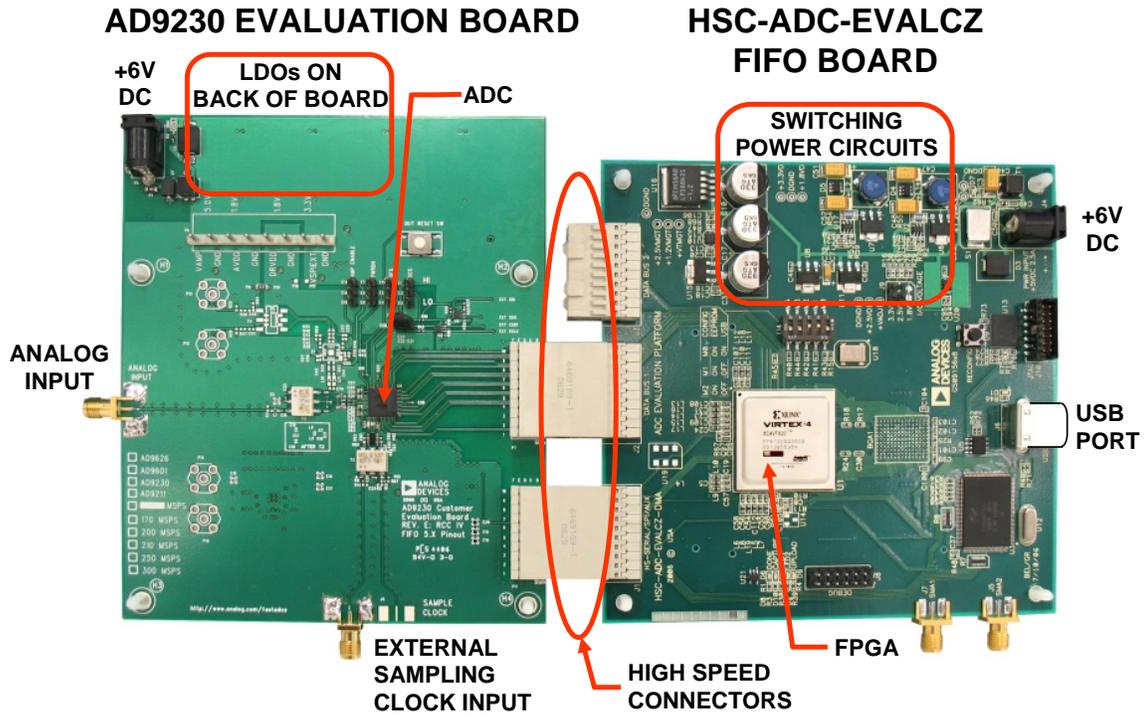
The system is designed to use a common memory board which interfaces to product-specific ADC evaluation boards. Connection between the two boards is made using high speed connectors.

Because this system is used to evaluate ADCs with high SFDR (>90 dB) and SNR (>80 dB) its layout has been optimized to achieve the maximum performance possible.

The boards have 4-layers with two outer components and signal layers, a ground plane layer, and a power plane layer. The boards use a single ground plane, but analog components are separated from digital components.

Switching supplies are used to power the FIFO board, and LDOs power the ADC on the evaluation board.

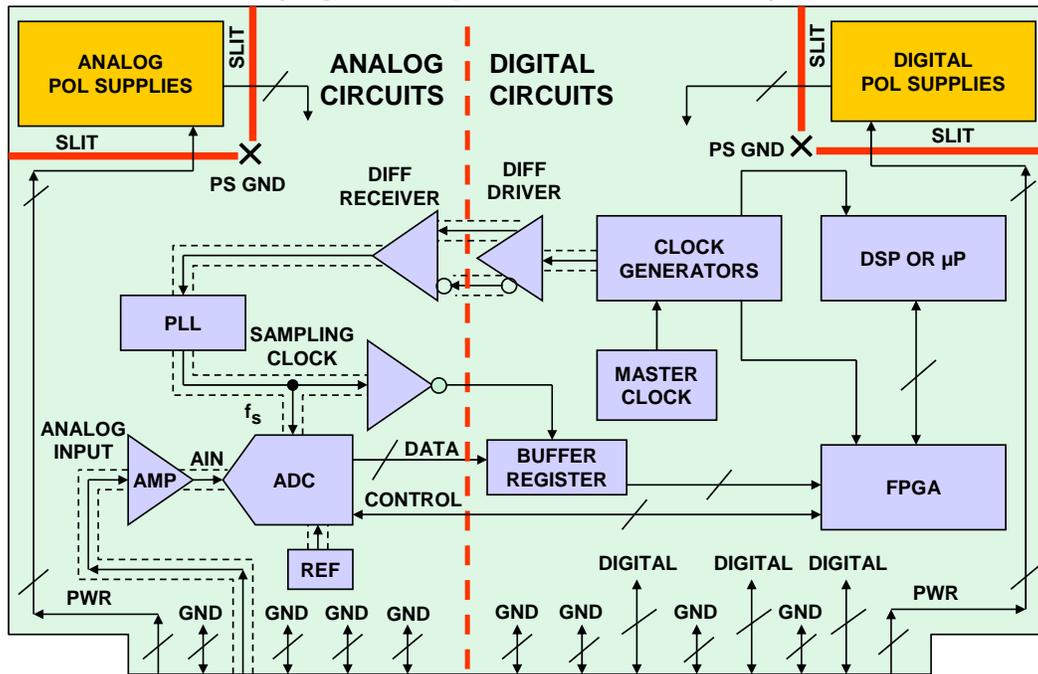
ADC/FPGA System Board Layouts
(Physical Separation Avoids Noise)



This shows a photo of an actual ADC evaluation board connected to the FIFO board. Note the location of the power circuits on each board.

The CAD files are available for all Analog Devices' evaluation boards and can be helpful in system layout.

Optimum PCB Layout Begins with Critical Component Placement (Physical Separation Avoids Noise)



This is an optimum PC board layout which incorporates many components in a typical system.

The dotted PCB traces are extremely critical and are kept well away from any digital traces. Note that the PLL which generates the sampling clock is located on the analog side of the board close to the ADC.

The digital circuits are located on the right side of the board. The master clock is transmitted across the interface using a differential driver and receiver and then to the PLL. The function of the PLL is to "clean up" the noisy digital clock and reduce phase noise and jitter.

The analog and digital POL supplies are located away from the rest of the circuits. This is especially important if switching converters are used. The ground plane is slit so that the noisy switching currents are isolated from the ground plane. This corresponds to the "power ground" point in the switching supply circuit.

At least 30% of the connector pins should be dedicated to ground. Ground pins are used to isolate the critical analog input signal from the other traces. Ground and power can be used to isolate other signals as well.

Noise and Ripple Reduction Techniques Summary

- ◆ **Proper Layout and Grounding (using Ground Plane) Mandatory**
- ◆ **Low ESL/ESR Capacitors Give Best Results**
- ◆ **External LC Filters Very Effective in Reducing Ripple**
- ◆ **Use simulated LC filter initially, then prototype**
- ◆ **Completely Analytical Approach Difficult, Prototyping is Required for Optimum Results**
- ◆ **Linear Post Regulation Effective for Noise Reduction and Best Regulation**
- ◆ **High Frequency Localized Decoupling at IC Power Pins is Still Required**
- ◆ **Once Design is Finalized, Do Not Switch Vendors or Use Parts Substitutions Without First Verifying Their Performance in Circuit**
- ◆ **PHYSICAL SEPARATION AVOIDS NOISE**

This summarizes noise and ripple techniques discussed thus far in this section. Section 4 discusses layout issues related to switching regulators.

Reducing Noise in Mixed-Signal Circuits by Proper Grounding

Before starting this somewhat controversial topic, we should make it clear that there is no single foolproof method for system grounding. What we can do is point out some general principles that are correct and let you apply them to your own system design.

One concept that is not subject to interpretation is that at least one low impedance ground plane is required in practically all systems. In addition, power supplies must be properly decoupled to the ground plane as previously discussed.

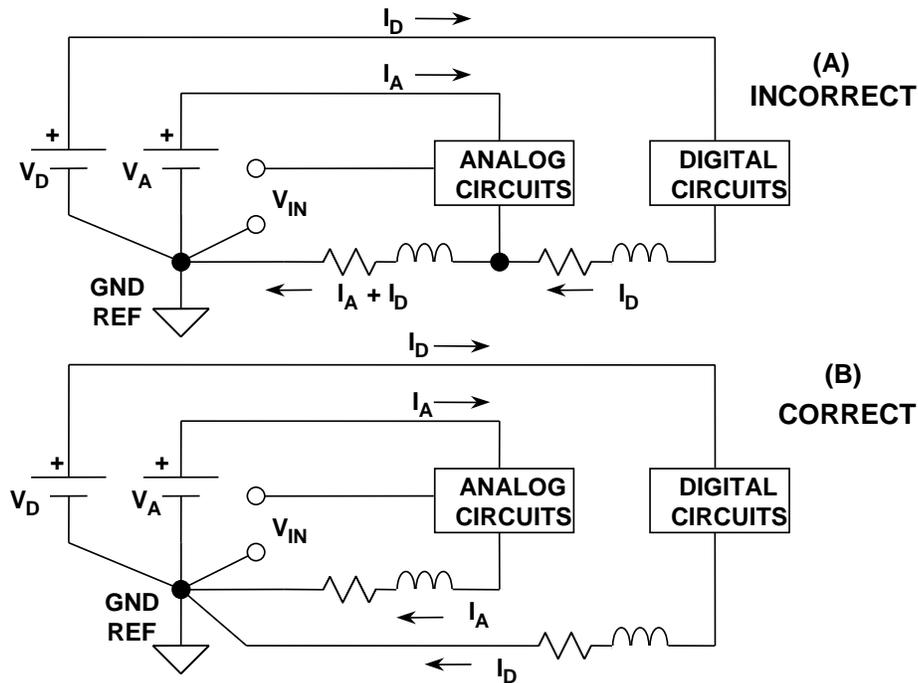
In some systems, two ground planes are used: an analog ground plane for sensitive analog circuits, and a digital ground plane for noisy digital circuits. Each printed circuit board has two such non-overlapping ground planes, and they are kept separate until they are ultimately joined at one point which becomes the system "star" ground point.

In some systems, a single ground plane for both analog and digital circuits is used, and the desired system performance is also achieved.

Some customers start out using the split ground approach and later find that the single ground plane gives better performance.

In this section we will illustrate both approaches and focus on how mixed-signal components should be grounded—an issue which seems to confound many engineers.

Digital Currents Flowing in Analog Return Path Create Error Voltages



Because ground is the power return for all digital circuits, as well as many analog circuits, one of the most basic design philosophies is to separate digital ground returns from analog ground returns.

If the ground returns are not separated, not only does the return current from the analog circuitry flow through the analog ground impedance, but the digital ground current also flows through the analog ground return, and the noisy digital ground current is typically much greater than the analog ground current. This produces unwanted noise at the V_{IN} input to the analog circuit as shown in (A). Remember, grounds are not zero impedance.

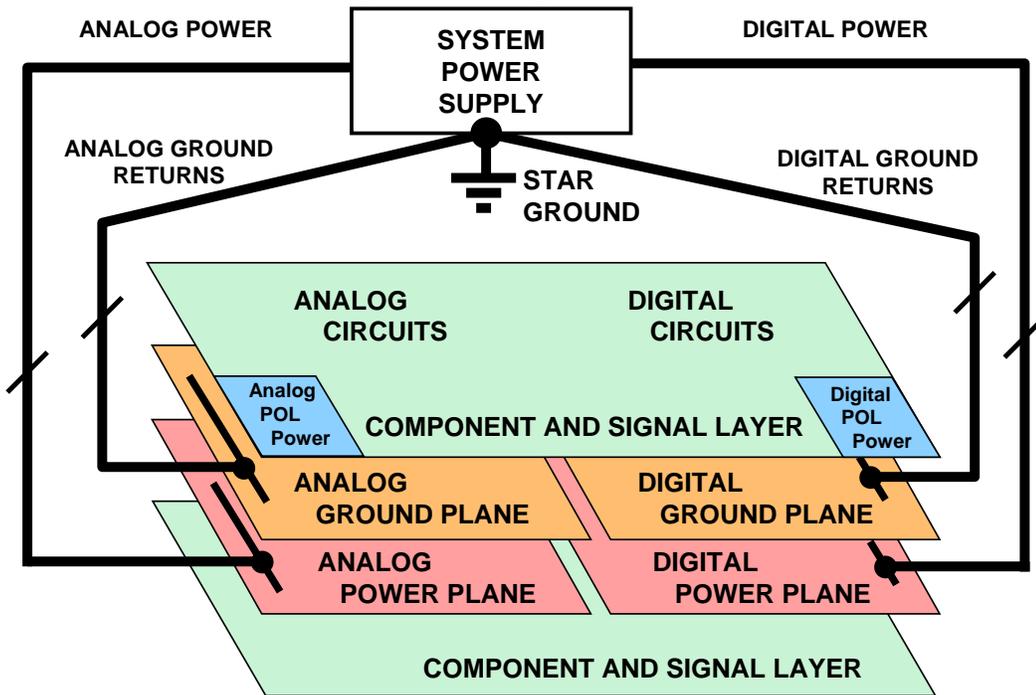
As the frequency of digital circuits increases, the noise generated on the ground increases dramatically. TTL and CMOS logic families are of the saturating types. This means that the logic transitions cause large transient currents on the power supply and ground. CMOS outputs basically connect the power to ground through a low impedance during the logic transitions.

And it's not just the basic clock rate that is a problem. Digital logic waveforms are basically rectangular waves, which implies many higher frequency harmonic components, starting at the fundamental clock rate.

The preferred method is shown in the lower diagram (B) where the analog and digital current return paths are separate and are joined at a single ground reference point.

While this concept is relatively easy to illustrate in a diagram, implementing it in an actual system can be quite complex because of the many return paths required. This is where the ground plane comes to the rescue (sometimes).

Simple Four Layer Board Stack with Split Analog and Digital Ground Planes



A key concept in grounding is that both the power and ground return paths should have the lowest impedance possible, i.e., the parasitic inductance and resistance should be kept to a minimum. In a practical system this is accomplished by the use of PC boards with ground and power planes.

A simple two-layer board needs one layer for ground and the other layer for signal and power runs. For dense boards with lots of interconnections, it is difficult to maintain a reasonably solid ground plane because of signal and power crossovers. For this reason, modern systems generally use multilayer PC boards.

This figure shows a simple four-layer multilayer board stack which incorporates the principles of analog/digital ground return separation shown in the previous diagram. The outer two layers are for signal traces and components, and the inner two are for power and ground. Most of the ICs are generally mounted on one of the outer layers, and the other outer layer reserved for signals and perhaps decoupling capacitors and inductors.

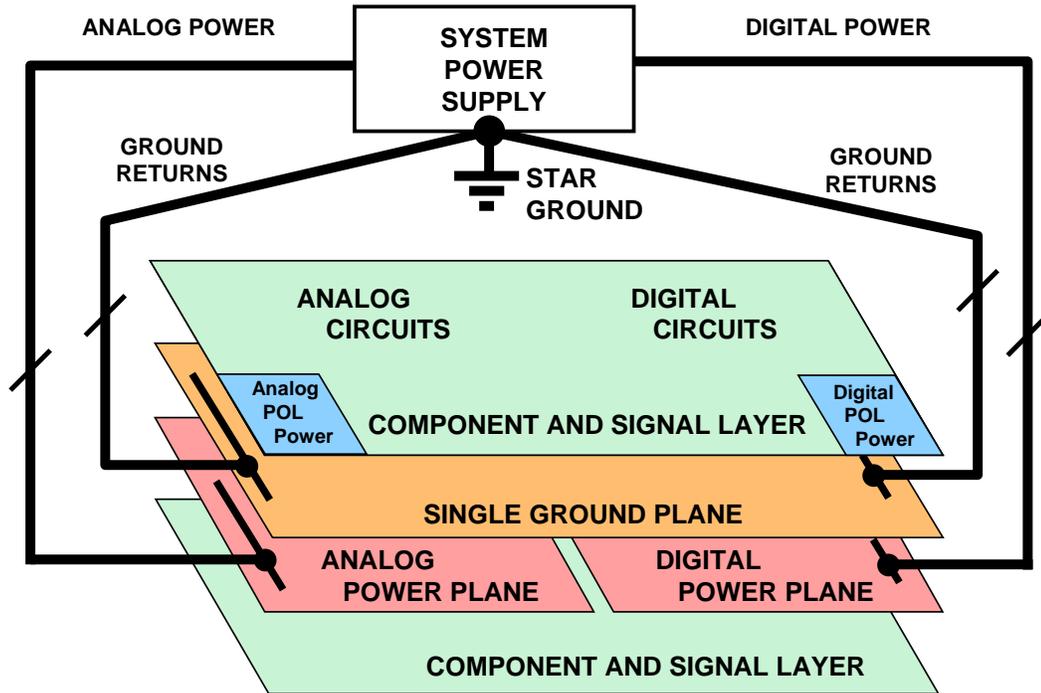
The analog components are grounded to the analog ground plane, and the digital components to the digital ground plane.

Note that the analog ground plane is kept separate from the digital ground plane all the way back to the main system power supply. In addition, there will be point-of-load regulators on the PC board where required. The analog and digital power supplies are also kept separate.

The analog ground plane should not overlap the digital ground plane because the inter-plane capacitance will cause unwanted noise coupling. The capacitance of a trace over a ground plane is approximately 2.8 pF/cm^2 for a standard PC board.

In a multiboard system the power and ground connections to the PC board are made through a connector which is usually located on one edge of the board, unlike the diagram above.

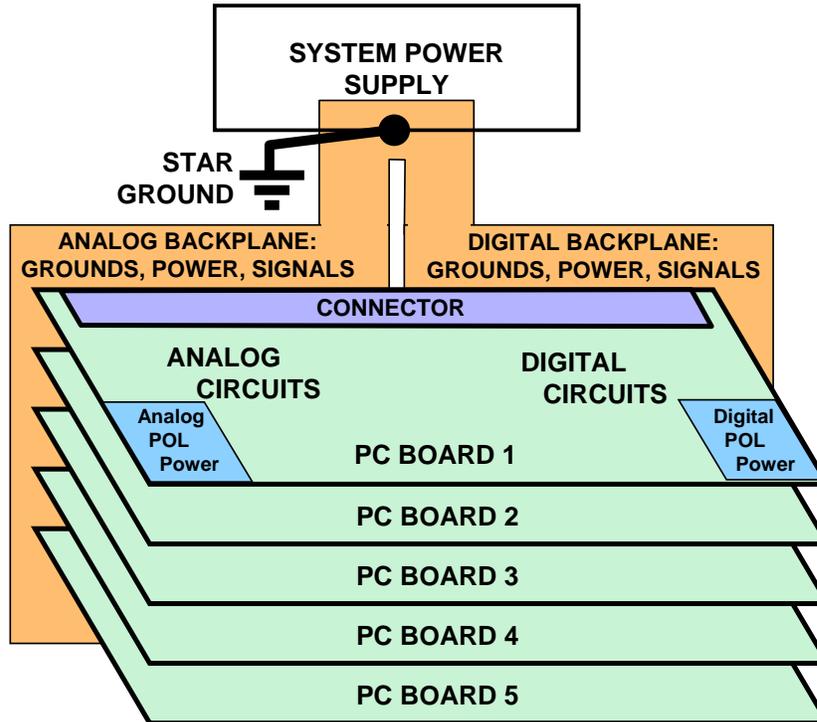
**Simple Four Layer Board Stack
with Single Ground Plane**



Some systems can be designed using a single ground plane for both analog and digital components. This is especially true if the digital circuits are minimal and have relatively low dv/dt outputs.

This four layer PC board utilizes a single ground plane for both analog and digital circuits, but the analog circuits are still physically separated from the digital ones.

Maintaining Low Impedance to Power Supply

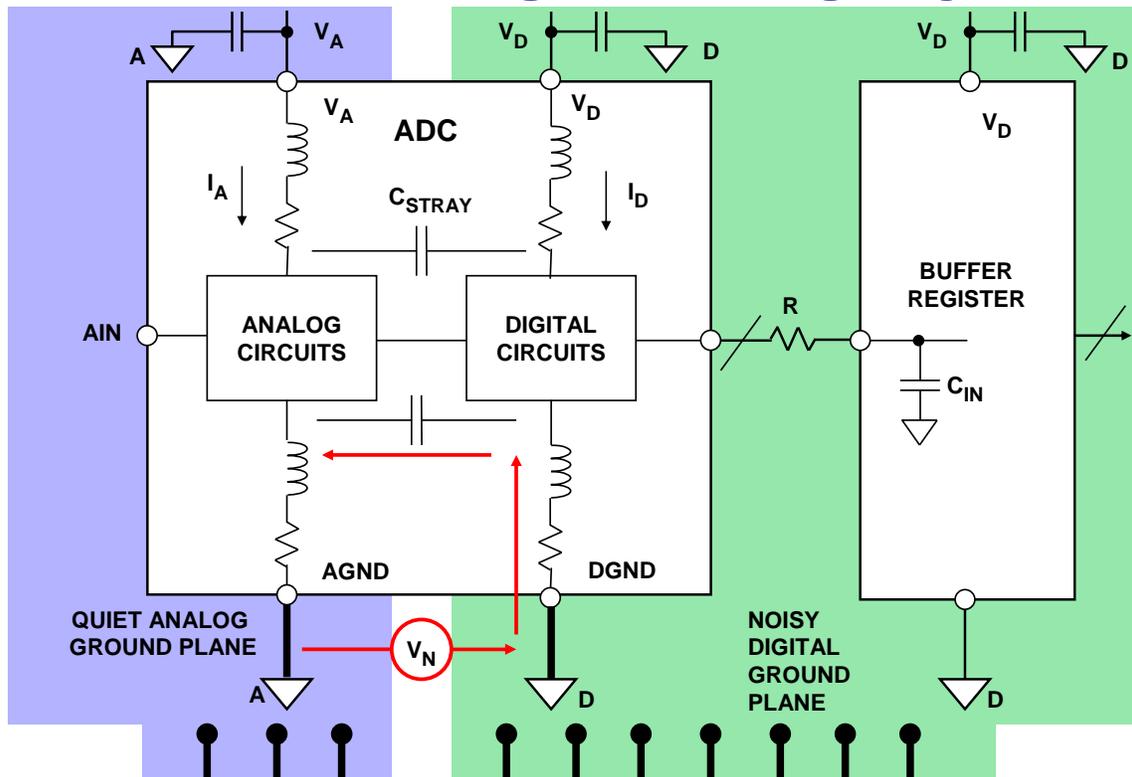


The previous figure showed a single PC board, but most systems require multiple boards as shown here. This shows how the low impedance PC board ground is carried through multiple pins on the connectors to the backplane ground planes and then to the system power supply.

If the system is using split analog and digital ground planes, then they should remain separated on the backplane and joined at the system power supply.

If the system uses a single ground plane, then the PC board ground planes are connected to the backplane ground plane without separation.

ADC Grounding: The Wrong Way



Some of the most troublesome components to ground properly are mixed-signal devices (such as ADCs or DACs) which have both analog ground (AGND) and digital ground (DGND) pins.

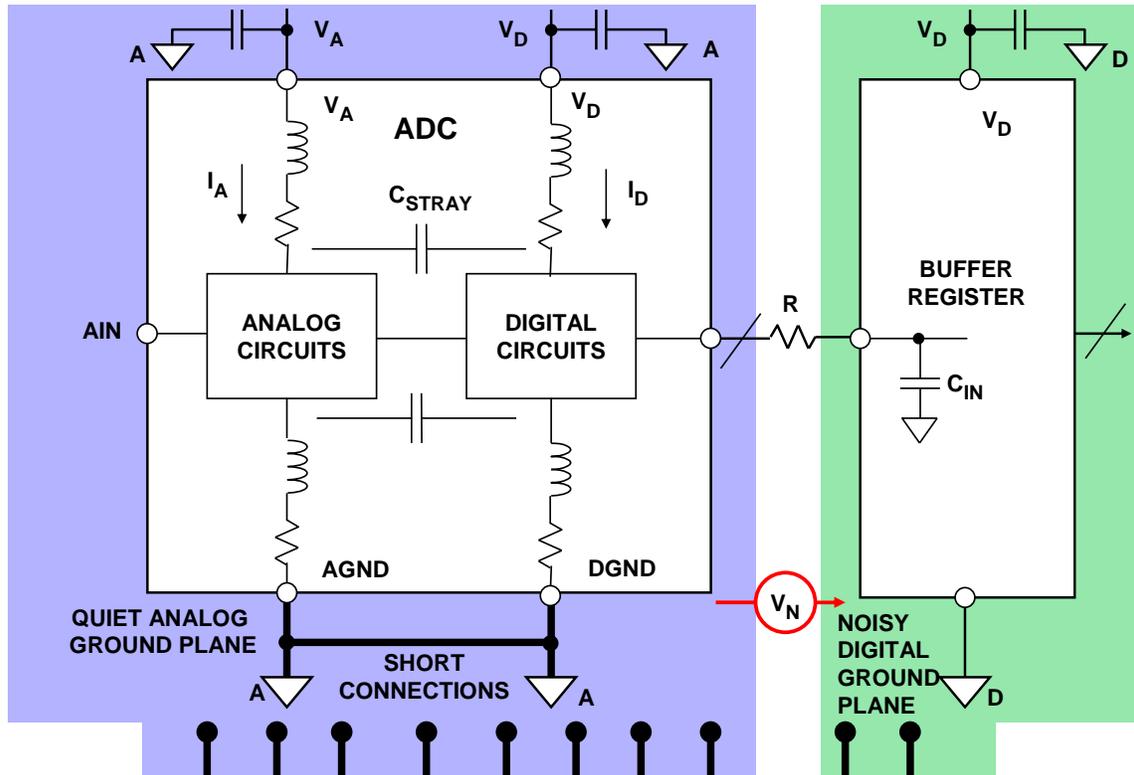
As previously mentioned, a common method for isolating analog and digital circuits is to use separate ground planes for each type. This shows a PCB with separate analog and digital ground planes which are ultimately connected together at the system ground (sometimes called the "star" ground) generally located at the system power supply.

Analog circuits are grounded to the analog ground plane, and digital circuits to the digital ground plane. But what about the ADC? Logically you would think AGND goes to the quiet analog ground plane and DGND to the noisy digital ground plane as shown here.

WRONG!

The analog and digital return current paths are kept separate within the ADC in order to prevent the digital return current from corrupting the analog circuits. Separate AGND and DGND pins are brought out from the chip. Externally, however, AGND and DGND should always be connected to each other and the same ground plane with short connections. If connected to separate planes as shown here, the V_N noise between the two planes couples into the ADC through the DGND pin and corrupts the analog signal (shown by the arrows).

Split Ground Planes, Connected at System PS



In a system with split ground planes, the AGND and DGND pins should be connected to each other and to the analog ground plane with short connections as shown here. The digital currents generated by the ADC are typically fairly low and can be isolated by proper decoupling of the ADC V_D power pin.

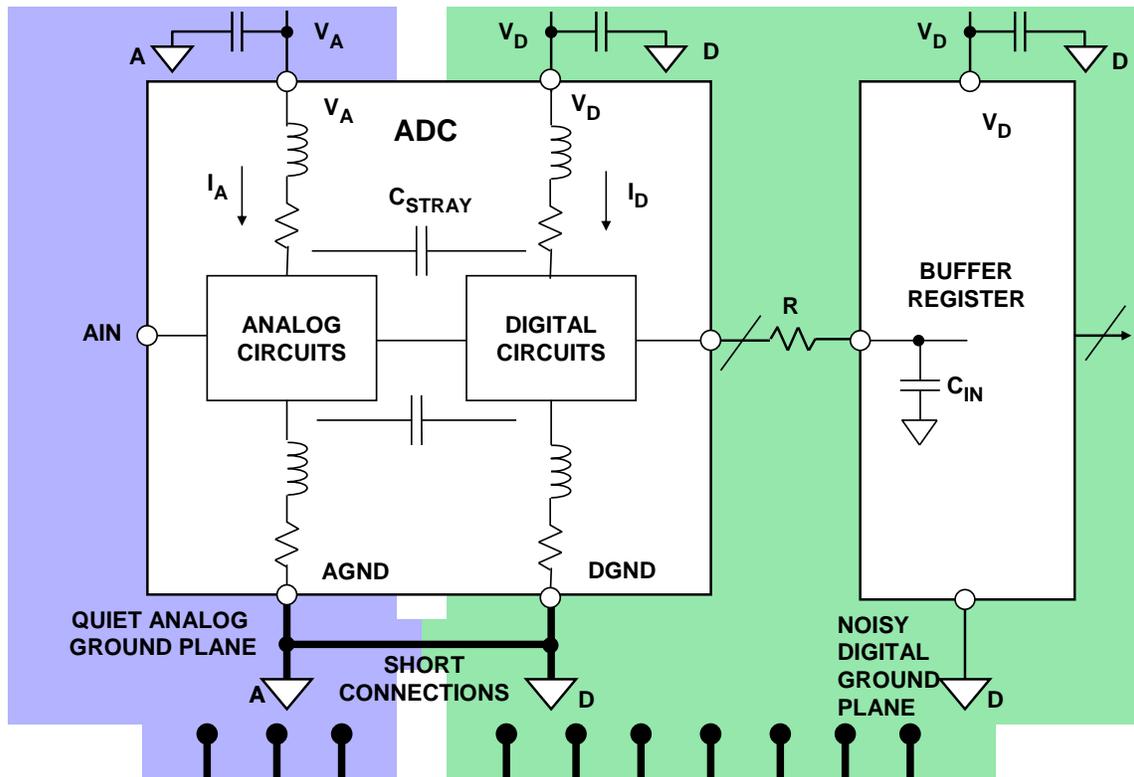
The noise between the two planes appears at the digital interface where it results in a slight degradation in noise margin. If the digital outputs of the ADC are differential (LVDS, PECL, or CML, for example) then the noise between the two planes will be common-mode and mostly rejected by the differential receiver.

The digital outputs of the ADC have fast edges, so a small resistor ($50\ \Omega$ to $500\ \Omega$) should be inserted to isolate the high dv/dt digital outputs from the input capacitance of the buffer register. The digital outputs should have minimum fan out in order to minimize digital currents due to capacitive loading. Under no circumstances should the digital outputs of a high performance converter be connected to a noisy data bus. An intermediate buffer register should always be used as shown here.

The series resistor value should be chosen so that the RC time constant is less than about $0.1T$, where T is the period of the data rate frequency on the output pin. This is to ensure that the data settling time is not significantly degraded by the additional time constant.

It should be noted that the loop area formed by returning the currents to the power supply must also be considered, especially at high frequencies.

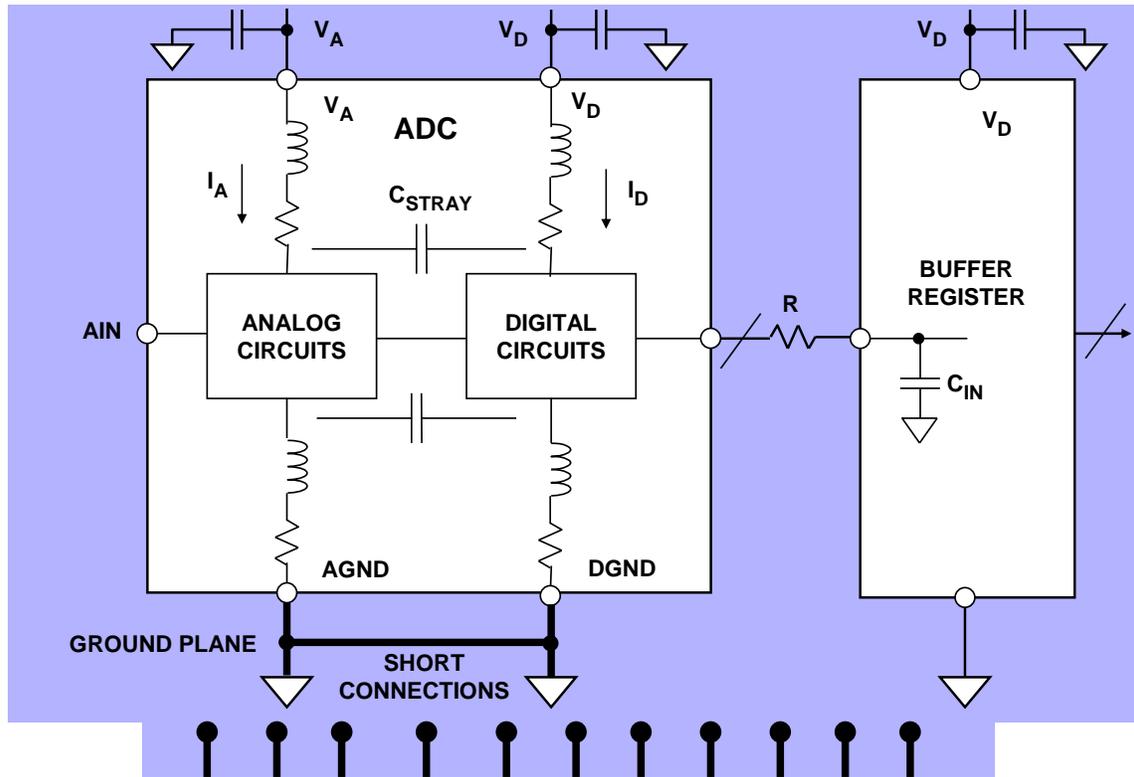
Split Ground Planes, Connected at ADC



In a system with a single PC board, the analog and digital ground planes can be separated as shown but must be joined together at the ADC with very short connections. This layout is often seen on ADC evaluation boards and is an effective way of separating analog and digital currents.

In systems with multiple ADCs and PC boards, this approach creates a connection between the analog and digital ground planes at each ADC. These multiple connections may create unwanted ground loops.

Single Ground Plane



In some systems, a single ground plane can be used provided the analog and digital circuits are physically isolated. As before, the AGND and DGND pins should be connected to each other and to the ground plane with short connections.

The choice between split and single ground planes is not an easy one to make. The conservative approach is to initially design the PC boards with split ground planes but provide extra vias which can later be used to "jumper" the planes together. Performance can be measured under both conditions.

As a general rule, systems with lots of high current digital circuitry are more likely to benefit from the split ground approach than systems with moderate digital currents.

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Notes: