

Practical Power Solutions

1. Point-of-Load Power
2. System Power Management and Portable Power
3. Power for Mixed Analog/Digital Systems
4. Hardware Design Techniques

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SECTION 1 POINT-OF-LOAD POWER

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Fixed Power Point-of-Load Applications

Today's system power requirements have become quite challenging, and design engineers must deal with multiple supply voltages, sequencing issues, high transient load currents, thermal considerations, and many others. In most cases, these problems must be addressed at the PC board level, and not at the system power supply. Therefore, some type of point-of-load (POL) power supplies are required on most PC boards, even those of modest complexity.

This seminar is aimed at design engineers who are not power supply experts, but must deal with the design of these POL supplies as part of their general system design projects.

In this section of the seminar we will discuss some important issues relating to powering non-portable systems, focusing primarily on digital system power (as opposed to analog power). Non-portable systems are often referred to as "fixed power" systems, and generally imply any system that does not operate on a battery. Specific issues relating to powering sensitive analog circuits can be found in Section 3 of the seminar.

This section also touches briefly on the fundamental concepts of linear and switching regulators, without delving into the detailed mathematical issues and theory relating to their design. Complete coverage of these topics can be found in textbooks as well as in online material. We believe that system design engineers are more interested in how comprehensive design tools can provide solutions to their specific power application problems.

"Fixed Power" and "Portable Power" Applications

Fixed Power

- ◆ Does Not Require Battery (except for "keep alive" functions)
- ◆ Desktop Computers
- ◆ Base Stations
- ◆ Servers



Portable Power

- ◆ Requires a Battery to Operate
- ◆ Notebook Computers
- ◆ Handsets
- ◆ Handheld Electronics



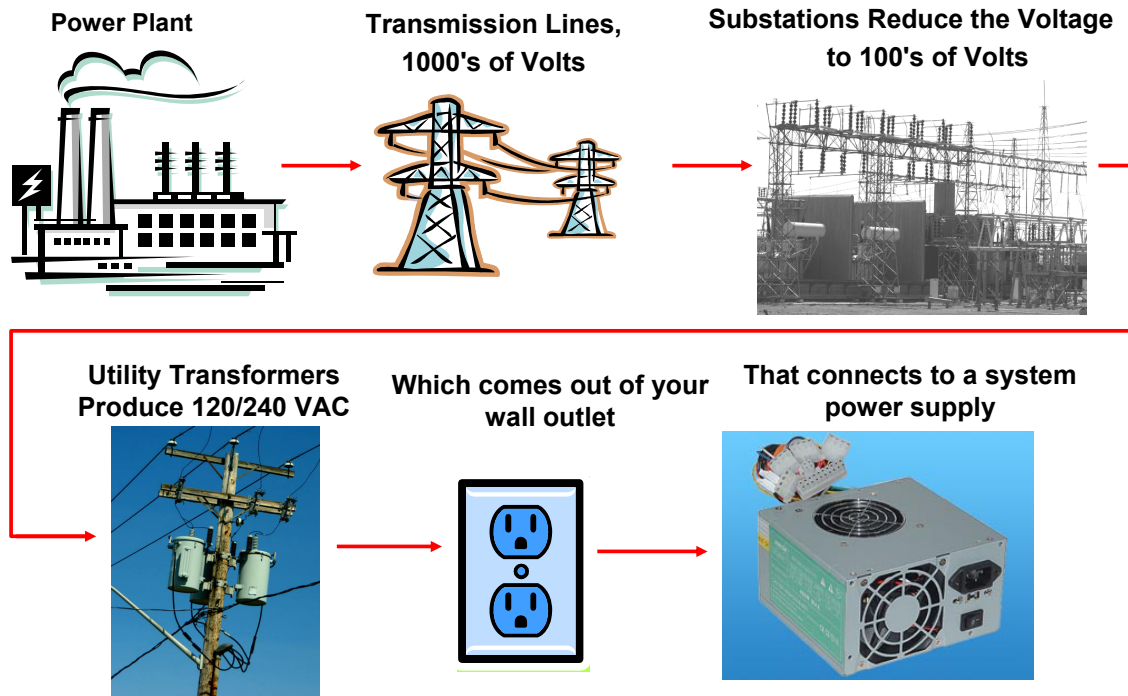
For the purposes of this seminar, system power applications are divided into two broad categories: fixed and portable.

"Fixed" power applications are those that do not require a battery (except for "keep alive" or memory backup functions).

Portable power applications require a battery for operation.

Although there is much commonality in powering the two types of systems, portable systems have certain specific requirements relating to efficiency, size, cost, and weight. The issues important to portable systems are covered in Section 2 of this seminar.

Power Distribution System-1 (Down We Go in Voltage)



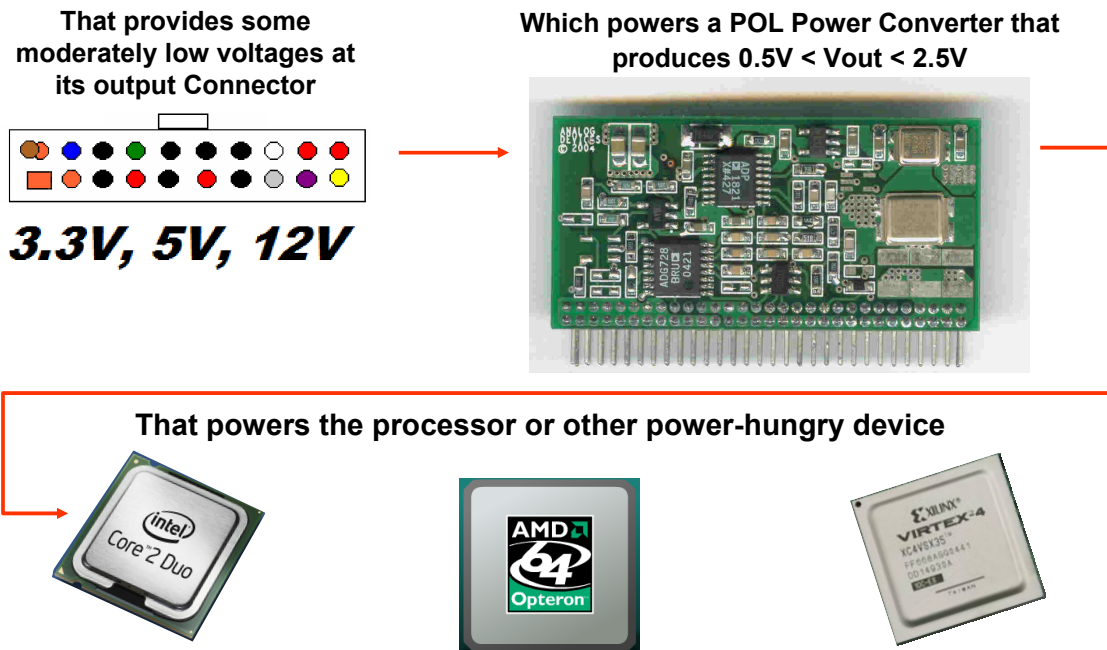
This figure illustrates how power is distributed from the power plant to the system power supply.

Power from the power plant is distributed to the substations over high voltage transmission lines at 1000's of volts. Since the product of the voltage, V , and the current, I , at any point in the system is constant ($P = V \times I$), the use of high distribution voltages reduces the current flow through the lines and hence the I^2R losses. For a given amount of transmission line resistance, it is always more efficient to transmit power at voltages which are as high as practical.

The substations reduce the voltage to 100's of volts, and utility transformers reduce the voltage for home or business to 480 V, 240 V, or 110 V.

The same principle of power distribution is applicable to the system power supply as shown in the next figure.

Power Distribution System-2 (Down We Go in Voltage)



A desktop computer power supply is a good example of a "fixed" power application. The power supply converts the ac line voltage to a number of common individual voltages which are distributed from the power supply to the various PC boards in the system. This figure shows common distribution voltages of 3.3 V, 5 V, and 12 V.

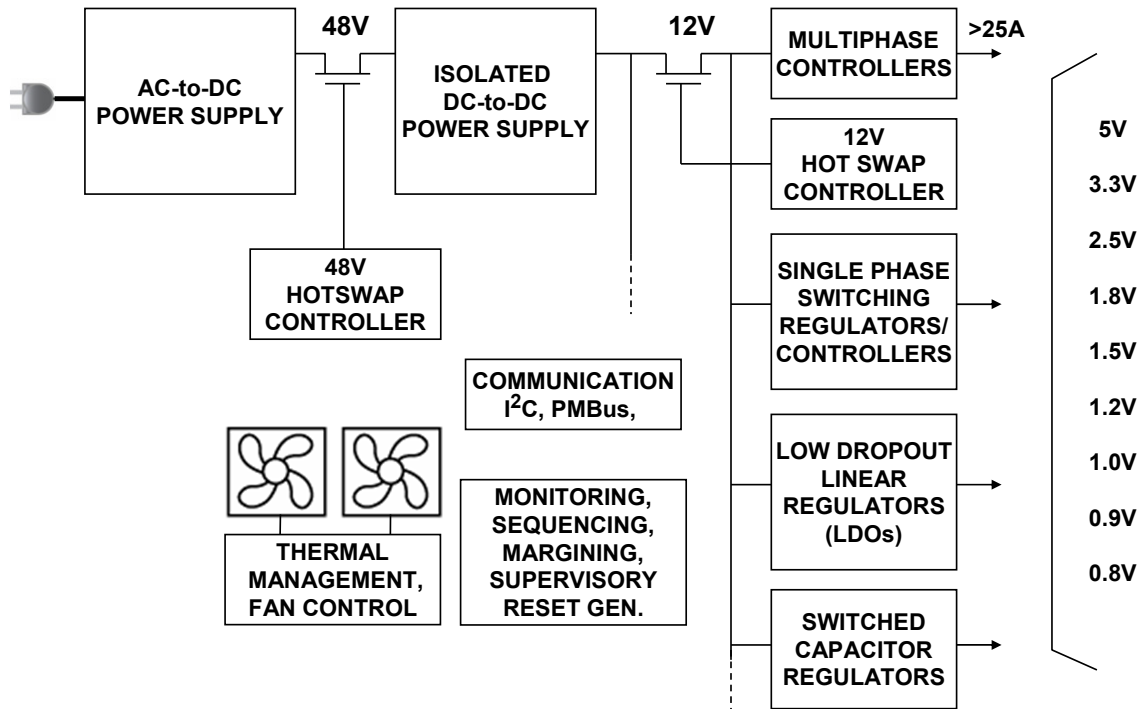
Devices in the system often require other regulated voltages, however, such as the core voltage for the processor. This voltage can be 0.8 V, 1.0 V, 1.2 V, 1.5 V, 1.8 V, etc. This requires a point-of-load (POL) regulated supply on the PC board specifically designed for the core voltage, which may be 10's of amps. The specific processor requirements often dictate other power supply requirements, such as load transient recovery, standby modes, etc.

The processor generally requires additional POL regulated voltages for the input/output (I/O) interface, and perhaps other auxiliary voltages.

Flexibility in the various voltages is important because of the trend toward ever faster, smaller geometry processes which require correspondingly lower core voltages.

One can easily see that it is both impractical and inefficient to generate these multiple voltage rails within the system power supply, and that POL regulation provides the best solution. In addition, local regulation generally provides "cleaner" voltage rails which is particularly important with low core voltages.

Fixed Power Signal Chain Functional Blocks



This figure shows the typical functional blocks in the signal chain of a modern fixed power system.

The POL supplies can be either LDOs, single, or multiphase switched controllers, depending on the current output and efficiency requirements. The switched capacitor (also called charge pump, or "inductorless") regulator is also shown, but is more often associated with portable systems. (See Section 2 for further discussion of switched capacitor regulators).

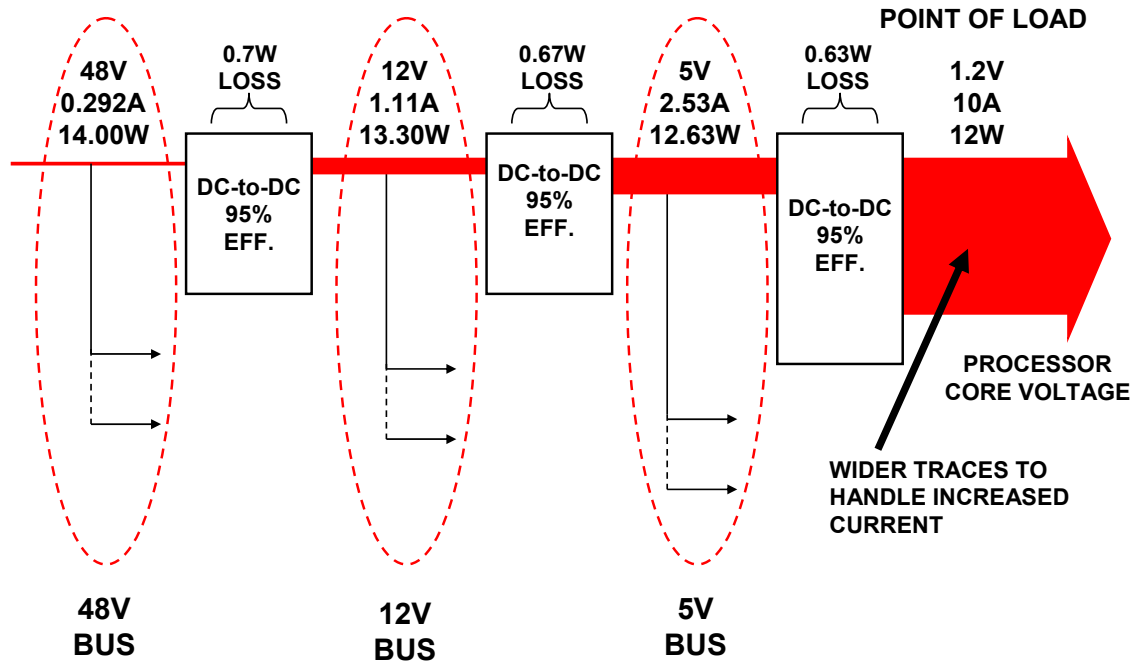
In addition to the POL regulators, there are also important auxiliary functions such as monitoring, sequencing, margining, and supervisory functions, such as power-on reset generators.

Thermal management and fan control is also an important part of modern power designs.

For telecommunications and server applications, hot swap controllers allow PC boards to be exchanged under power-on conditions.

A typical fixed power system may consist of some or all of the above functions, depending on the complexity and type of system.

Intermediate Bus Structure and Point of Load Regulation Offer Flexibility and Efficiency



The use of intermediate bus structures and POL regulation offers both flexibility and efficiency as shown in this figure.

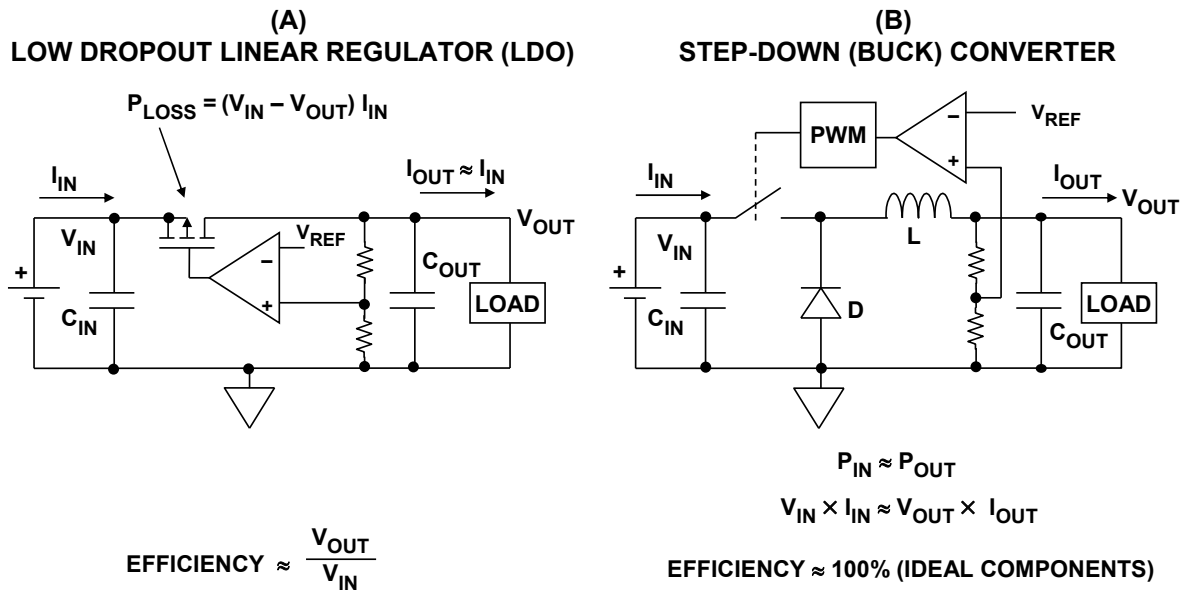
The path from the 48 V bus to the 1.2 V processor core is highlighted. In this example there are intermediate bus voltages of 12 V and 5 V which are distributed to other parts of the system.

It is assumed that the efficiency of each dc-to-dc converter is 95%. The power losses in the individual converters are shown. The only path shown is that for the processor core voltage. Additional currents supplied by each intermediate bus are not shown.

In order to maintain the same voltage drop in the PC traces, the trace width should be proportional to the amount of current carried. Note that POL regulation and the use of the intermediate bus architecture allow a short trace for the 10 A processor core current because the regulator is located close to the processor.

Further discussion of PC board layout issues can be found in Section 4.

Two Popular Methods of Regulation: Linear and Switching



There are basically two types of POL regulators: linear and switching.

The linear regulator is the simplest type but generally the least efficient. However, linear regulators do not produce switching noise and ripple and are therefore useful in supplying power to sensitive analog components.

The power loss in a linear regulator is equal to the output current times the voltage dropped across the pass element (as shown in A). The efficiency is equal to the ratio of the output voltage divided by the input voltage, neglecting internal losses in the regulator, which should be relatively low.

Switching regulators, such as the buck (step-down) converter shown in B, transfer energy from input to output via an inductor that has the voltage polarity across it switching at a high frequency. If the circuit elements are ideal, the input power equals the output power, and the converter is 100% efficient. Regulation of the output voltage is achieved using a feedback loop which controls the duty cycle of the pulse width modulator (PWM), which in turn controls the on-time and off-time of the switching element, and hence the amount of energy transferred to the load.

Most popular switching regulators are based on magnetic elements, however the switched capacitor (or charge pump) regulator is often used in low current portable applications where the current requirement is less than approximately 200 mA. This type of regulator is discussed in more detail in Section 2.

Linear Regulators vs. Switchers

<ul style="list-style-type: none"> ◆ Linear Regulator Advantages <ul style="list-style-type: none"> ● Simple low-cost design ● Uses few external components; less board space required ● No switching noise; low output ripple ◆ Disadvantages <ul style="list-style-type: none"> ● Use only to generate a voltage lower than the input voltage ● Efficiency $\approx V_{OUT} / V_{IN}$ ● Power dissipation (heat rise) may be a concern ◆ Linear Regulator is best when <ul style="list-style-type: none"> ● $V_{IN} - V_{OUT}$ is small ● Low-to-medium current applications ● Low output ripple and noise are important ● Space and cost are important ● Powering sensitive analog circuits 	<ul style="list-style-type: none"> ◆ Switching Regulator Advantages <ul style="list-style-type: none"> ● Good for voltage increase, decrease, or inverting ● High efficiency, 70% to 95% ● Lower power dissipation ◆ Disadvantages <ul style="list-style-type: none"> ● More complex and costly design ● High output ripple ● More components ◆ Switching Regulator is best when <ul style="list-style-type: none"> ● $V_{IN} - V_{OUT}$ is large ● Low-to-high current applications ● Efficiency is important ● Voltage needs to be increased or inverted ◆ Switched Capacitor Regulators are suitable for some applications <ul style="list-style-type: none"> ● Portable ● Low currents (less than $\approx 200\text{mA}$)
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The decision to use a linear or switching POL regulator is based on many factors. This table summarizes the key advantages and disadvantages of each type.

Linear regulators are certainly easier to use than switchers, require fewer external components, and occupy less board space. Linear regulators produce no switching noise and are often placed after a switching regulator to reduce the overall noise and ripple voltage. However, the PSRR of the linear regulator at the switching frequency must be carefully examined to determine its effectiveness in these applications.

The linear regulator is an excellent choice to power high performance analog circuits, such as ADCs, DACs, PLLs, DDS systems, data acquisition systems, instrumentation amplifiers, etc.

The chief disadvantage of the linear regulator is its efficiency, which is approximately V_{OUT}/V_{IN} . This may not be a problem for low output currents and low $V_{IN} - V_{OUT}$ values, but can be a real concern at high output currents and larger $V_{IN} - V_{OUT}$ values. Another concern is the power dissipation in the linear regulator at high output currents.

Most modern linear regulators use a low dropout (LDO) architecture which helps improve the efficiency. However, the switching regulator is the preferred choice in applications requiring high efficiency at high currents and large $V_{IN} - V_{OUT}$ values.

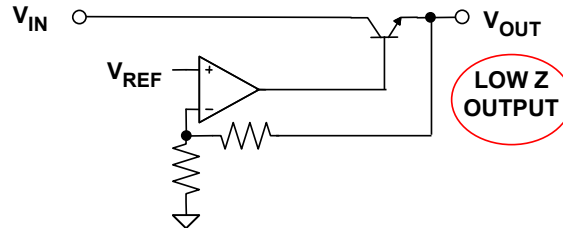
Switching regulators definitely are more complex to design, require more components, and take up more board space. Extreme care must be taken in the layout in order to minimize ground bounce. Modern design tools are available from manufacturers such as Analog Devices' ADIsimPower™ to make the design process relatively painless, and allow optimization of various parameters such as efficiency, cost, and board space.

Linear Regulators

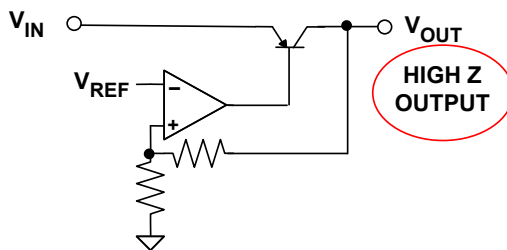
www.analog.com/ldo

Types of Linear Regulators

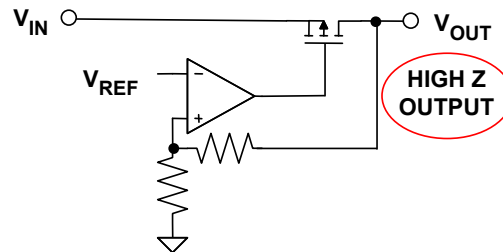
(A) BIPOLAR REGULATOR
WITH NPN EMITTER FOLLOWER



(B) PNP BIPOLAR LDO



(C) PMOS LDO



These are the three fundamental types of linear regulators. All three architectures use a pass transistor, a voltage reference, and a feedback control loop to provide output voltage regulation.

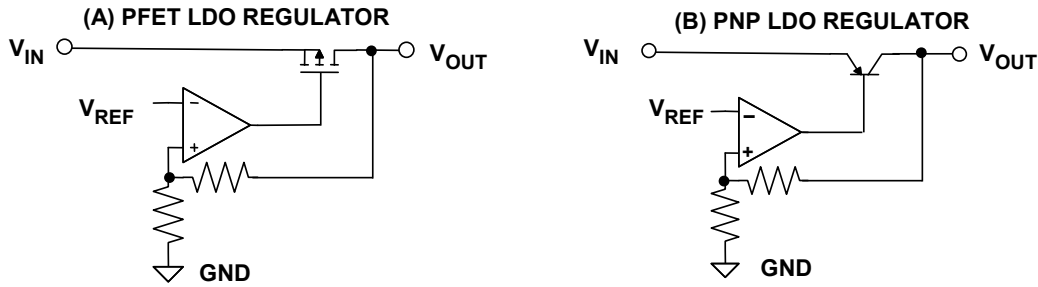
The circuit shown in (A) uses an NPN emitter follower as the pass device. Some NPN-based linear regulators use a darlington connection to reduce the base drive current. The advantage of this architecture is the inherently low output impedance and high bandwidth of the emitter follower which makes the regulator easy to stabilize under a variety of capacitive loads. The disadvantage of the NPN pass device is that the minimum value of $V_{IN} - V_{OUT}$ (the dropout voltage) is approximately 1 V for the single NPN, and 2 V for the darlington connection.

It is possible to use an NMOS pass device, however an external bias voltage several volts greater than the input voltage is required in order to drive the gate. This can be a big disadvantage if such a voltage is not available.

The LDO circuit shown in (B) uses a bipolar PNP transistor as the pass device, and the dropout voltage can be as low as a hundred millivolts or so and is limited by the saturation voltage of the transistor, V_{CESAT} . The regulator maintains operation as long as the transistor is in its linear region. The disadvantage of this architecture is that the output impedance is high and the regulator is much more difficult to stabilize with bulk capacitive loads. Another disadvantage of using a bipolar process for the LDO is the larger amount of bias, or "ground current" required.

The circuit shown in (C) makes use of a PMOS pass device, and the dropout voltage is limited by the on-resistance of the FET. Like the circuit of (B), this circuit has a high open-loop output impedance and is more difficult to stabilize with bulk capacitive loads. The CMOS LDO has an advantage of extremely low "ground current". In addition, MOSFETs can be "sized" to supply reasonably high currents.

PFET LDO vs. PNP LDO



PFET/PNP LDO COMPARISON

- ◆ Very low ground pin current does not increase with load
- ◆ Dropout voltage can be very low as set by the ON-Resistance of the FET (R_{ON})
- ◆ Ground pin current is higher: equals load current divided by beta (gain) of PNP transistor
- ◆ Higher ground pin current wastes power.
- ◆ Dropout voltage equals the saturation voltage of the PNP

ADP1715, CMOS LDO
 $I_{GND} @ 100\mu A = 100\mu A \text{ max}$
 $I_{GND} @ 500mA = \underline{650\mu A \text{ max}}$

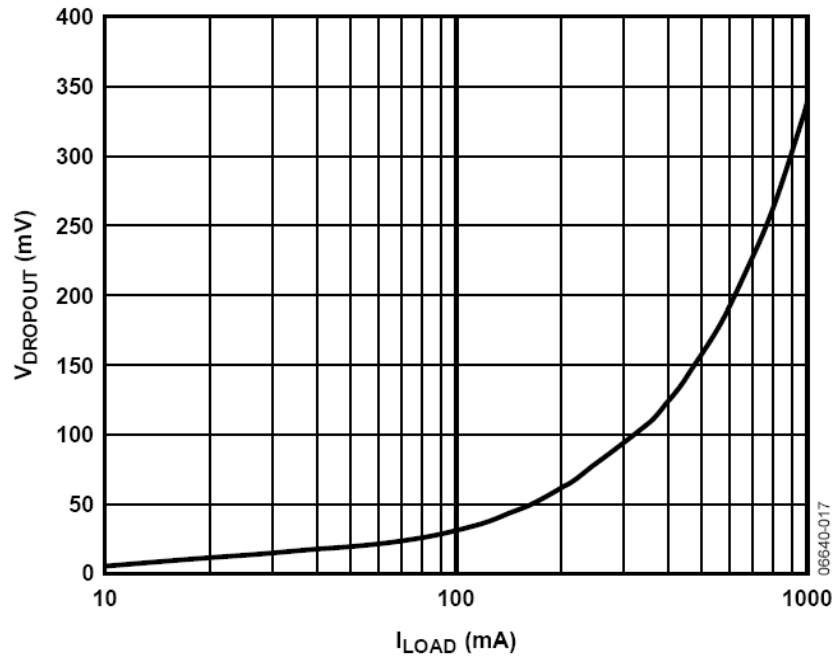
ADP3334, BIPOLAR LDO
 $I_{GND} @ 100\mu A = 130\mu A \text{ max}$
 $I_{GND} @ 500mA = \underline{10mA \text{ max}}$

This shows a comparison between a typical PFET LDO (A) and a PNP LDO (B).

For a 500 mA load current, the ADP1715 CMOS LDO has a ground current of only 650 μA compared to 10 mA for the ADP3334 bipolar LDO.

Most of the ground pin current in a PNP LDO is the current required to drive the base, which is equal to the load current divided by the beta of the PNP. Most bipolar processes do not support high beta PNP transistors.

ADP1706/ADP1707/ADP1708 CMOS LDO Dropout Voltage vs. Load Current



The dropout voltage of a CMOS LDO can be made very low by designing for a low on-resistance. This shows the dropout voltage of the ADP1706/ADP1707/ADP1708 LDOs as a function of load current.

Note that the dropout voltage at 1 A is typically 345 mV.

The ADP1706/ADP1707/ADP1708 are CMOS, low dropout linear regulators that operate from 2.5 V to 5.5 V and provide up to 1 A of output current. Using an advanced proprietary architecture, they provide high power supply rejection and achieve excellent line and load transient response with a small 4.7 μF ceramic output capacitor.

The ADP1706/ADP1707 are available in 16 fixed output voltage options. The ADP1708 is available in an adjustable version, which allows output voltages that range from 0.8 V to 5.0 V via an external divider. The ADP1706 allows an external soft start capacitor to be connected to program the start-up time; the ADP1707 and ADP1708 contain internal soft start capacitors that give a typical start-up time of 100 μs . The ADP1707 includes a tracking feature that allows the output to follow an external voltage rail or reference.

The ADP1706/ADP1707/ADP1708 are available in an 8-lead, exposed paddle SOIC package and an 8-lead, 3 mm \times 3 mm exposed paddle LFCSP, making them not only very compact solutions but also providing excellent thermal performance for applications requiring up to 1 A of output current in a small, low profile footprint.

Linear Regulator Specifications

- ◆ **Drop-Out Voltage**
 - Defined as the minimum Input to Output Differential Voltage required to maintain the output voltage within 100mV of the nominal value
 - This specification directly translates to efficiency and battery life

- ◆ **Ground Current (bias current)**
 - The current required by the regulator itself to operate over the full load range. Sometimes called quiescent current (I_Q).
 - Will vary with load current
 - Directly translates to efficiency, especially at light loads

- ◆ **Power Supply Rejection Ratio (PSRR)**
 - The ratio of output voltage change due to a change in the input voltage
 - This must be examined at the specific ripple frequency when using the LDO as a "ripple filter"

- ◆ **Regulator Output Error**
 - The output voltage deviation from the nominal or ideal value

This figure summarizes the key linear regulator specifications. It is common to specify total output accuracy as a percentage.

Note that many applications depend on the linear regulator to "filter" a switching regulator output. Extreme caution must be exercised in these applications to filter as much of the high frequency noise as possible BEFORE it enters the linear regulator. The PSRR of linear regulators at high frequencies is generally not sufficient to properly filter these transients.

In addition, carefully examine the PSRR of the linear regulator at the switching frequency of interest to make sure it is sufficient.

Regulator Output Error

- ◆ **Regulator Output voltage error is a combination of:**
 - **Line regulation ability (maintain a nominal output voltage with varying input voltage, $\Delta V_{OUT} / \Delta V_{IN}$)**
 - **Load regulation ability (maintain a nominal output voltage with varying load currents, $\Delta V_{OUT} / \Delta I_{OUT}$)**
 - **Internal Reference and Amplifier errors due to temperature and voltage changes**
- ◆ **Total error is expressed as a percentage of the nominal output voltage, usually from 1% to 3%**
- ◆ **Early bipolar regulators were generally more accurate than CMOS regulators due to having better internal references. Today, the distinction is minimal**

This figure defines the total regulator output voltage error. Total error generally is between 1% and 3%.

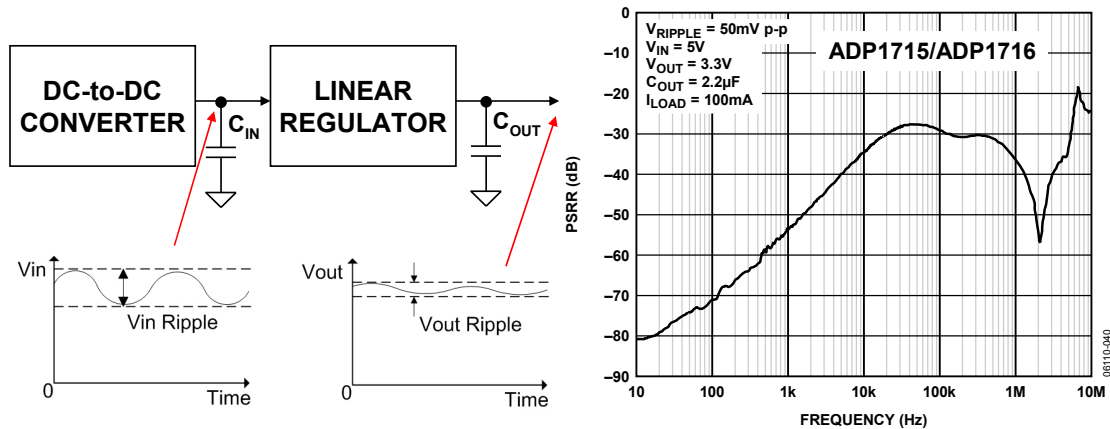
Early bipolar regulators were generally more accurate than their CMOS counterparts because of better internal voltage references. Today this distinction is minimal, and both technologies are capable of 1% accuracy.

There are two considerations regarding accuracy. The first is the absolute accuracy of a regulator. Ultimately this value should be traceable to a reference standard. In a practical regulator, accuracy is a function of input voltage (line regulation) and the load current (load regulation). The second is the drift due to temperature or ageing.

In most systems the initial accuracy errors can be removed by calibration, and the drift due to temperature or ageing are more important.

LDO Power Supply Rejection

- ◆ Power supply rejection ratio is a measure of how well a circuit rejects ripple at various frequencies coming from the input power supply
- ◆ Comparing ratio of output ripple to input ripple
- ◆ PSRR is expressed in dB, and is plotted on a log scale of dB vs. Frequency
- ◆ Frequency range of interest is usually 10Hz to 10MHz
- ◆ Devices with good PSRR typically have high gain and a high unity gain frequency
- ◆ High PSRR devices are sometimes used for post regulation of DC-to-DC converters



As previously mentioned, LDOs are commonly used to reduce the ripple from a switching regulator. In these applications, the PSRR of the LDO must be examined at the specific switching frequency of the switching regulator. LDO PSRR is typically shown from 10 Hz to 10 MHz.

The figure shows the PSRR (in dB) of the ADP1715/ADP1716 500 mA CMOS LDO as a function of frequency for a load current of 100 mA with a 2.2 μF ceramic output bulk capacitor.

Any good quality ceramic capacitors can be used with the ADP1715/ADP1716, as long as they meet the minimum capacitance and maximum ESR requirements. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior over temperature and applied voltage. Capacitors must have a dielectric adequate to ensure the minimum capacitance over the necessary temperature range and dc bias conditions. X5R or X7R dielectrics with a voltage rating of 6.3 V or 10 V are recommended. Y5V and Z5U dielectrics are not recommended, due to their poor temperature and dc bias characteristics. More discussion of capacitors can be found in Section 4.

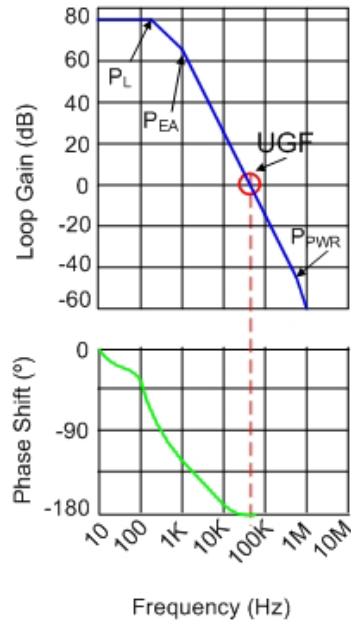
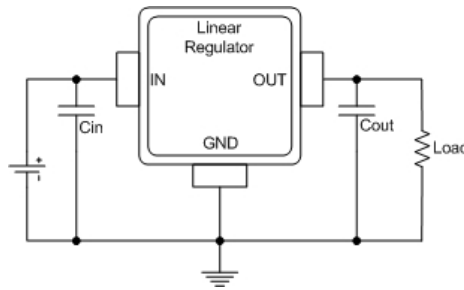
The PSRR curves show a characteristic "dip" at high frequencies. The start of the dip is due to the attenuating effect of the output bulk capacitor. However, the curve starts to rise again because of the output capacitor ESL. The "depth" of the dip is determined by the output capacitor ESR.

At high frequencies, (greater than approximately 10 MHz), the output capacitor and its characteristics dominate the PSRR. This illustrates the importance of localized decoupling at the power pins of each IC in addition to providing sufficient bulk capacitance at the LDO output to attenuate the lower frequency components.

In addition, sufficient capacitance is required at the LDO input to filter high frequency components

Stability Issues with Traditional PNP or PMOS LDOs

- ◆ Regulators with PNP or PMOS pass devices have several Poles around the control loop:
 - Low frequency Pole due to the output capacitor and the load resistance (P_L)
 - Low frequency Pole due to the error amplifier compensation (P_{EA})
 - High frequency Pole due to the power pass device (P_{PWR})
- ◆ Low frequency Poles are dominant and cause 180° of negative phase shift in the loop before the 0dB point (Instability)

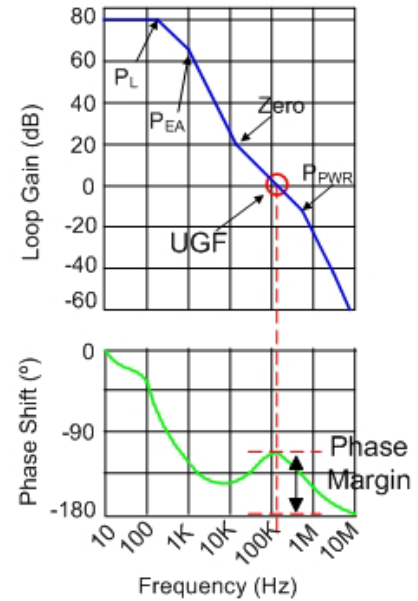
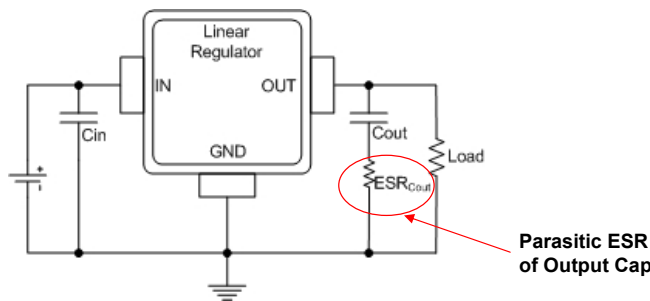


Traditional LDOs designed with PNP or PMOS pass devices have several poles around the control loop as shown. The first is labeled P_L and is due to the output capacitor and the load resistor. The second pole, P_{EA} , is due to the internal error amplifier compensation. There is an additional high frequency pole, P_{PWR} , due to the power pass device.

Note that the two low frequency poles, P_L and P_{EA} , cause 180° of phase shift at the point of unity gain, and therefore the system as shown is unstable.

Stabilizing the Regulator Loop Using the Zero Created by the Output Capacitor and its ESR

- ◆ A Zero is needed to cancel the phase shifting effect of one of the low frequency poles
- ◆ Designers make use of the parasitic ESR of the output cap to provide this necessary low freq Zero.
- ◆ A well placed Zero will add positive phase shift to the loop and therefore make it stable
- ◆ Zero also increases the loop bandwidth (higher 0dB point), Beware!

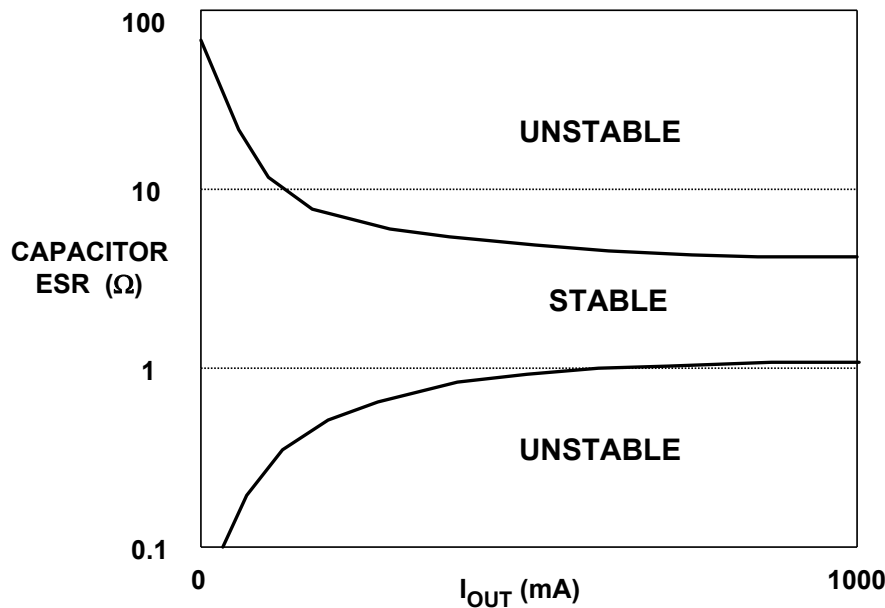


An external zero is needed to cancel the phase shift of one of the low frequency poles. LDO designers have often used the parasitic ESR of the output capacitor to provide this necessary low frequency zero as shown in the above figure.

However, the additional zero must be placed at the correct frequency and will also increase the loop bandwidth.

This results in a "zoned" ESR requirement on the external bulk capacitor. Relying on this approach for stabilization is risky because ESR may not be repeatable from capacitor to capacitor. There can be additional distributed decoupling capacitors located at individual ICs which create more variables.

Zoned Load Capacitor ESR Can Create an LDO Applications Nightmare



A typical PNP or PMOS LDO using traditional designs has an allowable range of bulk capacitor ESR values which will ensure stability. The ESR value is also a function of the load current.

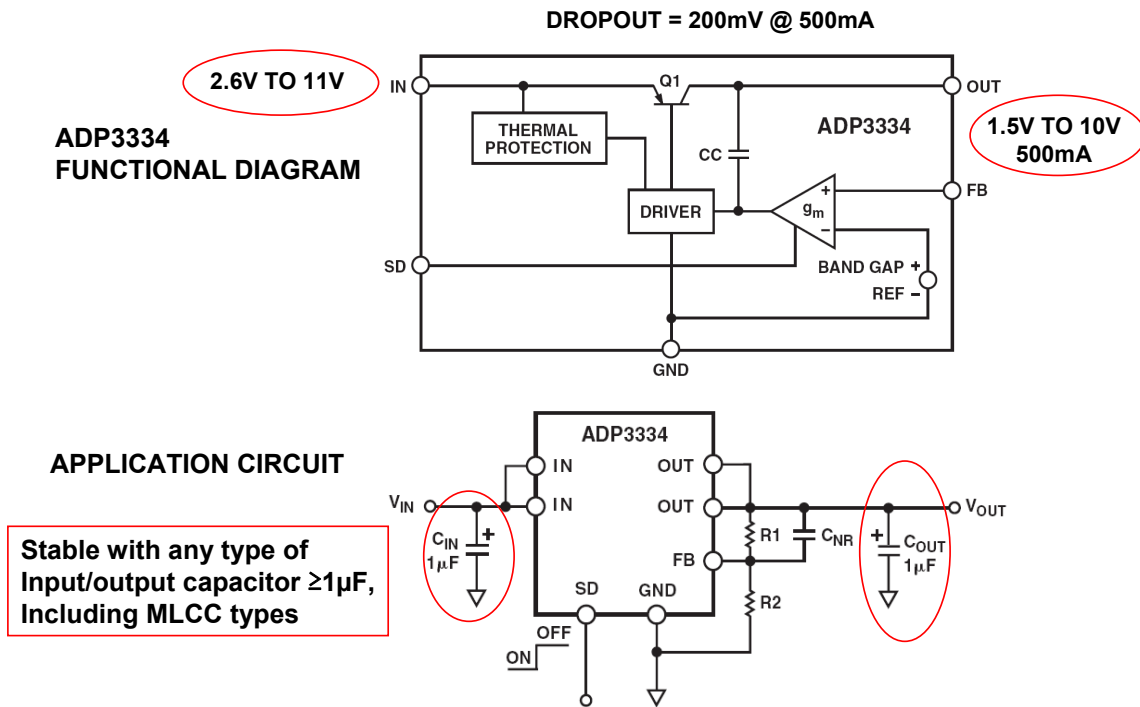
The "zoned" ESR requirement on the external capacitor is an applications nightmare because the engineer is relying on a parasitic parameter for stability.

A zoned ESR chart such as this is meant to guide the user of an LDO in picking an output capacitor which confines ESR to the stable region, i.e., the central zone, for all operating conditions. Note that this generic chart is not intended to portray any specific device, just the general pattern. Unfortunately, capacitor facts of life make such data somewhat limited in terms of the real help it provides. Bearing in mind the requirements of such a zoned chart, it effectively means that general purpose aluminum electrolytic are prohibited from use, since they deteriorate in terms of ESR at cold temperatures.

Very low ESR types such as OS-CON or multilayer ceramic units have ESRs which are too low for use. While they could in theory be padded up into the stable zone with external resistance, this would hardly be a practical solution.

This leaves tantalum types as the best all around choice for LDO output use where "zoned" ESR is required. Finally, since a large capacitor value is likely to be used to maximize stability, this effectively means that the solution must use a more expensive and physically large tantalum capacitor. This is not desirable if small size is a major design criteria.

Bipolar LDOs Use anyCAP Design



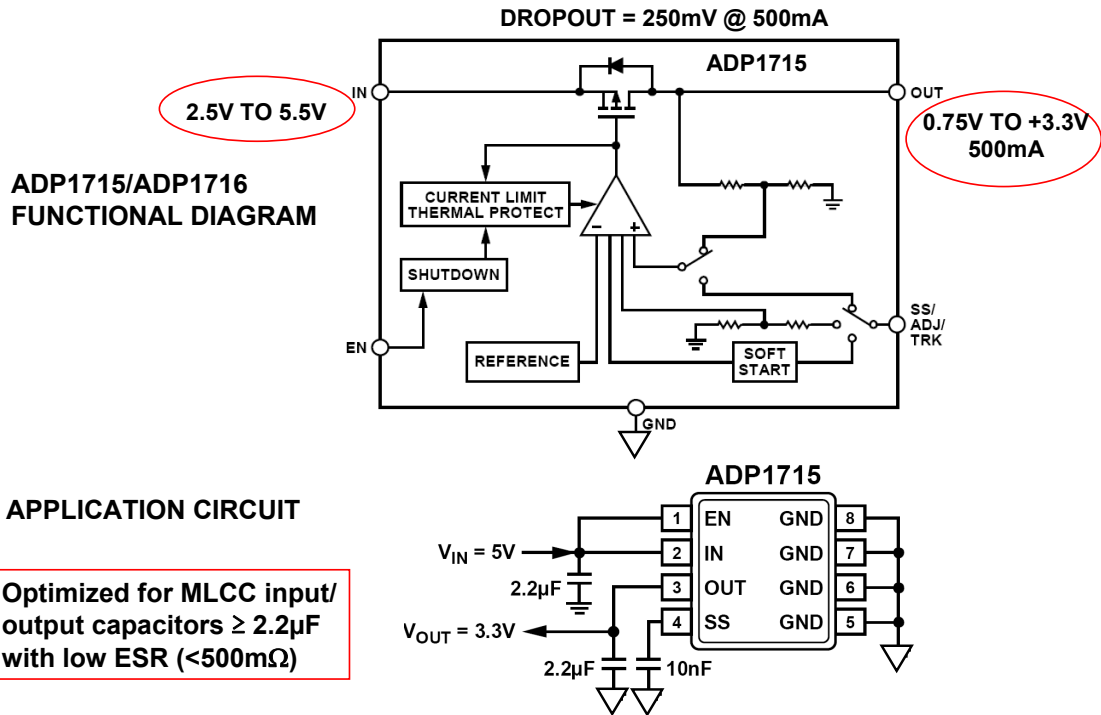
The Analog Devices' family of anyCAP bipolar LDOs, introduced in the mid-1990s, pioneered the use of a different control loop topology which removed the "zoned" ESR requirement on the external bulk capacitor. This family is stable with any type of input/output capacitor greater than 1 μF , including the low ESR multilayer ceramic (MLCC) types.

This figure shows the functional diagram of the series as well as a typical application circuit.

A detailed description of the anyCAP design is found in the following reference:

Walt Kester, *Analog-Digital Conversion*, Analog Devices, 2004, ISBN: 0916550273 Chapter 7. Also available as *Data Conversion Handbook*, Elsevier-Newnes, 2005, ISBN: 0750678410, Chapter 7.

Analog Device's CMOS LDOs



As was previously mentioned, CMOS LDOs provide low on-resistance PFET pass devices as well as low quiescent (ground) current. Advances in voltage reference technology now allow CMOS LDOs to match the accuracy of bipolar LDOs.

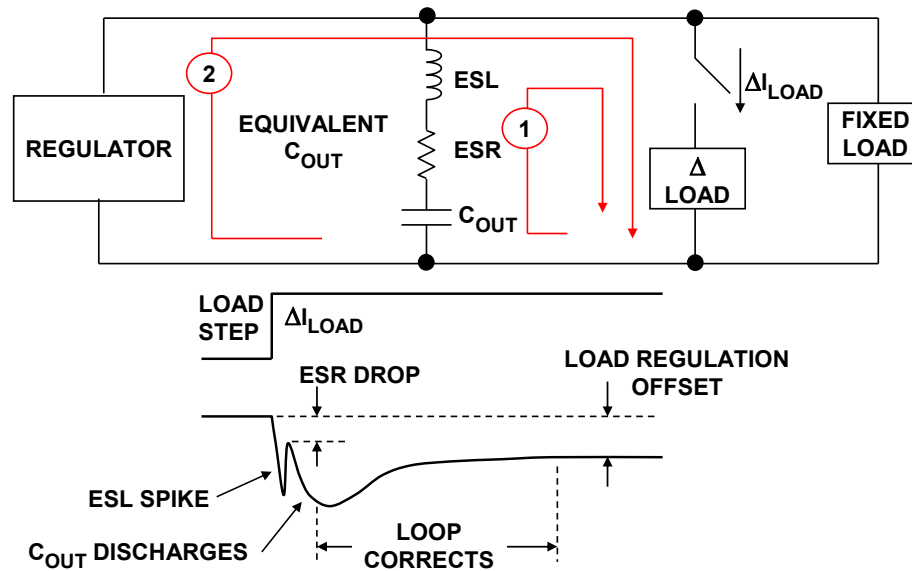
The ADP1715/ADP1716 family of CMOS LDOs are designed for operation with small, space-saving ceramic capacitors, but they will function with most commonly used capacitors as long as care is taken about the effective series resistance (ESR) value. The ESR of the output capacitor affects stability of the LDO control loop. A minimum of 2.2 μF capacitance with an ESR of 500 m Ω or less is recommended to ensure stability of the ADP1715/ADP1716.

Transient response to changes in load current is also affected by output capacitance. Using a larger value of output capacitance improves the transient response of the ADP1715/ADP1716 to large changes in load current.

Any good quality ceramic capacitors can be used with the ADP1715/ADP1716, as long as they meet the minimum capacitance and maximum ESR requirements. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior over temperature and applied voltage. Capacitors must have a dielectric adequate to ensure the minimum capacitance over the necessary temperature range and dc bias conditions. X5R or X7R dielectrics with a voltage rating of 6.3 V or 10 V are recommended. Y5V and Z5U dielectrics are not recommended, due to their poor temperature and dc bias characteristics.

This figure shows a block diagram of the ADP1715 500 mA CMOS LDO and a typical application circuit. The external 10 nF capacitor provides a soft-start time of approximately 7 ms.

Transient Response to Current Load Step



- ◆ (1) C_{OUT} must supply initial current to load during the first few microseconds after switch closes.
- ◆ (2) Then the regulator loop takes over and eventually supplies all the static load current

Transient response to a current load step is important, especially when the LDO is powering a digital device with widely varying load currents, such as an FPGA or DSP.

In many cases, the core allowable voltage tolerance specification includes not only the static voltage error but also transient error. Exceeding these limits under either static or transient conditions can cause erratic operation of the DSP, FPGA, or other processor. For example, a total tolerance of $\pm 5\%$ is common on the core voltage for an FPGA. For a 1.2 V core voltage, the total allowable error is therefore only ± 60 mV.

This figure shows a typical load transient response to a load step in current.

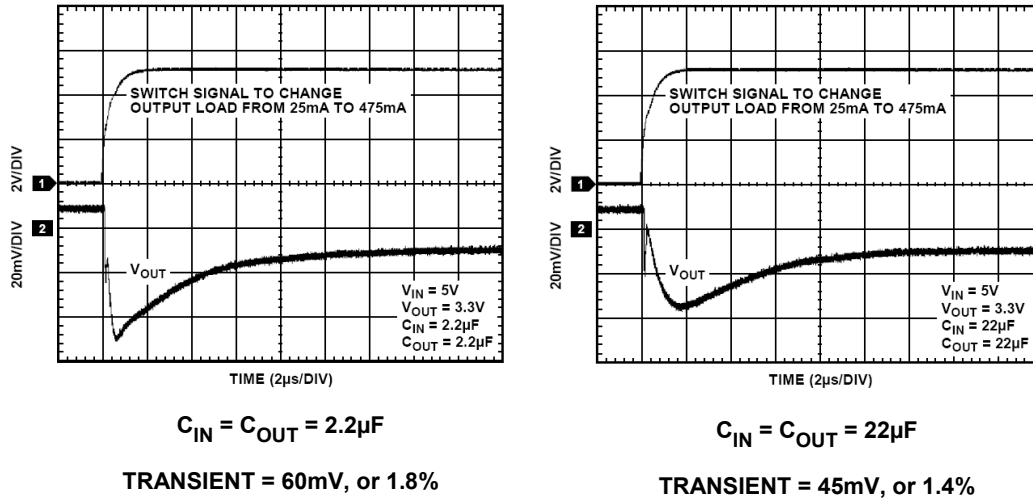
Before the application of the load step, the LDO supplies all the static load current.

Immediately after the application of the load step, the output capacitor must supply all of the transient current as shown in the loop labeled "1". There is an initial voltage drop due to the capacitor ESR which is followed by an inductive spike due to the capacitor ESL. The capacitor then begins to discharge into the load for a few microseconds until the LDO feedback loop begins to correct for the load current change.

As the feedback loop continues to correct (shown in the loop labeled "2"), the output voltage settles to a final value which is determined by the load regulation of the LDO. At this point, the LDO once again supplies all the static load current.

It is important to remember that the total output capacitance also includes the distributed localized capacitors at the various ICs which make up the load as well as PC board parasitics.

Linear Regulator Load Current Step Transient Response for ADP1715/ADP1716



This figure shows the load current step transient response of the ADP1715/ADP1716 CMOS LDO for a load step change from 25 mA to 475 mA. The input voltage to the LDO is 5 V, and the output voltage is 3.3 V.

The left-hand response is for an input and output MLCC capacitor of 2.2 µF, and the right-hand response is for a 22 µF input and output capacitor. The transient amplitude is 60 mV (1.8%) and 45 mV (1.4%), respectively.

The lack of ringing in the transient response indicates good stability and phase margin for the LDO control loop.

The transient response is also a function of the amplitude of the current step. Small current steps produce less initial voltage drop across the output capacitor ESR, but the total transient settling time is dependent on the control loop and its compensation and may not reduce proportionally.

Other Useful Features for Low Dropout Linear Regulators

- ◆ **Adjustability**, use of external resistors to set the nominal output voltage
- ◆ **Enable Pin**, to externally control when the regulator turns on and off
- ◆ **Soft-Start**, controls the rise time of the output voltage during power-up, thus limiting inrush current
- ◆ **Tracking Feature**, external voltage rail can be fed into the regulator, the output will track this external voltage
- ◆ **Error Pin**, indicates when output is about to go out of regulation
- ◆ **Overcurrent Protection**, limits the output current
- ◆ **Thermal Shutdown**, turns the regulator output off if the junction temperature rises above 150°C
- ◆ **Noise Reduction**, allows external bypassing of the regulator's reference voltage, thus reducing noise on the output rail

Modern LDOs are available with many features which greatly aid in their application. This figure lists a few.

In some applications it is desirable to set the output voltage to a specific value using external resistors.

The *Enable* function can be used to externally control when the regulator turns on and off, and the *Soft-Start* function can control the rise time of the output voltage during power-up thus limiting the inrush current.

The *Soft-Start* feature is especially important when powering devices such as FPGAs which require a monotonic ramp-up of voltage. When the regulator output voltage begins to rise, the regulator must supply current to charge the total output bulk capacitance ($I = C \times dv/dt$) as well as the current required by the load. If the sum of these currents is greater than the current limit of the regulator, the output will become non-monotonic. Accurate control of the ramp-up time (dv/dt) is therefore critical in this type of application.

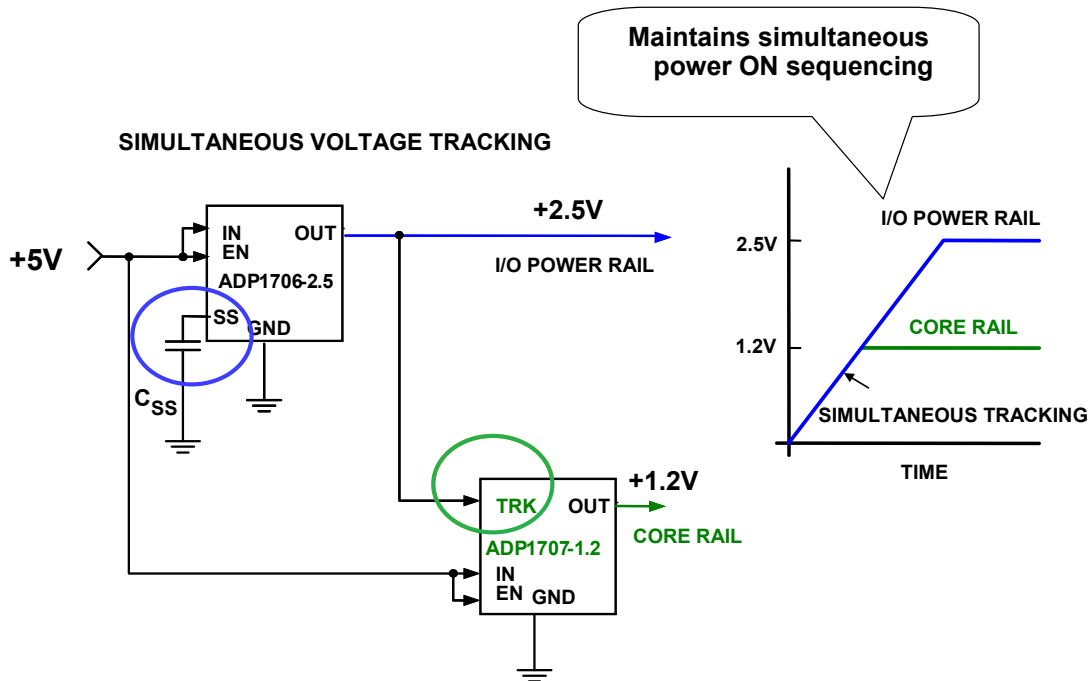
A *Tracking* feature is useful in performing simple sequencing functions between regulators.

An *Error* function pin indicates when the output is about to go out of regulation.

Overcurrent and *Thermal Shutdown* features protect downstream circuitry as well as the LDO.

The addition of a *Noise Reduction* pin allows external bypassing of the regulator's internal reference voltage, thereby reducing noise on the output.

ADP1707 Simultaneous Voltage Tracking



Simple sequencing and power-on issues can be resolved by utilizing the Soft-Start, Enable, and Tracking functions available on new LDOs such as the ADP1706, ADP1707, and ADP1708 family of 1 A CMOS regulators.

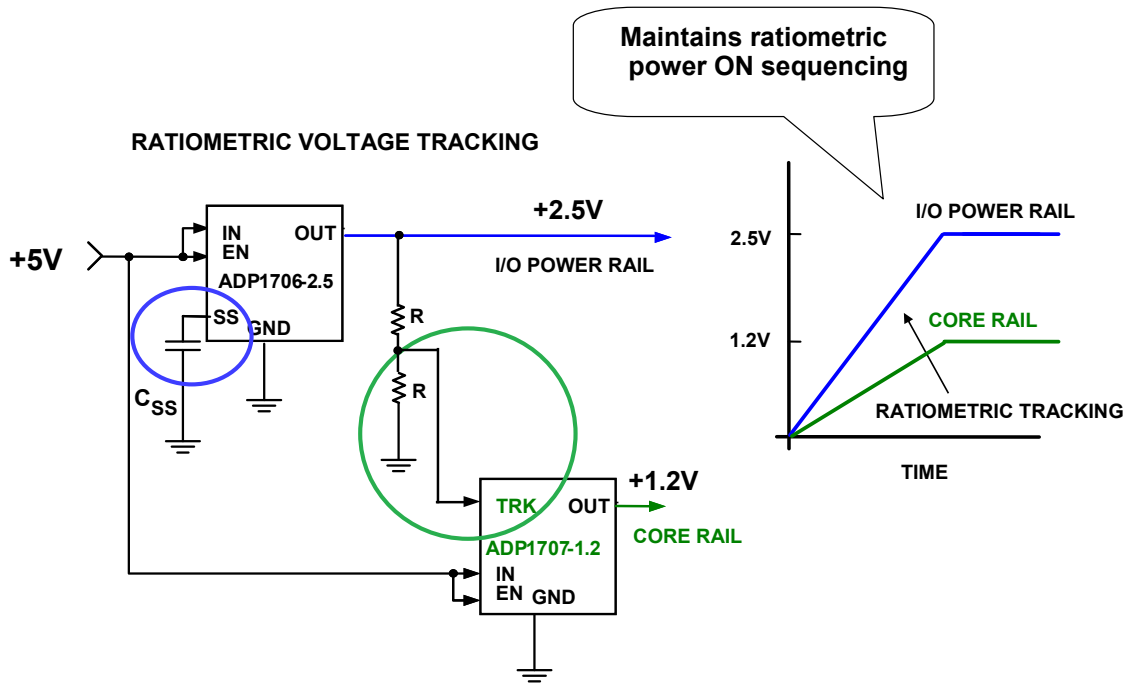
All parts in the family have an Enable function. The three parts are differentiated by the function assigned to Pin 8. The ADP1706 has a Soft-Start function (SS) on Pin 8 which can be programmed using an external capacitor, the ADP1707 has an internal Soft-Start function which gives a typical start-up time of 100 μ s. The ADP1707 has a Tracking function (TRK) assigned to Pin 8 that allows the output to follow an external voltage rail or reference.

The ADP1706 and ADP1707 come in 16 fixed output voltage options, while the ADP1708 output voltage is adjustable from 0.8 V to 5.0 V by connecting the appropriate external resistor between Pin 7 and Pin 8.

In the application shown in this figure, it is desired to bring up the 2.5 V I/O power rail and the 1.2 V core power rail simultaneously upon the application of the 5 V rail and the Enable function. The 2.5 V I/O start-up ramp slope is controlled by the external capacitor connected to the Soft-Start (SS) pin of the ADP1706-2.5. The Soft-Start time is calculated by $T_{SS} = V_{REF} \times (C_{SS}/I_{SS})$, where $V_{REF} = 0.8$ V, and $I_{SS} = 1.2$ μ A. For $C_{SS} = 10$ nF, $T_{SS} \approx 7$ ms.

The output of the upper 2.5 V I/O regulator (ADP1706-2.5) is applied to the Tracking input of the lower 1.2 V core regulator (ADP1707-1.2) which forces the output of the 1.2 V core regulator to track the output of the 2.5 V I/O regulator. This provides the desired simultaneous tracking as shown.

ADP1707 Ratiometric Voltage Tracking



In this figure, the particular processor requires ratiometric sequencing as shown.

Ratiometric sequencing is easily implemented using a circuit very similar to the previous figure, except here the Tracking input of the 1.2 V core regulator is driven by the attenuated ($\div 2$) output of the 2.5 V I/O regulator.

If the voltage applied to the TRK pin is less than the nominal output voltage, the output voltage is equal to the voltage at TRK. Otherwise, the output voltage is regulated to its nominal output value. In this example, the 1.2 V core regulator begins to regulate when the I/O voltage reaches 2.4 V.

It should be noted that the sequencing and power-up requirements differ widely between various FPGAs, DSPs, etc., and the examples shown in the last two figures are only shown to illustrate two possible arrangements.

Switching Regulators and Controllers

www.analog.com/regulators

www.analog.com/controllers

www.analog.com/adisimpower

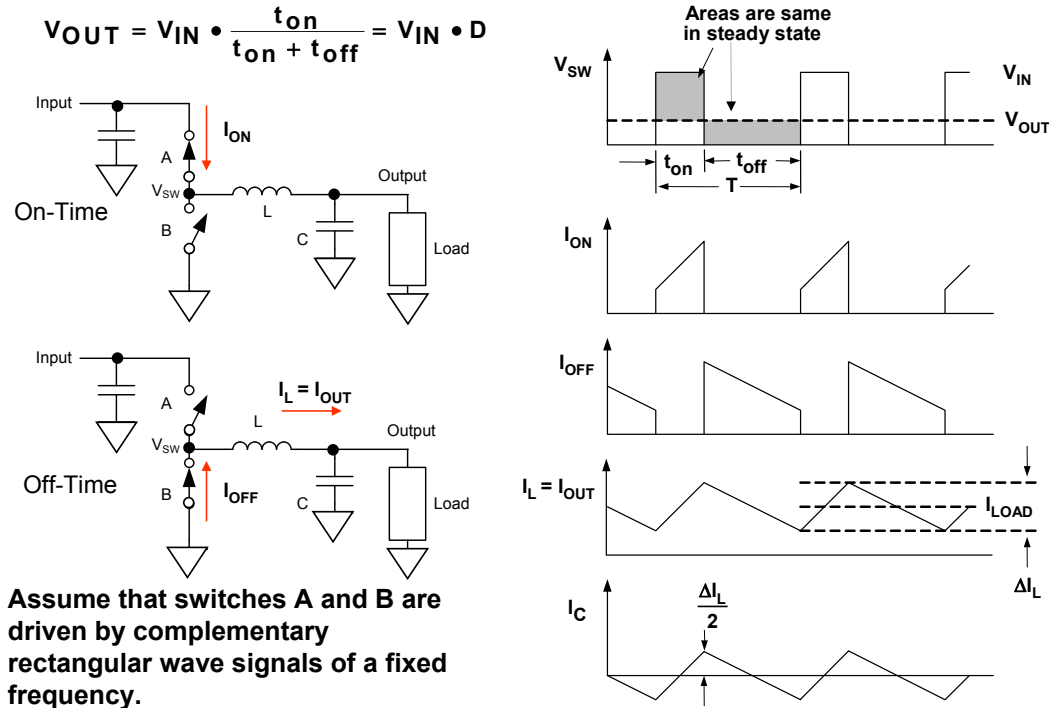
Soon after the invention and proliferation of the integrated circuit, system designers were somewhat successful in standardizing on a few popular voltages. For instance, the analog circuits typically ran on ± 15 V or ± 12 V supplies, and the digital logic on +5 V. The design of the "system power supply" (silver box) was relegated to the reclusive "power supply designer," and the voltages from the central power supply were distributed over the wiring and the backplane to the various system PC boards which were most often designed by other engineers.

Although a "silver box" equivalent still exists in most systems, this simple design philosophy has been complicated by the need for "intermediate" supply busses and point-of-load regulation. This is largely due to the proliferation of multiple rails, the trend toward lower power and lower voltages, and many other factors. Modern design engineers working at the PC board level must therefore be competent in the application of both linear and switching regulators in order to complete their designs. The silver box "guru" may not be amenable to designing the local 10 A supply for the 1.2 V FPGA core voltage.

Like the linear regulator, the magnetic switching regulator has become a fundamental building block in today's point-of-load applications, primarily because of its efficiency and flexibility. Fortunately, a complete theoretical understanding of the various intricacies of switching regulator design is not required in order to successfully apply them.

The concepts presented in the following section along with appropriate design tools (ADIsimPower) and application support should certainly make the design of the switching regulator less daunting to modern PC board designers. Textbooks and other reference material abound for those wishing to obtain a deeper understanding.

Step-Down (Buck) Converter



This shows the basic operation of a buck, or step-down, converter. If all circuit elements are ideal there is no power loss, and the circuit is 100% efficient. The input power is equal to the output power: $P_{IN} = P_{OUT}$, and therefore $V_{IN} \times I_{IN} = V_{OUT} \times I_{OUT}$.

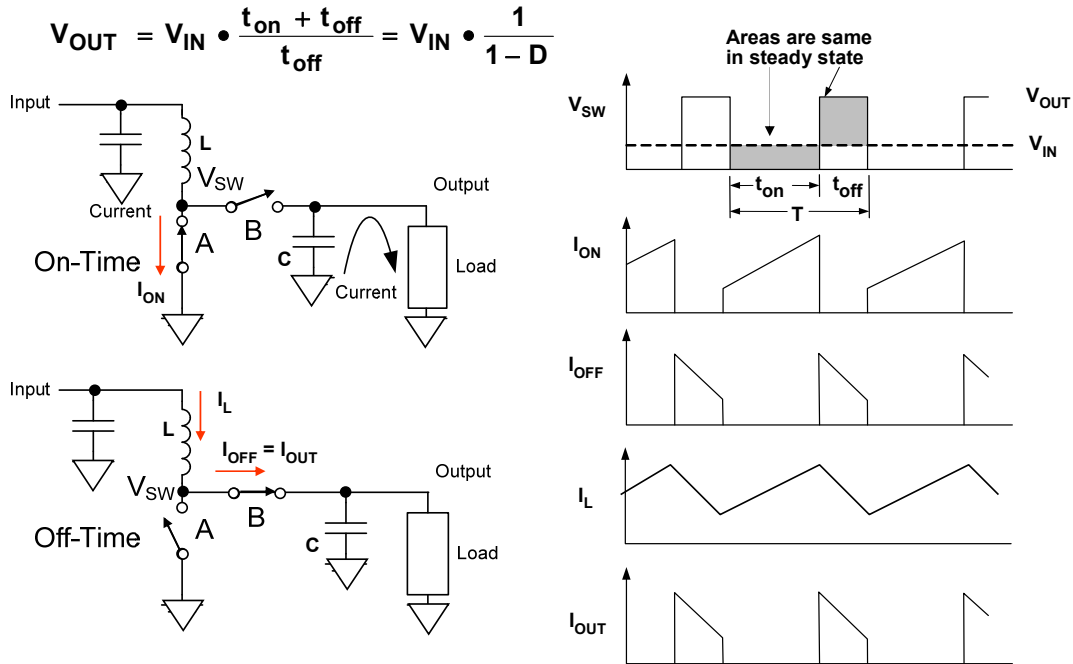
The switches are driven by complementary rectangular wave signals of a fixed frequency, but varying duty cycle (i.e., pulse width modulation, or PWM). During the "on-time" cycle when switch A is closed, there is a positive voltage dropped across the switching inductor causing current through it to ramp up linearly and store energy in the inductor's magnetic field. During the "off-time" cycle when switch B is closed, there is a negative voltage dropped across the inductor causing the current to ramp down linearly and releasing the energy stored in the inductor as it is transferred to the load.

The output voltage is equal to the input voltage multiplied by the duty cycle, D, of the PWM signal ($V_{IN} \times D = V_{OUT}$). The duty cycle is defined as the percentage of time of the total switching period that switch A is closed. The output voltage is regulated by a feedback loop which senses the output voltage, compares it to a fixed reference, and adjusts D accordingly. This method of control is called "voltage mode" control (VMC). Another popular control technique is "current mode" control (CMC) which uses an additional feedback loop which senses the inductor current as well.

The output capacitor (also called the "bulk" capacitor) acts in conjunction with the inductor to filter the voltage waveform at the switch node, V_{SW} . In addition, it must be able to handle the ripple current which is typically 20% to 30% of the static output current. The output ripple voltage magnitude is a function of the output capacitance, its parasitic equivalent series resistance (ESR), and the PCB parasitic impedances. In the normal operation of a buck converter, the output current is continuous, and the input current is discontinuous. This generally implies that additional filtering on the input is required in order to prevent EMI/RFI problems.

Note that as the load current decreases, it is possible for the inductor current to go to zero if switch B is unidirectional. This is called the "discontinuous" mode as opposed to the "continuous" mode when the inductor is always conducting.

Step-Up (Boost) Converter



The step-up or boost converter is rarely used in fixed power POL applications, because of the advantages previously discussed of always stepping down in voltage. The boost converter finds its primary use in portable equipment where the battery voltage is not great enough to power part or all of the electronics.

The basic boost converter shown here uses two switches and an inductor. The topology simply switches the position of the input and output to that of a buck converter. The result is a configuration which provides an output voltage which is greater than the input voltage. If all circuit elements are ideal there is no power loss, and the circuit is 100% efficient (practical circuits with real losses can approach 95% with careful design). The input power is equal to the output power: $P_{IN} = P_{OUT}$, and therefore $V_{IN} \times I_{IN} = V_{OUT} \times I_{OUT}$. This can mean very large input currents for large V_{OUT}/V_{IN} ratios.

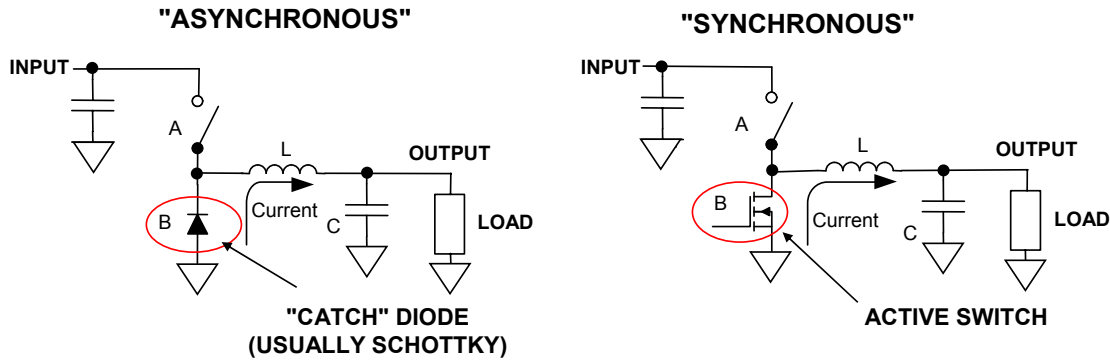
As in the buck converter, the boost converter switches are driven by two complementary PWM waveforms whose duty cycle determines the output voltage. The duty cycle is controlled by sensing the output voltage, comparing it to a known reference, and adjusting the duty cycle, D , accordingly. The relationship between the input and output voltages and D is given by $V_{OUT} = V_{IN} / (1 - D)$. Duty cycle (D) is defined as the percentage of time of the total switching period that switch A is closed.

During the "on-time" cycle when switch A is closed, the voltage across the inductor is equal to the input voltage, and the inductor current ramps up linearly as energy is stored in its magnetic field. Also during the "on-time" cycle, the bulk capacitor and the load are disconnected from the converter, the capacitor must supply the load current. During the "off-time" cycle when switch B is closed, there is a negative voltage dropped across the inductor equal to the output voltage minus the input voltage causing the inductor current to ramp down linearly as energy is delivered to the load via the inductor.

Unlike the buck converter, the boost converter has a discontinuous output current and a continuous input current. Output filtering requirements for the boost converter are therefore more stringent than in the buck converter, although the input to the boost converter is more benign.

DC-to-DC Converter Terminology:

- ◆ **Switching Regulator:** Switches are Internal (<5A)
- ◆ **Switching Controller:** Switches are External (0.1A to 40A)
- ◆ **Multiphase Switching Controllers:** Switches are External (About 40A / phase)



It is important to define some general terminology relating to dc-to-dc converters. Although these are widely accepted industry definitions, there may be some variation in usage between manufacturers.

The term switching *Regulator* implies that the switches are internal to the IC. These types of converters are typically limited to less than 5 A output current, although there are a few exceptions.

The term switching *Controller* implies that the switches are *External* to the IC. By using external PMOS and/or NMOS FETs, output currents up to about 40 A are possible.

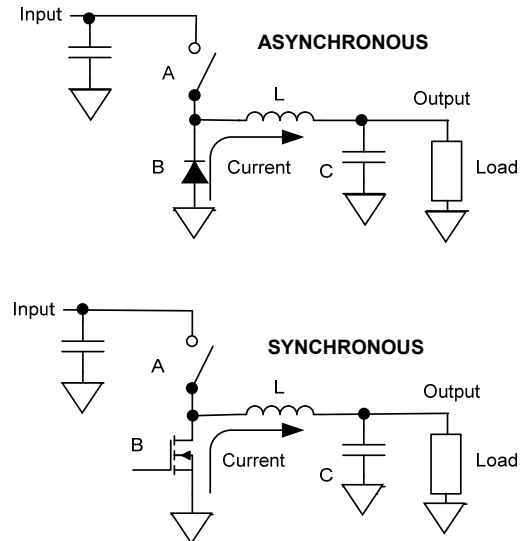
For higher currents, a parallel arrangement of buck converters, each operating with a phase offset. These types of converters are referred to as *Multiphase* controllers and can handle up to 40 A/phase.

The left side of the figure shows what is commonly referred to as an *Asynchronous* converter. A diode (usually a schottky diode) acts as the second switch. The diode is sometimes called a "freewheeling" diode or a "catch" diode.

The right side of the figure shows what is know as a *Synchronous* converter. In this case, both switches are active devices. The term "synchronous" implies that the switch drive signals must be carefully synchronized in order to ensure that both switches are not turned on at the same time, shorting the input to ground.

Step-Down DC-to-DC Converters: Synchronous Rectification

- ◆ Switch B can be either a diode or a NMOS device because inductor current is going only in one direction.
- ◆ Switch B traditionally is a freewheeling, "catch" diode that turns on automatically when Switch A is turned off. (Asynchronous Operation)
- ◆ Many modern step-down converters have replaced the diode with a NMOS device (Synchronous Operation)
- ◆ Advantages of Synchronous Rectification
 - Higher efficiency at nominal load because $I_{RMS}^2 \times R_{DS(ON)} < I_{RMS} \times V_D$
- ◆ Disadvantages of Synchronous Rectification
 - NMOS device can be more expensive than diode
 - Need for complementary drivers with anti-shoot through circuitry.
 - Efficiency is reduced at light loads because charge is removed from the output capacitor when the inductor current goes negative (This can be solved by adding a zero current crossing detector to disable the NMOS.)



We now look at synchronous rectification in more detail. Synchronous rectification has the chief advantage of higher efficiency because the diode is replaced with a low on-resistance NMOS device. The power dissipated in the NMOS device is generally less than that dissipated in the schottky diode for nominal output currents. As the duty cycle (V_{OUT}/V_{IN}) decreases the gains in efficiency will increase in the synchronous rectification buck configuration. This is because the low-side B switch is "on" a higher percentage of the time for low duty cycles, and therefore its power dissipation becomes more significant. For high current loads, several NMOS FETs can be paralleled. At steady state operation current will be evenly shared because the NMOS gate-to-source temperature coefficient is positive. Catch diodes, on the other hand, should not be paralleled because their temperature coefficient is negative, and one of the diodes could start to carry the majority of the current causing thermal runaway.

Synchronous rectification requires careful timing in the two switch drive signals in order to ensure that both switches are not on simultaneously.

The efficiency of the synchronous rectifier is reduced at light loads because charge is removed from the output capacitor when the inductor current goes negative. This can be prevented by using a scheme that can change switch B to a unidirectional device at light output loads.

Care must be taken when the synchronous regulator is powered up that there is no voltage on the load (referred to as a *pre-biased load*). Otherwise the low-side switch will short the voltage to ground, unlike the simple diode low-side switch. Most modern synchronous regulators sense this pre-bias condition and disable the low-side switch until the output voltage reaches its nominal value.

What Topology Depends Primarily on Output Current (Approximate Values Given Below)

◆ <5A:

- Asynchronous Controller (External Diode, External High Side Switch), ADP1864
- Synchronous Regulator (Internal High Side and Internal Low Side Switches), ADP2102, ADP2105, ADP2106, ADP2107, ADP2108

◆ 0.1A to 40A:

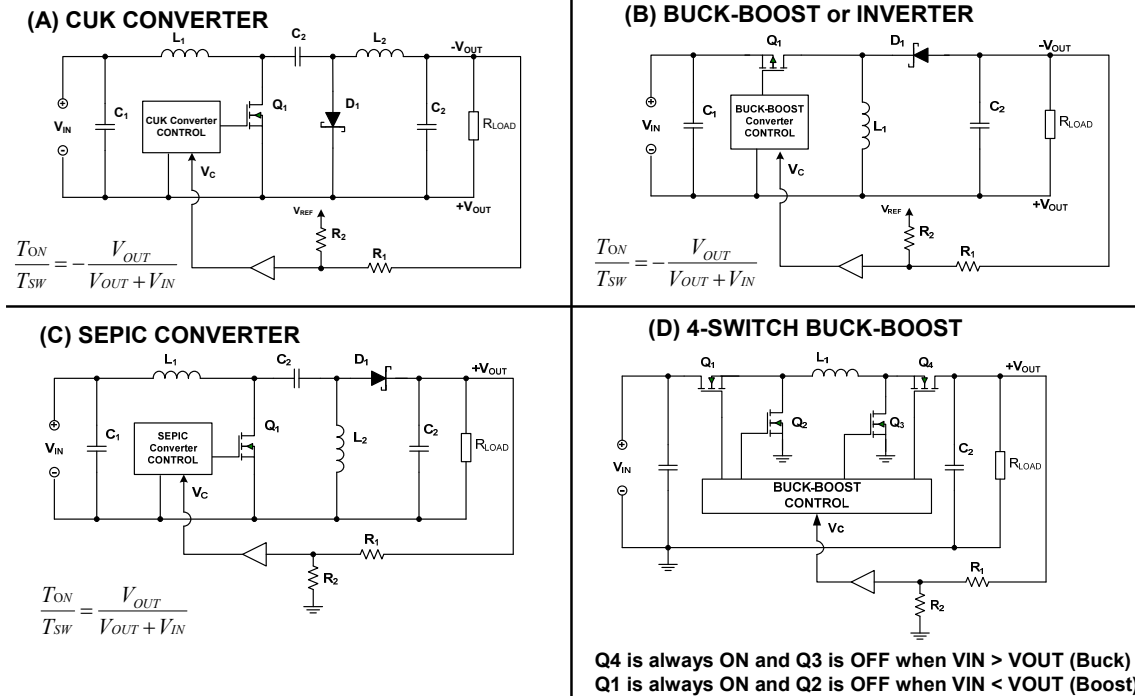
- Synchronous Controller (External High Side and External Low Side Switches), ADP1821, ADP1822, ADP1823, ADP1828, and ADP1829
- The ADP182x series have internal drivers capable of driving multiple N-channel MOSFETS in parallel. If the thermal environment allows for it, it is possible to get about 20A per pair, so the 40A is reached with a pair of MOSFETS on the high side and a pair on the low side.

These are some general guidelines showing where asynchronous and synchronous regulators and controllers are most often used.

For output currents less than 5 A, an asynchronous controller with an external diode and an external high-side switch, such as the ADP1864, is a good solution. For higher efficiency, synchronous regulators having internal high-side and low-side switches, such as the ADP2102, ADP2105, ADP2106, ADP2107, ADP2108 are good solutions.

For currents between approximately 0.1 A and 40 A, synchronous controllers with external switches, such as the ADP1821, ADP1822, ADP1823, ADP1828, and ADP1829, are good choices.

Other Switching Topologies



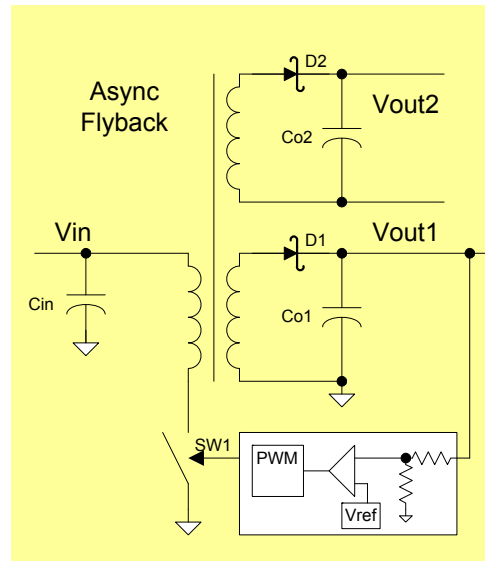
There are a variety of other switching converter topologies, and this figure shows a few of the more popular ones.

The CUK and Buck-Boost (Inverter) topologies shown in (A) and (B) provide a negative output voltage. The SEPIC and 4-Switch Buck-Boost shown in (C) and (D) provide a positive output voltage. The 4-switch Buck-Boost is an interesting topology, since it can step-up or step-down the input voltage and finds applications in battery operated devices. When the input voltage of the buck-boost is close to the output voltage, the converter runs in a 4-switch mode which allows a graceful transition between buck and boost modes. This feature can be extremely useful in battery powered systems.

The ADP2503 (0.6 A) and ADP2504 (1.0 A) are synchronous buck-boost regulators which have an input voltage range of 2.3 V to 5.5 V and outputs of 2.8 V, 3.3 V, 3.5 V, 4.2 V, 4.5 V, and 5 V. The 2.5 MHz switching frequency allows the use of a small 1 μ H ceramic inductor in an 0805 package. The devices use the basic topology of the 4-Switch Buck-Boost shown in (D) above.

Isolated Topologies: Asynchronous Buck-Boost-Flyback

- ◆ Multiple outputs track at fixed loading
- ◆ Most popular buck-boost
- ◆ $V_{OUT} > V_{IN}$ or $V_{IN} > V_{OUT}$
- ◆ ADP1610, ADP1611, ADP1621
- ◆ Easy to isolate V_{OUT}
- ◆ One magnetic element for multiple output voltages.
- ◆ Discontinuous Input Current
- ◆ Discontinuous Output Current



There is an entire family of switching converter architectures which make use of transformers rather than a simple inductor. These are referred to as "isolated" topologies because of the electrical isolation provided by the transformer. These types of converters are generally more suitable system power supplies rather than simple POL applications. It is, however, worth mentioning a few of the most popular.

Flyback converters have been very popular in consumer equipment due to low cost, low parts count potential, and ease of isolation. At low output power, multiple outputs track reasonably well, but a low cost LDO is often used to improve regulation and reduce ripple. Noise in the form of switching spikes and ringing increases with output power, making this topology most useful for supplies which are 50 W or less.

The ADP1621 controller is well suited for this topology. The gate drive voltage on the ADP1621 is limited to 5 V, making it useful with FETs rated for 100 V or less. For a 1:n transformer (coupled inductor), the voltage applied across SW1 when the output diode is conducting is equal to $V_{IN} + V_{OUT}/n$. There is also ringing on this node due to parasitics in the transformer, PCB, and switch, so the voltage rating of the primary side switch needs to be approximately $1.2 \times (V_{IN} + V_{OUT}/n)$ or higher, but not exceed 100 V.

Key Specifications

- ◆ **Input Voltage Range:** Specifies the regulator input supply voltage range where all the regulator specifications are satisfied.
- ◆ **Output Voltage Accuracy:** Specifies the output voltage error due to line, load, process, and temperature variations. In some cases the accuracy is specified for a given input voltage and output current value. In this situation, we need to add the Line and Load variations in order to estimate the total regulator accuracy.
- ◆ **Load Regulation:** Is the circuit's ability to maintain the output voltage regulation under varying loading conditions.

$$LoadReg = \frac{\Delta V_{OUT}}{\Delta I_{OUT}} \text{ in (mV or V). Another form can be: } LoadReg(\%) = 100 \times \frac{\Delta V_{OUT}}{V_{OUT} \times \Delta I_{OUT}} \text{ in \% / A or \% / mA}$$

- ◆ **Line Regulation:** Is the circuit's ability to maintain the output voltage regulation under varying input supply voltage conditions.

$$LineReg = \frac{\Delta V_{OUT}}{\Delta V_{IN}} \text{ in (mV or } \mu\text{V). Another form can be: } LineReg(\%) = 100 \times \frac{\Delta V_{OUT}}{V_{OUT} \times \Delta V_{IN}} \text{ in \% / V or \% / mV}$$

- ◆ **Dropout Voltage:** Is the minimum difference between unregulated input voltage and regulated output voltage for which the regulator operates within specification
- ◆ **Efficiency:** Specifies the power wasted by the regulator to perform input-output conversion

$$\eta(\%) = \frac{P_{OUT}}{P_{IN}} \times 100 \quad ; \quad P_{LOSS} = P_{IN} (1 - \eta)$$

The key regulator specifications are listed here for reference.

Key Specifications (Continued)

- ◆ **Quiescent Current (Ground Current):** Is the biasing current for the regulation circuit, typically in μA range. This parameter is important in battery operated equipment since the quiescent current will be consumed even if the load is removed. In some cases a shutdown pin is available to disable completely the biasing circuit of the regulator ($V_{\text{OUT}} = 0\text{V}$).
- ◆ **PSRR or Power Supply Rejection Ratio:** Is intimately related to the Line Regulation since the Operational (Error) Amplifier and regulator supply input are the same. The PSRR is expressed in dB and usually specified at specific frequency (PSRR deteriorate at higher frequency).

$$PSRR_{dB} = 20 \times \log_{10} \frac{\Delta V_{\text{OUT}}}{\Delta V_{\text{IN}}}$$

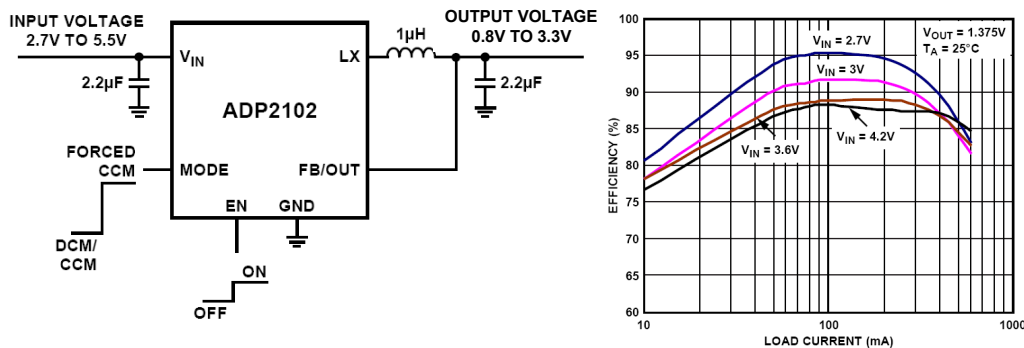
- ◆ **Output Noise:** This specification applies to Linear Regulators and quantifies the amount of noise generated by the internal circuits, most notably the Band Gap, it is specified in $\mu\text{V rms}$ over a specific frequency range (typically 10Hz to 100kHz). Low-Noise Regulators provide a bypass filter pin for an external bypass capacitor.
- ◆ **Load Transient Response:** Specifies the regulator's ability to respond to rapid changes of the load current. In most cases the data sheet shows a waveform of the output voltage perturbation due to load current change. This information is useful to test the regulator's stability. Expressed as ΔV_{OUT} for a ΔI_{OUT} at a given di/dt . ΔV_{OUT} will be a function of the converter bandwidth, Phase Margin, and power stage filter components.
- ◆ **Line Transient Response:** Similarly to Load Transient Response this parameter specifies the regulator ability to respond at rapid changes of the input voltage. Expressed as ΔV_{OUT} for a ΔV_{IN} at a given dV/dt .
- ◆ **Cross-Regulation:** In multi-regulator devices it is important to measure the influence of one regulator to another. For example in a dual regulator circuit the Cross-Regulation is specified as:

$$CrossReg = \frac{\Delta V_{\text{OUT1}}}{\Delta I_{\text{OUT2}}} \quad \text{or} \quad \frac{\Delta V_{\text{OUT2}}}{\Delta I_{\text{OUT1}}}$$

This is a continuation of key specifications.

Switching Frequency Considerations

- ◆ Early switchers operated in the 20kHz to 100kHz region
- ◆ Higher frequencies allow smaller inductors, but produce larger switching losses
- ◆ Modern switchers operate in the 100kHz to 3MHz range
- ◆ Frequency of some switchers can be "dithered" (spread spectrum) to reduce EMI/RFI
- ◆ Frequencies of some switchers can be synchronized to avoid beat frequency interaction
- ◆ ADP2102 3MHz synchronous switching regulator uses 1 μ H inductor with 95% efficiency for a 2.7V input and a 1.375V output @ 200mA



Early switchers operated in the 20 kHz to 100 kHz range, but there are several reasons for increasing the switching frequency. Higher frequencies allow smaller inductors and decrease size and parts cost. However, higher switching frequencies generate more switching loss and therefore require faster switches in order to maintain high efficiency.

In some applications where EMI/RFI is a major concern, it is possible to "dither" the switching frequency and reduce EMI/RFI. This is done by intentionally varying the switching frequency so that the switching energy is spread over a band of frequencies, thereby reducing the energy contained at any single frequency.

Some switchers can have their switching frequency synchronized to other switchers.

The ADP2102 switching regulator (internal switches) operates at 3 MHz and yields 95% efficiency for a 2.7 V input and a 1.375 V output at a 200 mA using a 1 μ H ceramic inductor in an 0805 package. Ceramic inductors are smaller and cheaper than winding coils, and typically half price. Minimum required input and output capacitors are 2.2 μ F ceramics with X5R or X7R dielectrics.

The ADP2108 switching regulator also operates at 3 MHz and can supply up to 600 mA. Input voltage range is 2.3 V to 5.5 V. Fixed output voltage options are available from 1.0 V to 3.3 V.

Methods for Designing Switchers

- ◆ **The Traditional Way:**
 - Use equations on the data sheet and a hand calculator (more than 50 equations are sometimes required (all of which will probably ignore non-linearities))
 - Design a spreadsheet to solve the equations
 - Ridley's Excel-Based "POWER 4-5-6"
 - These methods assume an experienced power designer
- ◆ **The Easier Way:**
 - Use manufacturer's website design tool (ADIsimPower) for straightforward POL applications
 - Use manufacturer's FAE support organization for complex designs
- ◆ **Based on design requirements, a good design tool should yield:**
 - An optimized design that "barely" meets the dc and ac specifications and is not an "overdesign"
 - Complete schematic
 - Top-level electrical, stability, and thermal analysis
 - Reasonable "What if" capability
 - Bill of materials, including manufacturers' part numbers
 - Evaluation boards for prototyping

The textbook approach to design a switching converter can be a daunting task for the engineer who must quickly design a point-of-load supply on a PC board. Most IC switching converter data sheets supply the large number of required equations, but solving them can easily get out of hand even using a spreadsheet.

Fortunately most successful manufacturers of switching converter ICs provide user-friendly selection guides and interactive website design tools for straightforward POL applications. An experienced field applications engineering support group should be available to assist with more complex designs.

Rapid design turnaround times are usually required because history tells us that the power supply portion of the PC board is usually the last thing to be designed.

There are several requirements of a good design tool. First and foremost, the design should be optimized to meet the required specifications, but should not be an "overkill." It should "barely" meet the dc and ac performance objectives.

The tool should yield a complete schematic, a top-level electrical, stability, and thermal analysis. In addition a complete bill of materials including manufacturer's part numbers is needed.

The tool should also provide some capability in playing "what if" scenarios, such as optimizing for efficiency, parts count, parts cost, or real estate.

Evaluation boards should be available for prototyping the final design. Custom evaluation boards for qualified opportunities should be available within one week.

Analog Devices' ADIsimPower design tool is discussed later in this section, and meets the requirements specified above.

Fundamental Switcher Calculations: This is Only the Beginning!

- ◆ **Select the Inductor Current Ripple, ΔI_L (Peak-to-Peak)**
 - Typically 30% to 40% of the nominal load current.
 - Increased inductor ripple current improves transient response and can decrease physical size.
 - Increased inductor ripple also increases output voltage ripple, RMS currents through inductor and switches, and inductor core loss.
- ◆ **Calculate the Inductor Value Based on Ripple Current, T_{ON} , and T_{OFF}**
 - $L = T_{ON} \times V_{ON} / \Delta I_L = T_{OFF} \times V_{OFF} / \Delta I_L$
 - Through the principle of Volt-second balance one can equate the target inductance value through either the off-time or on-time equation.
- ◆ **Calculate the Output Voltage Ripple Based on:**
 - Inductor Ripple Current
 - Bulk Capacitor Value
 - Bulk Capacitor ESR

Continued.....

This shows a few of the beginning steps in a switching converter design. Most switching converter data sheets provide these design steps along with the appropriate equations.

Stability and Transient Considerations

- ◆ **A switching regulator/controller is a closed-loop feedback system and is analyzed using basic control loop theory.**
- ◆ **There are excellent tutorials, equations, and graphs on the data sheet which provide the procedure for stabilizing the loop and optimizing load transient response.**
- ◆ **Stability/transient analysis depends on control mode architecture:**
 - Voltage control mode
 - Current control mode
- ◆ **PWM (Pulse Width Modulation)**
 - Constant frequency
- ◆ **PSM (Power Saving Mode) for efficiency for light loads**
- ◆ **PFM (Pulse Frequency Modulation)**
 - Constant ON time
 - Constant OFF time
- ◆ **The total output voltage deviation upon a large high di/dt load step is primarily dependent on the regulator's large signal behavior, which is not characterized by the control loop.**

Continued.....

Since a switching converter is a closed-loop feedback system, it must be analyzed for stability and transient response using basic control loop theory. This aspect of switching converter design can become especially tedious to the engineer unfamiliar with switching supplies.

Stability and transient analysis depend on the control architecture: voltage mode, or current mode.

Again, the data sheets provide guidelines in the design, but there is an easier way!

Power Losses in Switching Supplies Determine Efficiency

◆ **Efficiency Depends on the Total Power Loss in the Components:**

- Regulator/Controller IC Power Loss
- Inductor Power Loss (conduction and core loss)
- Input and Output Bulk Capacitor Power Loss (due to ESR)
- Diode Power Loss (Asynchronous)
- MOSFET Switching Power Loss
- MOSFET Conduction Losses
- Sense Resistor Power Loss
- Feedback Resistor Network Power Loss
- Efficiency Equations:

$$\eta = \frac{P_{IN} - P_{LOSS}}{P_{IN}} \quad P_{LOSS} = P_{IN}(1 - \eta) \quad \eta(\%) = \frac{P_{OUT}}{P_{IN}} \times 100$$

◆ **Thermal Analysis**

Continued.....

It is important to calculate the power loss in the various elements in the switching converter. This not only allows efficiency to be calculated but provides the necessary information to perform a thermal analysis.

Calculating each of these loss elements can be relatively easy ($P = I \times V$) or extremely difficult. MOSFET switching loss, for example, is a number that is not incredibly difficult to approximate. However, if all non-linearities are taken into account, one could spend a considerable amount of time arriving at an answer. Fortunately, the parasitics that cause switching loss can be approximated to arrive at results that are close enough.

ADIsimPower is Analog Devices' new dc-to-dc converter power management tool. This tool is available on the ADI website. The user provides power supply parameters, and ADIsimPower provides a solution selection guide that offers a list of topologies, ICs, and performance estimates. From this information, the designer can then proceed to the next step of the tool where he will get a customized schematic, BOM, and performance specs optimized to the design criteria.

ADIsimPower requires no login and no registration. The tool is created by experienced power supply designers. You can find a link to ADIsimPower under the Design Tools link on www.analog.com.

Before discussing ADIsimPower in detail, we will examine a few typical examples of POL power applications.

Powering FPGAs

FPGA Power Supply Considerations

- ◆ **Variable requirements between manufacturers and within part families**
 - Xilinx: *Spartan*[™] II, IIE, 3; *Virtex*[™] II, II Pro, II Pro X, 4, 5
 - Altera: *Cyclone*[™] II, III; *Stratix*[®] II, IIGX III, IIIL, IIIE, IIIGX, *Aria* GX
- ◆ **Multiple Voltage Rails Required: Core, Auxiliary, I/O, Transceivers, etc.**
- ◆ **Core Voltage (Typically 1.2V for 90nm processes, 0.9V for 65nm)**
 - Monotonic Ramp-Up required for proper initialization sequence.
 - Tolerance of 50mV or 60mV (5%) includes steady state, ripple, and load transient.
- ◆ **Core Current must be calculated based on design: 1A to 10A typical,**
 - But designer should allow adequate margin for error and software changes which can affect dynamic current.
- ◆ **High speed I/O transceivers generally require low noise linear regulators.**
- ◆ **External SDRAM Voltage Requirement: 1.8V (2.5V older SDRAMs).**
- ◆ **Power supply sequencing may be needed, but requirements vary.**

Field programmable gate arrays (FPGAs) are critical building blocks in many system designs. Manufacturers of FPGAs, such as Altera, Xilinx, and others, provide extensive documentation and on-line assistance in selecting, programming, and calculating the power requirements for these devices.

Each manufacturer offers several product families of FPGAs, each family offering varying degrees of performance, processing capability, and size. Simply selecting the appropriate device for a given application can be a daunting task.

After selecting the FPGA, calculating the current requirements and power dissipation based on the number of active tiles and other parameters is a critical step. Here again, the manufacturers also offer various tools to assist in the task.

FPGAs almost always require dedicated POL supplies. At a minimum, the FPGA will require a separate I/O voltage and a core voltage. Other auxiliary voltages may also be needed, as well as low noise supplies for the high-speed I/O section, if using such a device.

There is generally a fairly tight requirement on the supply voltage, typically $\pm 5\%$. This implies ± 60 mV for a 1.2 V core voltage. The $\pm 5\%$ specification includes transient response to load steps as well as dc tolerance and ripple voltage.

There is also a requirement that the supply voltage ramp-up monotonically in a defined period of time to ensure proper internal initialization. In some cases, the voltages must be applied in a specific sequence.

Proper Application of Power to FPGA

- ◆ **A certain sequence of events happens within the FPGA as the core voltage is applied (power-on reset, memory and timing initialization, etc.)**
- ◆ **Must reach core voltage monotonically between T_{MIN} and T_{MAX} to ensure proper initialization. It is mandatory that the POL regulator has a soft-start feature in order to control this ramp-up.**
- ◆ **Ramp rates also specified for other voltages: V_{CCAUX} , V_{CCO}**
- ◆ **Too little bulk capacitance makes load transient too large.**
- ◆ **Too much bulk output capacitance reduces load transient but increases charging current requirement.**
- ◆ **Increasing bulk capacitance beyond a certain point will force regulator into current limit and possibly cause a non-monotonic condition.**

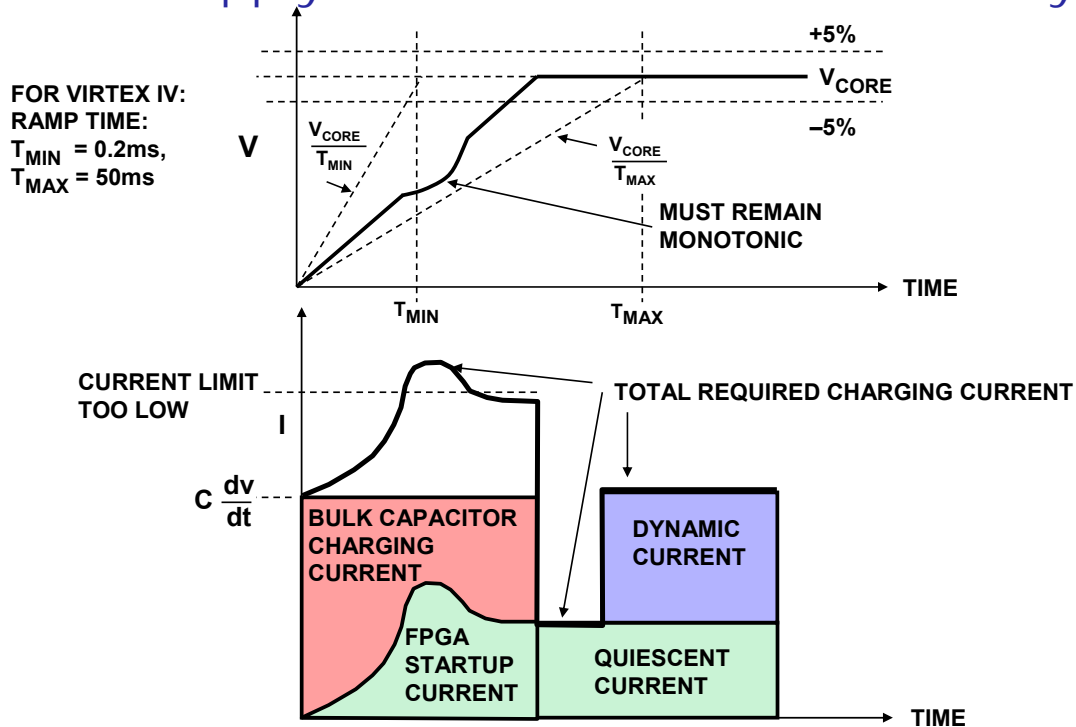
A certain sequence of events internal to the FPGA must occur during power-up in order for proper initialization and operation of the device. This includes power-on reset, memory, and timing initialization, etc.

For proper initialization, the core voltage must ramp-up to its final value monotonically within a specified time interval between T_{MIN} and T_{MAX} . The same ramp rate requirement generally applies to the other voltages as well. A POL regulator with a soft-start feature is mandatory in these applications.

In order to minimize transients due to rapid load step current changes, the total bulk capacitance on the POL regulator output can be quite large. However, the regulator must charge the bulk capacitor at a specified ramp rate, dv/dt , which implies a minimum charging current, $I = C dv/dt$. In addition, the regulator must supply the start-up current to the FPGA. If the regulator goes into current limit, its output will cease to be monotonic, and the FPGA may not initialize properly.

The bulk capacitor should therefore be large enough for proper load step transient response, but not so large that the POL regulator current limits and is non-monotonic.

Power Supply Must Charge Bulk Capacitance and Supply Inrush Current Monotonically



This is a good example of where too much bulk capacitance can hurt.

The voltage ramp-up must be completed within a specified time, in this case, 50 ms. The regulator must charge the bulk capacitance with a current of $I = C \frac{dv}{dt}$. In addition, the regulator must supply the FPGA start up current. The capacitor charging current and the FPGA start-up current must not exceed the current limit of the POL regulator, or a "dip" in the output voltage can occur, causing non-monotonicity.

In the figure above, the current limit of the POL regulator is too low, and the start-up voltage ramp has a corresponding "dip" which could cause initialization problems.

As previously mentioned, the soft-start feature of the POL regulator can be used to control the ramp rate, but care must be taken in selecting the value for the total bulk capacitance in order to ensure that both load transient performance and monotonic ramp-up can be achieved simultaneously.

Sequencing/Power-On Issues with FPGAs

- ◆ **Most FPGAs do not have "strict" sequencing requirements**
- ◆ **However, some FPGAs have "recommended" sequencing that will minimize inrush current at power-on**
- ◆ **Maximum required "Start-Up or Power-On" current is usually specified by FPGA manufacturer.**
- ◆ **The "power-on" current does not include the extra current required to charge the bulk capacitance at the specified ramp rate**
- ◆ **In most cases, sequencing is not required if supplies can meet the power-on current requirements, and the supplies are brought up more or less simultaneously.**
- ◆ **As with all CMOS logic, the digital input voltages to the FPGA should not be more than 0.3V to 0.5V above the I/O power supply during startup.**
- ◆ **The external FPGA clock oscillator must be running during the start-up sequence for proper initialization.**
- ◆ **Always read the FPGA data sheet and user manual.**

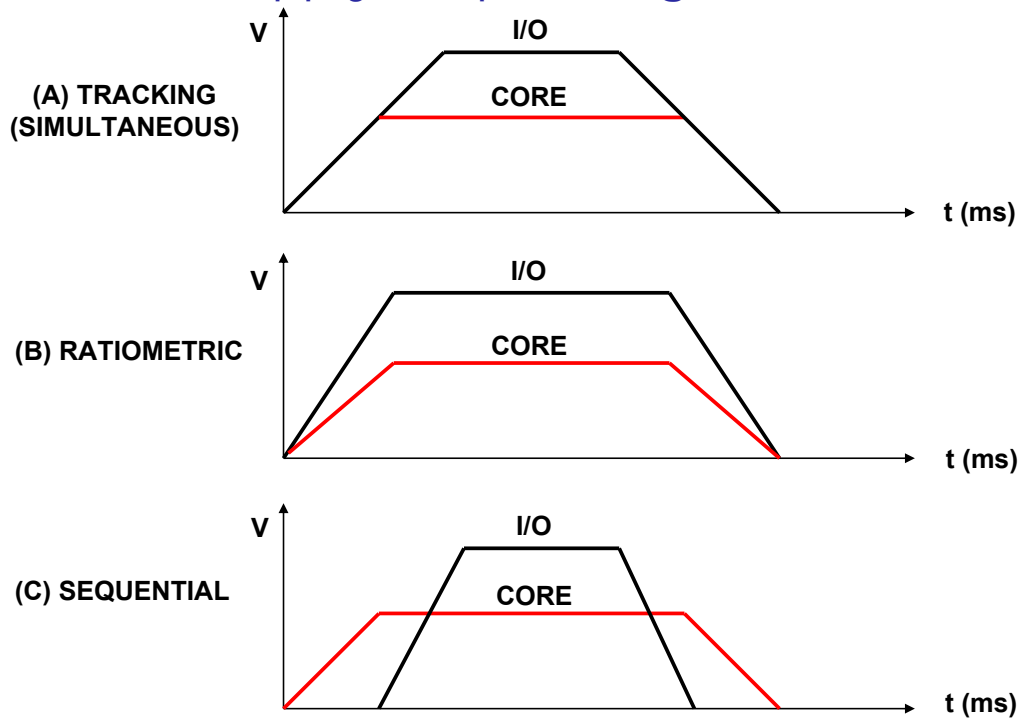
Most FPGAs do not have specific sequencing requirements. However, it may be desirable to sequence the supplies in order to prevent large inrush current, and many FPGAs have a recommended sequence if the supplies are not turned on simultaneously.

However, there is usually no need for sequencing if the supplies can meet the inrush current requirements and maintain a monotonic ramp.

As with all CMOS logic, the digital input voltages to the FPGA should not be more than 0.3 V to 0.5 V above the I/O power supply during startup.

The FPGA data sheet should be consulted with respect to the external clock oscillator requirements. In most cases, the oscillator must be running during the ramp-up sequence for proper initialization.

Simultaneous, Ratiometric, and Sequential Supply Sequencing Methods



This shows the three common methods of sequencing the core and I/O voltages.

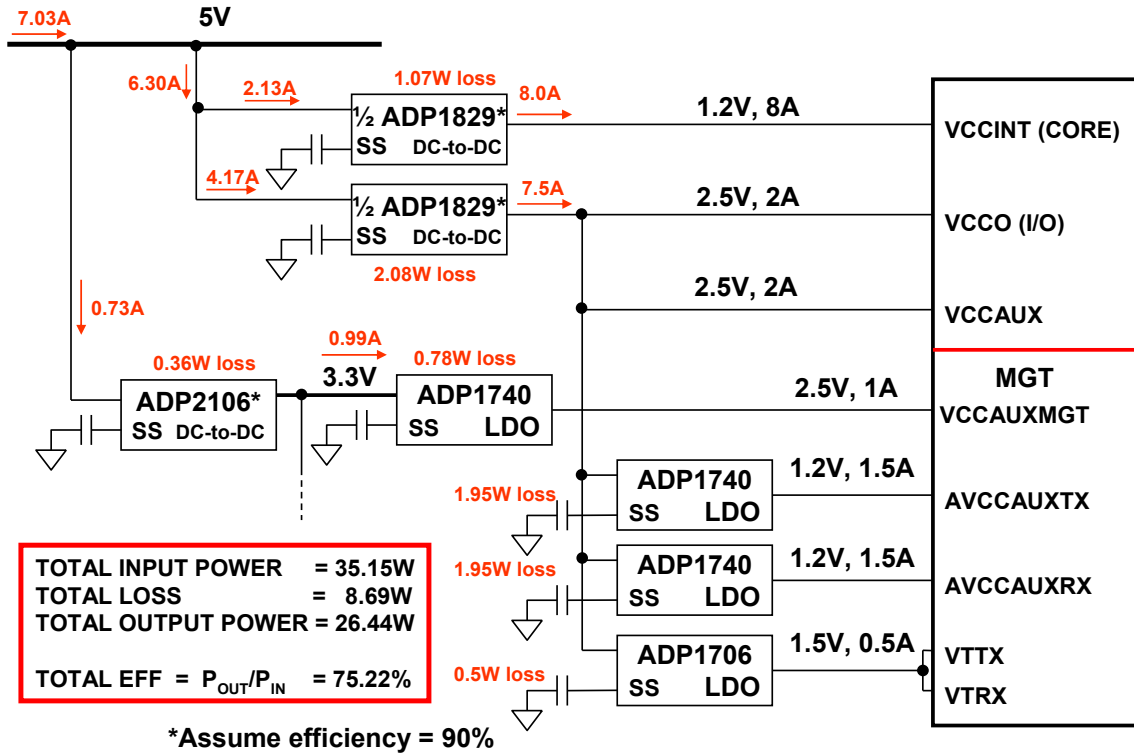
The *Simultaneous* method is shown in (A), where the core and I/O voltages track each other during power-on.

The *Ratiometric* method of sequencing is shown in (B).

The *Sequential* method shown in (C) is often used to prevent large inrush currents.

Sequencing is most easily accomplished with ICs designed specifically for the task and is described in more detail in Section 2 of the seminar.

Xilinx Virtex-4 FPGA Power Supplies



This shows a possible arrangement for supplying power to the Virtex-4 FPGA from a single 5 V bus.

The values of current chosen in the example are representative. An actual FPGA design may have different values and therefore a different power structure could be required.

The core voltage of 1.2 V and the 2.5 V I/O and auxiliary voltage are supplied by a dual synchronous switching controller, the ADP1829. The ADP1829 phase shifts the switching of the two step-down converters by 180°, thereby reducing the input ripple current. This reduces the size and cost of the input capacitors.

The 2.5 V output of the ADP1829 also acts as an intermediate bus to supply the low noise LDOs required to drive the MGT portion of the FPGA. The soft-start feature of the various regulators and controllers can be used to control the slope of the ramp during power up. Finally, an ADP2106 synchronous switching regulator generates an intermediate 3.3 V bus which drives an ADP1740 LDO which in turn generates the auxiliary 2.5 V for the MGT section.

The 3.3 V can be distributed to other parts of the system if desired.

Note that the diagram does not show the important localized decoupling at each of the power supply pins of the FPGA.

Switching Supply Error Budget Must Include Transient in Most FPGA Applications

**Total Error Budget (Including Load Transient)
for 1.2V Core Voltage = ±5% (±60mV)**

ERRORS	CALCULATION	%
$V_{REF}: \pm 1.0\%$	1.0%	1.00
1% FEEDBACK RESISTORS	WORST CASE = 1%	1.00
OUTPUT RIPPLE	1% OF V_{OUT} (p-p)	0.50
LINE REG: 0.12mV/V	$0.12\text{mV/V} \times 5\text{V} \times 5\%$	0.03
LOAD REG: 0.07%/A	$0.07\%/A \times 10\text{A}$	0.70
TOTAL STATIC ERRORS		3.23
LOAD TRANSIENT ERROR	$\{(5\% - 3.23\%) \div 100\} \times 1.2\text{V}$	21.2mV

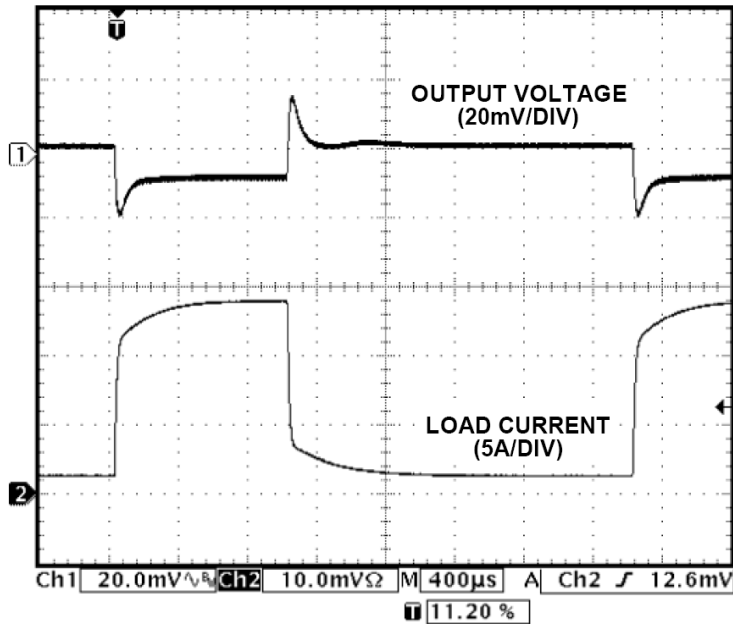
DATA BASED ON ADP1829 SWITCHING CONTROLLER

The power supply error budget for an FPGA must not only include the static errors but also the load transient error resulting from the load step.

This table shows how the various error sources are allocated for a typical application using the ADP1829 dual synchronous switching controller.

The basis core voltage of 1.2 V has a total tolerance of ±5% (± 60 mV). The total static errors include the following: internal voltage reference error, feedback resistor tolerance, output voltage ripple, line regulation, and load regulation. The sum of the static errors is 3.23%. This leaves $5\% - 3.23\% = 1.77\%$, or 21.2 mV for the transient error.

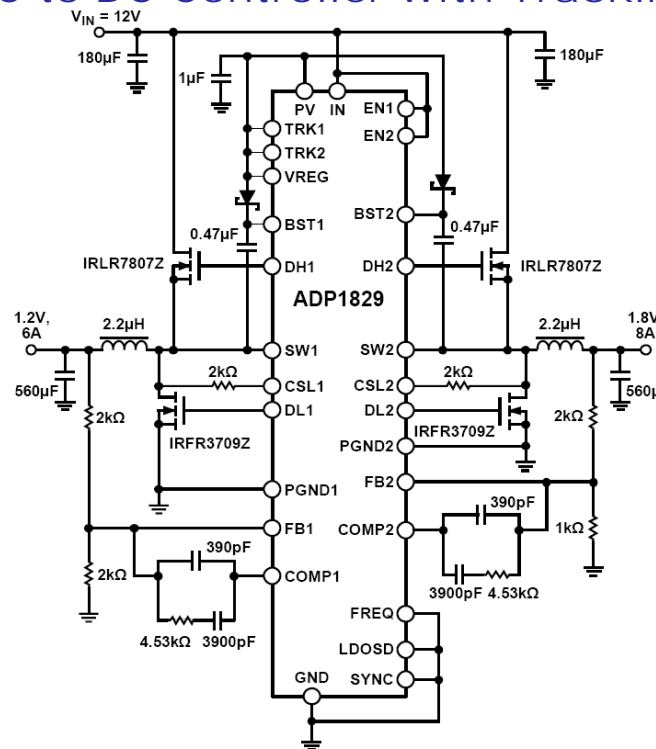
ADP1829 Load Transient Response

**1.5A TO 15A LOAD TRANSIENT, 12V INPUT**

The ADP1829 load transient response is shown here for a load current step of 1.5 A to 15 A. Note that the total output transient is approximately 38 mV p-p.

It should be noted that achieving this level of transient performance often involves some level of in-circuit optimization as well as a good design tool (ADIsimPower).

ADP1829 Dual, Interleaved, Step-Down DC-to-DC Controller with Tracking



The ADP1829 is a versatile, dual, interleaved, synchronous PWM buck controller that generates two independent output rails from an input of 3.0 V to 18 V, with power input voltage ranging from 1.0 V to 24 V. Each controller can be configured to provide output voltages from 0.6 V to 85% of the input voltage and is sized to handle large MOSFETs for point-of-load regulators. The two channels operate 180° out of phase, reducing stress on the input capacitor and allowing smaller, low cost components.

The ADP1829 is ideal for a wide range of high power applications, such as DSP and processor core I/O power, and general-purpose power in telecommunications, medical imaging, PC, gaming, and industrial applications. The ADP1829 operates at a pin-selectable, fixed switching frequency of either 300 kHz or 600 kHz, minimizing external component size and cost.

For noise-sensitive applications, it can also be synchronized to an external clock to achieve switching frequencies between 300 kHz and 1 MHz. The ADP1829 includes soft start protection to prevent inrush current from the input supply during startup, reverse current protection during soft start for precharged outputs, as well as a unique adjustable lossless current-limit scheme utilizing external MOSFET sensing.

For applications requiring power supply sequencing, the ADP1829 also provides tracking inputs that allow the output voltages to track during startup, shutdown, and faults. This feature can also be used to implement DDR memory bus termination.

The ADP1829 is specified over the -40°C to +125°C junction temperature range and is available in a 32-lead LFCSP package.

Interleaving the switching of the two step-down converters by 180° reduces the input ripple current. This reduces the size and cost of the input capacitors.

Powering DSPs

www.analog.com/dsp

Typical Low Power DSP and FPGA Voltage and Current Requirements

	PART NUMBER	V _{CORE} (V)	V _{I/O} (V)	I _{CORE} (mA)	I _{I/O} (mA)
ADI	ADSP-21xx (16-bit)	1.8 to 2.5	3.3	25 to 200	15
	ADSP-BF531, ADSP-BF532, ADSP-BF533	0.8 to 1.4	2.5 to 3.3	25 to 300	150
	ADSP-BF534, ADSP-BF536, ADSP-BF537	0.8 to 1.2	2.5 to 3.3	25 to 300	150
	ADSP-21xxx (SHARC)	1.2 to 3.3	3.3	940 (typ)	72
Marvell	PXA270 (Intel)	0.8 to 2.0	1.5 to 3.4	600 (typ)	150
Xilinx	Spartan IIE FPGA XC2S50E, XC2S300E	1.8	1.5 to 3.3	200 to 2000	500
Altera	Max II CPLDs	1.8 to 3.3	1.5 to 3.3	100 to 400	150 to 400
	Cyclone FPGA	1.5	1.5 to 3.3	1000 (typ)	600

NOTE: Approximate currents only. Actual currents depend on operating conditions.

DSPs are optimized for performing fast arithmetical operations. A repetitive series of multiplications and accumulations forms the basis of digital filters and FFT processing, and DSPs perform these functions much faster and more efficiently than standard microprocessors.

Field programmable logic gate arrays (FPGAs) and complex programmable logic devices (CPLDs) can also be programmed to perform these and other functions.

This table lists some popular relatively low power processors suitable for general purpose applications, along with the core and I/O typical voltages and currents.

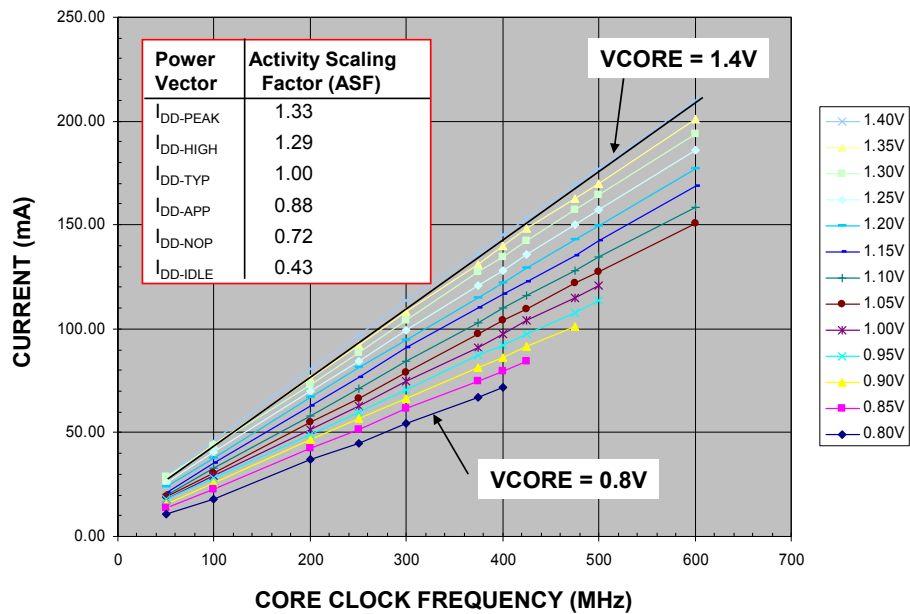
It should be noted that the actual core and I/O currents (to a lesser degree) are highly dependent on the task activity, core voltage, clock frequency, process, and temperature.

These devices all have current requirements less than 2 A, which makes them ideal candidates for integrated synchronous switching regulators.

Because of their widespread usage in portable applications, efficiency, parts cost, and total size are important parameters of the POL design.

In the following section we examine the DSP core current variation and offer some easy solutions to core and I/O voltage supplies.

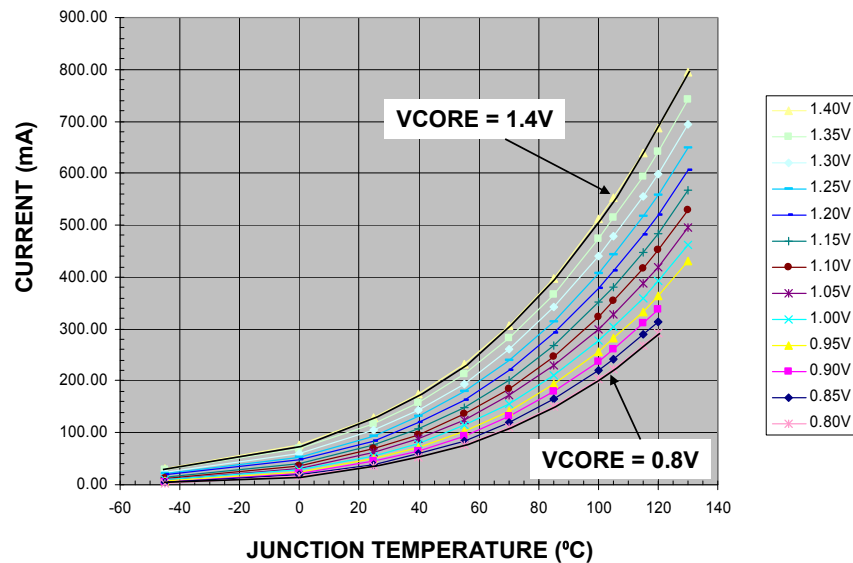
ADSP-BF534, ADSP-BF536, ADSP-BF537 I_{DD} Typical Dynamic Current ($I_{DD-BASELINE-DYN}$)



DSP dynamic operating current is highly dependent on the core voltage and the processor clock frequency as shown in this figure for the ADSP-BF534, ADSP-BF536, and ADSP-BF537 family of processors. This allows the core voltage and clock frequency to be optimized for a specific task.

This is a "baseline" current and can be viewed as being scaled by the type of instructions being executed in the processor. There is a table in the figure that gives some representative activity scaling factors. The peak value is a worst case with dual multiply-accumulates (MACs), and is not sustainable—a real application would be a mix of activities, and would typically correspond to a 1.0 multiplier. For low to idle activity, the current consumption drops about in half of the baseline value.

ADSP-BF534, ADSP-BF536, ADSP-BF537 Maximum Static Current ($I_{DD-DEEP\ SLEEP}$)



One issue that should definitely be considered is the relatively high leakage currents of some of the latest high speed CMOS processes, (i.e the 0.13 μm "fast" process used for the ADSP-BF537). The graph in the figure shows the "deep sleep" maximum static current as a function of junction temperature for various core voltages. Also, part-to-part variations in the process can have > 50 mA variation in current while in the "sleep" mode. As we target faster frequencies, a price is paid with higher leakage currents and wider variations in the process parameters. ADI is introducing an "LP" version of the Blackfin® ADSP-BF52x parts which will be on a slower process and limited to lower operating frequencies (300 MHz to 350 MHz core). In addition, DSPs with large internal memories can have significant leakage when in the "sleep" modes.

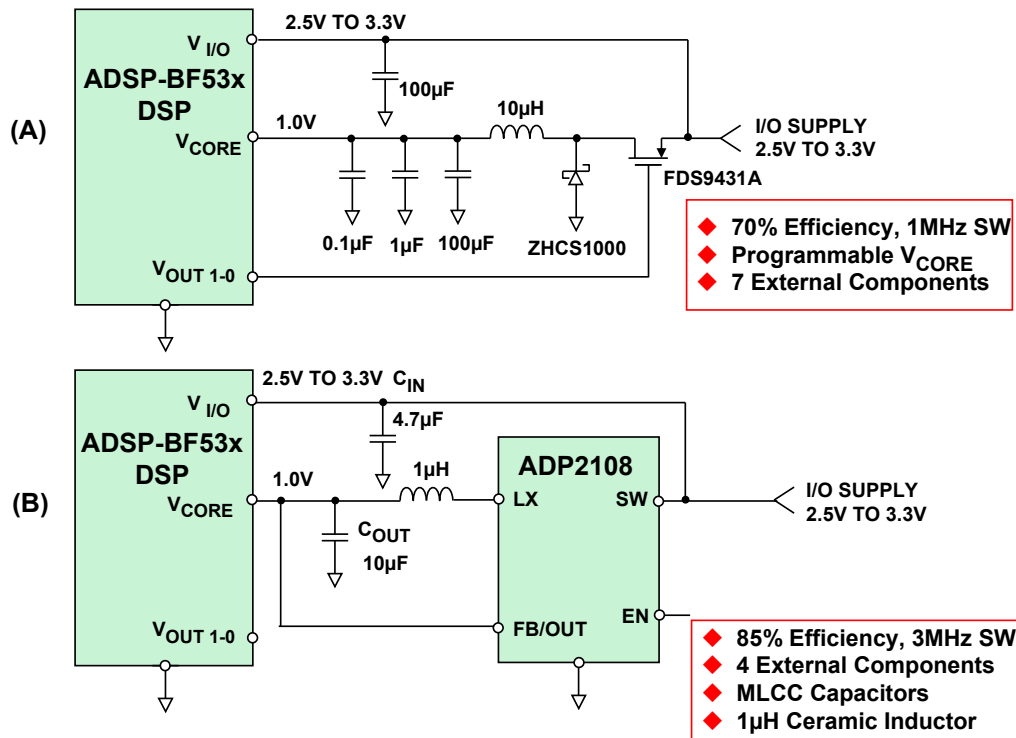
And another very significant issue is the relationship of static current to temperature. This again is primarily due to the high leakage currents of fast processes, and can lead to a $5\times$ increase in current as temperature goes from 20°C to 100°C—and it is more of an exponential relationship (and also increases with core voltage). Therefore, the "static" leakage can be as high as the "dynamic" current.

A good guideline is a 1:4 ratio of "low" load to "high" load for the processors, and for the ADSP-BF537, this would approximately be 80 mA to 320 mA.

REFERENCE:

"Estimating Power for ADSP-BF534/BF536/BF537 Blackfin Processors," *Engineer-to-Engineer Note EE-297*, 2007, Analog Devices, www.analog.com

Blackfin Power Solutions



Most of the Blackfin DSPs have an on-chip 1 MHz switching controller as shown in (A). The core voltage is derived from the I/O voltage. This circuit requires an external PMOS high-side switch and a free-wheeling Schottky diode as well as input and output filter capacitors. The core voltage can be programmed in 50 mV increments, and the efficiency is approximately 70%.

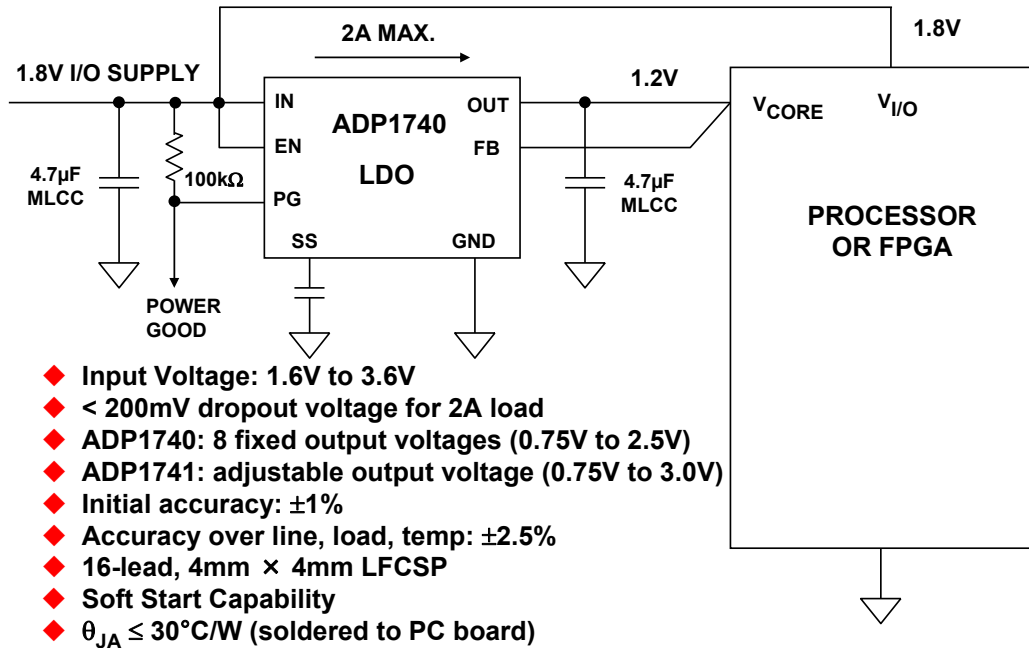
The ADP2108 600 mA 3 MHz synchronous switching regulator makes an attractive alternative to the internal regulator. The design is shown in (B). Only 4 external components are required (including the ADP2108), and the efficiency is greater than 80% for a 600 mA load current. Its input voltage range is 2.3 V to 5.5 V. In this application, it is driven by the I/O supply which must be between 2.5 V and 3.3 V for the BF53x series. A small 1 µH ceramic inductor and two MLCC capacitors are the only passive components required in the design. The design shown in (B) was done using ADIsimPower.

Most DSPs are relatively immune to power supply sequencing issues. They are usually initialized through an external non-volatile RAM, and an external supervisory circuit should always be used to reset the DSP on power-up. The DSP data sheet should be carefully checked for clock requirements on power-up. Some DSPs require that the clock be present during the initial power-on reset time. Regardless, the data sheet must always be consulted regarding these issues.

REFERENCES:

1. "Switching Regulator Design Considerations for ADSP-BF533 Blackfin Processors," *Engineer-to-Engineer Note, EE-228*, Analog Devices, 2005, www.analog.com.
2. "Using External Switching Regulators with Blackfin Processors," *Engineer-to-Engineer Note, EE-339*, Analog Devices, 2008, www.analog.com.

A Simple Solution to a Tricky Problem: Replacing 1.8V Core Supply with 1.2V Supply



Processors are rapidly moving to faster CMOS processes which have correspondingly lower geometries and hence lower core voltage requirements. For instance, upgrading from a 1.8 V to a 1.2 V core voltage is a common problem. Rather than redesign the switching supply, an attractive alternative can be the use of a simple LDO as shown in this figure.

The ADP1740 LDO has only 200 mV dropout voltage for a 2 A load. In the example shown it is used to regulate the 1.8 V I/O supply down to 1.2 V. The power that must be dissipated in the ADP1740 is therefore $2 \text{ A} \times 0.6 \text{ V} = 1.2 \text{ W}$. The ADP1740 16-lead, 4 mm × 4 mm LFCSP package with an exposed pad has a thermal resistance of $\theta_{JA} = 30^{\circ}\text{C/W}$, therefore the junction-to-ambient temperature rise is only $1.2 \text{ W} \times 30^{\circ}\text{C/W} = 36^{\circ}\text{C}$.

The ADP1740 is designed to operate with V_{IN} as low as 1.6 V to increase efficiency. The low 200 mV nominal dropout voltage at a 2 A load improves efficiency and allows operation over a wider input voltage range. In the above example, the efficiency is $1.2 \div 1.8$, or 67%.

The ADP1740 optimizes powering of core voltages between 0.13 μm to 65 nanometer process geometries directly from the I/O voltage. This minimizes complexity by reducing component count and ensures proper supply voltage sequencing protecting the system IC device load.

The ADP1740 has an internal soft start that provides a constant startup time of 200 μs . Short circuit protection and thermal overload protection protect the devices in adverse conditions.

A power good output allows power system monitors to digitally check the health of the output power rail voltage.

For lower core currents, the ADP170, 300 mA LDO operates on input voltages between 1.6 V and 3.6 V. Output voltage options from 0.8 V to 3.0 V are available.

For I/O voltages less than 1.6 V, the ADP130 dual, 350 mA LDO operates with input voltages between 1.2 V and 3.3 V. The device requires an additional bias voltage of 2.3 V to 5.5 V.

ADIsimPower

www.analog.com/adisimpower

What is ADIsimPower?

- ◆ **Web based DC-to-DC power management tool available to anyone with an internet connection**
- ◆ **Includes integrated “solution” selection guide**
- ◆ **Produces a Schematic, BOM, and performance specs customized for *your* application**
- ◆ **Requires no registration and no login**
- ◆ **Architected, designed, and used by Power Management Application Engineers**
- ◆ **Where do I find it?**



ADIsimPower is Analog Devices’ new dc-to-dc converter power management design tool. This tool is available on the ADI website. The user provides power supply parameters, and ADIsimPower provides a solution selection guide that offers a list of topologies, ICs, and performance estimates. From this information, the designer can then proceed to the next step of the tool where he will get a customized schematic, BOM, and performance specs optimized to the design criteria.

ADIsimPower requires no login and no registration. The tool is created by experienced power supply designers. You can find a link to ADIsimPower under the Design Tools link on www.analog.com, or simply go to www.analog.com/adisimpower.

ADIsimPower Value Advantages

- ◆ **Differentiators**
 - **Intelligent Selector Guide that predicts performance in the four major design goals to rank available solutions**
 - **User chooses the primary design goal: Cost, Size, Efficiency, or Parts Count**
 - **Pre-qualified components library includes unpublished data**
 - **Comparative 1k pricing given on all components**
 - **Input filter support for crosstalk suppression**
 - **Designs for load transient steps from 10% to 100% of maximum output current**
 - **Dissimilar output capacitors are used to achieve large and small signal targets**
 - **Prototyping PCBs sold for fast verification**
- ◆ **ADIsimPower is NOT a Simulation Program**
 - **Competitors offer simulation in place of custom design support**
 - **Users must use a simulator and hours of design time trying to tweak a data sheet circuit to meet requirements**

ADIsimPower is not a copy of any other design tool. It mimics the process a power engineer would use to design a converter. It has several features that distinguish it from competitors' tools.

The selector guide in View 2 is not a parametric IC search. It is a solution selector guide that estimates and compares performance of multiple converters and topologies. Many competitors' tools will provide you with a list of ICs that will work, but they do not qualify and quantify how they might perform in relation to each other.

ADIsimPower users can select their primary design goal based on their application.

The customized BOM has a list of components that are qualified and optimized to work in the configuration provided by the user. The qualification process uses data that is both published and unpublished. Analog Devices has worked with the manufacturers of the various components in the converter to get 1k pricing to allow the user make price versus performance tradeoff decisions.

ADIsimPower also has an option that will design an optimized input filter to suppress crosstalk if necessary.

The tool will design the output filter to meet load transient and output voltage ripple specifications by using dissimilar output capacitors, a feature which is not offered in competitors' design tools.

Once the user is satisfied with the design ADIsimPower has provided, he is given the means to build and test his design by ordering a blank PCB that will accommodate the design.

ADIsimPower is not a time-based simulation design tool. While simulation tools can be very useful, they generally require expertise in power electronics that most designers do not have.

Vendor Database

- ◆ **Total Number of Parts in Database Exceeds 4000**
 - All have behaviors that are unique to their construction that are modeled by working with their MFGs to get unpublished data.
- ◆ **Capacitors – MLCC, Tantalum, Aluminum Organic, Aluminum Electrolytic, and more...**
 - Performance predicted for:
 - ◆ DC Voltage Applied
 - ◆ Temperature
 - ◆ ESR over Frequency
- ◆ **Inductors – Ferrite, Powdered Iron, Hybrid Materials**
 - Range of applications: Mobile, VRM, Isolated
 - Core loss data obtained directly from manufacturer
 - Coilcraft parts included
- ◆ **MOSFETs and Diodes – Parts optimized for cost, efficiency, and size included in database**
 - Vendors
 - ◆ NEC, Infineon, Vishay, IR, ON, Diodes Inc
 - DC and transition losses predicted for:
 - ◆ Drive Voltage
 - ◆ Temperature
 - ◆ Vds Voltage Applied

The vendor database consists of the following parts:

Inductors

Materials matter when determining which is the best part. The unique properties of each of these materials has been taken into account via the core loss equations. Much of this data is not published by the manufacturer.

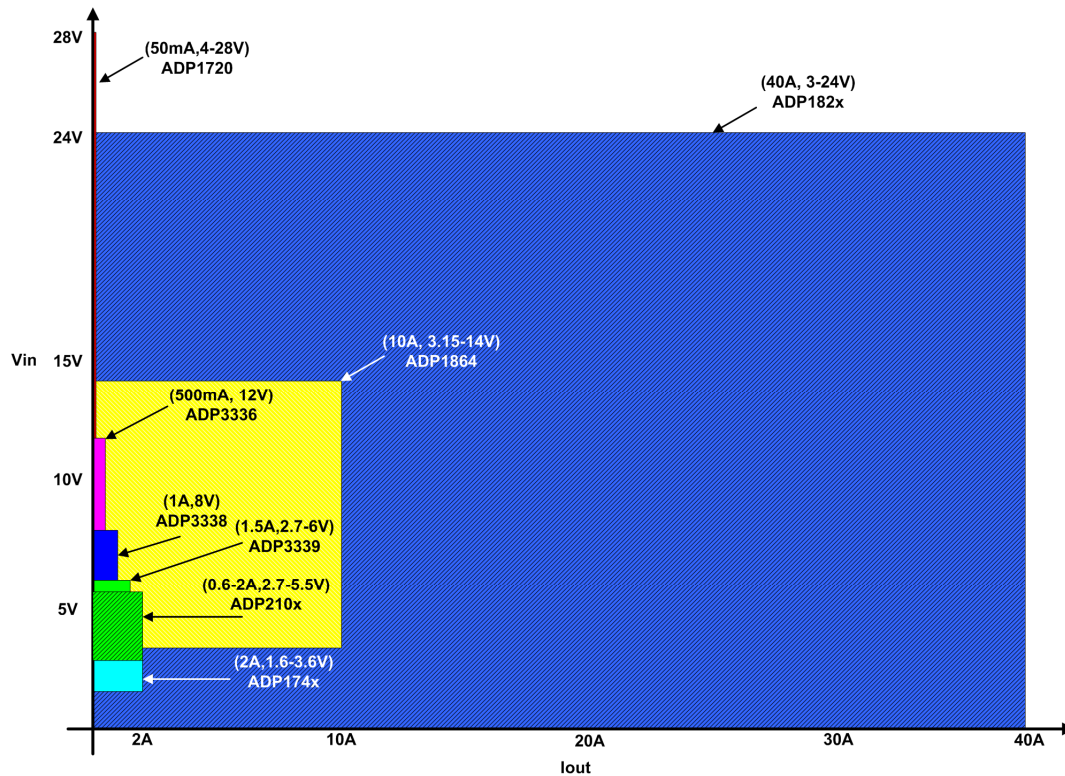
Capacitors

Many types are included in database. Each have different behavior over temperature and applied voltage, etc.

MOSFETs and Diodes

The best performers have been selected for efficiency, size, and cost.

Application Space Covered by ADIsimPower



This is a graph of the application space covered by ADIsimPower’s comprehensive solutions. Output load current is on the x axis and input voltage is on the y axis. You can see the ADP182x family of switching controllers takes up the majority of the area on this screen. This is a tool that is another true Analog Devices’ differentiator—no other tool in the industry provides customized and optimized full solutions for synchronous controllers.

Other families of parts included in the ADIsimPower comprehensive solution application space are the ADP210x integrated switching regulators, ADP1864 asynchronous switching controller, and all linear regulators in the ADI portfolio.

Analog Devices has many ICs in power management that cover spaces not shown in this graph. We are in the process of implementing comprehensive solutions for these ICs. The ADIsimPower tool will have quarterly updates, which will add more topologies and more application spaces.

ADIsimPower Video

ADIsimPower Step 1: Enter Your Design Criteria

The screenshot shows the ADIsimPower web interface. At the top, there is an Analog Devices logo and a search bar. Below the logo, there are navigation links: "ADI Home > Design Tools & Support > Design Tools". The main heading is "Design Tools: ADIsimPower™" with a "Submit Feedback" link. A progress bar shows four steps: "1 Enter Your Design Criteria", "2 View All Design Solutions", "3 View Solution Details", and "4 Build Your Design". The main content area is titled "Welcome to ADIsimPower™" and includes the text "- the most accurate and fastest DC-DC power management design tool! (Learn more...)". Below this, there is a section "Enter your design criteria or choose the IC you wish to design into your solution." with a form containing five input fields: Vinmin (V), Vinmax (V), Vout (V), Iout (A), and Tmax (°C). The Vinmin field has a value of 4.5 and a range of 2.50 ≤ x ≤ 80. The Vinmax field has a value of 5.5 and a range of 2.50 ≤ x ≤ 80. The Vout field has a value of 1.2 and a range of -7 ≤ x ≤ 100. The Iout field has a value of 0.3 and a range of 0.001 ≤ x ≤ 50. The Tmax field has a value of 55 and a range of -40 ≤ x ≤ 125. There are three buttons: "Find Solutions", "Use Dual Channel Device", and "Clear Fields". To the right of the form is a graphic with the text "ADIsimPower™" and a circuit diagram showing an ADP1025 and ADP1025 CH2 IC. At the bottom, there is a footer with links for "Privacy/Security", "myAnalog", "Contact ADI", "Site Map", "Registration", "Technical Support", and "Terms of Use", along with the copyright notice "© 1995-2008 Analog Devices, Inc. All Rights Reserved".

ADISimPower will guide you through a four step process, which will result in you receiving a complete solution including schematic, bill of materials, efficiency curves, and other key performance specifications for your application.

Step 1: Enter Your Design Criteria—

Enter your dc-to-dc power supply design requirements or if you know which IC you'd like to use, you may select it from a drop down list. This will take you directly to the third step, View Solution Details.

You'll enter the range of the input voltage the converter will see in Vinmin and Vinmax.

Enter the output voltage and output current of the converter in the Vout and Iout boxes respectively.

Finally enter the ambient temperature over which the converter must operate.

You can also click dual channel device if you'd like to use an IC that can generate two rails.

ADIsimPower Step 2: View All Design Solutions

All fields are required

Vinmin (V) Vinmax (V) Vout (V) Iout (A) Tmax (°C)

2.50 ≤ Vin ≤ 60 2.50 ≤ Vin ≤ 60 -7 ≤ Iout ≤ 100 0.001 ≤ Iout ≤ 50 -40 ≤ Tmax ≤ 125

[Find Solutions](#) [Use Dual Channel Device](#) [Clear Fields](#)

Recommended Solutions

Criteria	IC	Topology
View Solution	ADP2105	Buck
View Solution	ADP2105	Buck
View Solution	ADP2105	Buck
View Solution	ADP2106	Buck

ADIsimPower™ has found the best suited ICs for your application!

- Please pick your primary design goal - Lowest Cost, Smallest Size, Least Parts Count, and Most Efficient and click on the corresponding "View Solution" button.
- If a "View Solution" button is not selectable, a comprehensive design tool does not yet exist. The datasheet will probably have some information to help you out, so click on the part number to learn more.
- Below are other ICs that will work even though they may not be optimized for any of the four main design criteria. You can also filter out ICs that do not have features that are necessary for your application in the check boxes below. If you don't see the feature you need, click "View All Features," and the list will expand.

All Solutions

Criteria	IC	IC Description	Solution Cost [†] (USD)	Solution Size (mm ²)	Efficiency [*] (at load)	Component Count	Topology	Enable Shutdown	Power Good	Tracking	Light Load Efficiency	Synchronous
View Solution	ADP2106	Regulator	1.99	46	0.86	10	Buck	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>
View Solution	ADP2107	Regulator	2.06	46	0.86	10	Buck	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>
View Solution	ADP1821	Controller + Driver	2.78	188	0.82	29	Buck	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
View Solution	ADP1822	Controller + Driver	2.88	221	0.82	34	Buck	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
View Solution	ADP1828	Controller + Driver	2.86	213	0.82	22	Buck	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
View Solution	ADP2105	Regulator	1.87	46	0.82	10	Buck	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>
View Solution	ADP1864	Controller + Driver	2.15	119	0.73	11	Buck	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>
View Solution	ADP3050	Regulator	2.67	62	0.68	11	Buck	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>

Features
[Show all features \(17\)](#)

Step 2: View All Design Solutions—

In this step of the process you'll be able to pick from a list of possible solutions. Performance estimates are given for cost, size, efficiency, and component count for each solution. You can sort by each of these criteria as well as IC Description and Topology. The superlative of each of these design goals is at the top for quick access. A list of the IC features is available in the table at the bottom. You can view only ICs that have the features you want by clicking on the corresponding check box in the features list. If you don't see the feature you require, click on "Show all features" to see all 17 possibilities.

If you click on an IC, you'll get a pop up with various options including View Solution, View Product Page, View Data Sheet, Download Design Tool, Download Eval Board App Note. Once you have found the desired solution click on "View Solution" to go to the next step. If the View Solution button is grayed out, a comprehensive solution does not yet exist.

ADIsimPower Step 3: View Solution Details

Skip down to: [Bill of Materials](#) | [Efficiency Graph](#) | [Performance Data](#)

User Input Data & Solution Schematic [Build This Solution!](#) | [Back to Top](#)

Designed for: Lowest cost Part count Efficiency Size

Spec	Target Value	Actual Value	Units
Vout	1.200	1.209	Volt
Iout	0.300		Amp
Pout	0.360	0.363	Watt
TA	55		°C
Vinmin	4.5		Volt
Vinmax	5.5		Volt

Bill of Materials [Download Bill of Materials](#) | [Build This Solution!](#) | [Back to Top](#)

Designed for: Lowest cost Part count Efficiency Size

Note: Components with an "Item #" in orange can be changed. To select a different component, click on the Item # to edit. Updating components must be done in the order they appear in the BOM.

Item #	Des	Mfg	Part Number	Component Specs	Pkg	Part Qty	Area(mm ²)	Hgt(mm)	Cost(\$)*	
1	IC1	ADI	ADP1864AUJZ-R7	PFET Controller	TSOT-6	1	9	1	1.060	
2	L1	Coilcraft	ME3220-223	22µH,787mΩ,0.7Apk	Unshielded	1	8	2	0.230	
3	Rf1	Susumu	RL1220S-0R24-G	240mΩ	805	1	3.2	0.4	0.036	
4	D1	Vishay	BAT54V	0.2A,30V,max.0.89Vf	SOT23	1	7.5	1.1	0.036	
5	Q1	Siliconix	Si2301BDS	100mΩ,1.25Vth	SOT23-3	1	8.7	1.1	0.170	
6	Cin1	Taiyo Yuden	LMK212 BJ106KG-T	10µF,10V,7mΩ	805	1	2.5	1.3	0.031	
7	Cout1	Taiyo Yuden	JMK212 BJ106MG-T	10µF,6.3V,7mΩ	805	1	2.5	1.3	0.025	
8	Rf2	Vishay	1% tolerance	100kΩ	603	1	1.3	0.4	0.005	
9	Rf3	Vishay	1% tolerance	51.1kΩ	603	1	1.3	0.4	0.005	
10	Rc	Vishay	1% tolerance	43.2kΩ	603	1	1.3	0.4	0.005	
11	Cc1	Vishay	< 10% tolerance	1nF,X7R	603	1	1.3	1	0.010	
12	Cc0	Vishay	< 10% tolerance	15µF,X7R	603	1	1.3	1	0.010	
						Totals:	12	49	2.0	\$1.62

*Disclaimer:
1. BOM prices shown are 1000 piece estimates in US Dollars that should be used for comparison purposes only.
2. It is the user's responsibility to verify actual design performance through prototyping and test.

Step 3: View Solution Details—

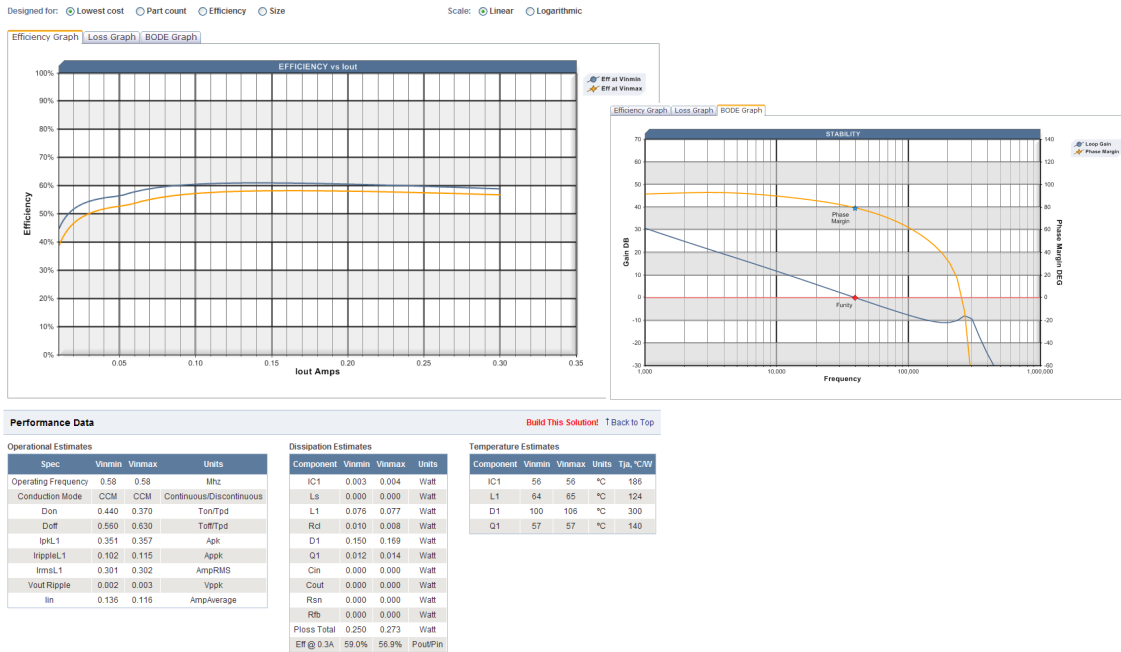
In the third step or the “View Solution Details” step, you’ll be able to view a schematic, bill of materials, efficiency graph, phase/gain plot, and performance data all customized for your specific input parameters.

You’ll be able to modify advance settings, which will include many things including but not limited to: output voltage ripple spec, load transient specs, maximum component height, input filter, and switching frequency options.

At the top of each section you’ll be able to change the design goal for your converter. Radial buttons will allow you to optimize for cost, parts count, efficiency, and size. You can watch your bill of materials and efficiency curve change as you select different design goals.

The bill of materials is fully customizable and can be exported to Excel. If the line item is red, you can click on it to see a list of other components that are prequalified to work in your design. As you view the list of parts, you’ll be given many parameters that will help you make your decision including but not limited to: cost, loss, area, height, part number, manufacturer, etc.

ADIsimPower Step 3: View Solution Details (Continued)

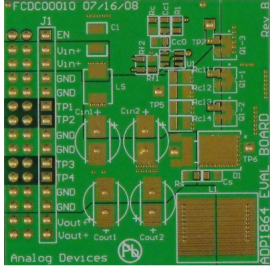


Scrolling down, you'll find an efficiency curve, which predicts the efficiency at the maximum and minimum output voltage. You can switch between log and linear scales depending on the area of interest on the curve. Another tab is the loss graph over load, which is the data from which the efficiency numbers are derived. The third tab in the graph list is the phase/gain analysis that shows the small signal stability of the converter as it is in your customized design.

Below the graphs is the performance data, which will offer predictions about how the converter will operate, power dissipation estimates for each component, and temperature estimates of each of the components.

Once you have finalized your design click on "Build This Solution."

ADIsimPower Step 4: Build Your Design



You've arrived at the final stage of ADIsimPower. Below is all the documentation that you need to build your customized design.

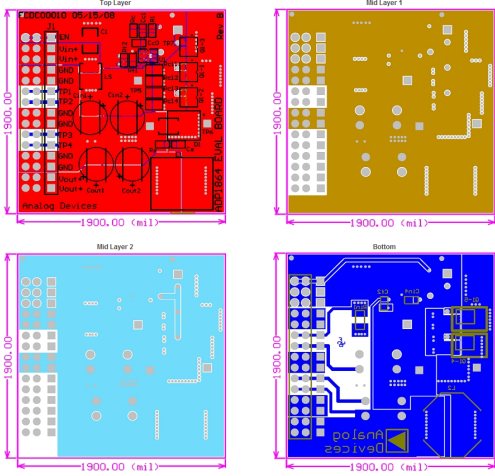
Just click on 'Buy It' to add the ADP1864EVALZ-R7 and the ADP1864-EVALZ to your shopping cart.

The evaluation board often has multiple configuration options that may not be applicable to your particular design, so the Bill of Materials may have more line items than the BOM of the previous page.

If you choose to build your own hardware instead of using the ADP1864-EVALZ below are pictures of each of the PCB layers to guide your layout.

Purchase Information: ADP1864

Model	Sample	Purchase
ADP1864EVALZ-R7	Add to Cart	Add to Cart
ADP1864-BL-EVALZ	Add to Cart	Add to Cart



Schematic

Step 4: Build Your Design—

This is the final step in ADIsimPower.

Here you will be given links to purchase evaluation boards that correspond exactly with the BOM and schematic you received that were customized for your design. You'll see a picture of the evaluation board, a schematic that is complete with component values placed on it (ideal for use in assembling the board), a bill of materials, and layout guidelines.

The schematic and evaluation board accommodate many different configurations, so the BOM and schematic may have quite a few components that you will not be required to populate for your application.

The layout recommendations usually come in the form of the artwork required for each of the PCB layers of the evaluation board.

Technical Reference Material

Analog Devices' Textbook References

1. Hank Zumbahlen, *Basic Linear Design*, Analog Devices, 2006, ISBN: 0-915550-28-1. Also available as *Linear Circuit Design Handbook*, Elsevier-Newnes, 2008, ISBN-10: 0750687037, ISBN-13: 978-0750687034. See Chapter 9.
2. Walt Kester, *Analog-Digital Conversion*, Analog Devices, 2004, ISBN: 0916550273. Also available as *Data Conversion Handbook*, Elsevier-Newnes, 2005, ISBN: 0750678410. See Chapter 7.
3. Walt Jung, *Op Amp Applications*, Analog Devices, 2002, ISBN: 0-916550-26-5. Also available as *Op Amp Applications Handbook*, Elsevier-Newnes, 2004, ISBN: 0-7506-7844-5. See Chapter 7.

Other Textbook References

1. Irving M. Gottlieb, *Power Supplies, Switching Regulators, Inverters, and Converters, Second Edition*, McGraw Hill (TAB Books), 1994.
2. Marty Brown, *Practical Switching Power Supply Design*, Academic Press, 1990.
3. Marty Brown, *Power Supply Cookbook*, Butterworth-Heinemann, 1994.
4. John D. Lenk, *Simplified Design of Switching Power Supplies*, Butterworth-Heinemann, 1995.
5. Keith Billings, *Switchmode Power Supply Handbook*, McGraw-Hill, 1989.
6. George Chryssis, *High-Frequency Switching Power Supplies: Theory and Design, Second Edition*, McGraw-Hill, 1989.
7. Abraham I. Pressman, *Switching Power Supply Design*, McGraw-Hill, 1991.

Notes: