Practical Power Solutions

1. Point-of-Load Power
2. System Power Management and Portable Power
3. Power for Mixed Analog/Digital Systems
4. Hardware Design Techniques

SECTION 2

SYSTEM POWER MANAGEMENT AND PORTABLE POWER

Designing a Typical System Power Chain

A Typical System Using AC Power
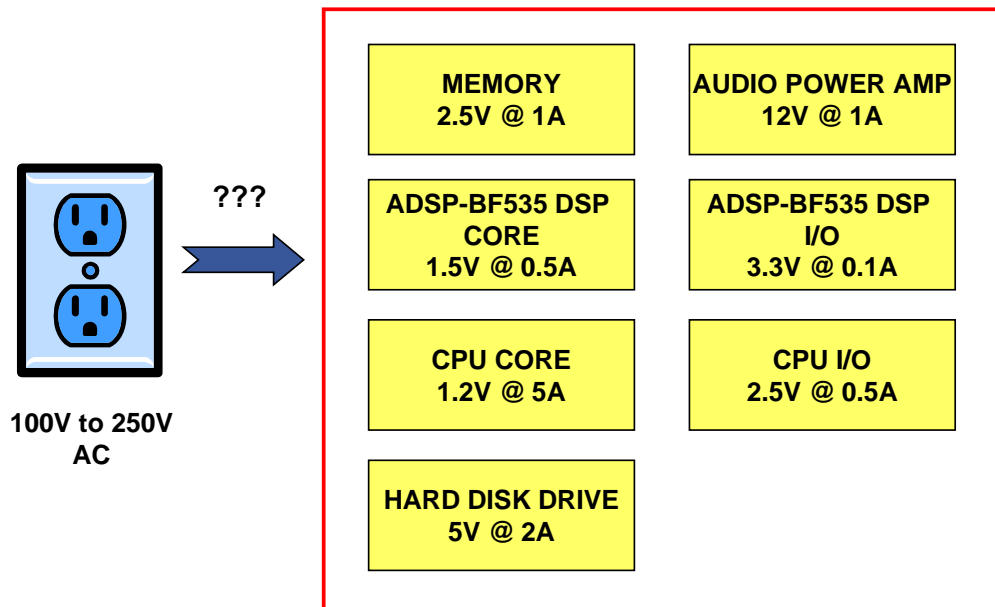
PEAK VALUES ASSUMED FOR CURRENTS AT NOMINAL VOLTAGES

In this portion of the seminar, we will examine a typical system and lay out an appropriate power chain.

This system consists of a CPU, DSP (Blackfin ADSP-BF535), an audio power amplifier, and a hard disk drive. Notice that the core and I/O voltages for the CPU and DSP are different—a typical situation often encountered in modern designs.

The various voltages and current requirements are shown in the diagram. The power must come from a standard ac wall outlet (rated at 15 A or 20 A).

It is assumed that the currents above represent maximum currents at the nominal voltages.

End Power Requirements for System

Function	Voltage (V)	Current (A)	Power (W)
Audio Power Amp	12.00	1.00	12.00
CPU Core	1.20	5.00	6.00
CPU I/O	2.50	0.50	1.25
Memory	2.50	1.00	2.50
Hard Disk Drive	5.00	2.00	10.00
ADSP-BF535 DSP Core	1.50	0.50	0.75
ADSP-BF535 DSP I/O	3.30	0.10	0.33
Total Power			32.83

PEAK VALUES ASSUMED FOR CURRENTS AT NOMINAL VOLTAGES

This figure breaks out the various voltages and currents required to power the system. The total power consumed is 32.83 W.

General Guidelines for Power Trains

◆ **Start with higher voltages and regulate down (buck), not up (boost)**
◆ **Do not make more voltages than you actually need**
  ● **Exception: For a low noise power rail, you may need to pre-regulate the input of an LDO with a buck (or maybe a boost) converter to keep power dissipation in the LDO low**
◆ **Do not run the power through more conversions than you need:**

OVERALL EFFICIENCY = 0.91 × 0.94 × 100% = 85.5%

| 12V → | **91% EFFICIENT DC-to-DC CONVERTER** | 5V → | **94% EFFICIENT DC-to-DC CONVERTER** | 1.2V @ 5A → |

OVERALL EFFICIENCY = 86%

| 12V → | **86% EFFICIENT DC-to-DC CONVERTER** | 1.2V @ 5A → |
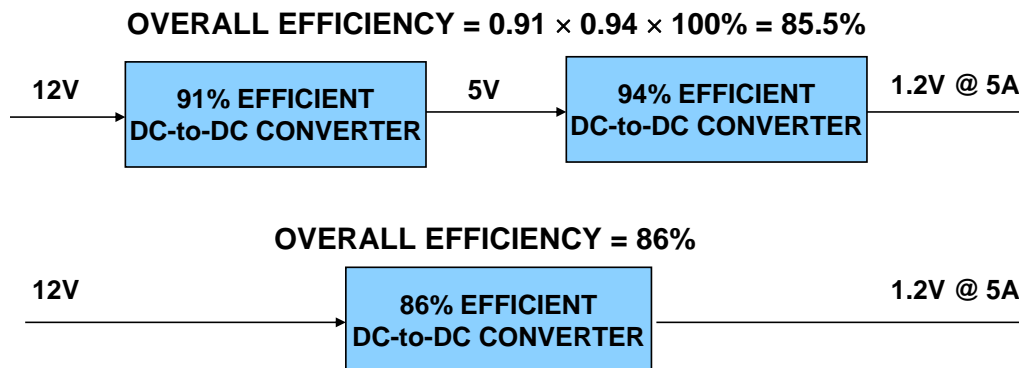
Before starting the design, it is useful to examine several useful guidelines relating to fixed (non-portable) power system design.

As previously discussed, it is wise to distribute higher voltages and then regulate down from them at the points-of-load using buck regulators or LDOs. It is generally unwise to use boost converters in fixed power applications. These are much more suitable for battery-operated portable systems. However, if the current is low enough, a boost converter can be useful in certain applications.

You should also try and design the system with as few voltages as possible; i.e. do not generate intermediate bus voltages that are not used in the system. There is one important exception to this rule where it is desirable to use an LDO to generate a low noise supply voltage, perhaps to power a mixed-signal device such as an ADC, PLL, or other noise-sensitive analog circuit. In this case it may be wise to use a buck converter (in some cases a boost converter) as a pre-regulator for the LDO. The output of the buck or boost converter is made slightly higher than the LDO output voltage plus the LDO dropout voltage. This minimizes power dissipation in the LDO.

Finally, try and minimize the number of power conversions in any given power path. Remember that the overall efficiency of two converters in series is equal to the product of the individual efficiencies. A 91% efficient converter in series with a 94% efficient converter yields a total efficiency of 85.5%.

The example above shows that the 12 V to 1.2 V buck converter is only 86% efficient, primarily because of the high V_{IN}/V_{OUT} ratio. Even though the individual 12 V to 5 V and 5 V to 1.2 V converters are more efficient (91% and 94%, respectively), their combined efficiency of 85.5% is no better than using the single converter.

Choice of AC Power Adapter
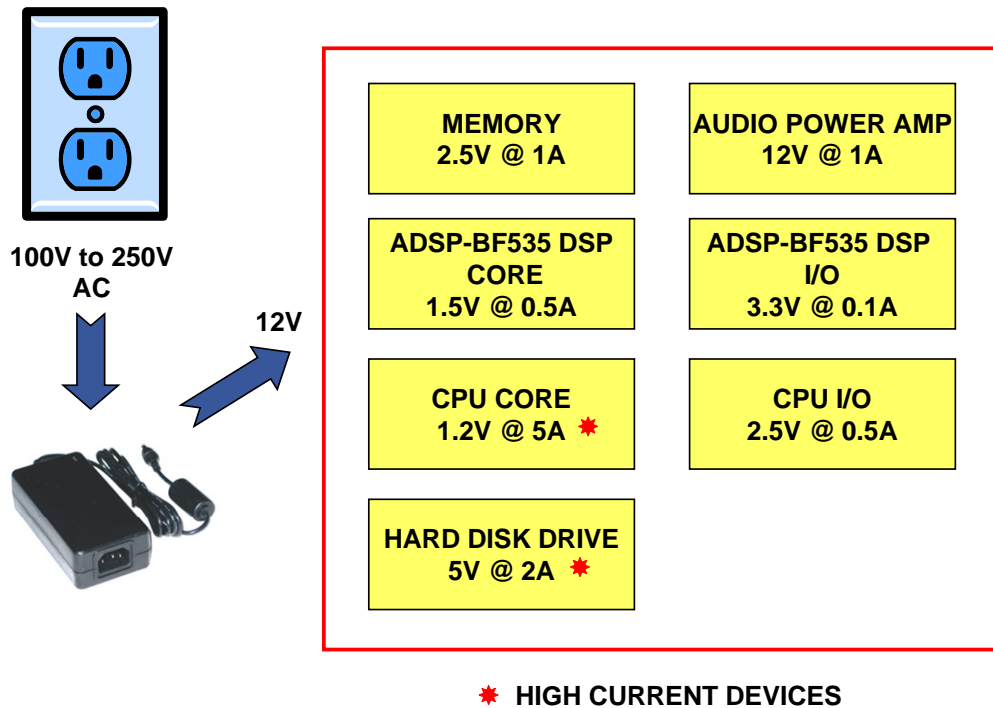

5V, 9V, 12V, 18V, 24V ????

◆ **This is the largest voltage that we need in the system**
◆ **We don't have to use a separate regulator for the 12V audio amp**
◆ **We can regulate down from here to get the other voltages**

The first step in the power design is to select the ac adapter output voltage. These adapters are available with a number of different dc voltage outputs.

We will select a 12 V adapter because 12 V can be used directly by the power amplifier. This way the power amplifier does not need its own regulator. Here we are assuming that after proper filtering, the 12 V supply is "quiet" enough to power the audio amplifier.

The 12 V output can be regulated down to get the other voltages required in the system.
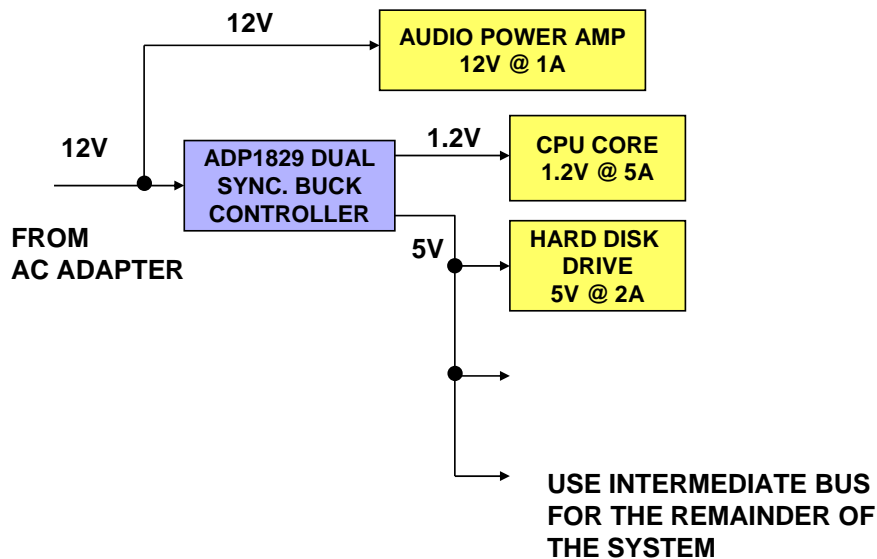
After Choosing a 12V Power Bus, What is the Next Step?

100V to 250V AC

12V

MEMORY 2.5V @ 1A	AUDIO POWER AMP 12V @ 1A
ADSP-BF535 DSP CORE 1.5V @ 0.5A	ADSP-BF535 DSP I/O 3.3V @ 0.1A
CPU CORE 1.2V @ 5A ✸	CPU I/O 2.5V @ 0.5A
HARD DISK DRIVE 5V @ 2A ✸	

✸ **HIGH CURRENT DEVICES**

Now that 12 V has been chosen as the primary dc bus, what is the next step in the design?

A good place to start is to examine the requirements for the voltages which require the largest current: the 1.2 V CPU core voltage (5 A) and the 5 V hard disk drive (2 A).

Powering the High Current Devices from a Dual Synchronous Buck Controller

```
        12V                    ┌──────────────────┐
    ┌──────────────────────────▶│ AUDIO POWER AMP  │
    │                          │    12V @ 1A      │
    │                          └──────────────────┘
    │
  12V    ┌────────────────┐   1.2V  ┌──────────────┐
  ───────▶│ ADP1829 DUAL   │────────▶│  CPU CORE    │
    │    │ SYNC. BUCK     │         │  1.2V @ 5A   │
    │    │ CONTROLLER     │         └──────────────┘
    │    └────────────────┘   5V    ┌──────────────┐
  FROM                        ──────▶│ HARD DISK    │
  AC ADAPTER                        │   DRIVE      │
                                    │  5V @ 2A     │
                                    └──────────────┘

                              USE INTERMEDIATE BUS
                              FOR THE REMAINDER OF
                              THE SYSTEM
```

Since there are two relatively high current rails, a dual synchronous buck controller such as the ADP1829 can be used to generate both the 5 V and 1.2 V rails from the 12 V input. The 5 V rail can then be used as an intermediate bus to generate the lower voltages required in the system.

Although it would be possible to generate the 1.2 V CPU core voltage from the intermediate 5 V bus, this puts two high current regulators in series, and the overall efficiency will be no better than generating the 1.2 V directly from the 12 V rail.

Finishing the Design using the 5V Intermediate Bus and More POL Regulators
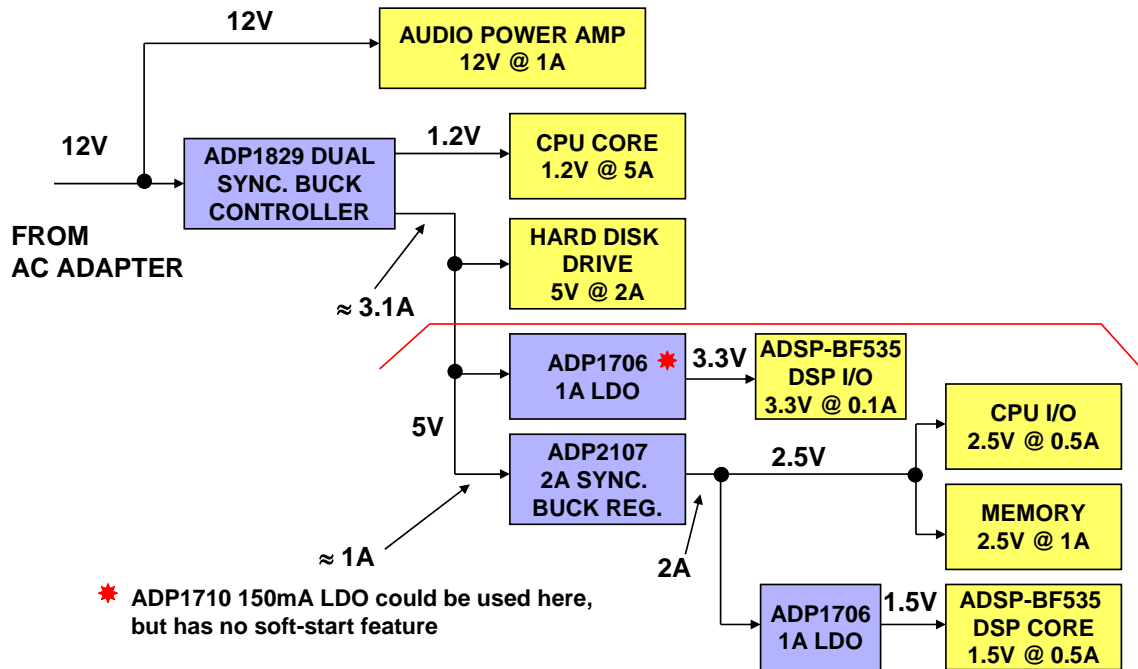
Continuing with the design, we will use an LDO to generate the 3.3 V required for the DSP I/O because the current requirement is only 0.1 A. The ADP1710 150 mA low cost LDO comes in a 5-lead TSOT package and has a worst case θ_{JA} = 170°C/W (assuming no surrounding copper area). In the circuit the part dissipates 0.17 W, giving a 29°C rise from ambient-to-junction. Although this is more than adequate for operation at 85°C ambient, the ADP1710 does not have a soft-start feature which might be needed for sequencing.
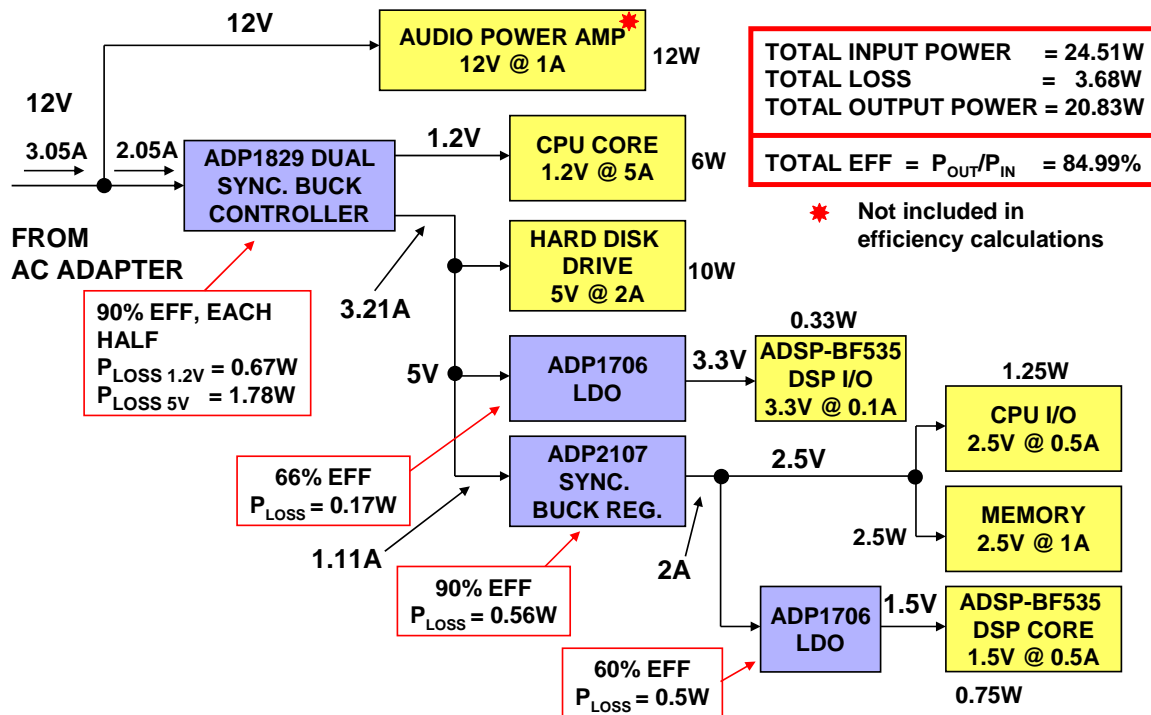
The ADP1706 handles 1 A and has a worst case θ_{JA} of 58°C/W in the 8-lead, exposed paddle SOIC; and a worst case θ_{JA} of 66°C/W in the 8-lead exposed paddle LFCSP. This part is rated for 1 A and has a soft-start feature.

We will use the ADP2107 2 A synchronous buck regulator to generate the 2.5 V for the CPU I/O and the memory.

The ADP1706 LDO is used to generate the 1.5 V core voltage for the DSP. In the circuit, the ADP1706 dissipates 0.5 W, so this yields an ambient to junction rise of 33°C using θ_{JA} = 66°C/W.

In order to maintain parts commonality and to allow for soft-start capability, we will use the ADP1706 LDO in both applications.

Overall System Efficiency Calculations

12V

AUDIO POWER AMP ✳
12V @ 1A   **12W**

12V

3.05A | **2.05A**

ADP1829 DUAL SYNC. BUCK CONTROLLER

1.2V

CPU CORE 1.2V @ 5A   **6W**

FROM AC ADAPTER

90% EFF, EACH HALF
$P_{LOSS\ 1.2V} = 0.67W$
$P_{LOSS\ 5V} = 1.78W$

3.21A

HARD DISK DRIVE 5V @ 2A   **10W**

5V

ADP1706 LDO

3.3V

0.33W
ADSP-BF535 DSP I/O 3.3V @ 0.1A

66% EFF
$P_{LOSS} = 0.17W$

ADP2107 SYNC. BUCK REG.

2.5V

1.25W
CPU I/O 2.5V @ 0.5A

1.11A

90% EFF
$P_{LOSS} = 0.56W$

2A

2.5V

2.5W
MEMORY 2.5V @ 1A

ADP1706 LDO   **1.5V**

ADSP-BF535 DSP CORE 1.5V @ 0.5A

60% EFF
$P_{LOSS} = 0.5W$

0.75W

TOTAL INPUT POWER = 24.51W
TOTAL LOSS = 3.68W
TOTAL OUTPUT POWER = 20.83W

TOTAL EFF = P_{OUT}/P_{IN} = 84.99%

✳ **Not included in efficiency calculations**

Here we have calculated the individual power losses for both the switching converters and the LDOs. An efficiency of 90% was assumed for the switching converters. The power dissipated in the LDOs was calculated by multiplying the LDO $V_{IN} - V_{OUT}$ by the output current.

The first step is to calculate the input currents for the switching converters based on their efficiency.

The total efficiency of the system is calculated by taking the ratio of the output power (power dissipated in the actual system blocks in yellow) to the input power (total system power dissipation including regulator losses). The efficiency works out to be a respectable 84.99%.

The 12 watts dissipated by the audio power amplifier is not counted in the efficiency calculations because it is powered directly from the ac adapter output. The total efficiency calculation does not include the efficiency of the ac adapter.

Efficiency Comparison: ADP2107 Synchronous Regulator vs. ADP1864 Asynchronous Controller

◆ **ADP2105/ADP2106/ADP2107: Synchronous Buck Regulator, Internal Switches**

- **Optimized for output currents of 1A (ADP2105), 1.5A (ADP2106), and 2A (ADP2107).**
- **V_{IN} = 2.7V to 5.5V, V_{OUT} = 0.8V to V_{IN}**
- **Synchronous gives good efficiency for higher currents, low voltages**
- **1.2MHz Switching Frequency**
- **For output currents less than 0.6A, ADP2102 or ADP2108 regulators offer compact solutions at 3MHz switching frequencies**

◆ **ADP1864: Asynchronous Buck Controller, External PMOS FET and Schottky diode**

- **V_{IN} = 3.15V to 14V, V_{OUT} = 0.8V to V_{IN}**
- **Generally used for outputs up to 5A**
- **Diode limits efficiency for high currents, low output voltages**
- **580kHz Switching Frequency**

For output currents less than a few amps, a synchronous buck regulator is a good choice, such as the ADP2105 (1 A), ADP2106 (1.5 A), and ADP2107 (2 A). The switches are integrated, and the parts therefore require only a few external components for a complete design. The synchronous switch gives good efficiency, especially for higher currents and low output voltages.
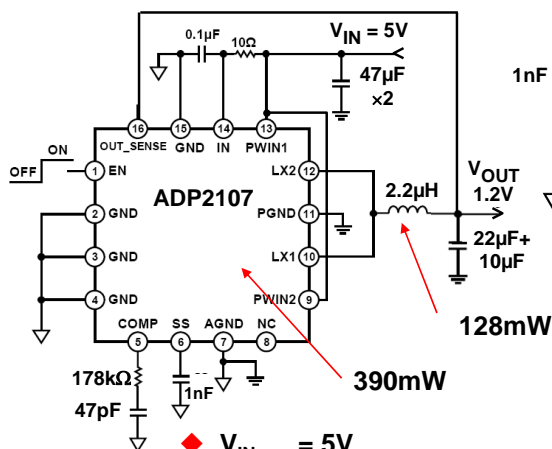
For currents of 600 mA or less, the ADP2102 and ADP2108 offer compact solutions because of their 3 MHz switching frequencies.

On the other hand, an asynchronous buck regulator using external components, such as the ADP1864, can be configured to supply more output current with a higher parts count and larger size. The ADP1864 is useful for output currents up to about 5 A.

In this exercise, we will let ADIsimPower create two designs. The first design uses the ADP2107 synchronous regulator, and the second design uses the ADP1864 asynchronous buck controller. The ADIsimPower designs allow comparisons between the efficiency, cost, and board space for the two approaches.
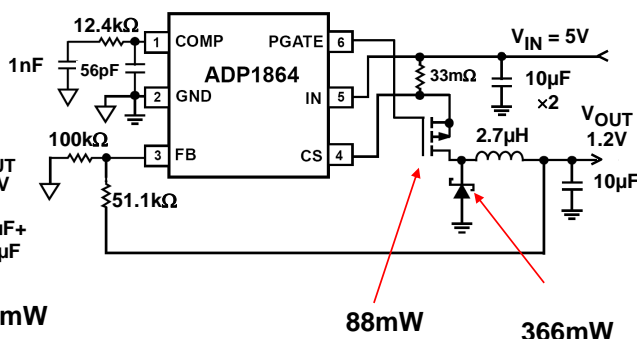
Design Solutions Using ADIsimPower

ADP2107 DESIGN

0.1µF 10Ω
V_{IN} = 5V
47µF ×2

ON
OFF — EN

OUT_SENSE GND IN PWIN1
16 15 14 13

1 EN
LX2 12
V_{OUT} 1.2V
2.2µH

ADP2107

2 GND
PGND 11

3 GND
LX1 10

4 GND
PWIN2 9

COMP SS AGND NC
5 6 7 8

178kΩ
1nF
47pF

22µF+ 10µF

128mW
390mW

- V_{IN} = 5V
- V_{OUT} = 1.2V @ 2A
- P_{OUT} = 2.4W
- P_{LOSS} = 530mW
- EFF = 82%

- COST ≈ $2.63
- AREA ≈ 74mm^2

ADP1864 DESIGN

12.4kΩ
1nF 56pF

COMP 1   PGATE 6
ADP1864
GND 2   IN 5
FB 3   CS 4

100kΩ
51.1kΩ

V_{IN} = 5V
33mΩ 10µF ×2
V_{OUT} 1.2V
2.7µH
10µF

88mW **366mW**

- V_{IN} = 5V
- V_{OUT} = 1.2V @ 2A
- P_{OUT} = 2.4W
- P_{LOSS} = 516mW
- EFF = 82%

- COST ≈ $3.02
- AREA ≈ 333mm^2

The design parameters entered into the ADIsimPower online design tool are:

1. V_{OUT} = 1.2 V

2. I_{OUT} = 2 A

3. V_{INMIN} = 5 V

4. V_{INMAX} = 5 V

5. T_{MAX} Ambient = 50°C

6. Optimize design for Efficiency (other choices are Lowest cost, Lowest Part count, and Smallest Size). Note that the design tool optimizes efficiency at the maximum specified current.

The figures above show the two designs obtained from ADIsimPower, which also gives a complete bill-of-material, thermal analysis, and parts cost.

To calculate efficiency, we must know the power losses. From ADIsimPower, the AD2107 design dissipates the largest amount in the IC itself due to the internal switching losses.

In the ADP1864 design, the two largest power loss contributors are the PFET switch (three Siliconix SI235DS FETs in parallel) and the free-wheeling Schottky diode (IR/Vishay 30BQ015).

Overall efficiency of the two designs at 2 A ouptut current is approximately the same, but the ADP1864 solution costs more and takes up about 5 times the area of the ADP2107 solution. Efficiency of the ADP2107 design is much better than the ADP1864 design at lower currents.

Efficiency of ADP1864 Asynchronous Buck Controller vs. ADP2107 PFM Synchronous Buck Regulator

V_{IN} = 5V, V_{OUT} = 1.2V

$V_{IN} = 5V, V_{OUT} = 1.2V$
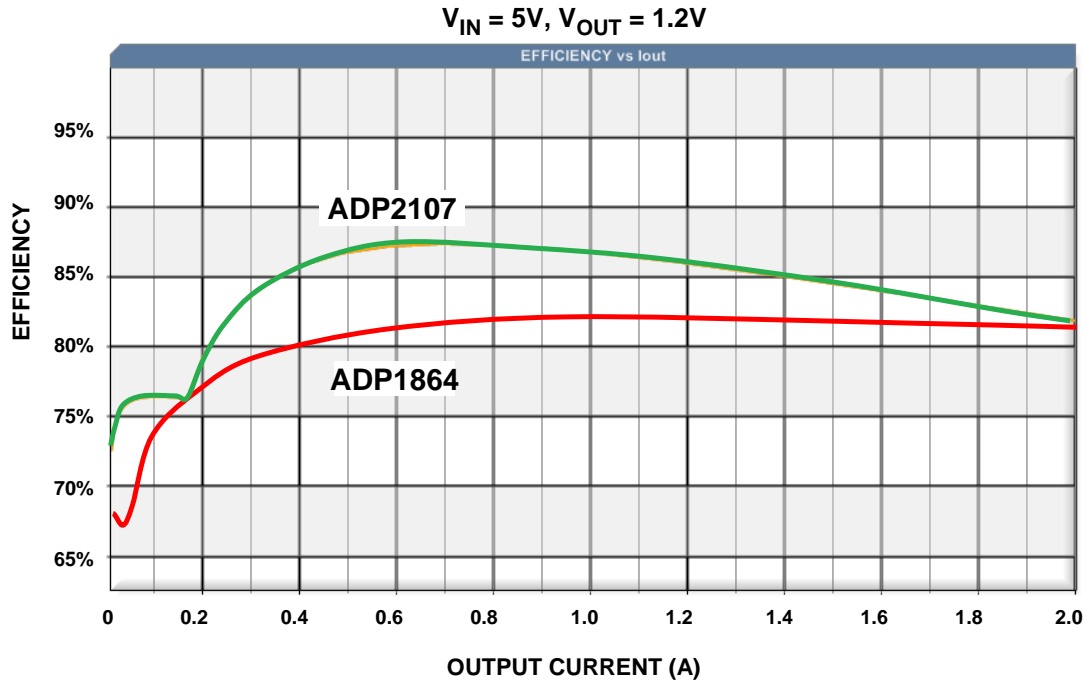
This shows the efficiency of the two designs from output currents of 10 mA up to 2 A.

The ADP2107 smoothly transitions from the PWM (pulse width modulation) mode to the variable frequency PFM (pulse frequency mode) mode of operation when the load current decreases below the pulse-skipping threshold current, switching only as necessary to maintain the output voltage within regulation. When the output voltage first dips below regulation, the ADP2107 enters the PFM mode for a few oscillator cycles to increase the output voltage back to regulation. During the wait time between bursts, both power switches are off, and the output capacitor supplies all the load current. Because the output voltage dips and recovers occasionally, the output voltage ripple in this mode is larger than the ripple in the PWM mode of operation.

The output current at which the ADP2107 transitions from variable frequency PFM control to fixed frequency PWM control is called the pulse-skipping threshold. The pulse-skipping threshold has been optimized for excellent efficiency over all load currents.

The efficiency of the ADP1864 design is not as good at low currents, and the cost, parts count, and area is greater.

The obvious conclusion is that it is better to use a fully integrated PFM synchronous regulator where possible for currents of a few amps or less.

Microprocessor
Supervisory Functions

www.analog.com/supervisory

Simple Reset and Power-On Reset Generator

t1 = RESET TIME = 240ms TYP
V_{REF} = RESET VOLTAGE THRESHOLD
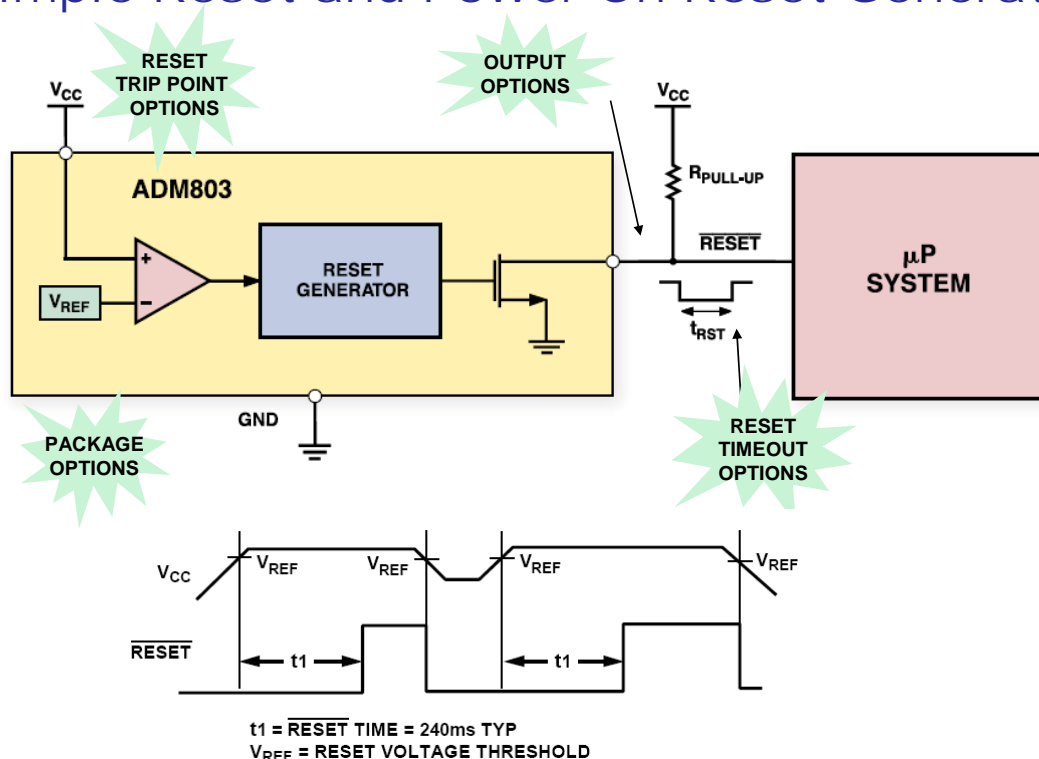
The initial state of a microprocessor after power-up must be predictable and repeatable. After power-up, a momentary out-of-limit voltage on the power supply can cause processing errors. For these reasons, some type of microprocessor supervisory circuit is generally used as a reset generator or power-on reset generator.

The simplest form of the power-on reset generator is shown in this figure. TheADM803 supervisory circuit monitors the power supply voltage in microprocessor systems. It provides a reset output during power-up, power-down, and brownout conditions. On power-up, an internal timer holds the RESET asserted for 240 ms. This holds the microprocessor in a reset state until conditions have stabilized. The RESET output remains operational with V_{CC} as low as 1 V. The ADM803 and ADM809 provide an active low reset signal, while the ADM810 provides an active high reset signal output. The ADM809 and ADM810 have push-pull outputs, whereas the ADM803 has an open-drain output which requires an external pull-up resistor.

Seven reset threshold voltage options are available, suitable for monitoring a variety of supply voltages.

The reset comparator features built-in glitch immunity, making it immune to fast transients on V_{CC}.

The ADM803/ADM809/ADM810 consume only 17 μA, making them suitable for low power, portable equipment. The ADM803 is available in a 3-lead SC70; the ADM809/ADM810 are available in 3-lead SOT-23 and SC70 packages.

ADM6710 Low Voltage Quad Supervisory Circuit
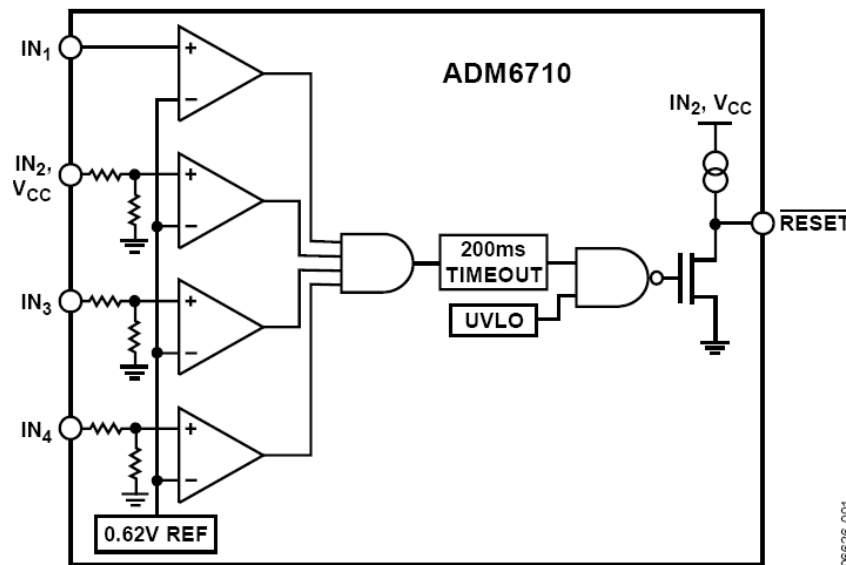
Many modern microprocessors require a separate core and I/O voltage. There may be other critical voltages in the system which need monitoring for out-of-limit conditions.

The ADM6710 is a low voltage, high accuracy supervisory circuit which monitors up to four system supply voltages.
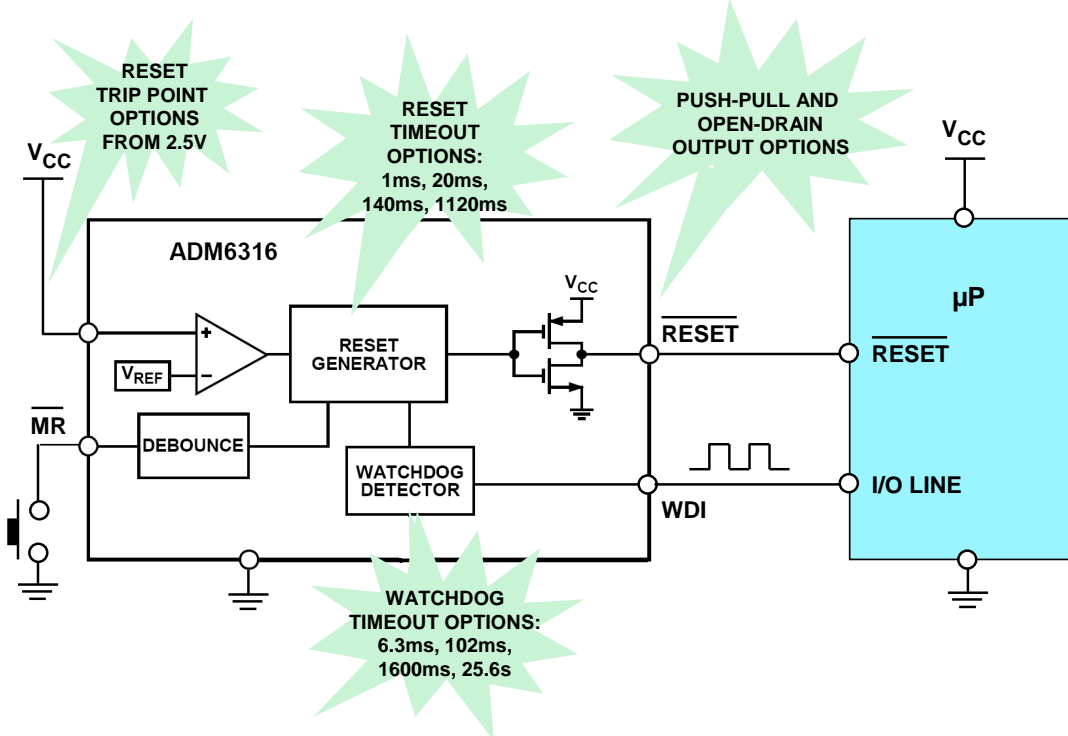
The ADM6710 incorporates a variety of internally pre-trimmed undervoltage threshold options for monitoring 1.8 V, 2.5 V, 3.0 V, 3.3 V, and 5.0 V supply voltages. The ADM6710Q offers three adjustable thresholds for monitoring voltages down to 0.62 V.

If a monitored power supply voltage falls below the minimum voltage threshold, a single active low output asserts, triggering a system reset. The output is open drain with a weak internal pull-up to the monitored IN2 supply (or to V_{CC} in the case of the ADM6710Q) of typically 10 µA. Once all voltages rise above the selected threshold level, the reset signal remains low for the reset timeout period (200 ms typical).

The ADM6710 output remains valid as long as IN1 or IN2 exceeds 1 V, whereas for the ADM6710Q, the output remains valid as long as VCC exceeds 2 V.

Unused monitored inputs should not be allowed to float or to be grounded, instead they should be connected to a supply voltage greater than their specified threshold voltages. The ADM6710 is available in a 6-lead SOT-23 package.

2.15

# Adding an External Reset and a Watchdog Timer to the Reset Generator

RESET TRIP POINT OPTIONS FROM 2.5V

RESET TIMEOUT OPTIONS: 1ms, 20ms, 140ms, 1120ms

PUSH-PULL AND OPEN-DRAIN OUTPUT OPTIONS

V_{CC}

V_{CC}

ADM6316

V_{CC}

+
−

V_{REF}

RESET GENERATOR

$\overline{\text{RESET}}$

μP

$\overline{\text{RESET}}$

$\overline{\text{MR}}$

DEBOUNCE

WATCHDOG DETECTOR

WDI

I/O LINE

WATCHDOG TIMEOUT OPTIONS: 6.3ms, 102ms, 1600ms, 25.6s

A wide range of reset generator circuits are available designed for use in microprocessor-based systems to monitor power supply voltage levels from 5 V down to 1.58 V. Their reset output signals are asserted whenever the supply voltage falls below a preset threshold level. Reset remains active for a fixed timeout period after the supply voltage has returned to a valid level, so that the supply has time to stabilize before the microprocessor starts up again.

The various models provide a choice of active low or active high and push-pull or open-drain output stages.

Microprocessors need to be reset when code execution errors occur, as well as when supply voltages fall to invalid levels. A watchdog function can detect code execution errors by monitoring frequent logic transitions on a microprocessor's output pin. If a transition is not detected within a certain time period, the watchdog circuit will initiate a reset signal that will take the microprocessor out of its invalid state. Many reset generator/watchdog circuits also feature a power fail detection comparator that asserts an active low signal when the unregulated power supply voltage falls below a predetermined level. This power fail output can be used to generate an interrupt, which allows the microprocessor to implement a shutdown procedure before power is lost.

Reset Generator and Battery Backup Circuit
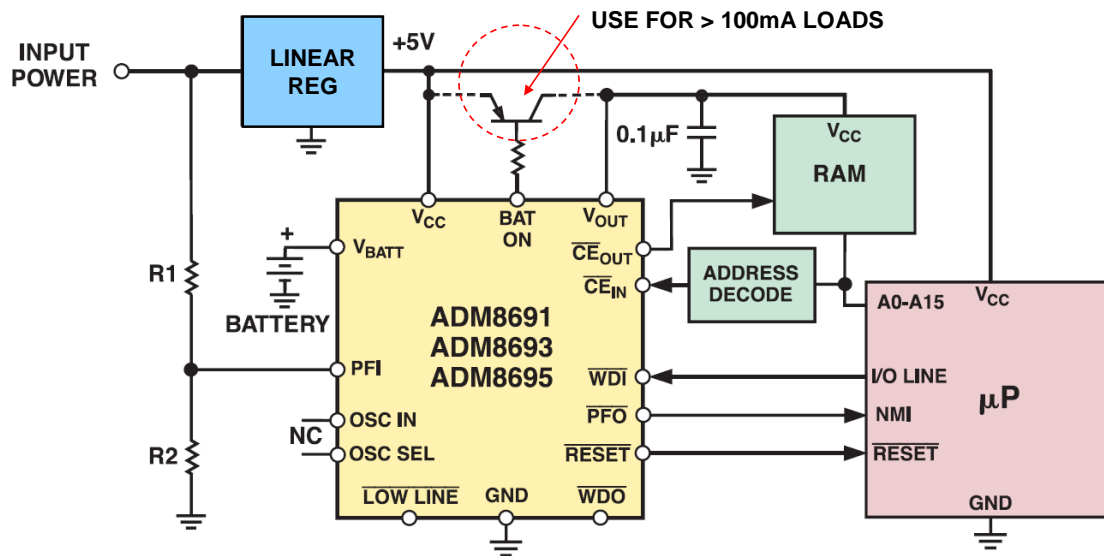
A battery backup circuit can be easily controlled with a supervisory circuit by adding an internal PMOS-based switch. In the above circuit, the battery switchover circuit compares V_{CC} to the V_{BATT} input, and connects V_{OUT} to whichever is higher. Switchover occurs when V_{CC} is 50 mV higher than V_{BATT} as V_{CC} falls, and when V_{CC} is 70 mV greater than V_{BATT} as V_{CC} rises. This 20 mV of hysteresis prevents repeated rapid switching if V_{CC} falls very slowly or remains nearly equal to the battery voltage.

During normal operation, with V_{CC} higher than V_{BATT}, V_{CC} is internally switched to V_{OUT} through an internal PMOS switch. This switch has a typical on resistance of 0.7 Ω and can supply up to 100 mA at the V_{OUT} terminal. V_{OUT} is normally used to drive a RAM memory bank. If instantaneous currents of greater than 100 mA are required, a 0.1 µF bypass capacitor should be connected to V_{OUT}. The capacitor provides the peak current transients to the RAM.

If the continuous output current requirement at V_{OUT} exceeds 100 mA, or if a lower $V_{CC} - V_{OUT}$ voltage differential is desired, an external PNP pass transistor can be connected in parallel with the internal transistor as shown above with the dotted connection. The BATT ON output (ADM8691/ADM8693/ADM8695) can directly drive the base of the external transistor.

These devices also provide the traditional power-on reset and watchdog timer functions in addition to the battery backup function.

On-Line Supervisory Parametric Search

Parametric Search - Supervisory

Found 5 Applicable Models. Jump to Results.

Settings for Single Supervisors

Search in: ⦿ Available Models ◯ All Models (includes unreleased)

Reset Trip Point (TP) typical (V)	Minimum Reset Timeout (RTO) minimum (ms)	Watchdog	Manual Reset	Reset Output Active-Low	Reset Output Active-High
3	100	Watchdog Input	Yes	Open Drain	Don't Care

Package Type		Watchdog Timeout (WTO) typical (ms)	Power Fail Comparator	Range of Operating Temperature (°C)
Don't Care	3 Lead Count / MSOP Package	150	Yes	Minimum <= -40 / Maximum >= 85

Search for Single Supervisors   **Reset Settings**   Contact ADI Experts about Supervisors

See All Results for: Dual (2) Supervisors | Triple (3) Supervisors | Quad (4) Supervisors | Battery Backup

Because of the wide variety of options available in supervisory products, some type of selection tool is mandatory in order to select the proper part for a specific application.

The online Supervisory Parametric Search performs parametric searches on all Analog Devices supervisory products, both those currently available, and those that can be ordered. Searches can be performed on trip points, reset timeouts, watchdog timeouts, reset types, and other features. This figure shows the opening screen of the search function where the data is entered.

In addition, a general ADI website tool provides cross-referencing between Analog Devices and competitive parts.

Results from Supervisory Parametric Search

**Found 5 Applicable Models** [Export to Excel]

Model	TP1 Typical (V)	TP1 % Accuracy	TP2 Typical (V)	TP2 % Accuracy	RTO min (ms)	Manual Reset	WTO min (ms)	Reset Polarity	Output Structure	Lead Count	Package	Temp min (°C)	Temp max (°C)	ICC max (µA)	Vcc min (V)	Vcc max (V)	Monitored Voltages	PFC	Price $ (1000 pcs.)	Availability
ADM13305-18ARZ	2.93	2.4	1.68	2.4	140	Yes	1600	Active Low & Active High	Push Pull	8	NSOIC	-40	85	40	2.7	5.5	2	-	0.96	Available
ADM13305-25ARZ	2.93	2.4	2.25	2.2	140	Yes	1600	Active Low & Active High	Push Pull	8	NSOIC	-40	85	40	2.7	5.5	2	-	0.96	Available
ADM13305-33ARZ	4.55	2	2.93	2.4	140	Yes	1600	Active Low & Active High	Push Pull	8	NSOIC	-40	85	40	2.7	5.5	2	-	0.96	Available
ADM13305-4ARZ	2.93	1	0.6	0.8	140	Yes	1600	Active Low & Active High	Push Pull	8	NSOIC	-40	85	40	2.7	5.5	2	-	0.96	Available
ADM13305-5ARZ	2.25	0.9	0.6	0.8	140	Yes	1600	Active Low & Active High	Push Pull	8	NSOIC	-40	85	40	2.7	5.5	2	-	0.96	Available

After entering the inputs, the parametric search narrows the list of products based on the inputs. In this manner, the proper part can be easily chosen for a specific application.

Power Supply Monitoring and Sequencing

www.analog.com/sequencing

Comparators as Voltage Monitors

DISCRETE SOLUTION

INTEGRATED SOLUTION WITH RESET
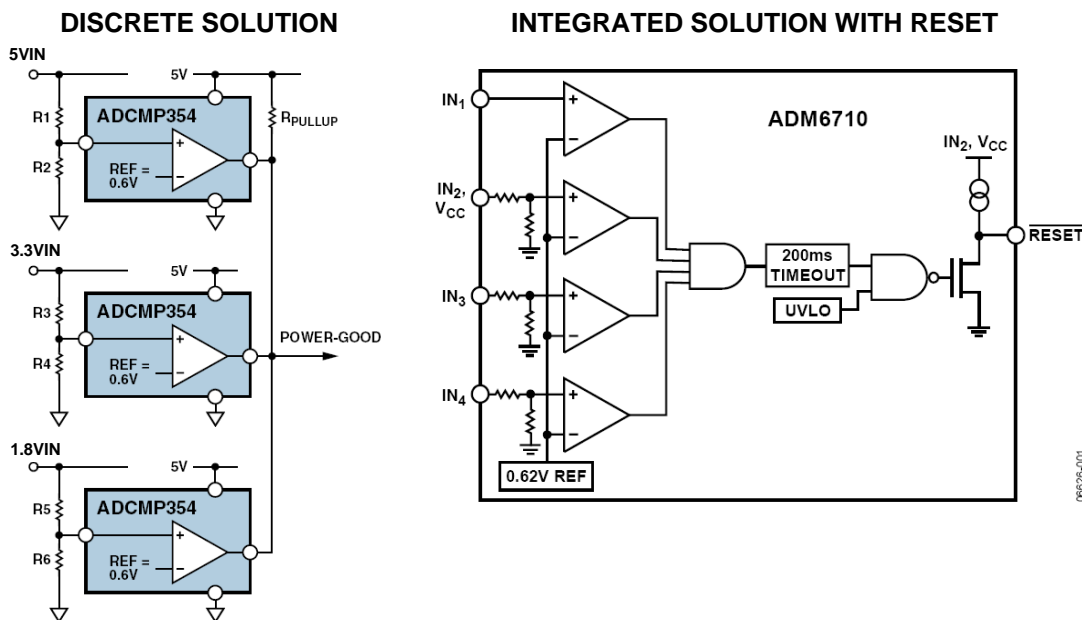
This shows a simple method for monitoring multiple voltage rails using the ADCMP354 comparator and reference IC. An individual circuit is used for each rail. Resistive dividers scale the voltage rails down, setting an undervoltage trip point for each supply. All outputs are tied together to generate a common power-good signal as shown in the diagram.

As previously discussed, supervisory circuits integrate the comparators as well as the reset generator in a single IC, such as the ADM6710.

These simple supervisory monitoring and reset functions may be sufficient for many systems. However, in systems with complex digital processors, memory, and multiple supply rails, power rails may require sequencing not only to prevent damage but to ensure proper initialization of various circuits. This problem becomes more complex as the number of supply rails increases.

In some cases it is not possible to predict the exact optimum sequencing order during the early design phases of a project, especially when working with the latest devices (such as FPGAs) which may not have complete characterization data available. In other cases, last minute changes in the design can affect the optimum power supply sequence, illustrating the need for flexible solutions.

The following section addresses several methods for solving these types of monitoring and sequencing problems.

Sequencing Supplies: I/O Before Core
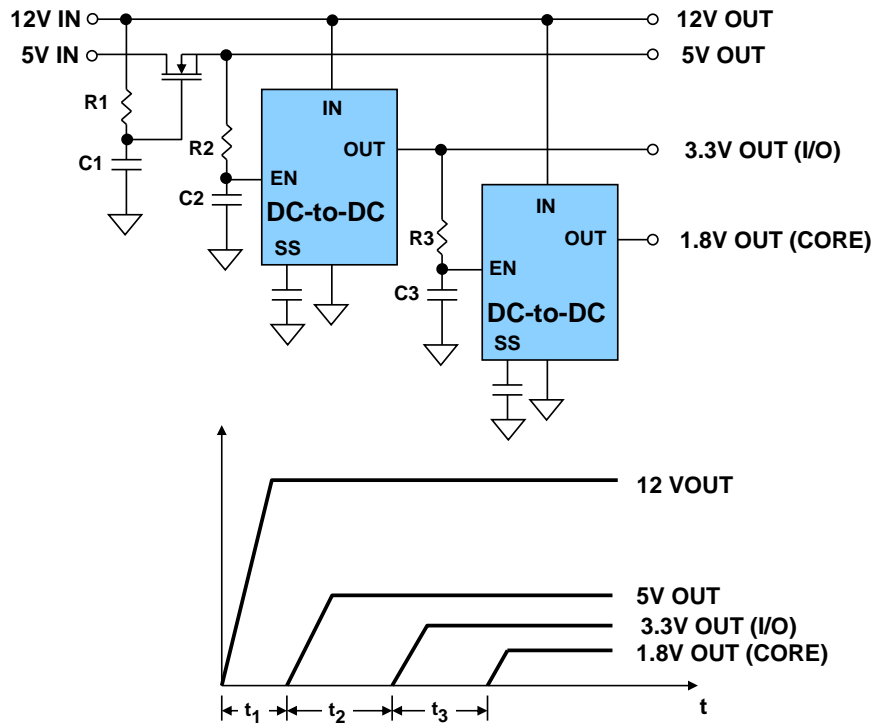
In this circuit, we use discrete components in conjunction with the Enable (EN) inputs of the dc-to-dc converters to perform a simple sequencing function. In this circuit, the desired sequence is 12 V, 5 V, 3.3 V (processor I/O), and 1.8 V (processor core).

Assume that the 12 V and 5 V input buses come up simultaneously. The R1-C1 network delays the gate drive signal to the NMOS FET which is derived from the 12 V input bus.

The R2-C2 network delays the application of the Enable signal to the 3.3 V I/O dc-to-dc converter.

The output of the 3.3 V dc-to-dc converter is delayed by the R3-C3 network and ultimately enables the 1.8 V core dc-to-dc converter. Note that the 1.8 V supply cannot be enabled before the 3.3 V supply.

The ramp-up slope of the 3.3 V and 1.8 V dc-to-dc converter outputs can be controlled using the Soft Start (SS) functions, if desired to reduce inrush currents.

Sequencing Supplies: Core Before I/O
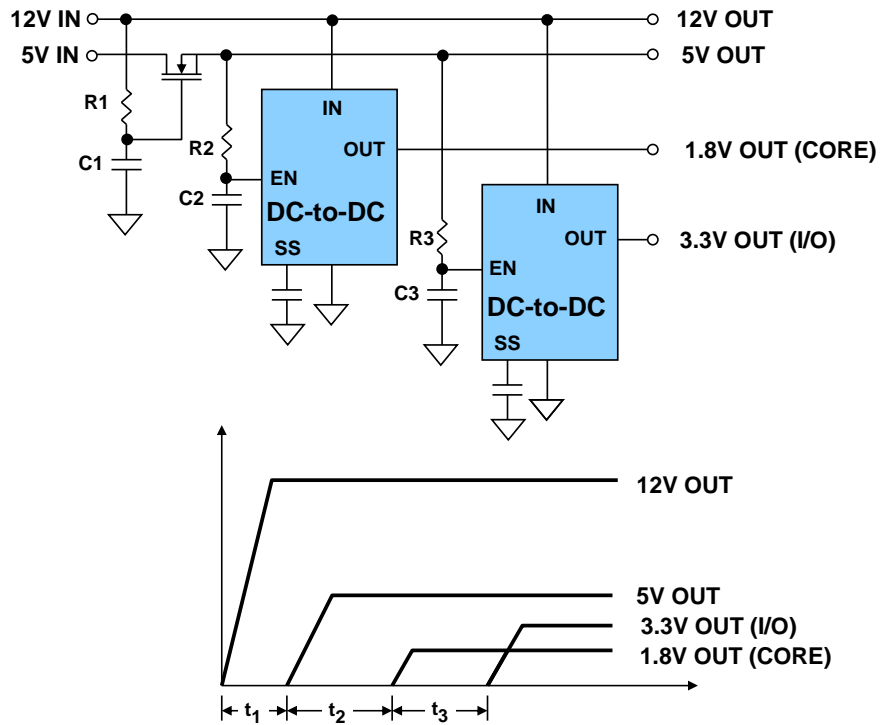
This circuit is similar to the previous one, except the 1.8 V core voltage is brought up before the 3.3 V I/O voltage.

The 3.3 V I/O voltage is enabled using the R3-C3 delay network which is powered from the 5 V bus output.

The proper sequence of the core voltage with respect to the I/O voltage is determined by the particular processor used. In most cases, the core voltage is brought up before the I/O in order to prevent invalid data on the I/O lines, but the processor data sheet should be carefully checked in each case.

Rather than use external discrete components to control sequencing, more integrated solutions are discussed in the next few pages. These ICs offer much more flexibility and accuracy in solving sequencing problems in multirail systems.

Basic Sequencing Using ADM1085
Simple Sequencer® and Regulator Enables
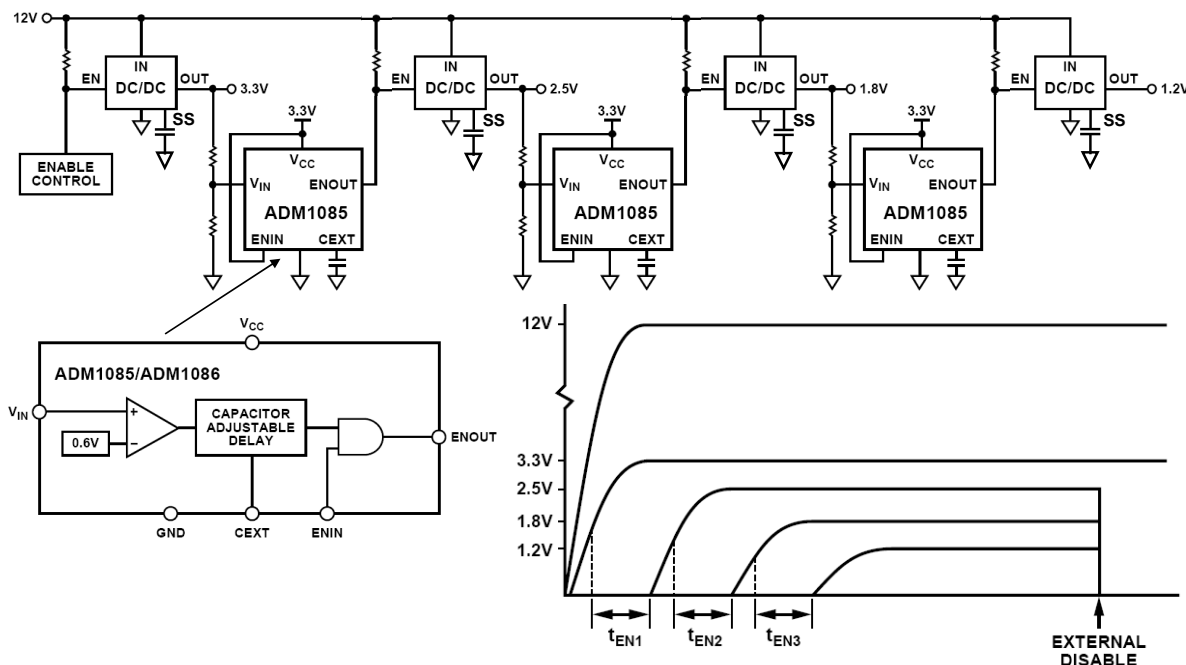
Here, three ADM1085 Simple Sequencers are used to sequence four individual supplies on power-up. The ADM1085 block diagram is also shown. The device consists of a comparator, capacitor-controlled adjustable delay, and an output stage, very similar to a microprocessor power-on reset circuit. The threshold voltage is set by the resistor divider which scales the particular supply voltage to the internal comparator reference voltage of 0.6 V. The positive-going threshold is 0.56 V to 0.64 V, and the negative-going threshold is 0.545 V to 0.645 V (over the operating temperature range of –40°C to +125°C). The accuracy of the 0.6 V threshold is approximately 7% over the full operating temperature range. The ADM1085 family of parts are in a 6-lead SC-70 package.

The delay is determined by the value of the capacitor on the CEXT pin. Separate capacitors on the CEXT pins determine the time delays between enabling of the 3.3 V, 2.5 V, 1.8 V, and 1.2 V supplies. Because the dc-to-dc converters and ADM1085s are connected in a cascade, and the output of any converter is dependent on that of the previous one, an external controller can disable all four supplies simultaneously by disabling the first dc-to-dc converter in the chain.

For power-down sequencing, an external controller dictates when the supplies are switched off by accessing the ENIN inputs individually.

The ADM1085/ADM1086/ADM1087/ADM1088 are compatible with voltage regulators and dc-to-dc converters that have active high or active low enable or shutdown inputs, with a choice of open-drain or push-pull output stages.

The sequence of the supplies is easily changed by simply changing the position of the dc-to-dc converter in the chain and adjusting the divider resistors appropriately.

The dc-to-dc converter soft-start (SS) function can be used to control the individual power supply ramp rates if desired to reduce inrush currents.

ADM1185 Quad Voltage Monitor & Sequencer

◆ **4 Monitoring Comparators :**
  ● **0.6V Reference, 0.8% Accurate**
  ● **Trip points set with external resistor dividers**
◆ **V$_{CC}$: 2.7V to 5.5V**
◆ **4 Open-Drain Outputs:**
  ● **Three Enable Outputs for Regulators**
  ● **Power Good Output (PWRGD)**
◆ **Logical Core:**
  ● **Provides power supply sequencing and fault detection**
◆ **Package:**
 ● **10-lead MSOP**
  ● **Industry's smallest Quad Sequencer**
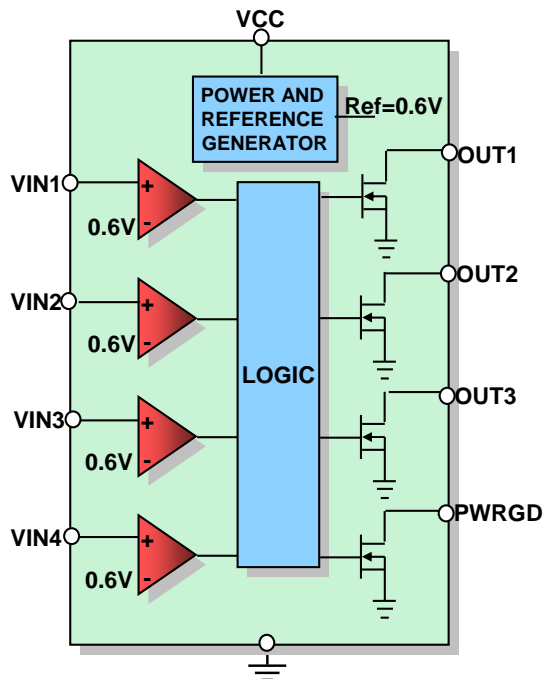
Rather than using an individual Simple Sequencer for each supply voltage as previously described, the ADM1185 allows monitoring and sequencing of up to four supplies. The part contains four individual comparators that are 0.8% accurate as well as a pre-programmed state machine for sequencing.

The hardwired logical state machine core interprets the status of the comparator outputs. Internal time delays can be used for sequencing the startup of subsequent power supplies enabled by the outputs. Supplies falling out of range are also detected and, as a result, appropriate outputs are disabled.

The ADM1185 has four open drain outputs. In a typical configuration, OUT1 to OUT3 are used to enable power supplies, while PWRGD is a common power-good output indicating the status of all monitored supplies, i.e., all four comparators are high.

It is important to note that as processor core voltages decrease, the accuracy required to reliably monitor them increases. ADI provides voltage monitoring and sequencing products with accuracies as good as 0.8%.

ADM1185 Typical Monitoring & Sequencing Application
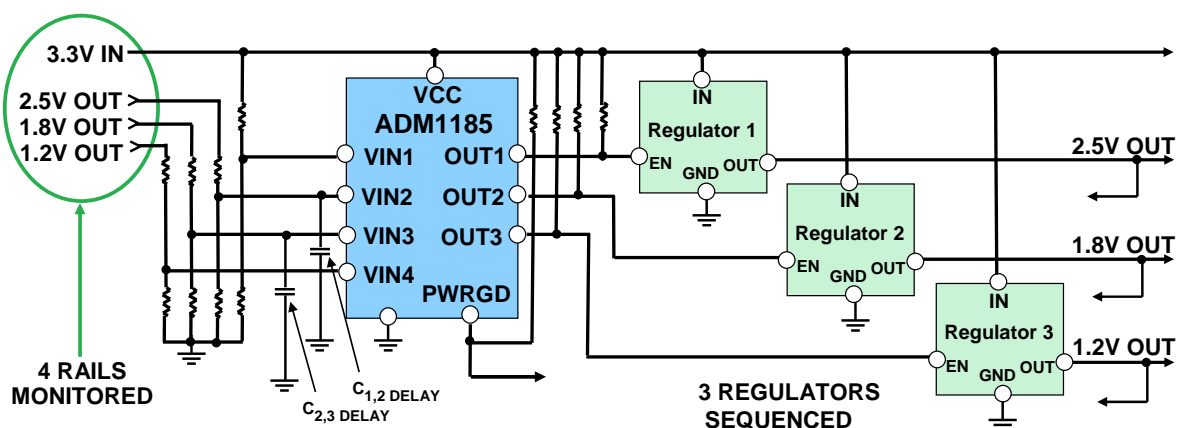
State	State Name	OUT1	OUT2	OUT3	OUT4	Next Event	Next State
1	Reset	0	0	0	0	VIN1 high for 190 ms	OUT1 On
2	OUT1 On	1	0	0	0	VIN1 and VIN2 high for 30 μs	OUT1, OUT2 On
3	OUT1, OUT2 On	1	1	0	0	VIN1 and VIN3 high for 30 μs	OUT1, OUT2, OUT3 On
4	OUT1, OUT2, OUT3 On	1	1	1	0	All high for 190 ms	Power Good
5	Power Good	1	1	1	1	VIN2 , VIN3, or VIN4 low for 30 μs	OUT1, OUT2, OUT3 On

This shows a typical application of the ADM1185 monitoring four supplies and sequencing three regulators. The resistor dividers scale the monitored voltages to equal the 0.6 V internal comparator reference voltage. External capacitors can be added in order to add more delay between the enabling of the regulators.

OUT1 is an open-drain active high output. In this application, OUT1 is connected to the enable pin of Regulator 1. Before the voltage on VIN1 has reached 0.6 V, this output is switched to ground, disabling Regulator 1. Note that all outputs are driven to ground as long as there is at least 1 V on the V_{CC} pin of the ADM1185. When the main system voltage reaches 2.9 V, VIN1 detects 0.6 V. This causes OUT1 to assert after a 190 ms (typical) delay. When this occurs, the open-drain output switches high, and the external pull-up resistor pulls the voltage on the Regulator 1 enable pin above its turn-on threshold, turning on the output of Regulator 1. The assertion of OUT1 turns on Regulator 1. The 2.5 V output of this regulator begins to rise. This is detected by input VIN2. When VIN2 detects the 2.5 V rail rising above its UV point, it asserts output OUT2, which turns on Regulator 2. A capacitor can be placed on the VIN2 pin to slow the rise of the voltage on this pin. This effectively sets a time delay between the 2.5 V rail powering up and the next regulator enable. The same scheme is implemented with the other input and output pins. Every rail that is turned on via an output pin, OUTx, is monitored via an input pin VIN(x + 1).

The final comparator inside the VIN4 pin detects the final supply turning on, which is 1.2 V in this case. The output pins, OUT1 to OUT3, are logically AND'ed together to generate a system power-good signal (PWRGD). There is an internal 190 ms delay (typical) associated with the assertion of the PWRGD output.

Note that the soft-start feature can be used if desired to control the output voltage ramp-up of any or all the regulators. Also, the regulators can be sequenced in any desired order by their placement in the chain with respect to OUT1, OUT2, and OUT3.

Timing Diagram for ADM1185

(A) POWER-UP

VIN1 — V_T (RISING)

30µs + REG.1 DELAY + $C_{1,2}$ DELAY

OUT1 — t_{PROP} — 190ms

30µs + REG.2 DELAY + $C_{2,3}$ DELAY

OUT2

OUT3

PWRGD — 190ms + REG.3 DELAY

(B) NEGATIVE-GOING GLITCH ON +3.3V

VIN1 — V_T (RISING), V_T (FALLING) = 0.6V, t_{PROP}, t_{PROP}

OUT1 — 190ms

OUT2

OUT3

PWRGD — 190ms
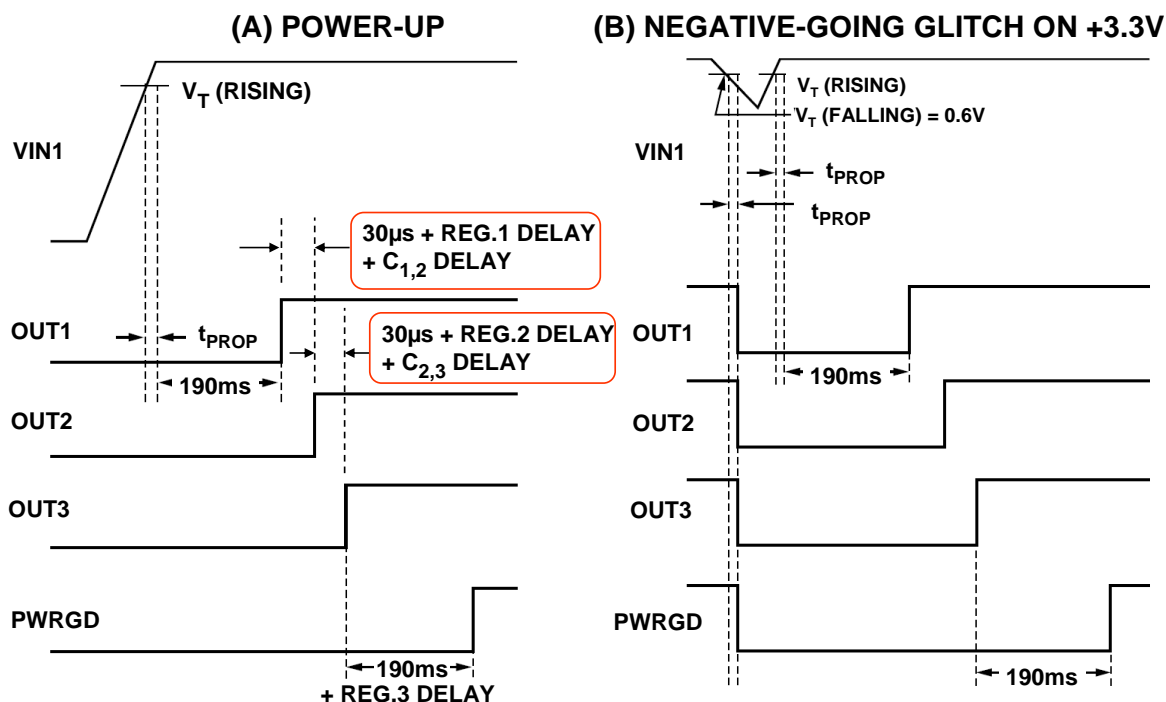
This shows the timing diagram for power-up (A) and for a negative-going glitch on the +3.3 V line (B).

The operation in the power-up state has been explained on the previous page.

Once PWRGD is asserted, the logical core latches into a different mode of operation. During the initial power-up phase, each output directly depends on an input (for example, VIN3 asserting causes OUT3 to assert). When power-up is complete, this function is redundant.

Once in the PWRGD state, the following behavior can be observed:

• If the main 3.3 V supply monitored via VIN1 faults in the power-good state, the PWRGD output is de-asserted to warn the downstream controller. All outputs (OUT1 to OUT3) are immediately turned off, disabling all locally generated supplies.

• If a supply monitored by VIN2 to VIN4 fails, the PWRGD output is de-asserted to warn the controller, but the other outputs are not de-asserted.

ADM1066 Super Sequencer®
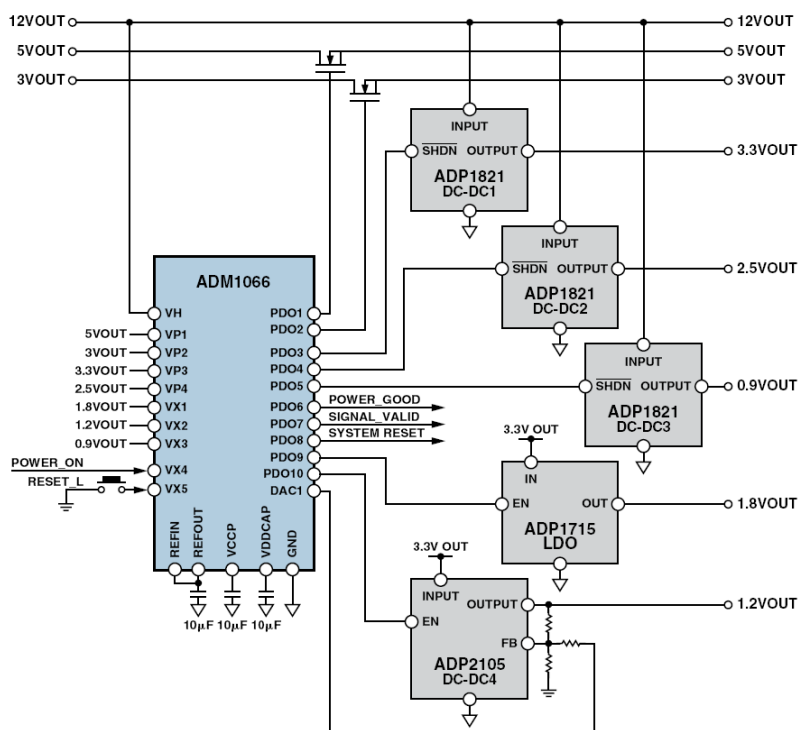
Sequencing more than three or four supply rails can become quite complex using individual sequencing ICs. Consider a system with eight voltage rails that requires a complex power-up sequence. Each rail must be monitored for undervoltage and overvoltage faults. In the event of a fault, all voltages could be turned off, or a power-down sequence could be initiated, depending on the failure mechanism. Actions must be taken depending upon the state of the control signals, and flags must be generated depending on the state of the power supplies. Implementing a circuit of this complexity with discrete devices and simple ICs may require hundreds of individual components, a huge amount of board space, and a significant combined cost. In systems with four or more voltages, it may make sense to use a centralized device to manage the power supplies. An example of this approach is shown above.

The ADM106x Super Sequencer family continues to use comparators, but with some important differences. Two comparators are dedicated to each input so that undervoltage and overvoltage detection can be implemented, thus providing windowed monitoring for the rails. An undervoltage fault is the normal condition of a rail before it powers up, so this indication is used for sequencing. An overvoltage condition usually indicates a critical fault—such as a shorted FET or inductor—and calls for immediate action.

Systems with higher supply counts usually have greater complexity, and thus have tighter accuracy constraints. Also, setting accurate thresholds with resistors becomes challenging at lower voltages, such as 1.0 V and 0.9 V. Although a 10% tolerance may be acceptable on a 5 V rail, this tolerance is generally insufficient on a 1 V rail. The ADM1066 allows input detector comparator thresholds to be set within 1% worst case, independent of the voltage (as low as 0.6 V)—and across the entire temperature range of the device. It adds internal glitch filtering and hysteresis to each comparator. Its logic inputs can be used to start the power-up sequence, shut down all rails, or perform other functions.

State Machine Based
Sequencing Engine Core
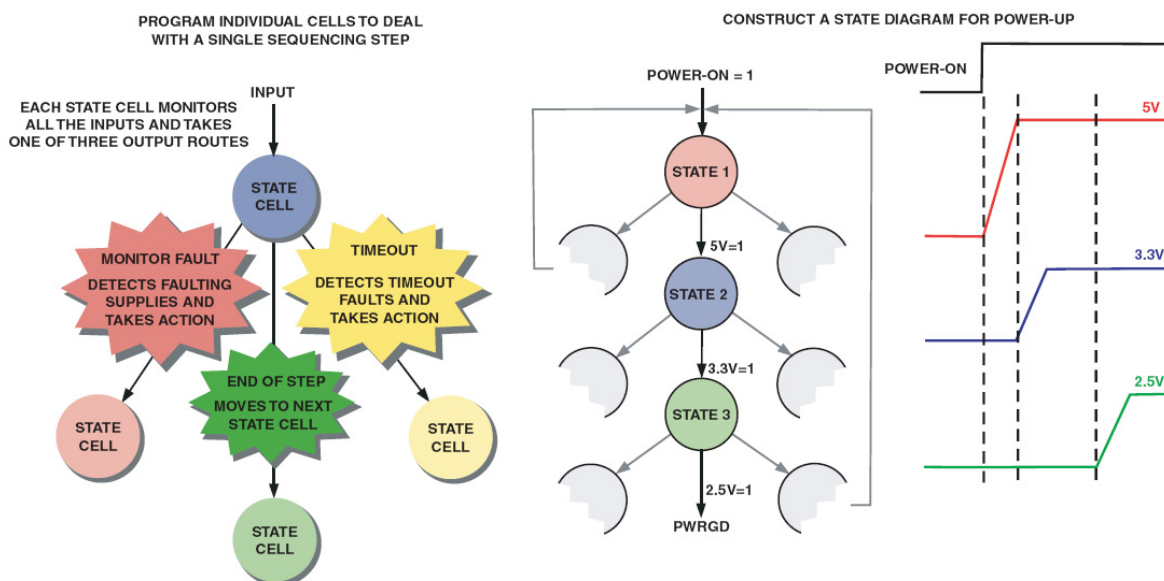
The information from the bank of comparators is then fed into a powerful and flexible stage machine core and can be used for various purposes:

1. Sequencing: When the output voltage of a recently enabled supply comes into a window, a time delay can be triggered to turn on the next rail in the power-up sequence. Complex sequencing, with multiple power-up and power-down sequences, or vastly different sequences for power-up and power-down is possible.

2. Timeout: If a rail that has been enabled does not come on as expected, a suitable course of action can be taken (such as generating an interrupt or shutting down the system). A purely analog solution would simply hang at that point in the sequence.

3. Monitoring: If the voltage on any rail moves out of the preset window, a suitable course of action can be taken—depending on the rail that faulted, the type of fault that occurred, and the current operating mode. Systems with more than five supplies are often expensive, so comprehensive fault protection is crucial. An on-board charge pump is used to generate approximately 12 V of gate drive, even if the highest available system voltage is as low as 3 V, allowing outputs to directly drive series NMOS FETs. Additional outputs enable or shut down dc-to-dc converters or regulators, allowing an output to internally pull up to one of the inputs or the on-board regulated voltage. The outputs can also be asserted open-drain. Outputs may also be used as status signals such as power good or power-on reset. Status LEDs can be directly driven from the outputs if required.

The state machine core is programmed via the industry-standard 2-wire SMBus interface.

ADM1066 Super Sequencer
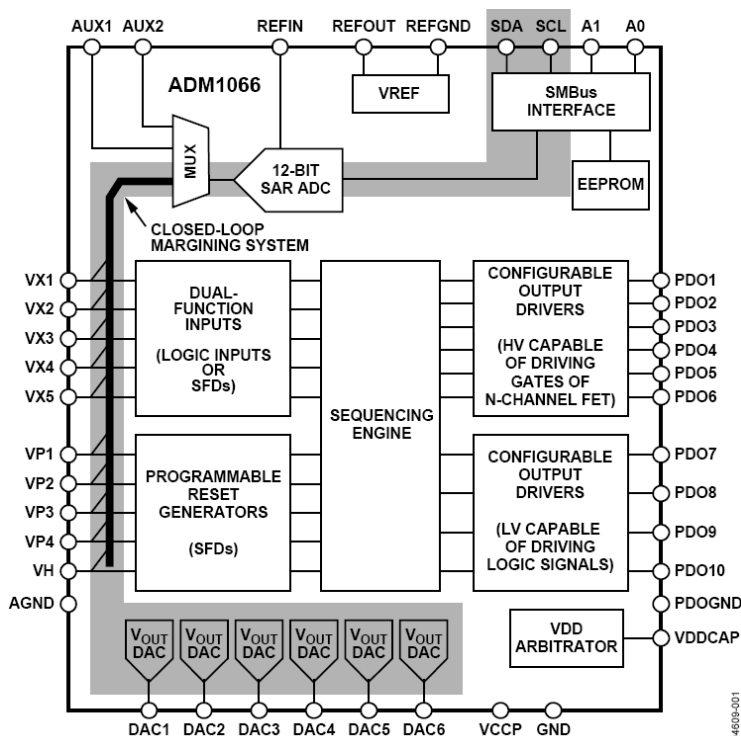
The ADM1066 is a configurable supervisory/sequencing device that offers a single-chip solution for supply monitoring and sequencing in multiple-supply systems. In addition to these functions, the ADM1066 integrates a 12-bit ADC and six 8-bit voltage output DACs. These circuits can be used to implement a closed-loop margining system that enables supply adjustment by altering either the feedback node or reference of a dc-to-dc converter using the DAC outputs.

Supply margining can be performed with a minimum of external components. The margining loop can be used for in-circuit testing of a board during production (for example, to verify the board's functionality at −5% of nominal supplies), or can be used dynamically to accurately control the output voltage of a dc-to-dc converter.

The device also provides up to 10 programmable inputs for monitoring under, over, or out-of-window faults on up to 10 supplies. In addition, 10 programmable outputs can be used as logic enables. Six of them can also provide up to a 12 V output for driving the gate of an NMOS FET, which can be placed in the path of a supply.

The logical core of the device is a sequencing engine. This state-machine-based construction provides up to 63 different states. This design enables very flexible sequencing of the outputs, based on the condition of the inputs.

The device is controlled via configuration data that can be programmed into an EEPROM. The whole configuration can be programmed using an intuitive GUI-based software package provided by Analog Devices, Inc. The on-board nonvolatile memory allows it to be reprogrammed as many times as necessary, while the sequencing and monitoring needs of the system evolve during the development process. This means that the hardware design can be completed early in the prototype process, and optimization of the monitoring and sequencing can be done as the project progresses.

Closed-Loop Supply Margining
Using ADM1062/ADM1066
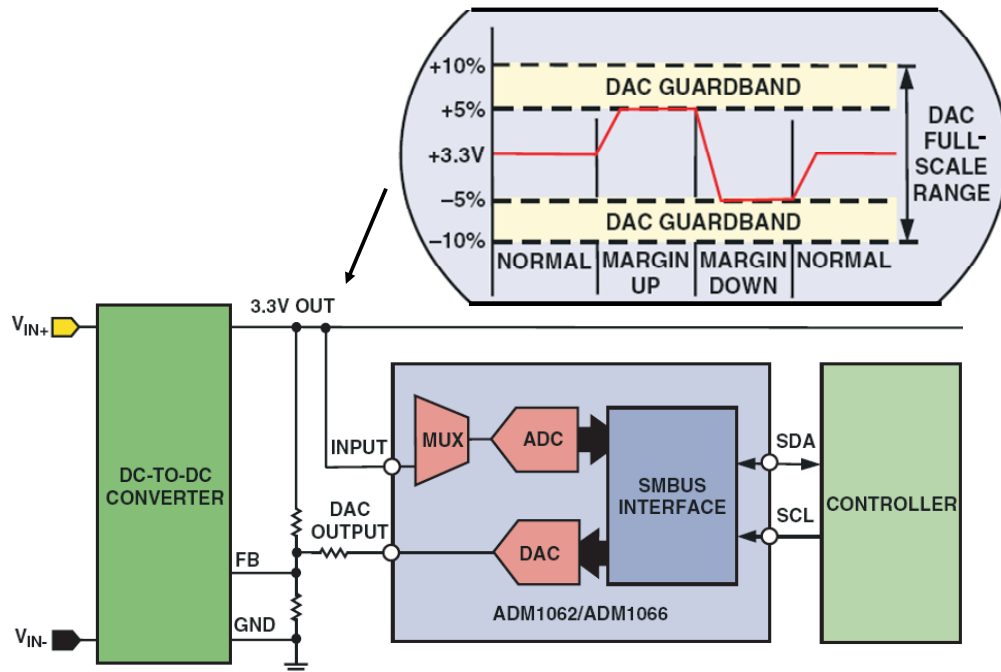
In addition to monitoring multiple voltage rails and providing a solution for complex sequencing, integrated power management devices, such as the ADM1066, also provide the tools to temporarily or permanently adjust individual rail voltages. The voltage output of a dc-to-dc converter or regulator can be altered by adjusting the voltage at the trim or feedback node of that device. Typically, a resistive divider between the output and ground of the module sets a nominal voltage at the trim/feedback pin. This, in turn, sets a nominal output voltage. Simple schemes involving switching extra resistors or controlling variable resistances in the feedback loop will alter the trim/feedback voltage and hence adjust the output voltage.

The ADM1066 is equipped with digital-to-analog converters (DACs) to provide direct control over the trim/feedback node. For maximum efficiency, these DACs do not operate between ground and a maximum voltage; instead they operate across a relatively narrow window centered on the nominal trim/feedback level. The value of an attenuation resistor scales the incremental change in the output of the power module with each LSB change of the DAC. This open-loop adjustment provides margin-up and margin-down levels equivalent to those obtained by digital resistance switching in the reference circuit, and will adjust the output to a similar accuracy.

The ADM1066 also includes a 12-bit analog-to-digital converter (ADC) to measure the supply voltages, so a closed-loop supply adjustment scheme can be implemented. With a given DAC output setting, the voltage output of the power module is digitized by the ADC and compared with the target voltage in software. The DAC can then be adjusted to calibrate the voltage output as closely as possible to the target voltage. This closed-loop scheme provides a very accurate method for supply adjustment. With a closed-loop method, the accuracy of the external resistors is completely irrelevant.

Hot Swap Controllers

www.analog.com/hotswap

What is a Hot Swap Controller?

◆ **A Hot Swap Controller is a device which allows a removable circuit board to be removed or inserted into a live system without interrupting the system's power supply bus.**

◆ **Typical Backplane Bus Voltages: –48V, +12V, +5V**

Hot swap controllers allow a circuit board to be removed or inserted into a live system without interrupting the system power supply bus.

They are useful in many critical infrastructure applications such as telecommunications systems, servers, switchers and routers, and base stations—virtually any system which uses high currents and must remain operational while repairs, upgrades, or modifications are made.

The standard backplane voltage for telecommunications is –48 V. This standard had its origins in the early days of the telephone network. The 48 V supply was considered to be the largest dc voltage that was not lethal under normal circumstances, and was a standard voltage easily generated by a battery backup bank made up of four 12 V batteries in series.

The negative voltage was chosen to minimize galvanic corrosion causing corrosion of cables under damp conditions. A conductor with a negative charge will repel chlorine ions, as Cl (chlorine) ions are negative also. If the conductor were to have a positive charge, Cl ions would be attracted. This form of corrosion protection is called cathodic protection. It is often used for pipelines, bridges, etc. Such protection was very important in the days of open wire transmission lines.

Other standard backplane voltages are +12 V and +5 V, and there are others.

Hot Swap Techniques

◆ **Using short pin on connector**
  - ● **Provided delay on enabling Power Supply to eliminate arcing at connectors.**

◆ **RC / Slew control on Power Supply Switch**
  - ● **This allowed the voltage to increase slowly and hence charge capacitors slowly reducing inrush current spikes.**

◆ **Some problems that remained**
  - ● **No overcurrent protection**
  - ● **No true inrush current protection—current limited**
  - ● **No Short circuit protection**

◆ **Benefits of Integrated Hot Swap controllers**
  - ● **Closed Loop Accurate Current Control**
  - ● **True linear Soft Start control**
  - ● **Programmable timing circuit breaker**
  - ● **NMOS series-pass FETs**

An early hot swap technique was to use a short pin on the connector for the power supply connection. This allowed all pins in the connector to be firmly in place before the actual power was applied, thereby minimizing arcing.

Other techniques were used, such as RC slew-rate limiting on the power supply switch, but modern ICs allow the function to be performed much more reliably and seamlessly.

Integrated hot swap controllers provide overcurrent protection, inrush current limiting, soft-start, and programmable timer controlled circuit breakers. The majority of IC hot swap controllers are designed to operate with low cost and highly reliable NMOS series pass FETs as the main power switching device.

Functions of a Hot Swap Controller

◆ **Limits Inrush Current**
◆ **Provides Short Circuit protection**
◆ **Provides Active Current limiting**
◆ **Based on Low Cost, Reliable NMOS Series Pass FETs**
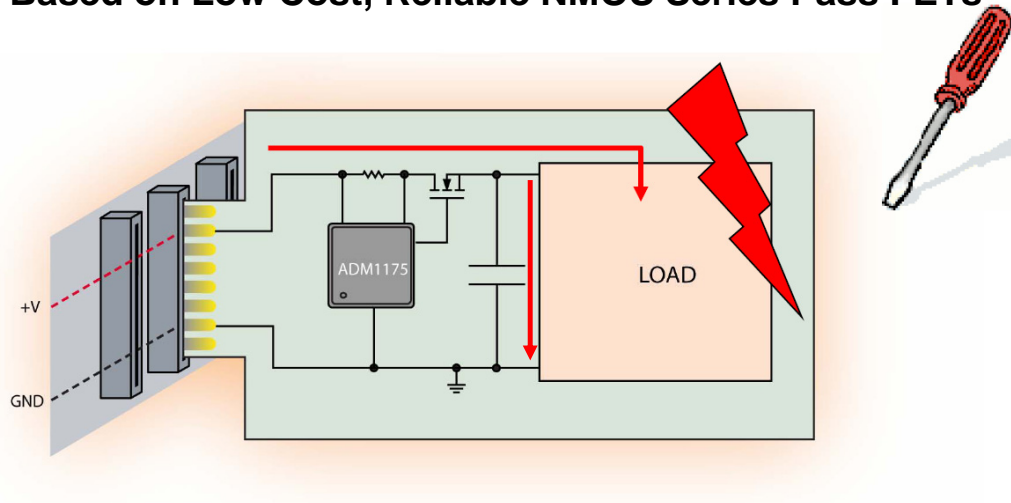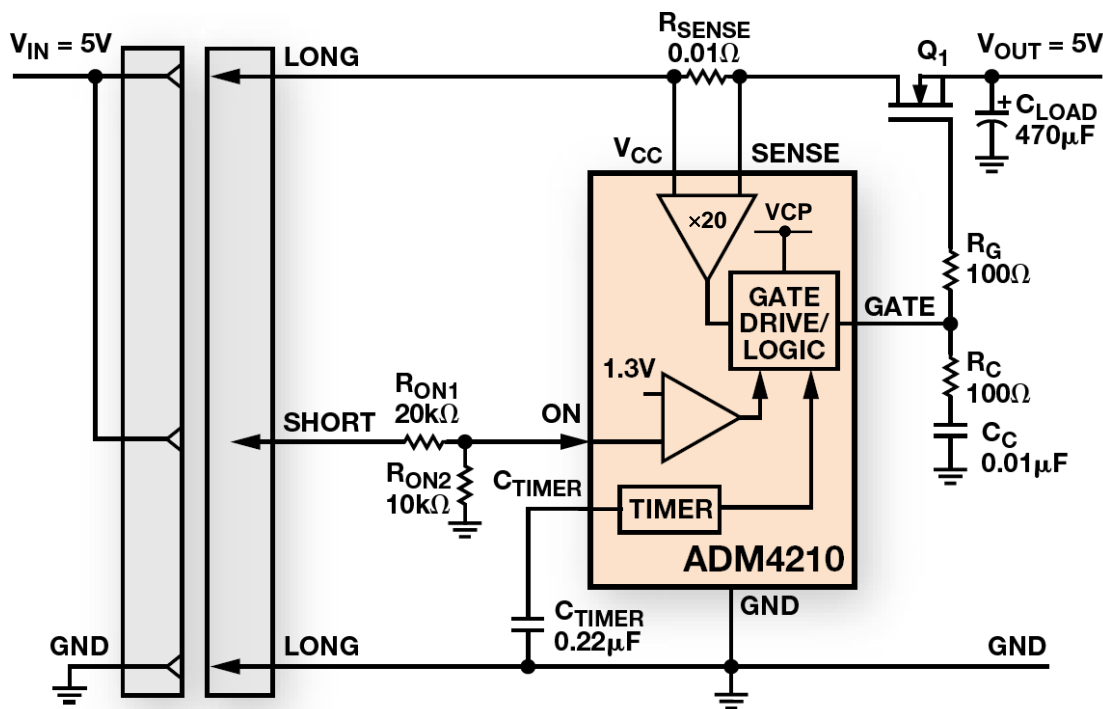

The basic functions of a hot swap controller are shown here. A primary function is to limit the inrush current when the card is inserted. The total inrush current can be quite high, since it is made up of not only the circuit current but also the initial current required to charge large bulk filter capacitors.

The hot swap controller must also provide short circuit protection as well as active current limiting.

The basic switch element chosen is almost always a low cost, reliable NMOS series pass FET as shown in the diagram.

The low output impedance of the NMOS FET source follower makes it relatively insensitive to bulk capacitor loads, and the control loop is fairly easy to stabilize. The gate drive signal to the NMOS FET must be several volts higher than the drain and source voltage, therefore charge pumps are often included in the hot swap controller IC to generate the required gate drive voltage. Although PMOS series pass devices do not require a separate supply for the gate drive, they have a higher output impedance, and the feedback loop is more difficult to stabilize. For this reason, the NMOS FET is the device of choice for the series pass element in a hot swap controller.

Components of a Hot Swap Controller

This shows the basic components of a hot swap controller. The external components required are a sense resistor (R_{SENSE}), NMOS FET switch, feedback compensation network (R_G, R_C, C_C), voltage divider (R_{ON1}, R_{ON2}), and a timer capacitor (C_{TIMER}).

The voltage divider sets the threshold voltage to the internal comparator in the hot swap controller IC. In the case of the ADM4210, the comparator reference voltage is 1.3 V. the divider network shown divides the 5 V bus voltage by a factor of 3. In this circuit, the threshold voltage referenced to the bus voltage is 3×1.3 V = 3.9 V.

The internal circuit breaker is controlled by a current sense comparator which starts an overcurrent timeout sequence when the sense voltage is equal to 50 mV. The sense resistor limits the fault current to 50 mV/R_{SENSE}. A sense resistor of 0.01 Ω gives a fault current of 5 A.

The timing control circuit gives an initial timing delay of 273 ms/µF $\times$ C_{TIMER} and a circuit breaker delay of 22 ms/µF $\times$ C_{TIMER}.

The timer generates ramp voltages by either sourcing or sinking current in or out of the C_{TIMER} capacitor. The gate drive is turned on or off by two additional comparators and control logic. The internal comparator threshold voltages are 0.2 V and 1.3 V.

The ADM4210 also contains a gate drive circuit for the external NMOS FET using an internal charge pump. The gate driver consists of a 12 µA pull-up current source from the internal charge pump voltage. The internal charge pump voltage range is typically 7.5 V to 11 V above V_{CC}, for V_{CC} between 3 V and 15 V.

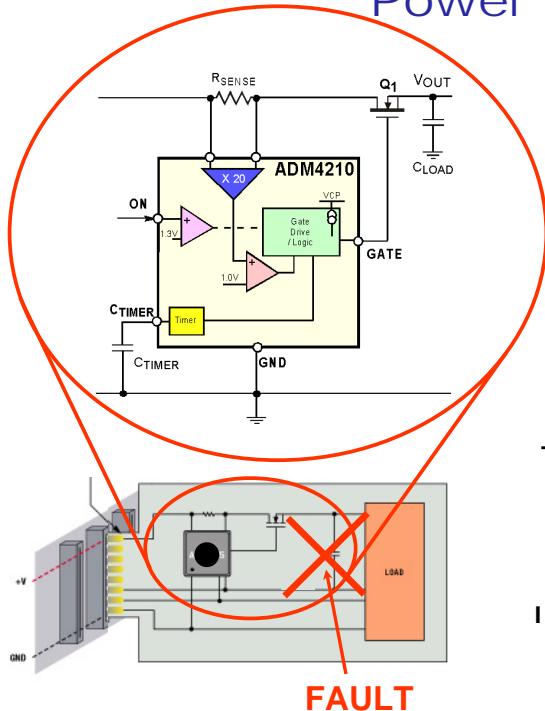# How the Hot Swap Controller Works for Normal Power Up
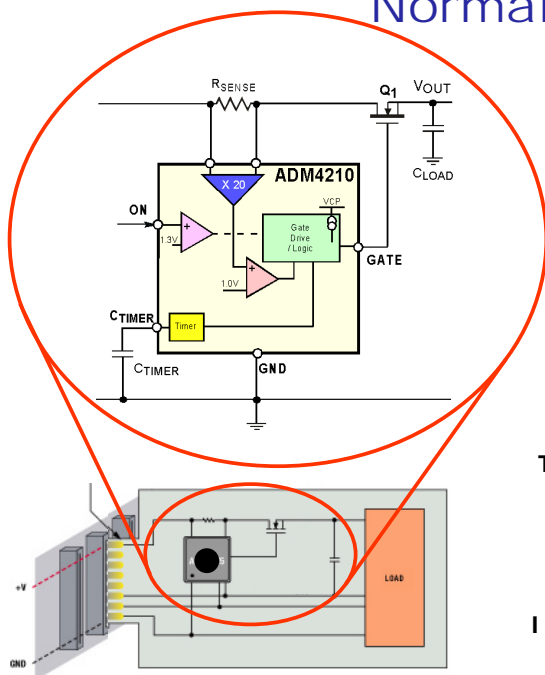
Normal Power Up

1. **Controller is enabled**
2. **Timer Cycles Initial Period**
3. **Gate comes up**
4. **Inrush Current is Limited**
5. **Inrush Current falls off to normal**
6. **Power up complete**
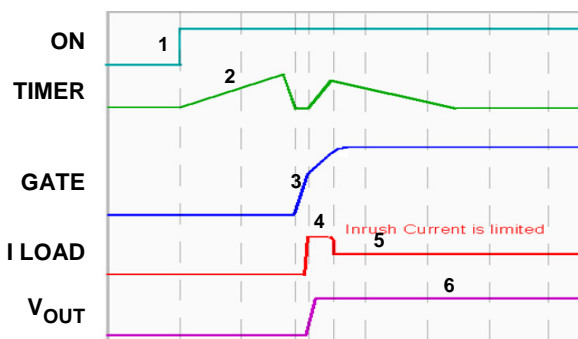
This figure shows how a typical hot swap controller works for normal power up conditions.
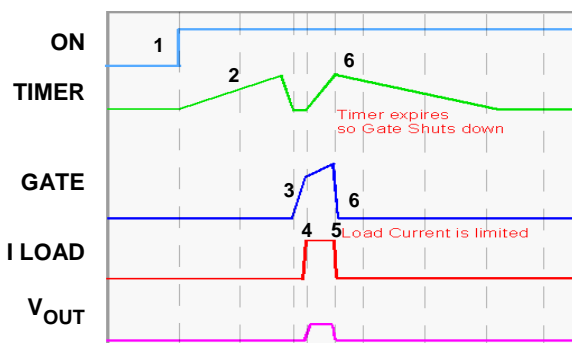
1. When the card is plugged in and the input voltage crosses the undervoltage lockout threshold, the controller is enabled, starting the internal timer.

2. The timer voltage ramps up at a rate controlled be the external C_{TIMER} capacitor and a pull-up current of 5 µA.

3. When the timer voltage reaches 1.3 V, this is the end of the first timing cycle. The timer current changes to a pull-down current of 100 µA, and the ramp voltage changes direction. When the ramp voltage reaches 0.2 V, the GATE pin is pulled high turning on the NMOS FET.

4. The second timer cycle is then enabled. When the voltage across the sense resistor exceeds the circuit breaker trip voltage, a timer pull-up current of 60 µA is activated.

5. If the sense voltage falls below the current limit level before the timer voltage reaches 1.3 V, the 60 µA pull-up is disabled and a 2 µA pull-down current is enabled. This is the normal operating mode if the overcurrent fault is only inrush current or a transient.

6. The 2 µA pull-down current causes the ramp voltage to return to zero, and the power-up cycle is completed.

How the Hot Swap Controller Works for Power Up Into a Fault

FAULT

Power Up into a Fault

1. **Controller is enabled**
2. **Timer Cycles Initial Period**
3. **Gate comes up**
4. **Inrush Current is Limited**
5. **Current remains at limit due to Fault**
6. **Timer Expires and FET is Shutdown**

This figure shows how the hot swap controller works when a card having a short circuit is plugged in.

1. When the card is plugged in and the input voltage crosses the undervoltage lockout threshold, the controller is enabled, starting the internal timer.

2. The timer voltage ramps up at a rate controlled be the external C_{TIMER} capacitor and a pull-up current of 5 µA.

3. When the timer voltage reaches 1.3 V, this is the end of the first timing cycle. The timer current changes to a pull-down current of 100 µA, and the ramp voltage changes direction. When the ramp voltage reaches 0.2 V, the GATE pin is pulled high turning on the NMOS FET.

4. The second timer cycle then enabled. When the voltage across the sense resistor exceeds the circuit breaker trip voltage, a timer pull-up current of 60 µA is activated.

5. The short circuit continues, and the ramp voltage reaches the 1.3 V threshold. The short circuit timer has now expired.

6. The gate drive is pulled low, disabling the FET.

On the ADM4210-1, the timer function activates the 2 µA pull-down once the 1.3 V threshold is reached, and continues to pull down until it reaches the 0.2 V threshold. At this point, the 100 µA pull-down is activated, and the GATE pin is enabled. The device then keeps retrying.

The duty cycle of this automatic retry cycle is set to the ratio of 2 µA/60 µA, which approximates 3.8% on. The value of the timer capacitor determines the on-time of this cycle.

The ADM4210-2 model has a latch-off system whereby when a current fault is detected, the GATE is switched off after a time determined by the timer capacitor. Toggling the ON-CLR pin, or pulling the TIMER pin to GND for a brief period, resets this condition.

Soft Start Gives Linear Inrush Current Control

◆ **Soft Start is a means by which Hot Swap controllers can control the inrush current increase to a safe level.**

◆ **If the nominal current limit was high (e.g. 10A), on start up, load capacitance may require all this current and more for a short period of time to charge up. This is inrush current.**

◆ **Even though the limit is maintained at 10A by the controller, the sudden jump from 0A to 10A can cause unwanted transients on the supply line.**

◆ **The effect of increasing soft start capacitor values on inrush current can be seen as follows:**

Increasing Soft Start Capacitor Value
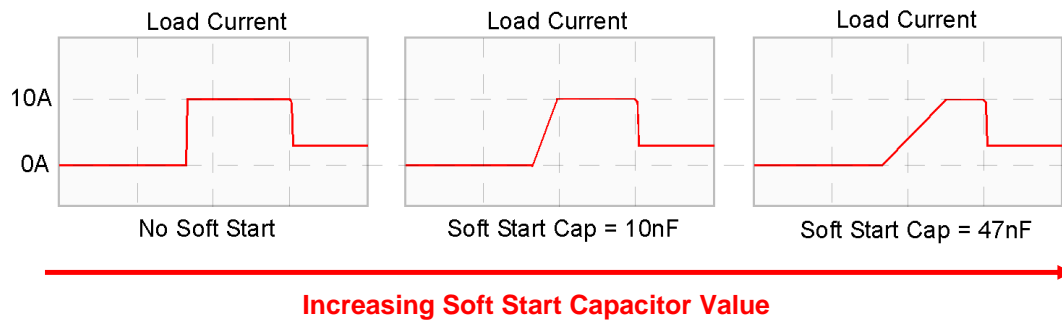
**Soft Start Available on ADM1170, ADM1171, ADM1177 and ADM1073 (−48V)**

Soft start is a means by which a hot swap controller can control the inrush current to increase at a safe level. The function operates in a manner similar to the soft start feature found on many linear and switching regulators.

Because of large values of bulk capacitance, with no soft start feature, the hot swap controller current can jump from zero to the current limit value. This current, called inrush current, is required to charge the input capacitance and can create unwanted transients on the supply line.

As shown in this figure, the soft start feature slows down the rate of increase in charging current and reduces transient effects. Increasing the value of the soft start capacitor produces a proportional increase in the ramp-up time.

Many full-featured hot swap controllers such as the ADM1170, ADM1171, ADM1177, and ADM1073 have the soft start feature.

Hot Swap Controller + Power Monitoring
ADM1175, ADM1176, ADM1177, ADM1178
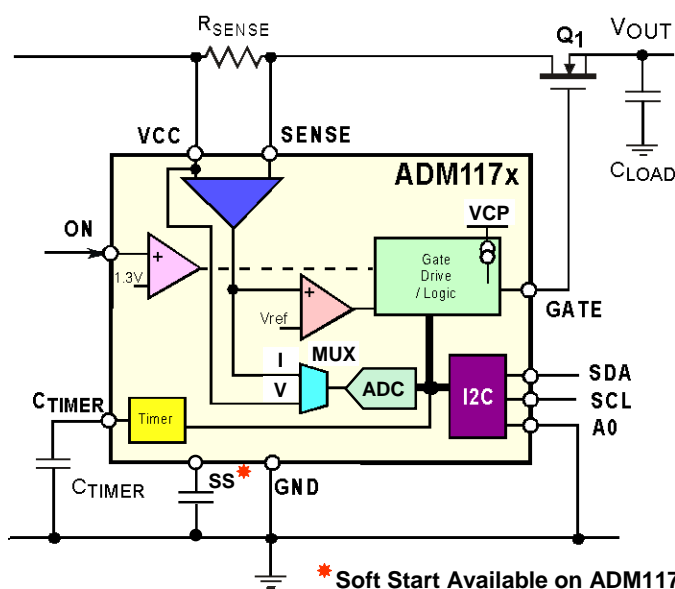
Hot Swap Controller

1. **Current Sense Comparator**
2. **Timer**
3. **ON Pin**
4. **FET Gate Driver**

+ Power Monitoring

5. **V_{CC} Voltage to MUX**
6. **CS AMP to MUX**
7. **12-Bit ADC to I²C**

＊Soft Start Available on ADM1177 and ADM1073 (–48V)

The ADM1175/ADM1176/ADM1177/ADM1178-series are integrated hot swap controllers that have on-chip current sense comparator, time, ON function, and FET gate driver. Operation of these functions is similar to the ADM4210 previously described.

In addition, this family of devices offers digital current and voltage monitoring via an on-chip, 12-bit analog-to-digital converter (ADC), communicated through an I²C® interface.

A 12-bit ADC can measure the current seen in the sense resistor, as well as the supply voltage on the V_{CC} pin. An industry-standard I²C interface allows a controller to read current and voltage data from the ADC. Measurements can be initiated by an I²C command. Alternatively, the ADC can run continuously, and the user can read the latest conversion data whenever it is required.

ADM117x/ADM119x Solution for Digital Power Measurement
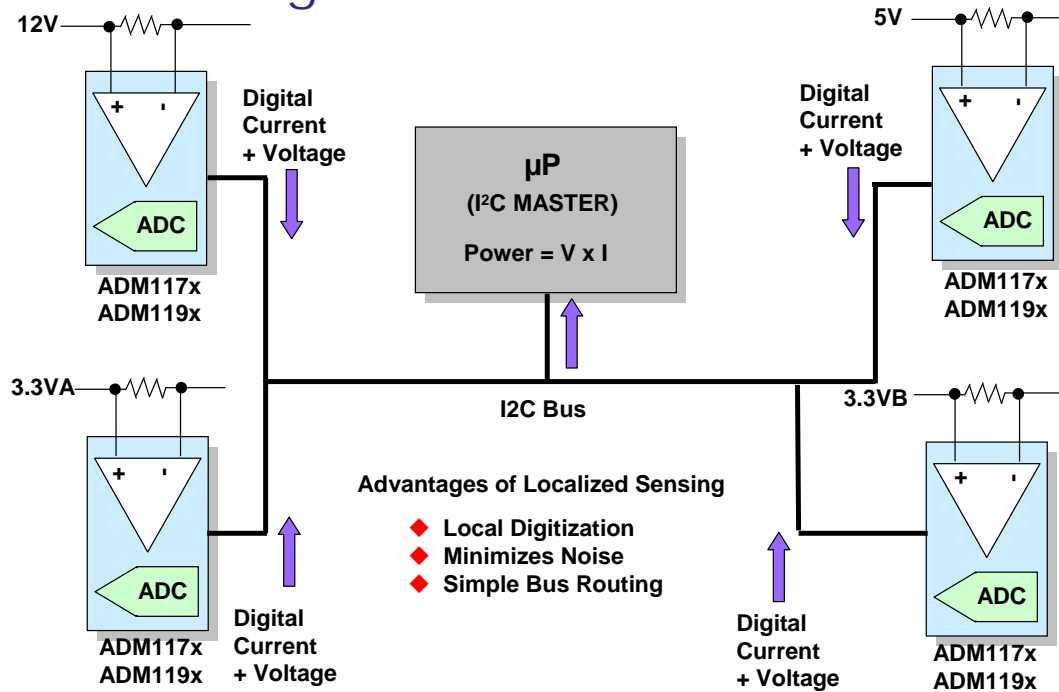
As well as performing the hot swap function, the ADM1175/ADM1176/ADM1177/ADM1178-series can monitor total power consumed by each PC board via the on-chip ADC and the I²C bus.

Noise is minimized by performing the digitization locally on each PC board and transmitting the current and voltage measurements digitally, rather than transmitting the actual PC board voltages and the current-sense signals over system wiring.

The ADM1191 and ADM1192 perform the power monitoring function, but without the hot swap feature.

Temperature Monitoring

www.analog.com/temperature

Types of Temperature Sensors

THERMOCOUPLE	RTD	THERMISTOR	SEMICONDUCTOR
Widest Range: **−184ºC to +2300ºC**	**Range:** **−200ºC to +850ºC**	**Range:** **0ºC to +100ºC**	**Range:** **−55ºC to +150ºC**
High Accuracy and Repeatability	**Fair Linearity**	**Poor Linearity**	**Linearity: 1ºC** **Accuracy: 1ºC**
Needs Cold Junction Compensation	**Requires Excitation**	**Requires Excitation**	**Requires Excitation**
Low-Voltage Output	**Low Cost**	**High Sensitivity**	**10mV/K, 20mV/K, or 1µA/K Typical Output**

Measurement of temperature is critical in modern electronic devices, especially expensive computers with densely packed circuits which dissipate considerable power in the form of heat. Knowledge of system temperature can also be used to control battery charging as well as prevent damage to expensive microprocessors.

Compact high power portable equipment often has fan cooling to maintain junction temperatures at proper levels. In order to conserve battery life, the fan should only operate when necessary. Accurate control of the fan requires a knowledge of critical temperatures from the appropriate temperature sensor.

Accurate temperature measurements are required in many other measurement systems such as process control and instrumentation applications. In most cases, because of low-level nonlinear outputs, the sensor output must be properly conditioned and amplified before further processing can occur.
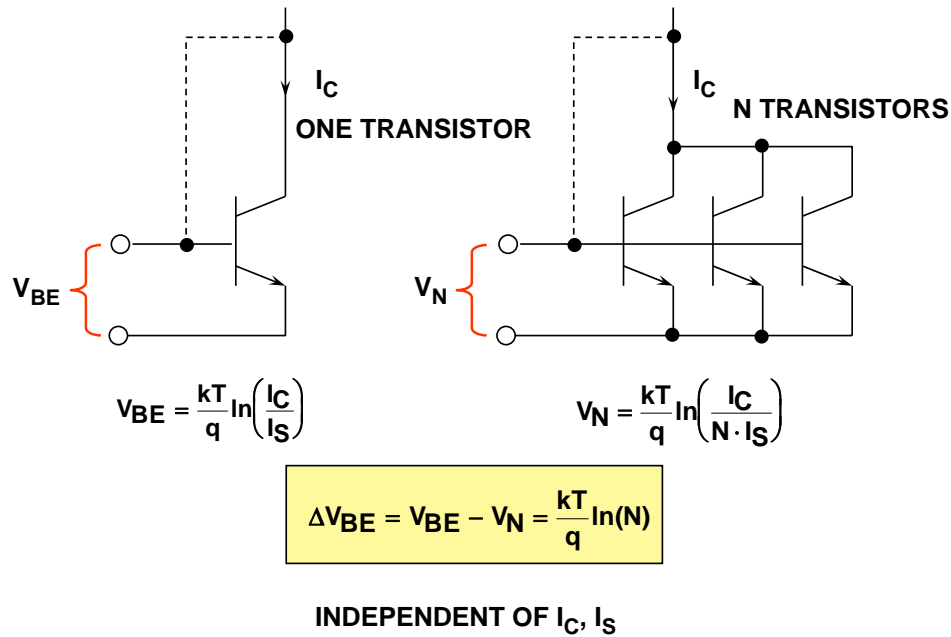
Thermocouples have the widest temperature range of all the sensors, but require specialized signal conditioning circuitry because of their low-level outputs and non-linear transfer functions

Resistance Temperature Devices (RTDs) are accurate, but require excitation current and are generally used in bridge circuits.

Thermistors have the most sensitivity but are the most non-linear. However, they are popular in portable applications such as measurement of battery temperature and other critical temperatures in a system.

Modern semiconductor temperature sensors offer high accuracy and high linearity over an operating range of about −55ºC to +150ºC. Internal amplifiers can scale the output to convenient values, such as 10 mV/ºC. Semiconductor temperature sensors can be integrated into multi-function ICs which perform a number of other hardware monitoring functions, and are ideal for most system applications where temperature is critical.

2.43

Basic Relationship for
IC Temperature Sensors

$$V_{BE} = \frac{kT}{q} \ln\left(\frac{I_C}{I_S}\right)$$

$$V_N = \frac{kT}{q} \ln\left(\frac{I_C}{N \cdot I_S}\right)$$

$$\Delta V_{BE} = V_{BE} - V_N = \frac{kT}{q} \ln(N)$$

INDEPENDENT OF I_C, I_S

Modern semiconductor temperature sensors offer high accuracy and high linearity over an operating range of about –55°C to +150°C. All semiconductor temperature sensors make use of the relationship between a bipolar junction transistor's (BJT) base-emitter voltage to its collector current:

$$V_{BE} = \frac{kT}{q} \ln\left(\frac{I_c}{I_s}\right)$$

where k is Boltzmann's constant, T is the absolute temperature (K), q is the charge of an electron, and I_s is a current related to the geometry and the temperature of the transistors. (The equation assumes a voltage of at least a few hundred mV on the collector, and ignores Early effects.)

If we take N transistors identical to the first and allow the total current I_c to be shared equally among them, we find that the new base-emitter voltage is given by the equation

$$V_N = \frac{kT}{q} \ln\left(\frac{I_c}{N \cdot I_s}\right)$$

Neither of these circuits is of much use by itself because of the strongly temperature dependent current I_s, but if we have equal currents in one BJT and N similar BJTs then the expression for the difference between the two base-emitter voltages is proportional to absolute temperature and does not contain I_s:

$$V_{BE} - V_N = \frac{kT}{q} \ln\left[\left(\frac{I_c}{I_s}\right) \Big/ \left(\frac{I_c}{N \cdot I_s}\right) \right] = \frac{kT}{q} \ln(N)$$
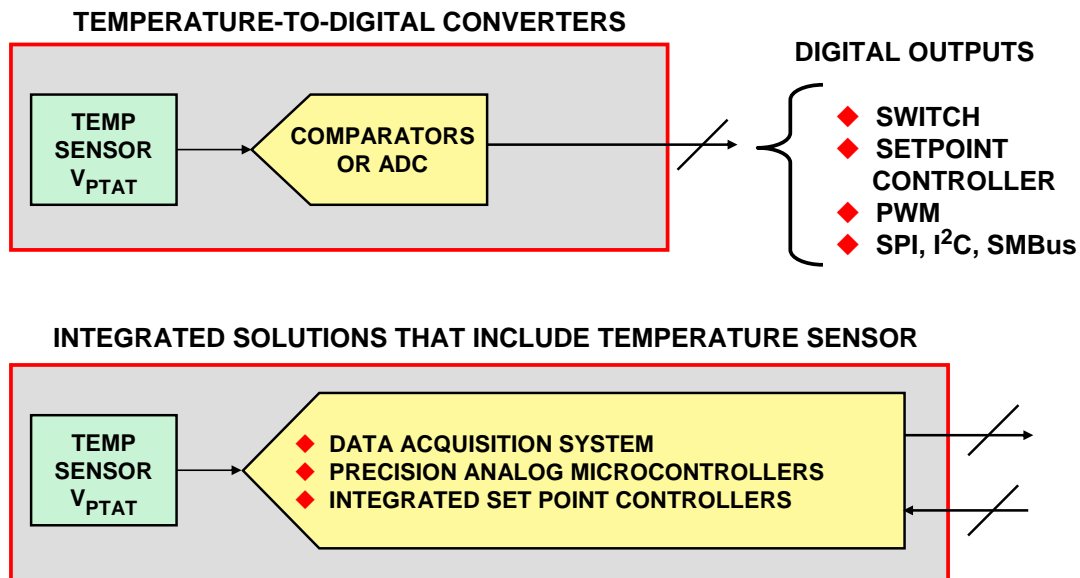
Classic Band Gap Temperature Sensor
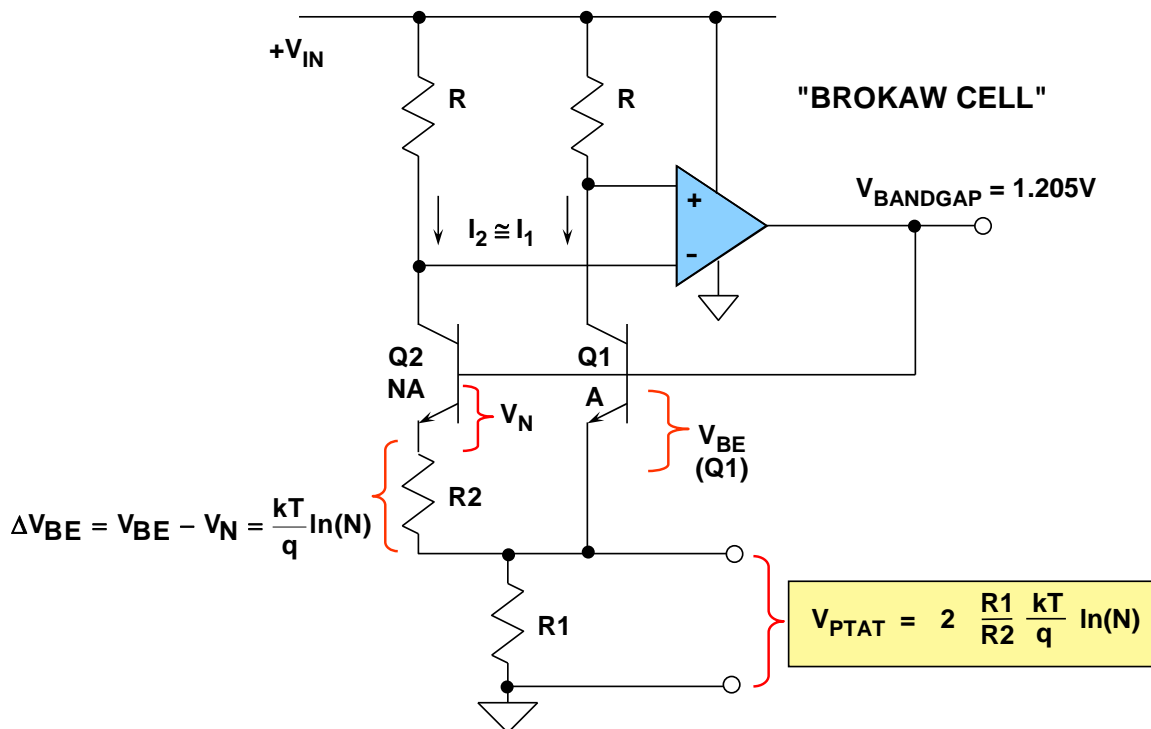
The circuit shown in this figure implements the previous equation and is known as the "Brokaw Cell". The voltage $V_{BE} - V_N$ appears across resistor R2. The emitter current in Q2 is therefore $(V_{BE} - V_N)$/R2. The op amp's servo loop and the resistors, R, force the same current to flow through Q1. The Q1 and Q2 currents are equal and are summed and flow into resistor R1. The corresponding voltage developed across R1 is proportional to absolute temperature (PTAT) and given by:

$$V_{PTAT} = \frac{2R1(V_{BE} - V_N)}{R2} = 2\frac{R1}{R2}\frac{kT}{q}\ln(N)$$

The band gap cell reference voltage, $V_{BANDGAP}$, appears at the base of Q1 and is the sum of $V_{BE(Q1)}$ and V_{PTAT}. $V_{BE(Q1)}$ is complementary to absolute temperature (CTAT), and summing it with V_{PTAT} causes the band gap voltage to be constant with respect to temperature (assuming proper choice of R1/R2 ratio and N to make the band gap voltage equal to 1.205 V). This circuit is the basic band gap temperature sensor, and is widely used in semiconductor temperature sensors.

Analog Temperature Sensors are Now Integrated into Many Different Parts

TEMPERATURE-TO-DIGITAL CONVERTERS

DIGITAL OUTPUTS

| TEMP SENSOR V_{PTAT} | → | COMPARATORS OR ADC |

- ◆ SWITCH
- ◆ SETPOINT CONTROLLER
- ◆ PWM
- ◆ SPI, I^2C, SMBus

INTEGRATED SOLUTIONS THAT INCLUDE TEMPERATURE SENSOR

| TEMP SENSOR V_{PTAT} | → |

- ◆ DATA ACQUISITION SYSTEM
- ◆ PRECISION ANALOG MICROCONTROLLERS
- ◆ INTEGRATED SET POINT CONTROLLERS

Voltage references form an integral part of data acquisition systems of all types. The V_{PTAT} voltage is conveniently part of the reference and is available for temperature sensing as well.

It is therefore relatively easy to integrate a temperature sensor into most modern ICs if one is required. The sensor monitors the temperature of its junction, which should be approximately equal to the ambient temperature, provided the total internal power dissipation of the device is low, and self-heating is not an issue.

Digital temperature sensors can take many forms. The simplest is a V_{PTAT} generator followed by a comparator which acts as a simple on/off function, depending on the comparator voltage reference. This type of temperature sensor forms the basis of modern setpoint controllers. More sophisticated digital temperature sensors use an ADC to convert the temperature sensor voltage into either a PWM signal, or bus-compatible digital signal.

Low Cost, 2.7V to 5.5V, Micropower Temperature Switches in SOT-23

✷ FROM 12-BIT SIGMA-DELTA MODULATOR
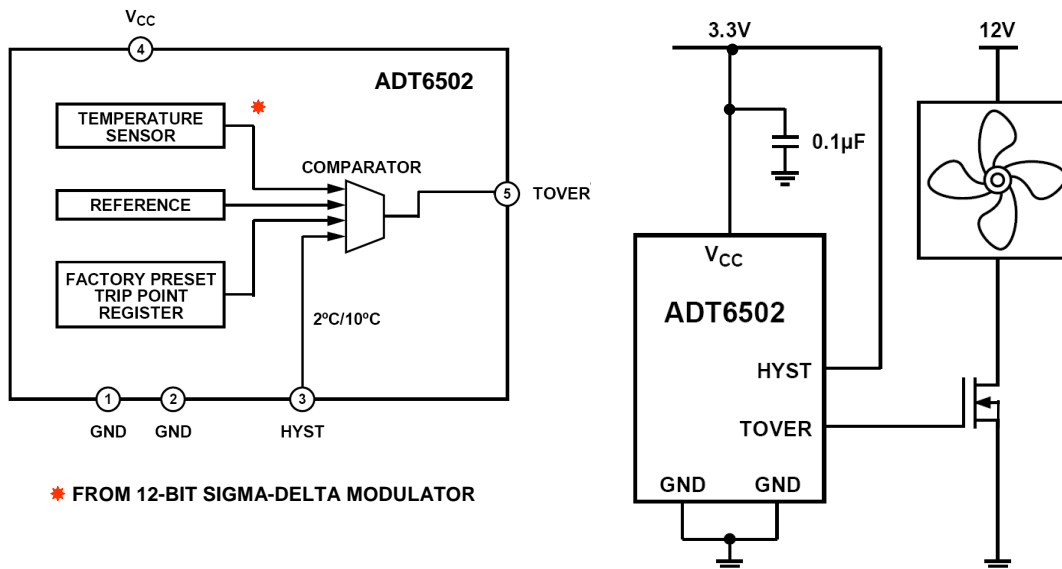
The ADT6501/ADT6502/ADT6503/ADT6504 are trip point temperature switches available in a 5-lead SOT-23 package. Each part contains an internal band gap temperature sensor for local temperature sensing. The band gap output voltage (V_{PTAT}) is digitized with a 12-bit sigma-delta modulator.

The 12-bit output from the modulator is input into a digital comparator where it is compared with a factory set trip level. The output trip pin is activated if the temperature measured is greater than the factory set trip level. Overall accuracy for the ADT650x family is ±6°C from −45°C to +115°C.

Factory set trip levels are available in 10°C increments from +35°C to +115°C for the ADT6501/ADT6502 and from −45°C to +15°C for the ADT6503/ADT6504.

The ADT6501/ADT6503 logic output is active low and open-drain. The ADT6502/ADT6504 logic output is active high and push-pull. The temperature is digitized to a resolution of 0.0625°C (12 bit). The factory settings are 10°C apart starting from −45°C to +15°C for the cold threshold models and from +35°C to +115°C for the hot threshold models.

These devices require no external components and typically consume 30 μA supply current. Hysteresis is pin-selectable at 2°C and 10°C. The temperature switch is specified to operate over the supply range of 2.7 V to 5.5 V.

The ADT6501 and ADT6502 are used for monitoring temperatures from +35°C to +115°C only. Therefore, the logic output pin becomes active when the temperature goes higher than the selected trip point temperature.

The ADT6503 and ADT6504 are used for monitoring temperatures from −45°C to +15°C only. Therefore, the logic output pin becomes active when the temperature goes lower than the selected trip point temperature.

The circuit shown uses the ADT6502 and an external NMOS FET to drive a fan. The output of the ADT6502 goes high when the temperature goes higher than the selected trip point temperature, turning on the FET and the fan.

Digital Isolation
and Isolated Power

www.analog.com/icoupler

Digital Isolators Based on *i*Coupler® Technology
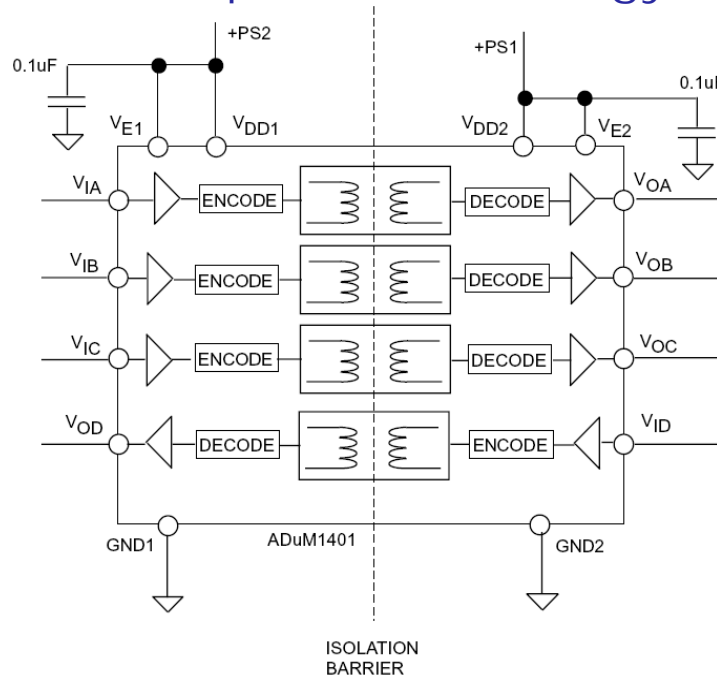
Digital isolators are extremely useful in separating system grounds. Designed primarily for galvanic isolation in industrial applications, the *i*Coupler isolator can be used to pass signals between ground planes at different potentials. No currents will circulate through the various grounds, since we are using transformers to isolate the grounds. The transfer rate through the *i*Coupler can be as high as 100 Mbps.
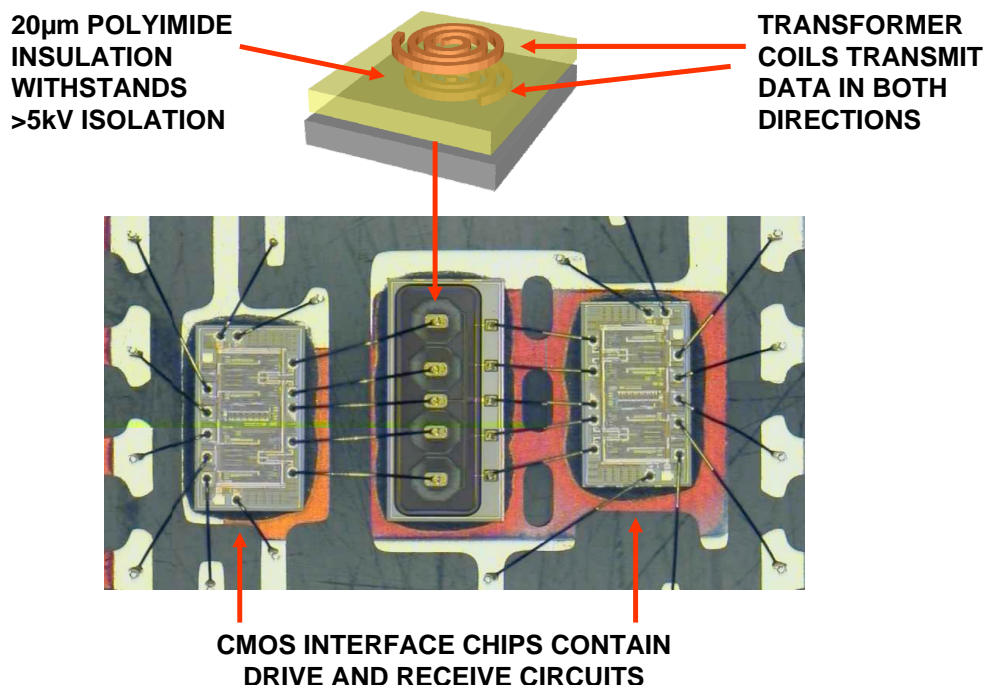
The ADuM140x1 are 4-channel digital isolators based on Analog Devices, Inc. *i*Coupler technology. Combining high speed CMOS and monolithic air core transformer technology, these isolation components provide outstanding performance characteristics superior to alternatives such as optocoupler devices.

By avoiding the use of LEDs and photodiodes, *i*Coupler devices remove the design difficulties commonly associated with optocouplers. The typical optocoupler concerns regarding uncertain current transfer ratios, nonlinear transfer functions, and temperature and lifetime effects are eliminated with the simple *i*Coupler digital interfaces and stable performance characteristics.

The need for external drivers and other discrete components is eliminated with these *i*Coupler products. Furthermore, *i*Coupler devices consume one-tenth to one-sixth the power of optocouplers at comparable signal data rates and are more cost effective.

The ADuM140x isolators provide four independent isolation channels in a variety of channel configurations and data rates. All models operate with the supply voltage on either side ranging from 2.7 V to 5.5 V, providing compatibility with lower voltage systems as well as enabling a voltage translation functionality across the isolation barrier. Unlike other optocoupler alternatives, the ADuM140x isolators have a patented refresh feature that ensures dc correctness in the absence of input logic transitions and during power-up/power-down conditions.

Construction of the *i*Coupler Digital Isolator

20μm POLYIMIDE INSULATION WITHSTANDS >5kV ISOLATION

TRANSFORMER COILS TRANSMIT DATA IN BOTH DIRECTIONS

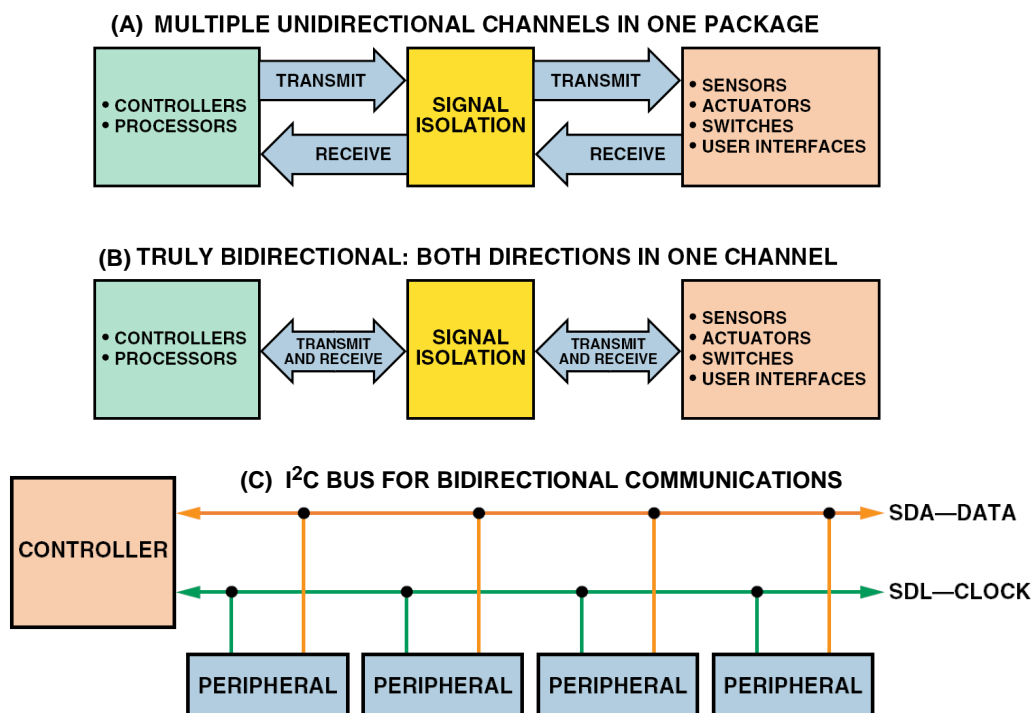**CMOS INTERFACE CHIPS CONTAIN DRIVE AND RECEIVE CIRCUITS**

This photo shows a 4-channel digital isolator, which houses three die in a single package. Two CMOS interface circuits (left and right) integrate drive and receive electronics. The middle die contains four chip-scale microtransformers, each comprising metal (AlCu and Au) coils on either side of a 20 μm polyimide insulation layer. The polyimide is capable of withstanding more than 5 kV rms for one minute.

In most applications that require isolated data transmission, isolated power must be available on both sides of the isolation barrier, or it must be provided separately. System designers typically introduce isolated power by designing an isolated power supply using discrete components—including a transformer with the appropriate isolation rating—or by purchasing a commercial off-the-shelf isolated dc-to-dc converter. Each approach has its advantages and disadvantages. In the first instance, isolated power supplies may be custom tailored to an application, allowing system designers to optimize their cost, isolation rating, power output, or other important specifications depending on the application requirements. The downside, however, is that custom solutions tend to be bulky, require safety certification, and can lengthen development times. Commercially available isolated power supplies, on the other hand, can reduce time to market, but they carry a price penalty and may not be optimized to fit a particular application. While smaller in size than their custom counterparts, they are still fairly bulky, with only limited availability of surface-mount package options.

A third way is *iso*Power®, which combines the benefits of both options. *i*Coupler digital isolators condition and drive data across the transformers. *iso*Power uses the same chip-scale microtransformer technology, but instead of transmitting only data, *iso*Power employs switches, rectifiers, and regulators to generate power that is isolated to the same degree as the data channels.
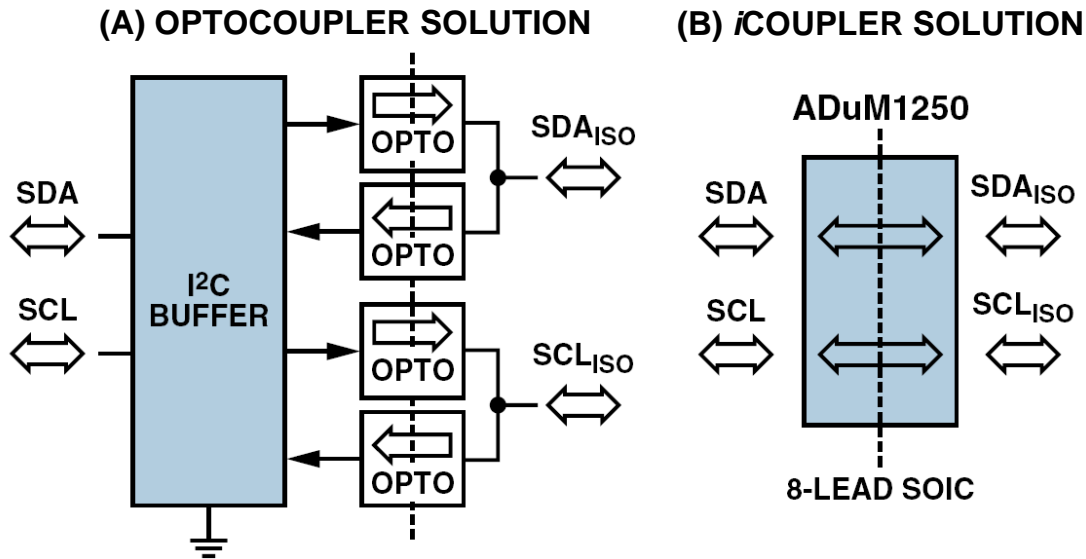
Unidirectional and Bidirectional Transmission

(A) MULTIPLE UNIDIRECTIONAL CHANNELS IN ONE PACKAGE

| • CONTROLLERS
 • PROCESSORS | TRANSMIT →
 ← RECEIVE | **SIGNAL ISOLATION** | TRANSMIT →
 ← RECEIVE | • SENSORS
 • ACTUATORS
 • SWITCHES
 • USER INTERFACES |

(B) TRULY BIDIRECTIONAL: BOTH DIRECTIONS IN ONE CHANNEL

| • CONTROLLERS
 • PROCESSORS | TRANSMIT AND RECEIVE | **SIGNAL ISOLATION** | TRANSMIT AND RECEIVE | • SENSORS
 • ACTUATORS
 • SWITCHES
 • USER INTERFACES |

(C) I^2C BUS FOR BIDIRECTIONAL COMMUNICATIONS

CONTROLLER — SDA—DATA / SDL—CLOCK — PERIPHERAL, PERIPHERAL, PERIPHERAL, PERIPHERAL

In isolation, the term *bidirectional* has traditionally referred to an isolator with separate *transmit* and *receive* channels in one package—the isolator as a whole is capable of bidirectional data transfer, but the individual channels are unidirectional as shown in (A). This approach is compatible with communications protocols such as RS-232, RS-485, and SPI, but it is not compatible with true bidirectional communication protocols, such as I^2C, SMBus, and PMBus, which support bidirectional data transfer through a single channel as shown in (B).

The inter-integrated-circuit (I^2C) bus is a popular 2-wire, bidirectional communication protocol that was developed to provide simple, low-cost, short-distance communication between an on-board controller and its peripherals. I^2C buses limit the cost of applications in which multiple devices share a single bus with a host controller, as shown in (C). Two bidirectional wires—one for the data and one for the clock—are used to achieve low cost at the expense of data rate, so I^2C is typically used in systems with many peripherals running at data rates less than 1 Mbps. Systems that use a limited number of peripherals running at higher data rates will often employ protocols such as SPI.
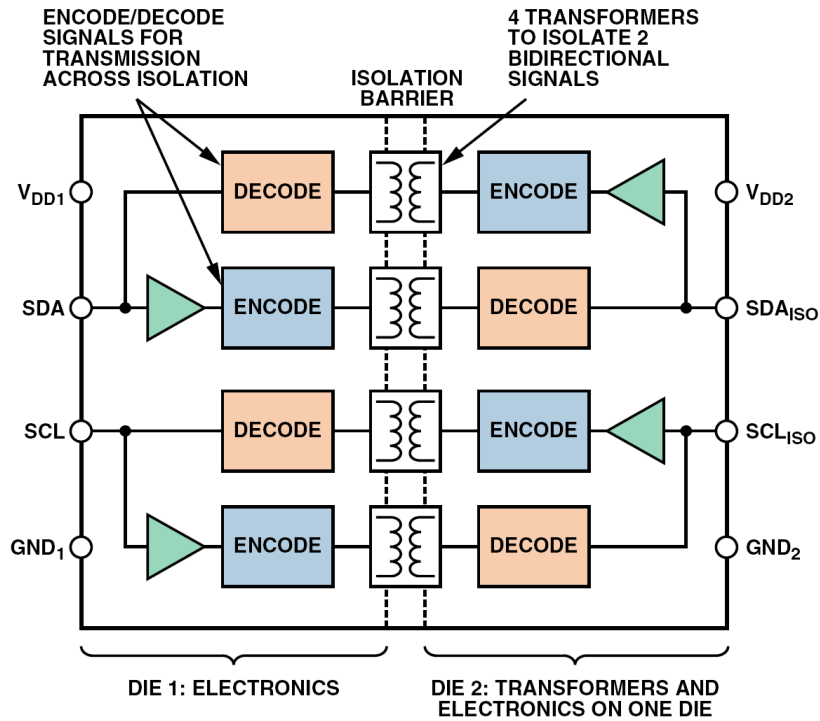
*i*Coupler Simplifies True Bidirectional Isolation

The I²C isolation challenge has been that optocouplers are based on diodes that can transmit in only one direction, and are therefore inherently unidirectional. A bidirectional I²C bus could be isolated using optocouplers as shown in (A), but the implementation is messy. A special buffer is used to separate each bidirectional channel into two distinct channels: transmit and receive. Once separated, the four unidirectional channels can be individually isolated and then recombined. This solution requires four isolators and expands the bus from two wires to four wires. Additional circuitry is also required, making this solution costly and large, and defeating the original purpose of the 2-wire bus implementation: to save money and space.

The good news is that by adopting the new digital isolation techniques the circuitry that is used to separate, isolate, and recombine the data channels can be integrated into a single package. This approach can be implemented with the new ADuM1250 and ADuM1251 hot-swappable dual I²C isolators. Figure (B) illustrates how much more compact the *i*Coupler solution is.

True Bidirectional Isolation Using the ADuM1250 Digital Isolator

ENCODE/DECODE
SIGNALS FOR
TRANSMISSION
ACROSS ISOLATION

ISOLATION
BARRIER

4 TRANSFORMERS
TO ISOLATE 2
BIDIRECTIONAL
SIGNALS

V_{DD1}	DECODE		ENCODE	V_{DD2}
SDA	ENCODE		DECODE	SDA_{ISO}
SCL	DECODE		ENCODE	SCL_{ISO}
GND_1	ENCODE		DECODE	GND_2

DIE 1: ELECTRONICS

DIE 2: TRANSFORMERS AND
ELECTRONICS ON ONE DIE

This figure shows how bidirectional isolation is achieved within the package. Just as the discrete solution employs a buffer to separate the two bidirectional channels into four unidirectional channels and four isolators, so, too, does the ADuM125x family. The difference is that all the electronics are integrated onto a single IC. A designer sees only the 2-wire interface, and the entire device is less than 40 mm², a 90% reduction compared with the optocoupler/buffer solution, which takes up about 350 mm².

The ADuM125x family operates at rates up to 1 MHz.

ADuM5240 Dual-Channel Isolator with *iso*Power Integrated DC-to-DC Converter
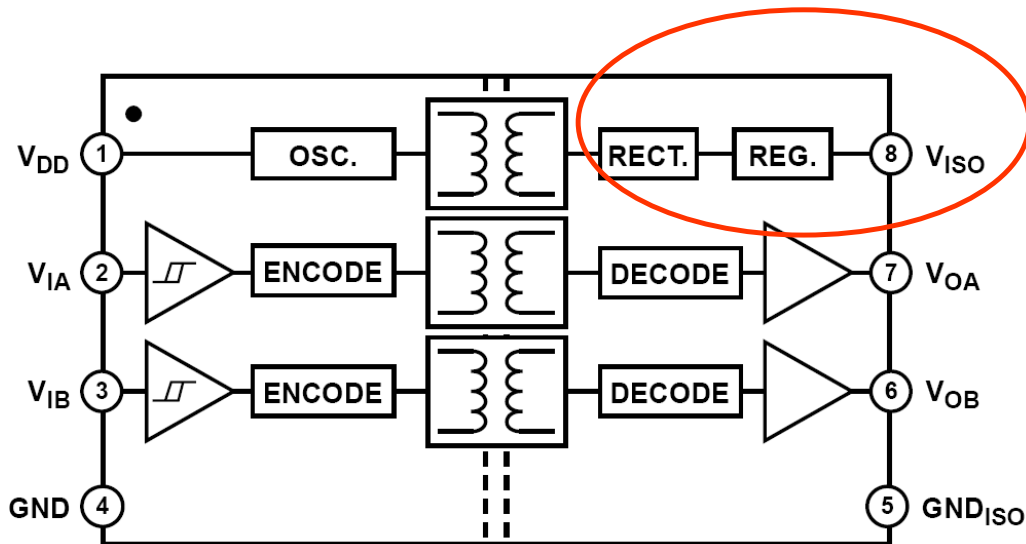

In addition to digital isolation, the capability of providing isolated power is important in many applications.

The ADuM524x are dual-channel digital isolators with *iso*Power integrated, isolated power. An on-chip dc-to-dc converter provides up to 50 mW of regulated, isolated power at 5 V, which eliminates the need for a separate isolated dc-to-dc converter in low power isolated designs.

The ADuM524x isolators provide two independent isolation channels in a variety of channel configurations, operating from a 5 V input supply. ADuM524x units may be used in combination with other *i*Coupler products to achieve greater channel counts.

The ADuM524x family of isolators operates at data rates up to 1 Mbps.

*iso*Power Digital Isolator
# Implements Isolated Power
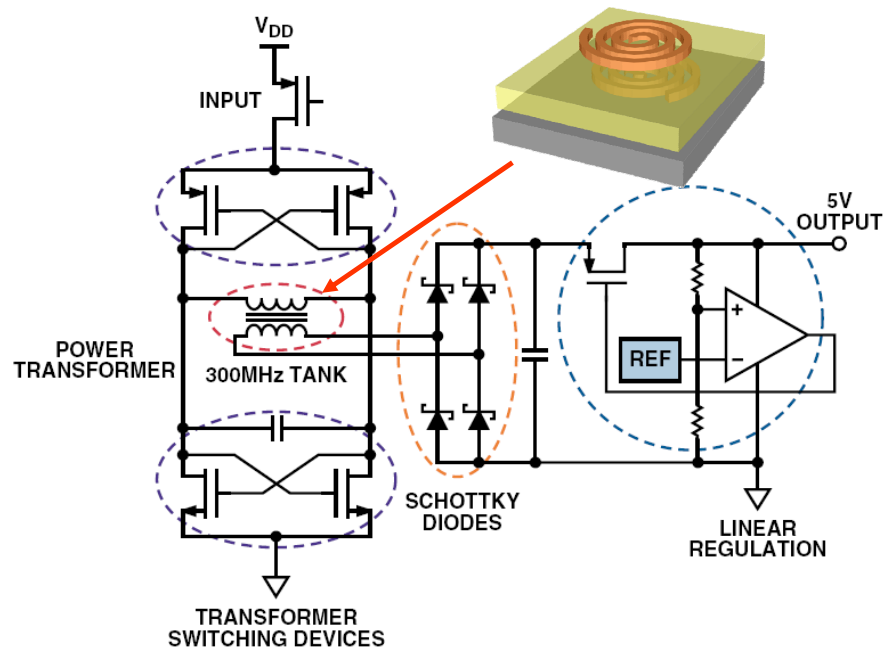
This figure shows the isolated power section of the ADuM5240, ADuM5241, and ADuM5242 the first *i*Coupler products with *iso*Power. Four cross-coupled CMOS switches generate an ac waveform that drives the transformer.

On the isolated side, Schottky diodes rectify the ac signal. The rectified signal is passed to a linear regulator, which maintains the output voltage at a nominal 5 V setpoint. The output is capable of supplying 10 mA of current.

The chip-scale microtransformers are made from 6 μm thick gold, separated by a 20 μm polyimide insulation layer, which is capable of providing greater than 5 kV rms isolation. Because the transformer coils, only 600 mm in diameter, have a low L/R ratio compared with conventional transformers, high-efficiency power generation requires high-frequency switching—on the order of 300 MHz.

As noted earlier, the transformers used to generate power employ the same process as those used to isolate data. The only significant difference between data and power channels is the conditioning circuitry on either side of the isolation barrier.

Isolated SPI Interface Using *i*Coupler Technology and Optocouplers

(A) *i*COUPLER SOLUTION — 72mm²

**(B) OPTOCOUPLER SOLUTION** — 363mm²
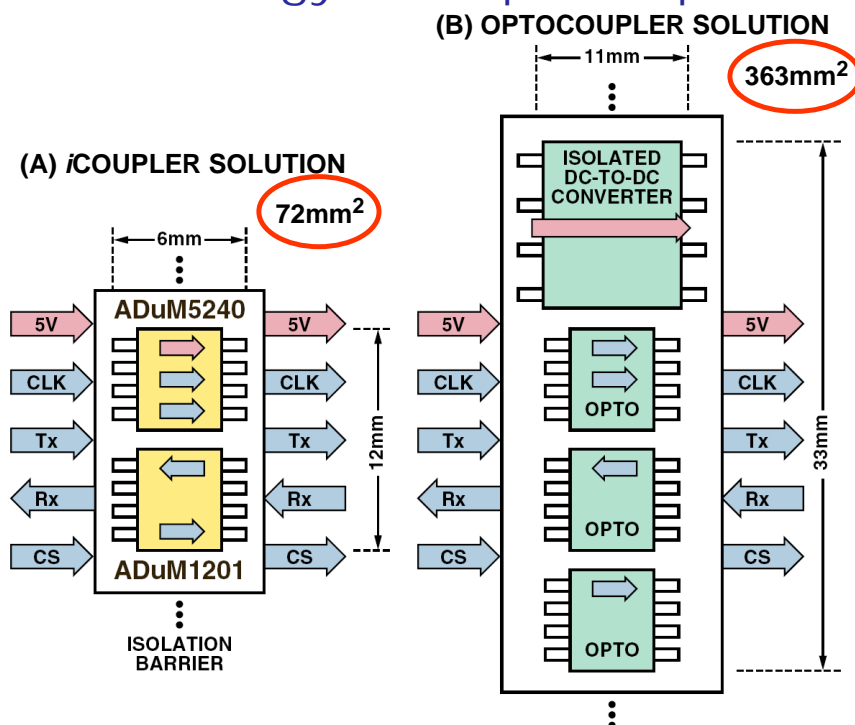
Combining data and power in a single, small, surface-mountable package, the ADuM524x family provides significant size and cost savings.

This figure shows typical physical configurations for isolated SPI interfaces. The *i*Coupler and *iso*Power solution (A) uses an ADuM5240 and an ADuM1201 to provide four channels of isolated data and up to 50 mW of isolated power, enough to power an ADC and a remote sensor. It is more compact and less expensive than the traditional approach using three optocouplers and an isolated dc-to-dc converter (B).

A third solution, using discrete transformers and other components, would consume even more area. Other combinations of ADuM524x *iso*Power and ADuM120x *i*Coupler products are possible, as are combinations of ADuM524x and most other *i*Coupler products.

Completely Isolated
Turbidity Sensor and ADC
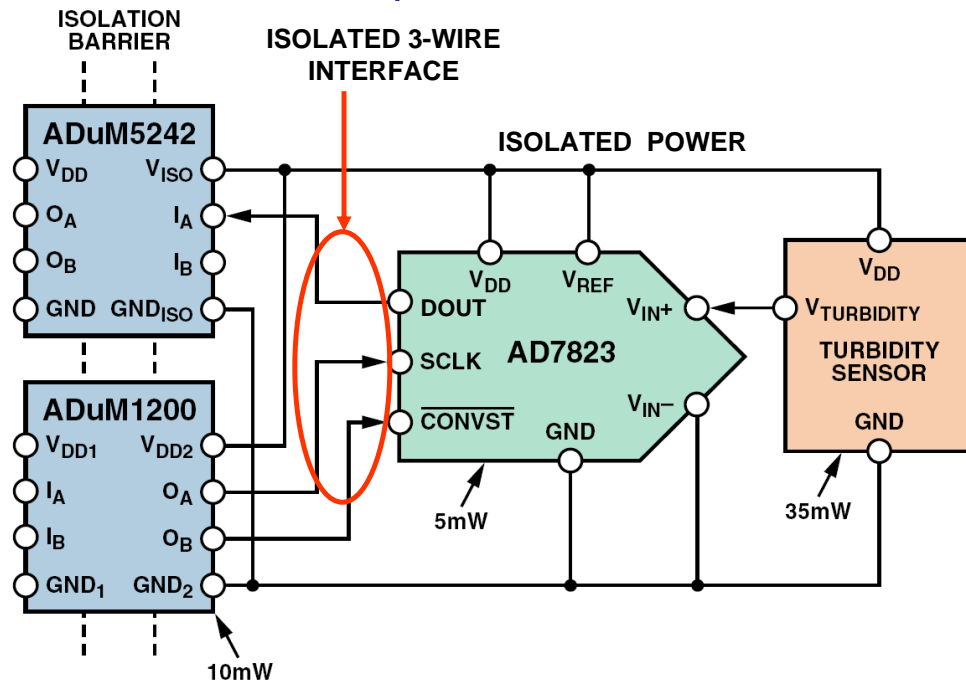
This figure shows a completely isolated turbidity sensor system that measures the amount of particulates in a liquid solution and can be used to determine the cleanliness of a volume of water. They are increasingly being used in home appliances, such as dishwashers and washing machines, both to conserve water and to improve cleaning performance. Conventional appliances wash or rinse for a set time, overestimating the required level of cleaning to ensure that the load is fully clean at the end of the cycle. A turbidity sensor, however, can let the system know when to stop cleaning. The machine will use the optimal amount of water for the optimal time, thus minimizing waste while maximizing useful cleaning performance.

Because turbidity sensors must be immersed in the water, they present two challenges to an appliance designer. First, the sensor must be small enough to fit unobtrusively anywhere within the space where clothes or dishes are to be placed. The size of the sensor is, therefore, critical. Second, the powered circuit is immersed in water, so the sensor must be safely isolated from the rest of the system. If the physical insulation should fail, the user and the system electronics must not be harmed, and there must be no possibility of fire. Both the power and the data must therefore be isolated.

This figure demonstrates a cost-effective solution. The AD7823 low-power 8-bit 200 kSPS SAR ADC uses a 3-wire interface to convert the analog output of a turbidity sensor. The digitized turbidity data is transmitted across the galvanic isolation barrier of the ADuM1200 and ADuM5242. The 50 mW of isolated power from the ADuM5242 is sufficient to supply the ADuM1200, the AD7823, and the turbidity sensor. The combined area of the isolators and converter is less than 100 mm², excluding external components.
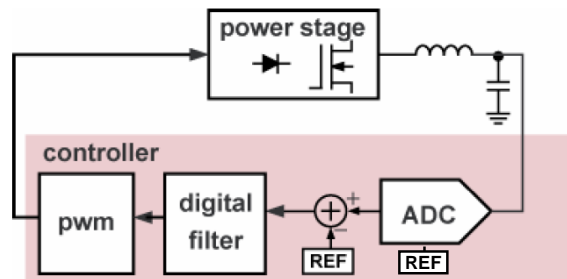
Digital Power Applications

Digital Power Management and Digital Power Control

◆ **Digital Power _Management_**
- **Voltage Monitoring**
- **Sequencing**
- **Margining**
- **Temperature Monitoring and Fan Control**
- **Supervision**
- **Communication via data bus (SMBus, I²C, PMBus)**

◆ **Digital Power _Control_**
- **Real-time control of a power converter using an ADC and digital techniques within a feedback loop**

We have seen how digital techniques are currently being used in voltage monitoring, sequencing, margining, temperature monitoring, fan control supervision, etc. These applications fall into the broad area loosely defined as digital power _management_. Although the results obtained through digital techniques (generally comparators or ADCs) may be used to control various system parameters, there is no real-time feedback loop in the classic sense of feedback control systems (operational amplifiers, servo systems, process control, etc.).

Digital power _control,_ on the other hand, refers specifically to the real-time control of a power converter (ac-to-dc or dc-to-dc) using an ADC and digital techniques (digital filter, for example) within a feedback loop as shown above. As is usually the case, the digital approach offers many advantages (neglecting the economic factor for the moment).

Currently most point-of-load switching converters use analog techniques to control output voltage. There is no technical reason why the digital techniques illustrated above can't be used. The slow migration to digital power control is mostly due to economic factors. The digital implementation is simply more costly using today's CMOS process technology.

Digital control is, however, beginning to appear in the high power primary-side ac-to-dc converters and in secondary-sided dc-to-dc converters, where the requirements and economics make digital control an attractive alternative to traditional analog techniques.

As digital processes continue to shrink (analog processes do too, but not as rapidly), digital control will eventually progress further downstream in the power chain.

Digital Control Loop Features

- ◆ **Integration of all typical controller functions**
  - ● **Remote and local voltage sense**
  - ● **Both primary and secondary side current sense**
  - ● **PWM control**
  - ● **Synchronous Rectifier control**
  - ● **Digital or Analog Current Share Bus**
- ◆ **Digital Control Loop**
  - ● **Integrated filter**
  - ● **Filter can be adapted through software**
    - ◆ **Easier to maintain phase margin with voltage-mode controllers**
    - ◆ **Faster development time**
    - ◆ **Faster debugging**
    - ◆ **Option to compensate for temperature**
  - ● **Programmability through I²C**
- ◆ **Digital control currently used in AC-to-DC primary-side converters and DC-to-DC secondary-side converters**

ADC technology in CMOS has progressed rapidly. The requirement for ADCs in digital power control is approximately 12 bits at sampling rates of a few MHz. This will obviously change due to product improvements, but represents the current requirement in primary and secondary-side power converters.

Other than increased reliability, functionality, power density, efficiency, reduced component count, etc., digital control offers design flexibility in the feedback control loop compensation. Current point-of-load supplies designed for powering high power microprocessors (such as Intel and AMD) are often manually adjusted on the system board for optimum load current step response. Digital adaptive feedback loop control and timing should eliminate this need.

Most analog switching converters use voltage-mode (VM), current-mode (CM), or a combination of the two in order to determine the value of feedback compensation values. Proper compensation of the feedback loop in order to maintain adequate phase margin in both the continuous conduction mode (CCM) and discontinuous conduction mode (DCM) is somewhat complicated. This is especially difficult when using only voltage-mode control. In a digital feedback control loop, the compensation is performed by digital filters whose characteristics can be easily changed depending on the mode of operation. This means that VM control is practical using adaptive digital filter techniques.

Typical Application of ADP1043 Secondary-Side Controller
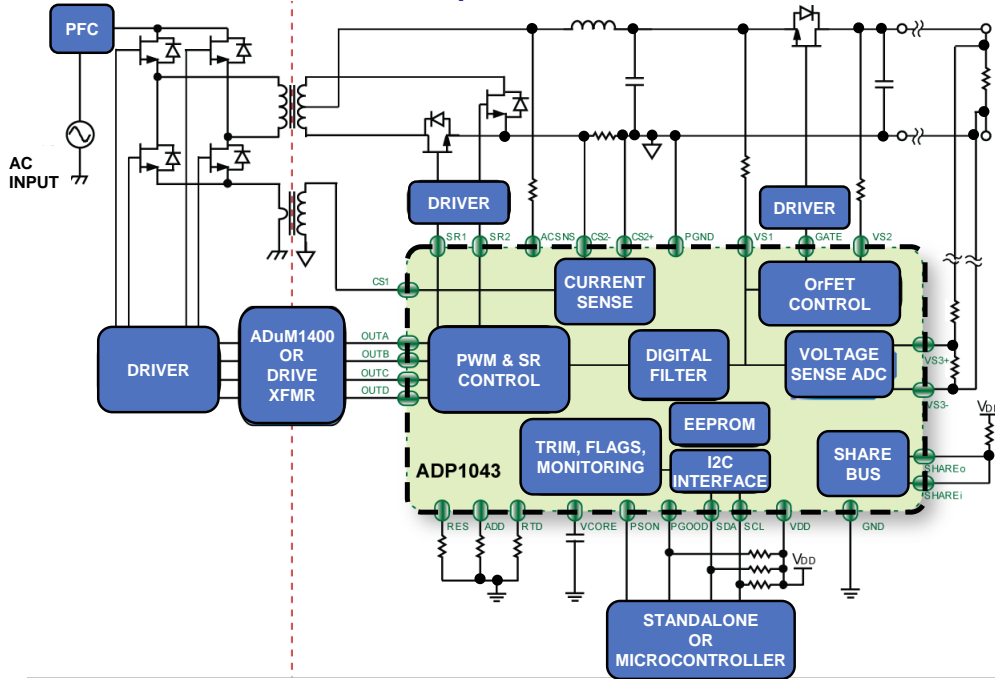
The ADP1043 is a secondary side digital power supply controller IC that is designed to provide all the functions that are typically needed in an isolated ac-to-dc or dc-to-dc control application. It is optimized for minimal component count, maximum flexibility, and minimum design time. Features include remote voltage sense, local voltage sense, primary and secondary side current sense, PWM control, synchronous rectifier control, and hot-swap sense and control. The control loop is digital, with an integrated programmable digital filter. Protection features include current limiting, ac sense, UVLO, and OVP (Overvoltage Protection).

The OrFET control feature allows multiple supplies to be connected in parallel.

The part supports current sharing and has an integrated programmable loop filter with an I²C interface. There is extensive on-chip fault detection and protection.

Fast calibration can be achieved using the on-chip 8 kB EEPROM, or and external microcontroller.

It should be noted that the ADM1041A secondary side controller uses traditional analog techniques.

Programmability and Monitoring (Through I^{2}C)

PROGRAMMABILITY

- ◆ **Output Voltage Setting**
- ◆ **Overcurrent (OCP) limit**
- ◆ **Overvoltage (OVP) limit**
- ◆ **Undervoltage (UVP) limit**
- ◆ **Overtemperature (OTP) limit**
- ◆ **Soft-Start & Soft-Stop timing**
- ◆ **Loop filter poles and gains**
- ◆ **PWM timing**
- ◆ **Duty cycle limits**
- ◆ **OrFET On/Off trip voltage**

MONITORING

- ◆ **Output current**
- ◆ **Output voltage**
- ◆ **Output Line Impedance**
- ◆ **Input current**
- ◆ **Output power**
- ◆ **Duty cycle**
- ◆ **Current share bus**
- ◆ **Temperature**

The use of the I^{2}C bus provides both programmability and monitoring functions. This figure lists some of the various functions included by each.

Powering
Portable Systems

Portable Power Considerations

◆ **Battery technology**
- ● **Lithium Ion battery of choice**
- ● **NiMH and NiCd being phased out**

◆ **Maximize battery life!**
- ● **Sleep and low power modes**
- ● **Need efficient, small, low cost buck, boost, and buck-boost regulators as well as LDOs**

◆ **Digital cameras, cell phones, PDAs, etc. require custom-tailored solutions**

Modern portable systems depend highly on battery technology and efficient power management techniques. Maximizing battery life is a prime concern of portable equipment manufacturers.

Average power reduction techniques such as sleep, standby, or idle modes are required as well as efficient, small, low cost regulators.

Buck, boost, and buck-boost switching regulators as well as LDOs must be carefully integrated into the power chain of a portable system. In many cases, a custom-tailored power management IC is required for the specific application.

The Energy System:
Lithium Ion (Li-Ion)
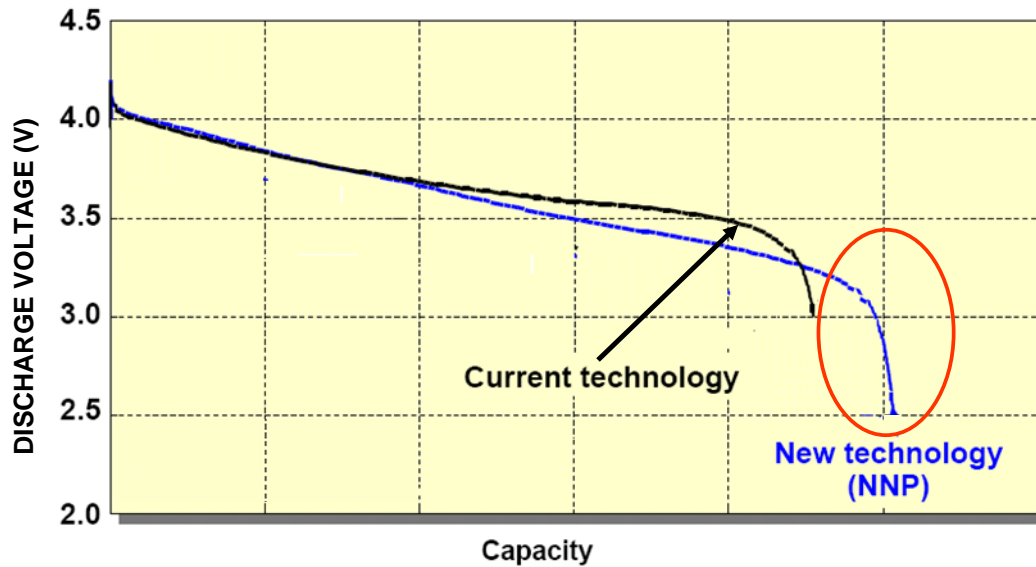
NNP = <u>N</u>ickel-Based <u>N</u>ew <u>P</u>latform, Matsushita Battery Industrial Co., LTD

By far the most popular battery technology for today's portable systems is Lithium-Ion (Li-Ion). The discharge curve is shown here. New technology (NNP) extends the capacity of the battery and is available. "NNP" is an abbreviation for <u>N</u>ickel-Based <u>N</u>ew <u>P</u>latform Lithium-ion technology from Matsushita Battery Industrial Co., LTD. Work is on-going to produce even greater capacity in Li-Ion batteries.

The discharge curve shown here indicates that the usable battery voltage for current technology Li-Ion extends from 4.2V (fully charged) to 3.0 V (discharged). This means that the portable system power supply must provide the necessary output voltages over this fairly wide input voltage range. If the electronics require a 3.3 V supply, then it is clear that a buck-boost regulator is needed as the input voltage discharges from 4.2 V to 3.0 V.
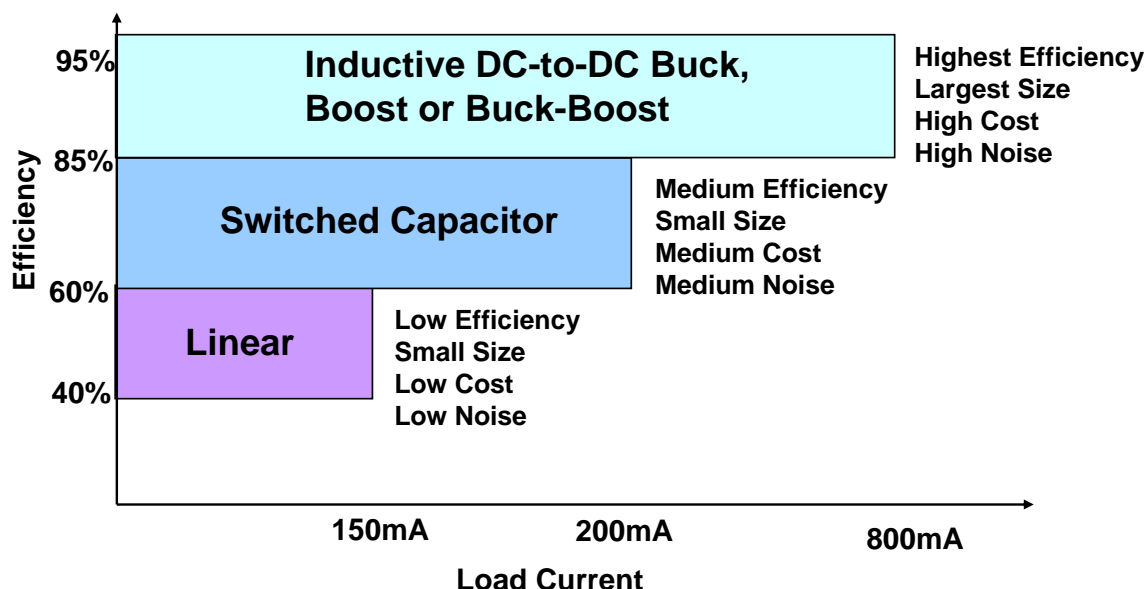
The new Li-Ion technology discharges to 2.5 V, thereby lowering the usable battery voltage and increasing the probability of needing a buck-boost regulator.

Techniques for Portable Power

Typical Conditions:
◆ V_{IN} = Li-Ion Battery = 3.0 V (2.5 V, NNP) to 4.2 V
◆ V_{OUT} = 1.8 V

There are three popular techniques for supplying portable power systems. The following guidelines apply specifically to a system powered by a single Li-Ion battery where the voltage ranges from 4.2 V to 3.0 V (2.5 V for NNP technology), and the output voltage is approximately 1.8 V.
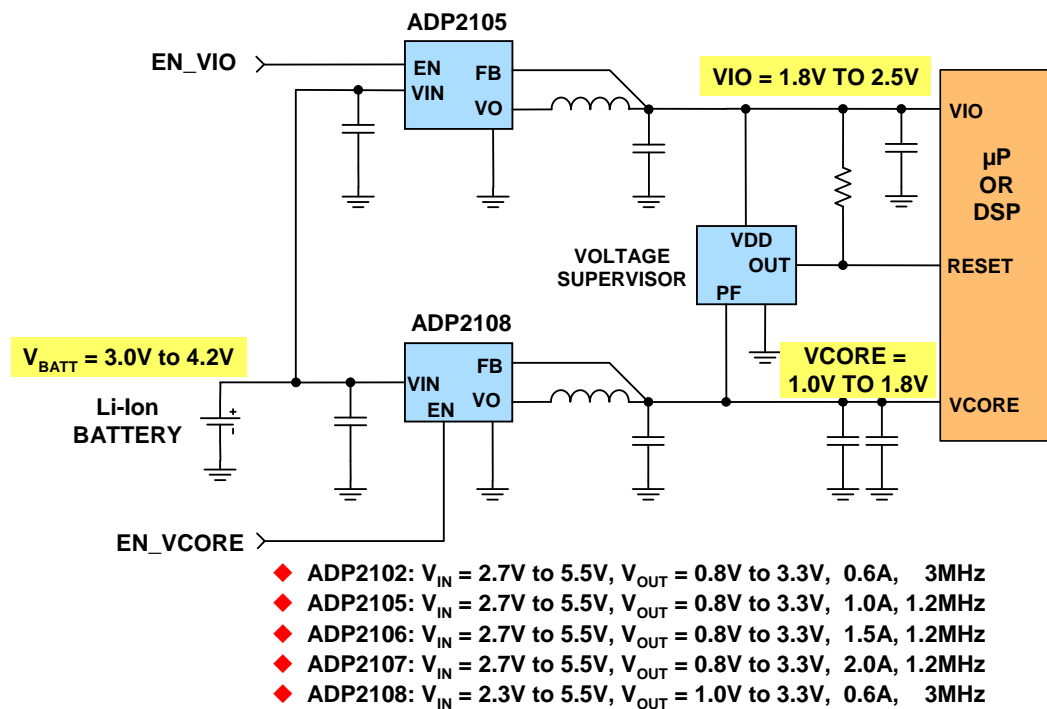
The inductive dc-to-dc buck, boost, or buck-boost regulator is the most efficient for higher currents, but takes up the most space and is generally the most costly of the three. Also the noise is the greatest.

The switched capacitor ("inductorless") regulator has medium efficiency, smaller size, lower cost, and less noise than the inductive regulators. However, the current capability is limited to approximately 200 mA.

The linear regulator (almost always an LDO) is by far the easiest to apply, the smallest, and has the lowest cost and noise of the three types. The efficiency of the LDO is approximately V_{OUT}/V_{IN}, so making general statements about their usage is somewhat dangerous. In applications where the $V_{IN} - V_{OUT}$ voltage is low, the LDO may be an ideal choice if the current requirement is relatively low.

We will now look at a few typical applications in portable systems and see how efficient use can be made of the available power management building blocks.

Processor Power Distribution with Separate Core and I/O Voltage

- ADP2102: V_{IN} = 2.7V to 5.5V, V_{OUT} = 0.8V to 3.3V, 0.6A, 3MHz
- ADP2105: V_{IN} = 2.7V to 5.5V, V_{OUT} = 0.8V to 3.3V, 1.0A, 1.2MHz
- ADP2106: V_{IN} = 2.7V to 5.5V, V_{OUT} = 0.8V to 3.3V, 1.5A, 1.2MHz
- ADP2107: V_{IN} = 2.7V to 5.5V, V_{OUT} = 0.8V to 3.3V, 2.0A, 1.2MHz
- ADP2108: V_{IN} = 2.3V to 5.5V, V_{OUT} = 1.0V to 3.3V, 0.6A, 3MHz
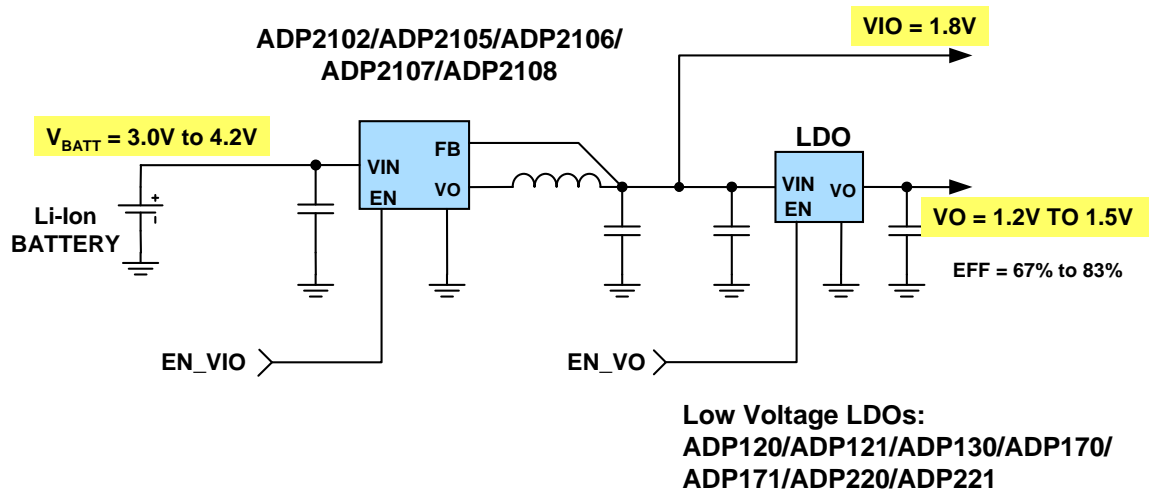
A common example in portable systems is generating the power for a microprocessor or DSP from a single Li-ion battery. As in "fixed" power applications, most modern microprocessors and DSPs for portable systems require a separate I/O and core voltage.

In this application, the ADP2105 synchronous buck regulator generates the I/O voltage which can be between 1.8 V and 2.5 V depending on the processor. The maximum current output is 1 A. The ADP2108 would also work if the current requirement is less than 600 mA.

The 1.0 V to 1.8 V core voltage is supplied by the ADP2108 synchronous buck regulator which can handle up to 600 mA.

Typical Application Using a Switching Regulator and an LDO in Cascade

ADP2102/ADP2105/ADP2106/
ADP2107/ADP2108

VIO = 1.8V

V$_{BATT}$ = 3.0V to 4.2V

LDO

VIN FB
EN VO

Li-Ion
BATTERY

VIN VO
EN

VO = 1.2V TO 1.5V

EFF = 67% to 83%

EN_VIO

EN_VO

Low Voltage LDOs:
ADP120/ADP121/ADP130/ADP170/
ADP171/ADP220/ADP221

In the case where $V_{IN} - V_{OUT}$ and the load current are both small, LDOs offer a simple, low cost, low noise regulator solution.
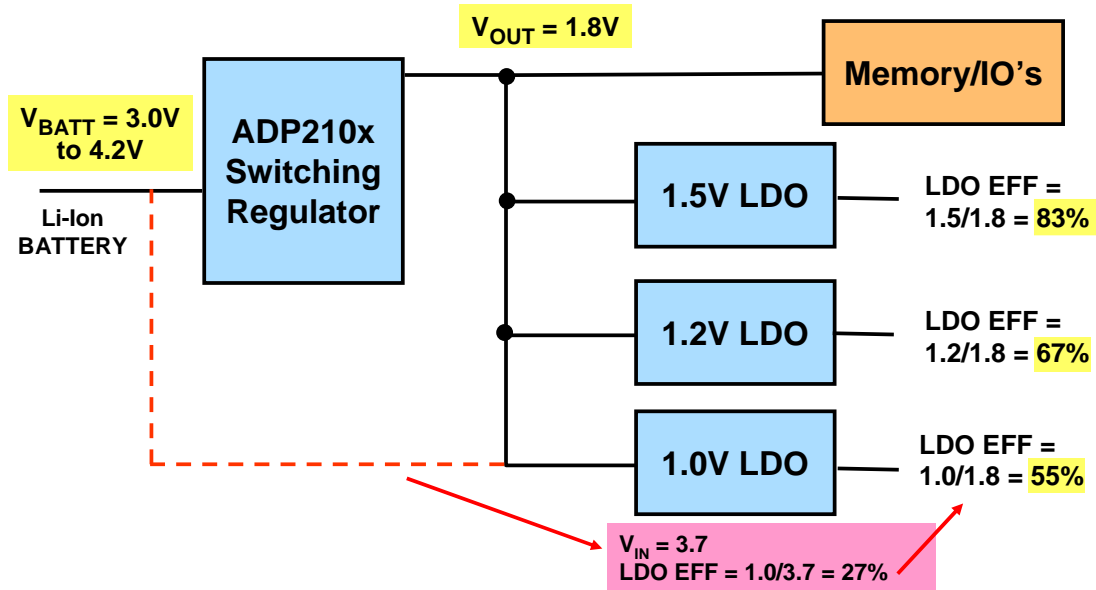
In this example, the LDO is in cascade with the 1.8 V switching regulator output. The LDO efficiency (V_{OUT}/V_{IN}) ranges from 67% to 83% for output voltages between 1.2 V and 1.5 V.

Point-of-Use Regulation Using LDOs with Low V_{IN} – V_{OUT}

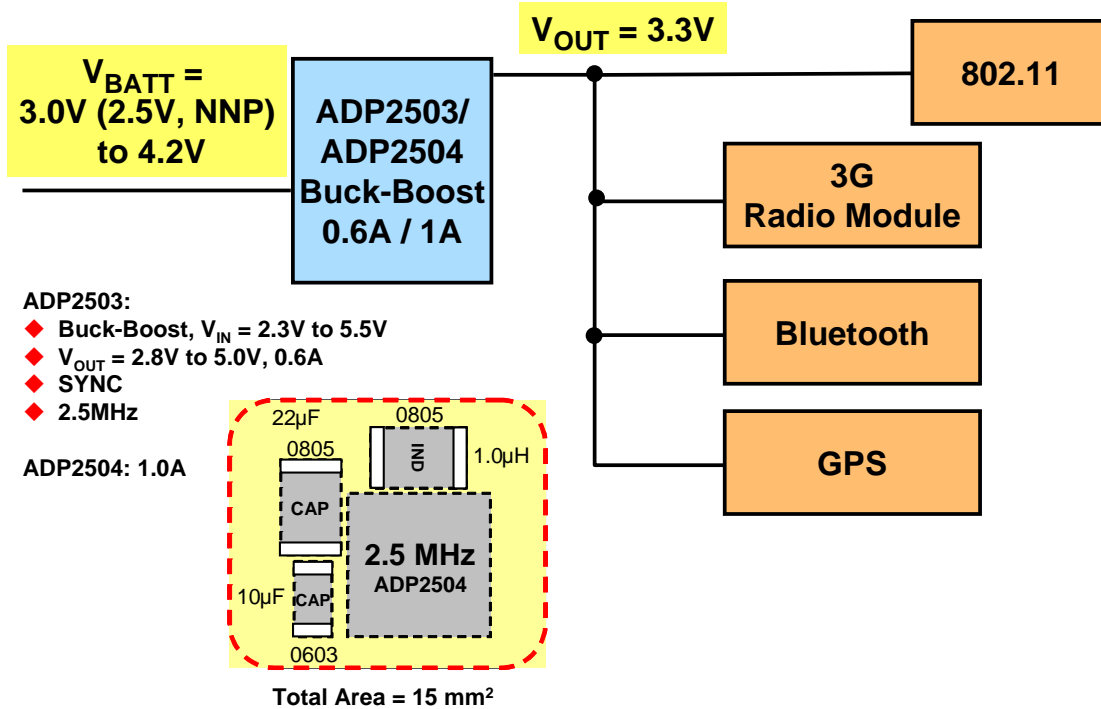**Efficiency improves from
27-40% to 55-83% by Operating LDOs on 1.8V
Low Voltage LDOs: ADP120/ADP121/ADP130/ADP170/ADP171/ADP220/ADP221**

V_{OUT} = 1.8V

Memory/IO's

V_{BATT} = 3.0V to 4.2V

ADP210x Switching Regulator

Li-Ion BATTERY

1.5V LDO — LDO EFF = 1.5/1.8 = **83%**

1.2V LDO — LDO EFF = 1.2/1.8 = **67%**

1.0V LDO — LDO EFF = 1.0/1.8 = **55%**

V_{IN} = 3.7
LDO EFF = 1.0/3.7 = 27%

In this application, LDOs are driven from the ADP210x switching regulator 1.8 V output and provide efficiencies between 55% and 83% for output voltages between 1.0 V and 1.5 V.

Without the intermediate bus voltage of 1.8 V, the 1.0 V LDO efficiency drops to 27% if driven directly from the Li-Ion battery with a nominal voltage of 3.7 V.

Buck-Boost Regulators Often Needed for Low Voltage Batteries

V$_{OUT}$ = 3.3V

V$_{BATT}$ = 3.0V (2.5V, NNP) to 4.2V

ADP2503/ ADP2504 Buck-Boost 0.6A / 1A

802.11

3G Radio Module

Bluetooth

GPS

ADP2503:
- Buck-Boost, V$_{IN}$ = 2.3V to 5.5V
- V$_{OUT}$ = 2.8V to 5.0V, 0.6A
- SYNC
- 2.5MHz

ADP2504: 1.0A

22µF 0805
0805
CAP
10µF CAP
0603
IND 1.0µH
2.5 MHz ADP2504

Total Area = 15 mm²

A common problem in portable systems is providing a switching regulator output when the input voltage from a discharging battery drops below the output voltage.

In this application, the switching regulator must supply a constant 3.3 V output as the input battery voltage discharges from 4.2 V to 2.5 V. This requires a switching regulator that can switch from the buck mode to the boost mode (buck-boost) while maintaining output regulation. The ADP2503 and ADP2504 are examples of buck-boost regulators that can supply 0.6 A and 1 A output currents, respectively, for input voltages from 2.3 V to 5.5 V.

Because of the high switching frequency of 2.5 MHz, small components can be used as shown to yield a solution that occupies only 15 mm² as shown in the figure, which uses a 1 µH ceramic inductor in an 0805 package.

Integrated Camera Module Solution
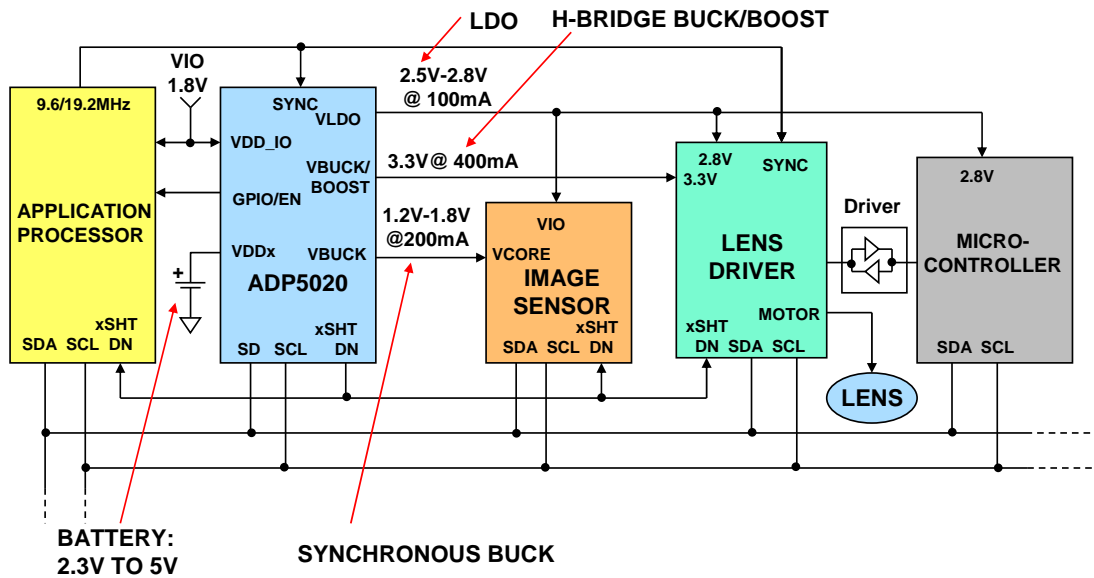
This figure shows an integrated power solution for a camera module. The ADP5020 controller provides the following outputs:

1. 3.3 V, 400 mA buck-boost output based on an H-bridge FET controller.

2. 1.2 V to 1.8 V buck output capable of 200 mA for core voltage.
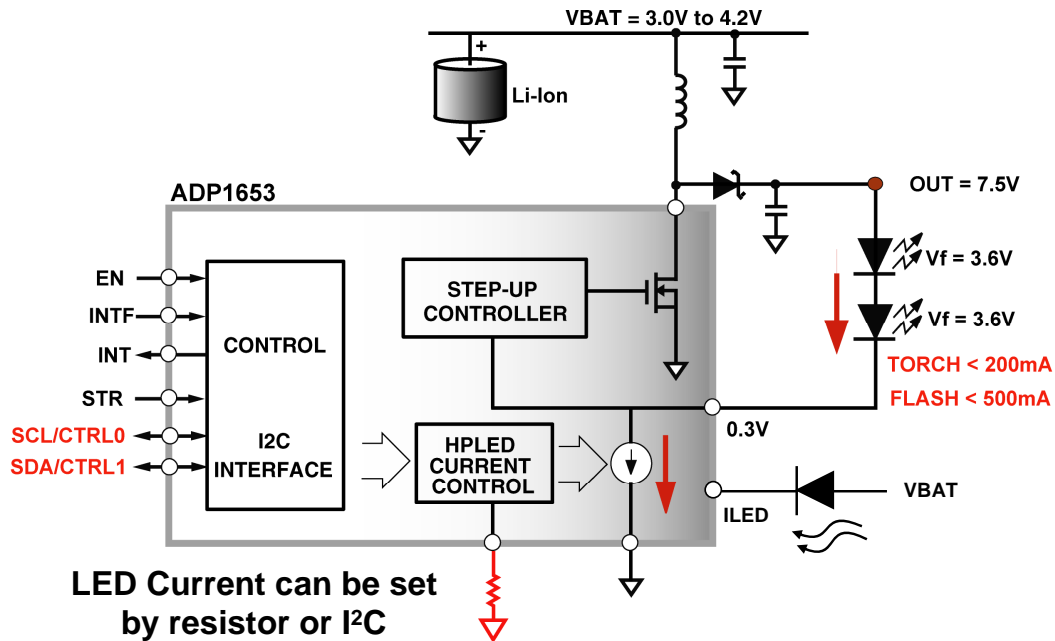
3. 2.5 V to 2.8 V 100 mA LDO output.

The device operates on an input voltage range of 2.3 V to 5.0 V, thereby covering all popular battery types.

The internal switching frequency of the regulators is 3 MHz.

The digital interface is I²C.

The figure shows the interface of the ADP5020 with the application process, image sensor, lens driver, and microcontroller.

2.71

ADP1653 Flash LED Driver Requires Boost Regulator

VBAT = 3.0V to 4.2V

Li-Ion

ADP1653

OUT = 7.5V

EN

INTF

INT

STR

SCL/CTRL0

SDA/CTRL1

CONTROL

STEP-UP CONTROLLER

I2C INTERFACE

HPLED CURRENT CONTROL

Vf = 3.6V

Vf = 3.6V

TORCH < 200mA

FLASH < 500mA

0.3V

ILED

VBAT

LED Current can be set by resistor or I²C

An excellent example of a boost regulator application is in a flash LED driver. The system typically operates on a single Li-ion battery (3.0 V to 4.2 V), but at least 7.5 V is required for the diode bias voltage. Flash systems generally use two LEDs in series, so the total voltage drop across the two diodes in the flash mode is $3.6 \times 2 = 7.2$ V. The current source shown in the figure needs a headroom of 0.3 V, so the total diode bias voltage required is 7.5 V. This voltage is generated by the ADP1653 boost regulator. The LED current can be set by a resistor or programmed using the I²C interface.

The ADP1653 is a very compact, high efficiency, high power, camera-flash LED driver optimized for cellular phones. The device's high efficiency and dynamic LED current control improve flash brightness and picture quality in dimly lit environments. Efficiency peaks at 92% and is higher than charge pump solutions over the Li-ion battery range.

The device has a dual-mode interface that is configurable to 2-bit logic or an I²C interface. The indicator LED and high power LED currents are programmable with external resistors or through the I²C interface. To maximize overall flash brightness, the ADP1653 offers an input to reduce flash LED current in less than 50 μs, referred to as the Tx mask. Tx masking reduces battery stress by scaling back flash LED current during an RF transmission.

The ADP1653 solution requires only four external components in I²C mode and fits in a 6.4 mm × 7.2 mm space. The part integrates multiple safety features such as soft start, flash timeout, output current limit, thermal protection, and overvoltage protection.

Basic Switched Capacitor Voltage Inverter and Voltage Doubler
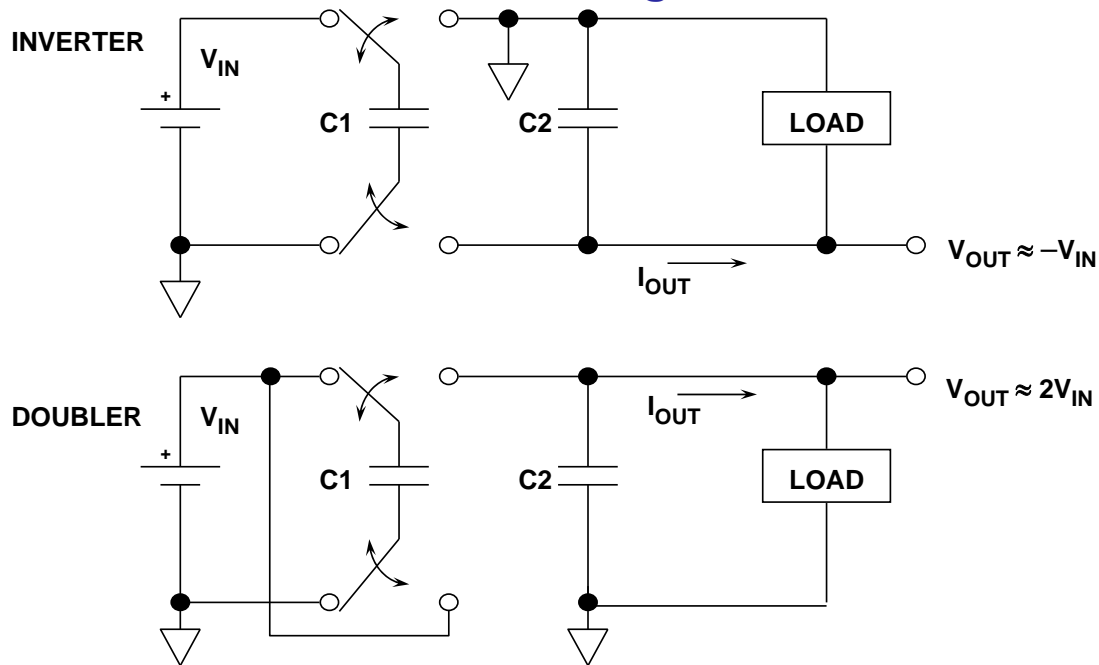

We have seen how inductors can be used to transfer energy and perform voltage conversions. This section examines switched capacitor voltage converters which accomplish energy transfer and voltage conversion using capacitors.

The two most common switched capacitor voltage converters are the voltage inverter and the voltage doubler circuit shown in the figure. In the voltage inverter, the charge pump capacitor, C1, is charged to the input voltage during the first half of the switching cycle. During the second half of the switching cycle, its voltage is inverted and applied to capacitor C2 and the load. The output voltage is the negative of the input voltage, and the average input current is approximately equal to the output current. The switching frequency impacts the size of the external capacitors required, and higher switching frequencies allow the use of smaller capacitors. The duty cycle—defined as the ratio of charging time for C1 to the entire switching cycle time—is usually 50%, because that generally yields the optimal charge transfer efficiency.

After initial start-up transient conditions and when a steady-state condition is reached, the charge pump capacitor only has to supply a small amount of charge to the output capacitor on each switching cycle. The amount of charge transferred depends upon the load current and the switching frequency. During the time the pump capacitor is charged by the input voltage, the output capacitor C2 must supply the load current. The load current flowing out of C2 causes a droop in the output voltage which corresponds to a component of output voltage ripple. Higher switching frequencies allow smaller capacitors for the same amount of droop. There are, however, practical limitations on the switching speeds and switching losses, and switching frequencies are generally limited to a few hundred kHz.

The voltage doubler works similarly to the inverter; however, the pump capacitor is placed in series with the input voltage during its discharge cycle, thereby accomplishing the voltage doubling function. In the voltage doubler, the average input current is approximately twice the average output current.

ADP3605 120mA Switched Capacitor Inverter with Regulated Output
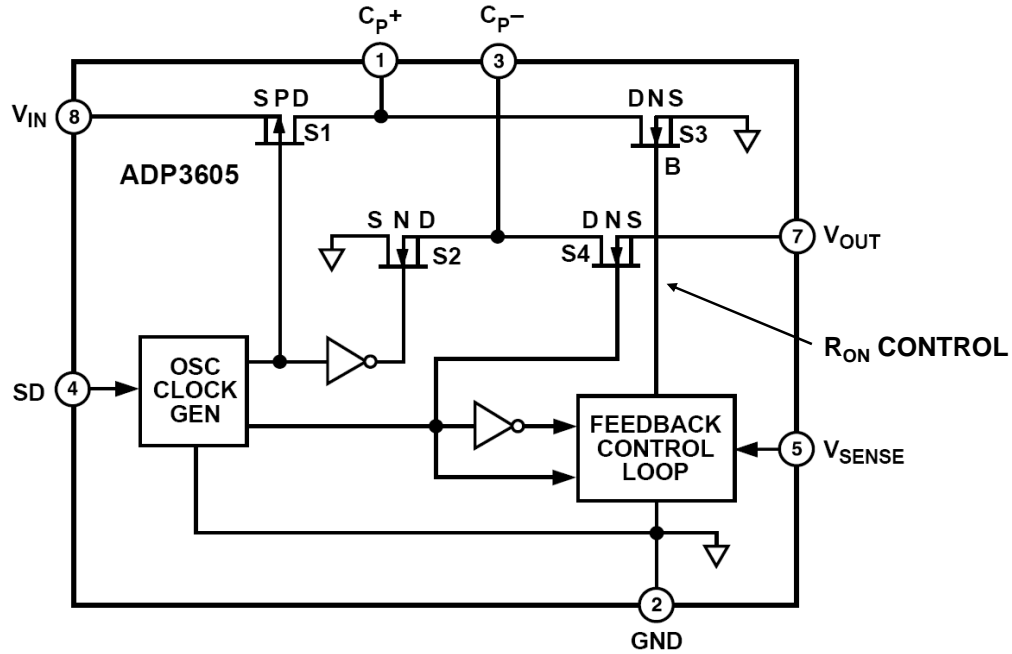
By far the simplest and most effective method for achieving regulation in a switched capacitor voltage converter is to use an error amplifier to control the on-resistance of one of the switches as shown in this figure, a block diagram of the ADP3605 120 mA voltage inverter. This device offers a regulated –3 V output for an input voltage of +3 V to +6 V. The output is sensed and fed back into the device via the V_{SENSE} pin. Output regulation is accomplished by varying the on-resistance of one of the MOSFET switches as shown by the control signal labeled "R_{ON} CONTROL" in the diagram. This signal accomplishes the switching of the MOSFET as well as controlling the on-resistance.

ADM8845 Charge Pump Driver
for LCD Displays with White LED Backlights
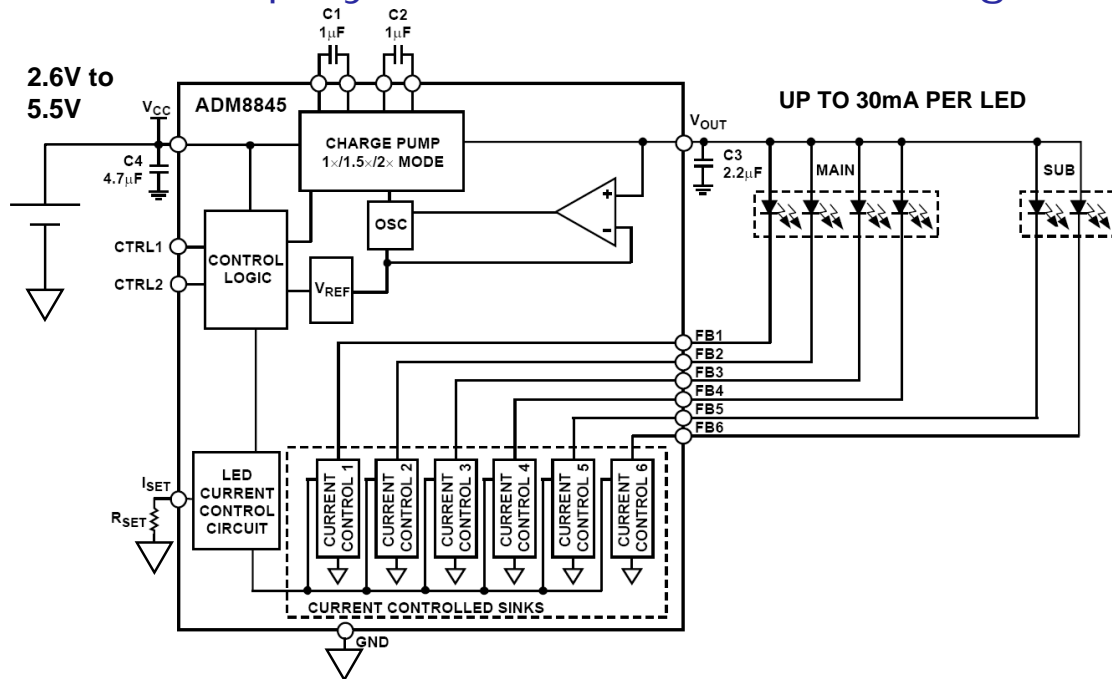
The ADM8845 uses charge pump technology to provide the power required to drive up to six LEDs. The LEDs are used for backlighting a color LCD display, having regulated constant current for uniform brightness intensity. The main display can have up to four LEDs, and the sub display can have one or two LEDs. The digital CTRL1 and CTRL2 input control pins control the shutdown operation and the brightness of the main and sub displays.

To maximize power efficiency, the charge pump can operate in a 1×, 1.5×, or 2× mode. The charge pump automatically switches between 1×, 1.5×, and 2× modes, based on the input voltage, to maintain sufficient drive for the LED anodes at the highest power efficiency.

Improved brightness matching of the LEDs is achieved by a feedback pin to sense individual LED current with a maximum matching accuracy of 1%.

Technical References

Analog Devices' Technical References

1. Hank Zumbahlen, *Basic Linear Design*, Analog Devices, 2006, ISBN: 0-915550-28-1. Also available as *Linear Circuit Design Handbook*, Elsevier-Newnes, 2008, ISBN-10: 0750687037, ISBN-13: 978-0750687034. See Chapter 9.

2. Walt Kester, *Analog-Digital Conversion*, Analog Devices, 2004, ISBN: 0916550273. Also available as *Data Conversion Handbook*, Elsevier-Newnes, 2005, ISBN: 0750678410. See Chapter 7.

3. Walt Jung, *Op Amp Applications*, Analog Devices, 2002, ISBN: 0-916550-26-5. Also available as *Op Amp Applications Handbook*, Elsevier-Newnes, 2004, ISBN: 0-7506-7844-5. See Chapter 7.

4. Sridhar Gurram, Oliver Brennan, Tim Wilkerson, "DC-to-DC Switching-Regulator Insights—Achieving Longer Battery Life in DSP Systems," *Analog Dialogue* 41-12, December 2007.