

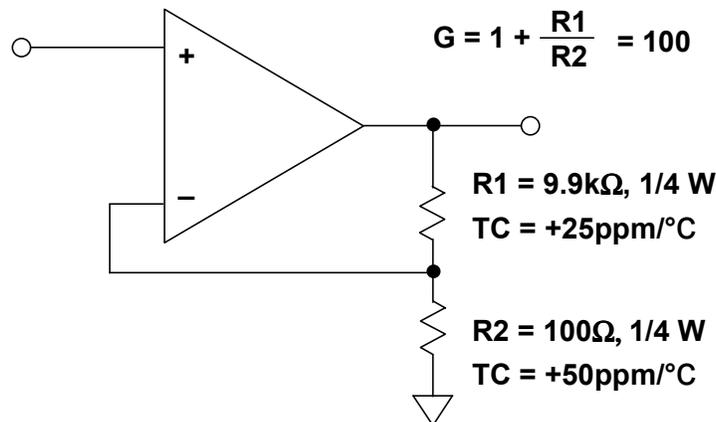
SECTION 10 HARDWARE DESIGN TECHNIQUES *Walt Kester*

RESISTOR AND THERMOCOUPLE ERRORS IN HIGH ACCURACY SYSTEMS

Walt Kester, Walt Jung, and James Bryant

Resistor accuracy is crucial in precision systems. The circuit element called a *resistor* should not be taken for granted! Figure 10.1 shows a simple non-inverting op amp where the gain of 100 is set by the external resistors R1 and R2. The temperature coefficients of the two resistors are a somewhat obvious source of error. Assume that the op amp gain errors are negligible, and that the resistors are perfectly matched at +25°C. If the temperature coefficients of the resistors differ by only 25ppm/°C, the gain of the amplifier will change by 250ppm for a 10°C temperature change. This is about 1 LSB in a 12-bit system, and a major disaster in a 16-bit system.

RESISTOR TEMPERATURE COEFFICIENT MISMATCHES CAUSE GAIN VARIATION WITH TEMPERATURE



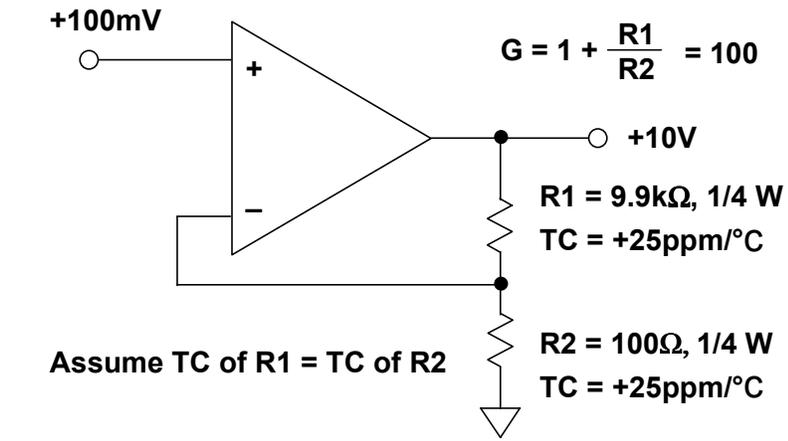
- Temperature change of 10°C causes gain change of 250ppm
- This is 1LSB in a 12-bit system and a disaster in a 16-bit system

Figure 10.1

Even if the temperature coefficients are identical, there still may be significant errors. Suppose R1 and R2 have identical temperature coefficients of +25ppm/°C and are both ¼W resistors. If the signal input in Figure 10.2 is zero, the resistors will dissipate no heat, but if it is 100mV there will be 9.9V across R1 which will dissipate 9.9mW and experience a temperature rise of 1.24°C (the thermal resistance of a ¼W resistor is 125°C/W). The 1.24°C rise causes a resistance change

of 31ppm, and a corresponding change in gain. R2, with only 100mV across it, is only heated 0.0125°C, which is negligible. The 31ppm gain error represents a fullscale error of ½ LSB at 14-bits, and is a disaster for a 16-bit system.

RESISTOR SELF-HEATING EVEN IN MATCHED RESISTORS CAN CAUSE GAIN VARIATION WITH INPUT LEVEL



- R1, R2 Thermal Resistance = 125°C / W
- Temperature of R1 will rise by 1.24°C, P_D = 9.9mW
- Temperature rise of R2 is negligible, P_D = 0.1mW
- Gain is altered by 31ppm, or 1/2 LSB @ 14-bits

Figure 10.2

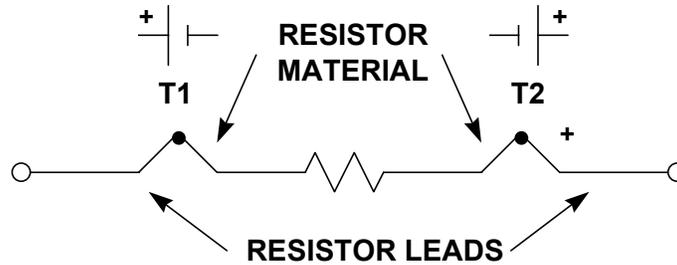
These, and similar errors, are avoided by selecting critical resistors that are accurately matched for both value and temperature coefficient, and ensuring tight thermal coupling between resistors whose matching is important. This is best achieved by using a resistor network on a single substrate - such a network may be within an IC or may be a separately packaged thin-film resistor network.

Another more subtle problem with resistors is the thermocouple effect, sometimes referred to as thermal EMF. Wherever there is a junction between two different conductors there is a thermoelectric voltage. If two junctions are present in a circuit, we have a thermocouple, and if these two junctions are at different temperatures, there will be a net voltage in the circuit. This effect is used to measure temperature, but is a potential source of inaccuracy in low level circuits, since wherever two different conductors meet, we have a thermocouple, whether we like it or not. This will cause errors if the various junctions are at different temperatures. The effect is hard to avoid, even if we are only making connections with copper wire, since a copper-to-copper junction formed by copper wire from two different manufacturers may have a thermoelectric voltage of up to 0.2µV/°C.

Consider the resistor model shown in Figure 10.3. The connections between the resistor material and the leads form two thermocouple junctions. The thermocouple EMF can be as high as 400µV/°C for carbon composition resistors and as low as

0.05 $\mu\text{V}/^\circ\text{C}$ for specially constructed resistors (Reference 1). Metal film resistors (RN-types) are typically about 20 $\mu\text{V}/^\circ\text{C}$.

RESISTORS CONTAIN THERMOCOUPLES



TYPICAL RESISTOR THERMOCOUPLE EMFs

■ CARBON COMPOSITION	$\approx 400 \mu\text{V}/^\circ\text{C}$
■ METAL FILM	$\approx 20 \mu\text{V}/^\circ\text{C}$
■ EVENOHM OR MANGANIN WIREWOUND	$\approx 2 \mu\text{V}/^\circ\text{C}$
■ RCD Components HP-Series	$\approx 0.05 \mu\text{V}/^\circ\text{C}$

Figure 10.3

These thermocouple effects are unimportant at AC or where the resistor is at a uniform temperature, but if the dissipation in a resistor, or its orientation with respect to heat sources, can cause one of its ends to be warmer than the other, then there will be a net thermocouple voltage differential, which will introduce a DC error into the circuit. For instance, using ordinary metal film resistors, a temperature differential of 1 $^\circ\text{C}$ will cause a thermocouple voltage of 20 μV which is quite significant when compared to the input offset voltage of truly precision op amps such as the OP177 or the AD707, and extremely significant when compared to chopper-stabilized op amps.

Figure 10.4 shows how resistor orientation can make a difference in the net thermocouple voltage. Standing the resistor on end in order to conserve board space will invariably cause a temperature gradient across the resistor, especially if it is dissipating any significant power. Placing the resistor flat on the PC board will eliminate this problem unless there is airflow across the resistor parallel to its axis. Orienting the resistor axis perpendicular to the airflow will minimize the error, since this tends to force the resistor ends towards the same temperature.

Figure 10.5 shows how to orient the resistor on a vertically mounted PC board, where the convection cooling air currents flow up the board. Again, the thermal axis of the resistor should be perpendicular to the convection flow to minimize the effect.

Because of their small size, the thermocouple effect in surface mount resistors is generally less than leaded types because of the tighter thermal coupling between the ends of the resistor.

AVOIDING THERMAL GRADIENTS MINIMIZES THERMOCOUPLE ERROR VOLTAGES

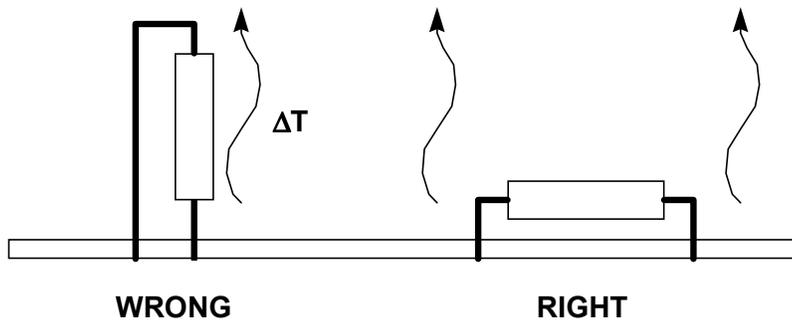


Figure 10.4

PROPER ORIENTATION OF SURFACE MOUNT RESISTORS MINIMIZES THERMOCOUPLE ERROR VOLTAGE

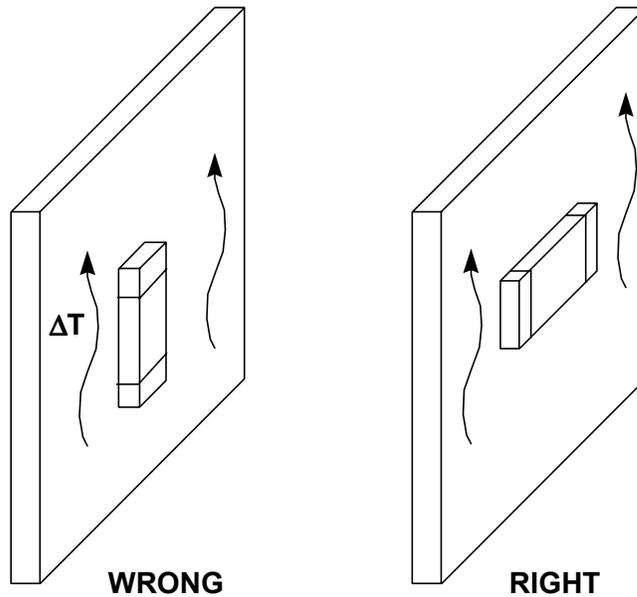


Figure 10.5

A simple circuit shown in Figure 10.6 will further illustrate the parasitic thermocouple problem. Here, we have a remote bridge driving an instrumentation amplifier which has current limiting resistors in each lead. Each resistor has four thermocouples: two are internal to the resistor, and two are formed where the resistor leads connect to the copper wires. Another pair of thermocouples is formed where the copper wire connects to the Kovar pins of the in-amp. The Copper/Kovar junction has a thermocouple voltage of about $35\mu\text{V}/^\circ\text{C}$. Most molded plastic ICs use copper leadframes which would be an order of magnitude or so less (e.g., the AD620 in-amp).

In addition, the copper wire has a resistance temperature coefficient (TC of 30 gage copper wire is approximately $0.385\%/^\circ\text{C}$) which can introduce error if the temperature of the wires is significantly different, or if they are different lengths. In this example, however, this error is negligible because there is minimal current flow in the wires.

Obviously, this simple circuit must have a good thermal as well as electrical design in order to maintain microvolt precision. Some good design precautions include minimizing number of thermocouple junctions, minimizing thermal gradients by proper layout or blocking airflow to critical devices using metallic or plastic shields, minimizing power dissipation in sensitive devices, proper selection of precision resistors, and matching the number of junctions in each half of a differential signal path by adding "dummy" components if required. Sockets, connectors, switches, or relays in the critical signal path can introduce unstable contact resistances as well as "unknown" thermocouple junctions which may not track to the required accuracy. They should be avoided if possible.

PARASITIC THERMOCOUPLES IN SIMPLE CIRCUIT

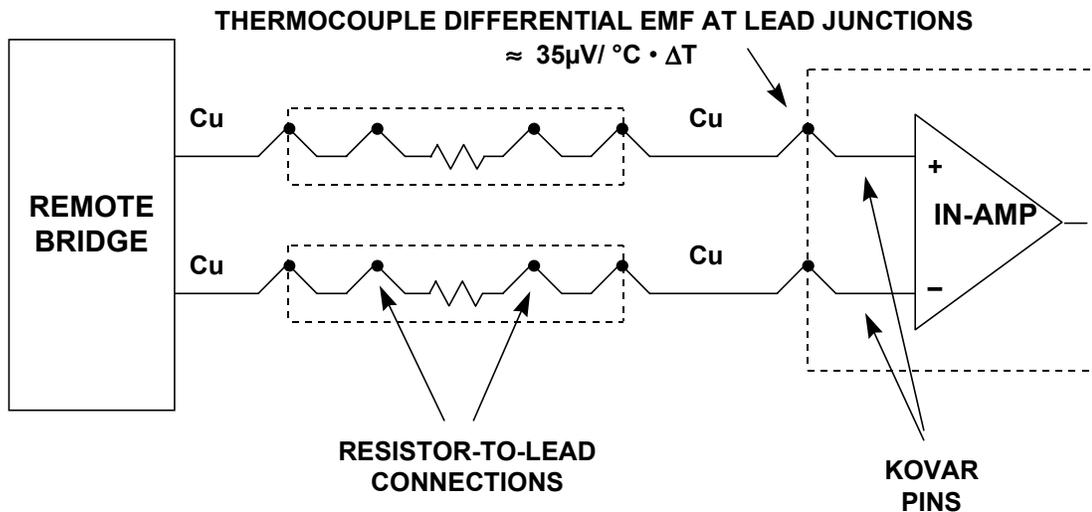


Figure 10.6

REFERENCES: RESISTOR AND THERMOELECTRIC ERRORS

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GROUNDING IN MIXED SIGNAL SYSTEMS

Walt Kester, James Bryant

Today's signal processing systems generally require mixed-signal devices such as analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) as well as fast digital signal processors (DSPs). Requirements for processing analog signals having wide dynamic ranges increases the importance of high performance ADCs and DACs. Maintaining wide dynamic range with low noise in hostile digital environments is dependent upon using good high-speed circuit design techniques including proper signal routing, decoupling, and grounding.

In the past, "high precision, low-speed" circuits have generally been viewed differently than so-called "high-speed" circuits. With respect to ADCs and DACs, the sampling (or update) frequency has generally been used as the distinguishing speed criteria. However, the following two examples show that in practice, most of today's signal processing ICs are really "high-speed," and must therefore be treated as such in order to maintain high performance. This is certainly true of DSPs, and also true of ADCs and DACs.

All sampling ADCs (ADCs with an internal sample-and-hold circuit) suitable for signal processing applications operate with relatively high speed clocks with fast rise and fall times (generally a few nanoseconds) and must be treated as high speed devices, even though throughput rates may appear low. For example, the 12-bit AD7892 successive approximation (SAR) ADC operates on an 8MHz internal clock, while the sampling rate is only 600kSPS.

Sigma-delta (Σ - Δ) ADCs also require high speed clocks because of their high oversampling ratios. The AD7722 16-bit ADC has an output data rate (effective sampling rate) of 195kSPS, but actually samples the input signal at 12.5MSPS (64-times oversampling). Even high resolution, so-called "low frequency" Σ - Δ industrial measurement ADCs (having throughputs of 10Hz to 7.5kHz) operate on 5MHz or higher clocks and offer resolution to 24-bits (for example, the Analog Devices AD7730 and AD7731).

To further complicate the issue, mixed-signal ICs have both analog and digital ports, and because of this, much confusion has resulted with respect to proper grounding techniques. Digital and analog design engineers tend to view these devices from different perspectives, and the purpose of this section is to develop a general grounding philosophy that will work for most mixed signal devices, without having to know the specific details of their internal circuits.

Ground and Power Planes

The importance of maintaining a low impedance large area ground plane is critical to all analog circuits today. The ground plane not only acts as a low impedance return path for decoupling high frequency currents (caused by fast digital logic) but

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also minimizes EMI/RFI emissions. Because of the shielding action of the ground plane, the circuits susceptibility to external EMI/RFI is also reduced.

Ground planes also allow the transmission of high speed digital or analog signals using transmission line techniques (microstrip or stripline) where controlled impedances are required.

The use of "buss wire" is totally unacceptable as a "ground" because of its impedance at the equivalent frequency of most logic transitions. For instance, #22 gauge wire has about 20nH/inch inductance. A transient current having a slew rate of 10mA/ns created by a logic signal would develop an unwanted voltage drop of 200mV at this frequency flowing through 1 inch of this wire:

$$\Delta v = L \frac{\Delta i}{\Delta t} = 20\text{nH} \times \frac{10\text{mA}}{\text{ns}} = 200\text{mV}.$$

For a signal having a 2V peak-to-peak range, this translates into an error of about 200mV, or 10% (approximate 3.5-bit accuracy). Even in all-digital circuits, this error would result in considerable degradation of logic noise margins.

Figure 10.7 shows an illustration of a situation where the digital return current modulates the analog return current (top figure). The ground return wire inductance and resistance is shared between the analog and digital circuits, and this is what causes the interaction and resulting error. A possible solution is to make the digital return current path flow directly to the GND REF as shown in the bottom figure. This is the fundamental concept of a "star," or single-point ground system. Implementing the true single-point ground in a system which contains multiple high frequency return paths is difficult because the physical length of the individual return current wires will introduce parasitic resistance and inductance which can make obtaining a low impedance high frequency ground difficult. In practice, the current returns must consist of large area ground planes for low impedance to high frequency currents. Without a low-impedance ground plane, it is therefore almost impossible to avoid these shared impedances, especially at high frequencies.

All integrated circuit ground pins should be soldered directly to the low-impedance ground plane to minimize series inductance and resistance. The use of traditional IC sockets is not recommended with high-speed devices. The extra inductance and capacitance of even "low profile" sockets may corrupt the device performance by introducing unwanted shared paths. If sockets must be used with DIP packages, as in prototyping, individual "pin sockets" or "cage jacks" may be acceptable. Both capped and uncapped versions of these pin sockets are available (AMP part numbers 5-330808-3, and 5-330808-6). They have spring-loaded gold contacts which make good electrical and mechanical connection to the IC pins. Multiple insertions, however, may degrade their performance.

DIGITAL CURRENTS FLOWING IN ANALOG RETURN PATH CREATE ERROR VOLTAGES

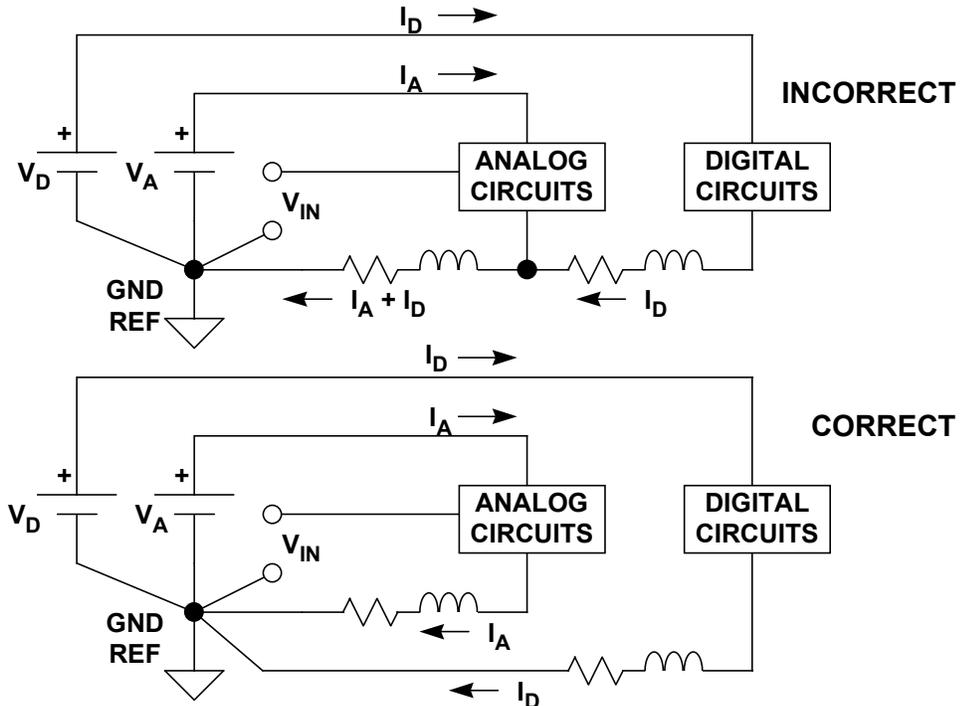


Figure 10.7

Power supply pins should be decoupled directly to the ground plane using low inductance ceramic surface mount capacitors. If through-hole mounted ceramic capacitors must be used, their leads should be less than 1mm. The ceramic capacitors should be located as close as possible to the IC power pins. Ferrite beads may be also required for additional decoupling.

Double-Sided vs. Multilayer Printed Circuit Boards

Each PCB in the system should have at least one complete layer dedicated to the ground plane. Ideally, a double-sided board should have one side completely dedicated to ground and the other side for interconnections. In practice, this is not possible, since some of the ground plane will certainly have to be removed to allow for signal and power crossovers, vias, and through-holes. Nevertheless, as much area as possible should be preserved, and at least 75% should remain. After completing an initial layout, the ground layer should be checked carefully to make sure there are no isolated ground "islands," because IC ground pins located in a ground "island" have no current return path to the ground plane. Also, the ground plane should be checked for "skinny" connections between adjacent large areas which may significantly reduce the effectiveness of the ground plane. Needless to say, auto-routing board layout techniques will generally lead to a layout disaster on a mixed-signal board, so manual intervention is highly recommended.

Systems that are densely packed with surface mount ICs will have a large number of interconnections; therefore multilayer boards are preferred. This allows a complete layer to be dedicated to ground. A simple 4-layer board would have internal ground and power plane layers with the outer two layers used for interconnections between the surface mount components. Placing the power and ground planes adjacent to each other provides additional inter-plane capacitance which helps high frequency decoupling of the power supply.

GROUND PLANES ARE MANDATORY!

- **Use Large Area Ground (and Power) Planes for Low Impedance Current Return Paths (Must Use at Least a Double-Sided Board!)**
- **Double-Sided Boards:**
 - ◆ **Avoid High-Density Interconnection Crossovers and Feedthroughs Which Reduce Ground Plane Area**
 - ◆ **Keep > 75% Board Area on One Side for Ground Plane**
- **Multilayer Boards**
 - ◆ **Dedicate at Least One Layer for the Ground Plane**
 - ◆ **Dedicate at Least One Layer for the Power Plane**
- **Use at Least 30% to 40% of PCB Connector Pins for Ground**
- **Continue the Ground Plane on the Backplane Motherboard to Power Supply Return**

Figure 10.8

Multicard Mixed-Signal Systems

The best way of minimizing ground impedance in a multicard system is to use a "motherboard" PCB as a backplane for interconnections between cards, thus providing a continuous ground plane to the backplane. The PCB connector should have at least 30-40% of its pins devoted to ground, and these pins should be connected to the ground plane on the backplane mother card. To complete the overall system grounding scheme there are two possibilities:

1. The backplane ground plane can be connected to chassis ground at numerous points, thereby diffusing the various ground current return paths. This is commonly referred to as a "multipoint" grounding system and is shown in Figure 10.9.
2. The ground plane can be connected to a single system "star ground" point (generally at the power supply).

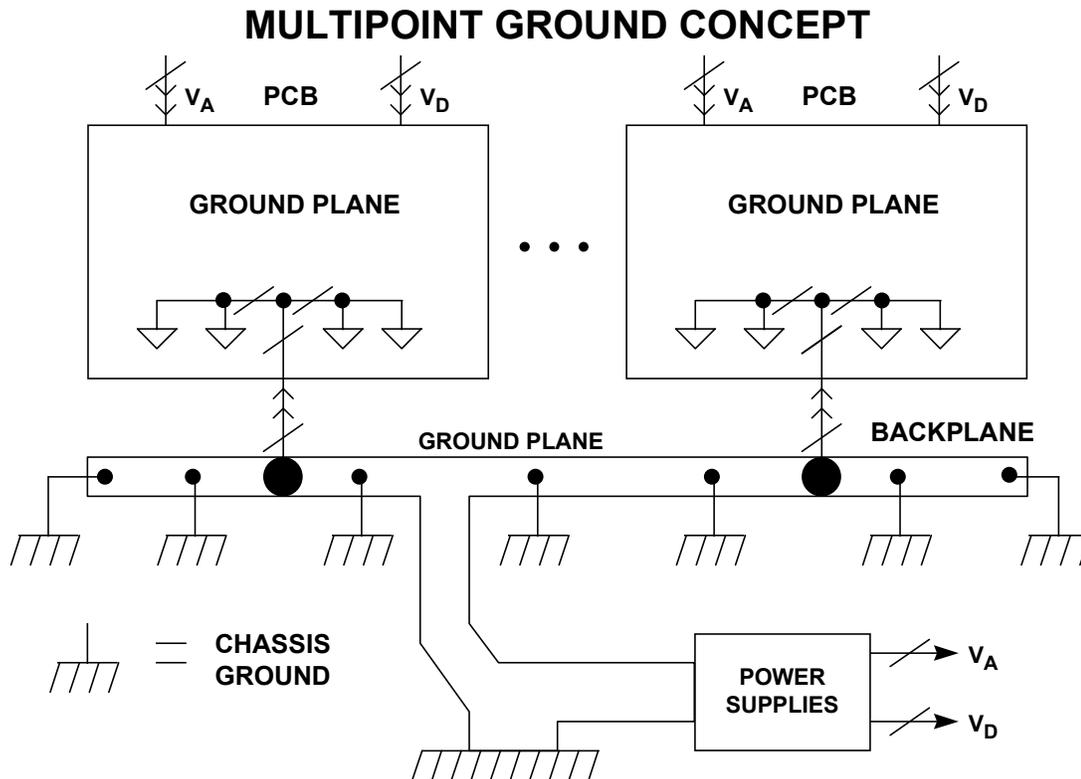


Figure 10.9

The first approach is most often used in all-digital systems, but can be used in mixed-signal systems provided the ground currents due to digital circuits are sufficiently diffused over a large area. The low ground impedance is maintained all the way through the PC boards, the backplane, and ultimately the chassis. However, it is critical that good electrical contact be made where the grounds are connected to the sheet metal chassis. This requires self-tapping sheet metal screws or "biting" washers. Special care must be taken where anodized aluminum is used for the chassis material, since its surface acts as an insulator.

The second approach ("star ground") is often used in high speed mixed-signal systems having separate analog and digital ground systems and warrants considerable further discussion.

Separating Analog and Digital Grounds

In mixed-signal systems with large amounts of digital circuitry, it is highly desirable to *physically* separate sensitive analog components from noisy digital components. It may also be beneficial to use separate ground planes for the analog and the digital circuitry. These planes should not overlap in order to minimize capacitive coupling between the two. The separate analog and digital ground planes are continued on the backplane using either motherboard ground planes or "ground

screens" which are made up of a series of wired interconnections between the connector ground pins. The arrangement shown in Figure 10.10 illustrates that the two planes are kept separate all the way back to a common system "star" ground, generally located at the power supplies. The connections between the ground planes, the power supplies, and the "star" should be made up of multiple bus bars or wide copper brads for minimum resistance and inductance. The back-to-back Schottky diodes on each PCB are inserted to prevent accidental DC voltage from developing between the two ground systems when cards are plugged and unplugged. Schottky diodes are used because of their low capacitance to prevent coupling between the analog and digital ground planes. However, Schottky diodes begin to conduct at about 300mV, so if the total differential peak-to-peak voltage (the sum of the AC and DC components) between the two ground planes exceeds this value, additional diodes in series should be used.

SEPARATING ANALOG AND DIGITAL GROUND PLANES

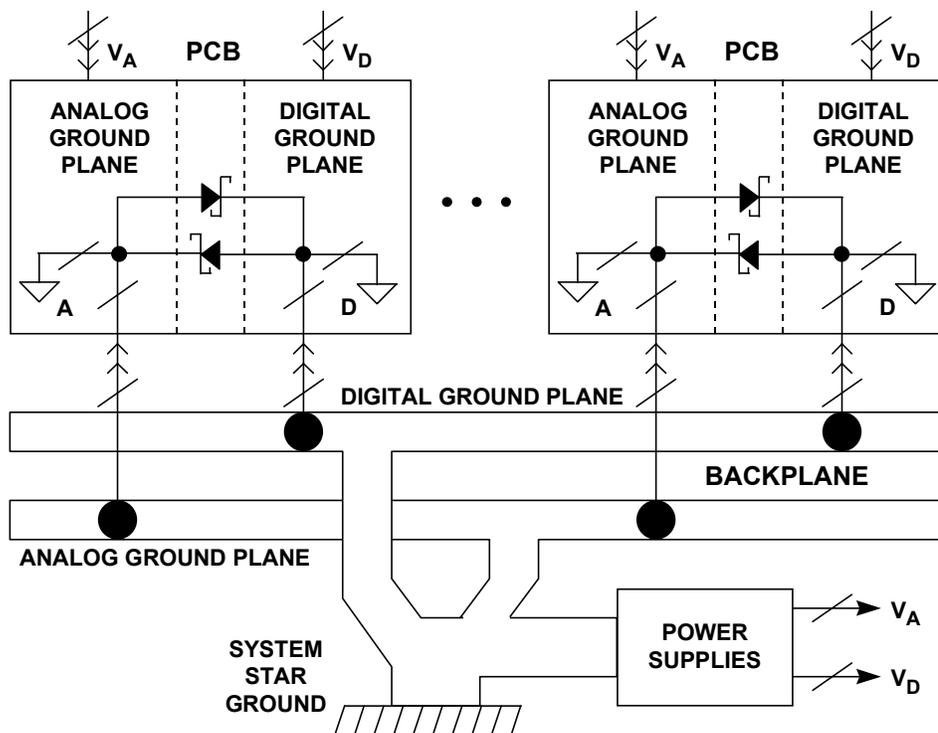


Figure 10.10

Grounding and Decoupling Mixed-Signal ICs

Sensitive analog components such as amplifiers and voltage references are always referenced and decoupled to the analog ground plane. *The ADCs and DACs (and other mixed-signal ICs) should generally be treated as analog components and also grounded and decoupled to the analog ground plane.* At first glance, this may seem somewhat contradictory, since a converter has an analog and digital interface and usually pins designated as *analog ground (AGND)* and *digital ground (DGND)*. The diagram shown in Figure 10.11 will help to explain this seeming dilemma.

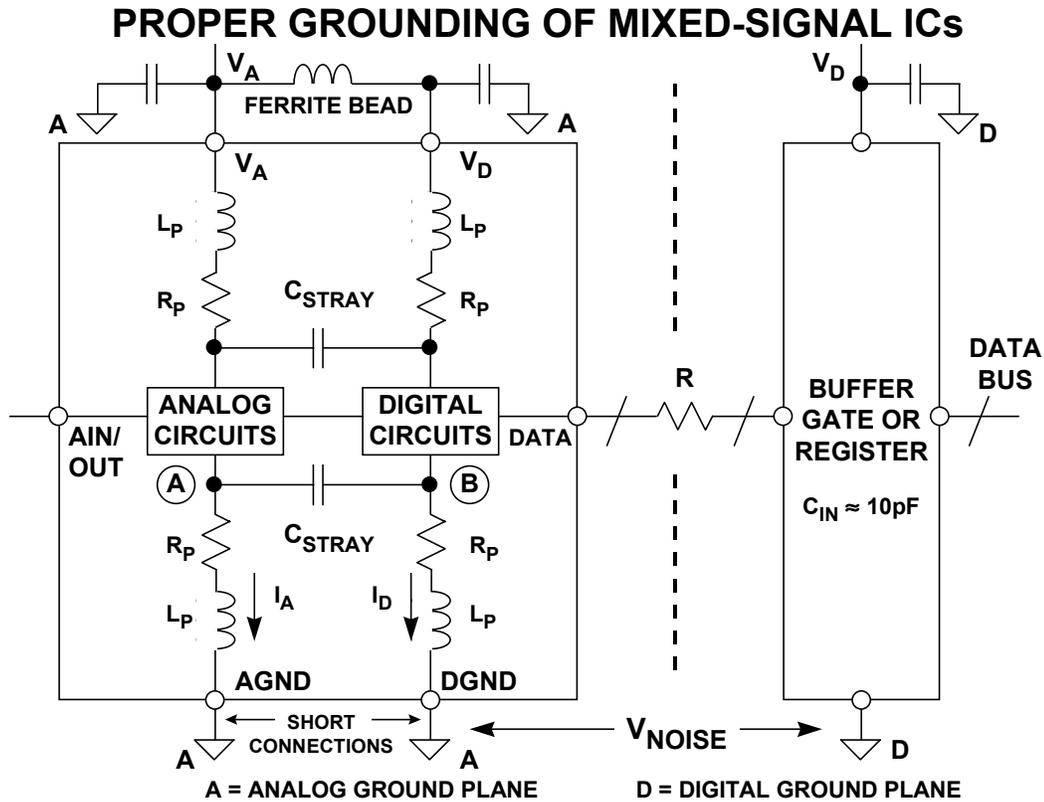


Figure 10.11

Inside an IC that has both analog and digital circuits, such as an ADC or a DAC, the grounds are usually kept separate to avoid coupling digital signals into the analog circuits. Figure 10.11 shows a simple model of a converter. There is nothing the IC designer can do about the wirebond inductance and resistance associated with connecting the bond pads on the chip to the package pins except to realize it's there. The rapidly changing digital currents produce a voltage at point B which will inevitably couple into point A of the analog circuits through the stray capacitance, C_{STRAY} . In addition, there is approximately 0.2pF unavoidable stray capacitance between every pin of the IC package! It's the IC designer's job to make the chip work in spite of this. However, in order to prevent further coupling, the AGND and DGND pins should be joined together externally to the *analog* ground plane with minimum lead lengths. Any extra impedance in the DGND connection will cause more digital noise to be developed at point B; it will, in turn, couple more digital noise into the analog circuit through the stray capacitance. *Note that connecting DGND to the digital ground plane applies V_{NOISE} across the AGND and DGND pins and invites disaster!*

The name "DGND" on an IC tells us that this pin connects to the digital ground of the IC. This does not imply that this pin must be connected to the digital ground of the system.

It is true that this arrangement will inject a small amount of digital noise onto the analog ground plane. These currents should be quite small, and can be minimized by ensuring that the converter output does not drive a large fanout (they normally

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can't, by design). Minimizing the fanout on the converter's digital port will also keep the converter logic transitions relatively free from ringing and minimize digital switching currents, and thereby reducing any potential coupling into the analog port of the converter. The logic supply pin (V_D) can be further isolated from the analog supply by the insertion of a small lossy ferrite bead as shown in Figure 10.11. The internal digital currents of the converter will return to ground through the V_D pin decoupling capacitor (mounted as close to the converter as possible) and will not appear in the external ground circuit. These decoupling capacitors should be low inductance ceramic types, typically between $0.01\mu\text{F}$ and $0.1\mu\text{F}$.

Treat the ADC Digital Outputs with Care

It is always a good idea (as shown in Figure 10.11) to place a buffer register adjacent to the converter to isolate the converter's digital lines from noise on the data bus. The register also serves to minimize loading on the digital outputs of the converter and acts as a Faraday shield between the digital outputs and the data bus. Even though many converters have three-state outputs/inputs, this isolation register still represents good design practice.

The series resistors (labeled "R" in Figure 10.11) between the ADC output and the buffer register input help to minimize the digital transient currents which may affect converter performance. The resistors isolate the digital output drivers from the capacitance of the buffer register inputs. In addition, the RC network formed by the series resistor and the buffer register input capacitance acts as a lowpass filter to slow down the fast edges.

A typical CMOS gate combined with PCB trace and through-hole will create a load of approximately 10pF . A logic output slew rate of 1V/ns will produce 10mA of dynamic current if there is no isolation resistor:

$$\Delta I = C \frac{\Delta v}{\Delta t} = 10\text{pF} \times \frac{1\text{V}}{\text{ns}} = 10\text{mA} .$$

A 500Ω series resistors will minimize this output current and result in a rise and fall time of approximately 11ns when driving the 10pF input capacitance of the register:

$$t_r = 2.2 \times \tau = 2.2 \times R \cdot C = 2.2 \times 500\Omega \times 10\text{pF} = 11\text{ns}.$$

TTL registers should be avoided, since they can appreciably add to the dynamic switching currents because of their higher input capacitance.

The buffer register and other digital circuits should be grounded and decoupled to the *digital* ground plane of the PC board. Notice that any noise between the analog and digital ground plane reduces the noise margin at the converter digital interface. Since digital noise immunity is of the orders of hundreds or thousands of millivolts, this is unlikely to matter. The analog ground plane will generally not be very noisy, but if the noise on the digital ground plane (relative to the analog ground plane) exceeds a few hundred millivolts, then steps should be taken to reduce the digital

ground plane impedance, thereby maintaining the digital noise margins at an acceptable level.

Separate power supplies for analog and digital circuits are also highly desirable. The analog supply should be used to power the converter. If the converter has a pin designated as a digital supply pin (V_D), it should either be powered from a separate analog supply, or filtered as shown in the diagram. All converter power pins should be decoupled to the analog ground plane, and all logic circuit power pins should be decoupled to the digital ground plane as shown in Figure 10.12. If the digital power supply is relatively quiet, it may be possible to use it to supply analog circuits as well, but be very cautious.

In some cases it may not be possible to connect V_D to the analog supply. Some of the newer, high speed ICs may have their analog circuits powered by +5V, but the digital interface powered by +3V to interface to 3V logic. In this case, the +3V pin of the IC should be decoupled directly to the analog ground plane. It is also advisable to connect a ferrite bead in series with power trace that connects the pin to the +3V digital logic supply.

GROUNDING AND DECOUPLING POINTS

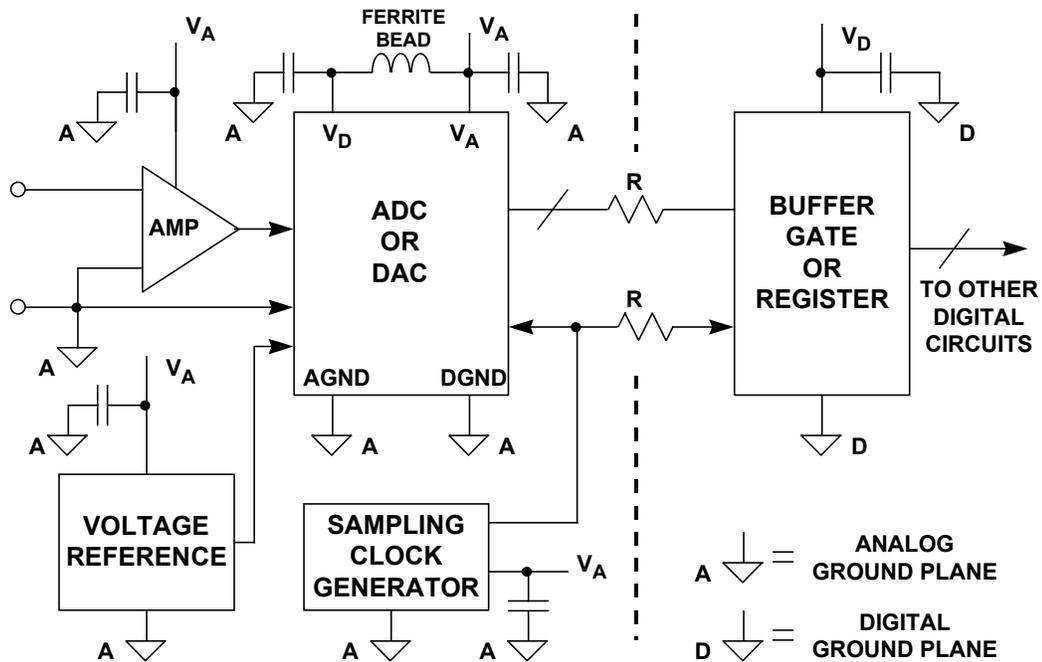


Figure 10.12

The sampling clock generation circuitry should be treated like analog circuitry and also be grounded and heavily-decoupled to the analog ground plane. Phase noise on the sampling clock produces degradation in system SNR as will be discussed shortly.

The Origins of the Confusion about Mixed-Signal Grounding: Applying Single-Card Grounding Concepts to Multicard Systems

Most ADC, DAC, and other mixed-signal device data sheets discuss grounding relative to a single PCB, usually the manufacturer's own evaluation board. This has been a source of confusion when trying to apply these principles to multicard or multi-ADC/DAC systems. The recommendation is usually to split the PCB ground plane into an analog one and a digital one. It is then further recommended that the AGND and DGND pins of a converter be tied together and that the analog ground plane and digital ground planes be connected at that same point. This essentially creates the system "star" ground at the mixed-signal device. While this approach will generally work in a simple system with a single PCB and single ADC/DAC, it is not optimum for multicard mixed-signal systems. In systems having several ADCs or DACs on different PCBs (or on the same PCB, for that matter), the analog and digital ground planes become connected at several points, creating the possibility of ground loops and making a single-point "star" ground system impossible. These ground loops can also occur if there is more than one mixed-signal device on a single PCB. For these reasons, this grounding approach is not recommended for multicard systems, and the approach previously discussed should be used.

Sampling Clock Considerations

In a high performance sampled data system a low phase-noise crystal oscillator should be used to generate the ADC (or DAC) sampling clock because sampling clock jitter modulates the analog input/output signal and raises the noise and distortion floor. The sampling clock generator should be isolated from noisy digital circuits and grounded and decoupled to the analog ground plane, as is true for the op amp and the ADC.

The effect of sampling clock jitter on ADC Signal-to-Noise Ratio (SNR) is given approximately by the equation:

$$\text{SNR} = 20 \log_{10} \left[\frac{1}{2\pi f t_j} \right],$$

where SNR is the SNR of a perfect ADC of infinite resolution where the only source of noise is that caused by the RMS sampling clock jitter, t_j . Note that f in the above equation is the analog input frequency. Just working through a simple example, if $t_j = 50\text{ps}$ RMS, $f = 100\text{kHz}$, then $\text{SNR} = 90\text{dB}$, equivalent to about 15-bits dynamic range.

It should be noted that t_j in the above example is the root-sum-square (RSS) value of the external clock jitter *and* the internal ADC clock jitter (called aperture jitter). However, in most high performance ADCs, the internal aperture jitter is negligible compared to the jitter on the sampling clock.

Since degradation in SNR is primarily due to external clock jitter, steps must be taken to ensure the sampling clock is as noise-free as possible and has the lowest possible phase jitter. This requires that a crystal oscillator be used. There are several manufacturers of small crystal oscillators with low jitter (less than 5ps

Some PC Board Layout Guidelines for Mixed-Signal Systems

It is evident that noise can be minimized by paying attention to the system layout and preventing different signals from interfering with each other. High level analog signals should be separated from low level analog signals, and both should be kept away from digital signals. We have seen elsewhere that in waveform sampling and reconstruction systems the sampling clock (which is a digital signal) is as vulnerable to noise as any analog signal, but is as liable to cause noise as any digital signal, and so must be kept isolated from both analog and digital systems.

The ground plane can act as a shield where sensitive signals cross. Figure 10.14 shows a good layout for a data acquisition board where all sensitive areas are isolated from each other and signal paths are kept as short as possible. While real life is rarely as tidy as this, the principle remains a valid one.

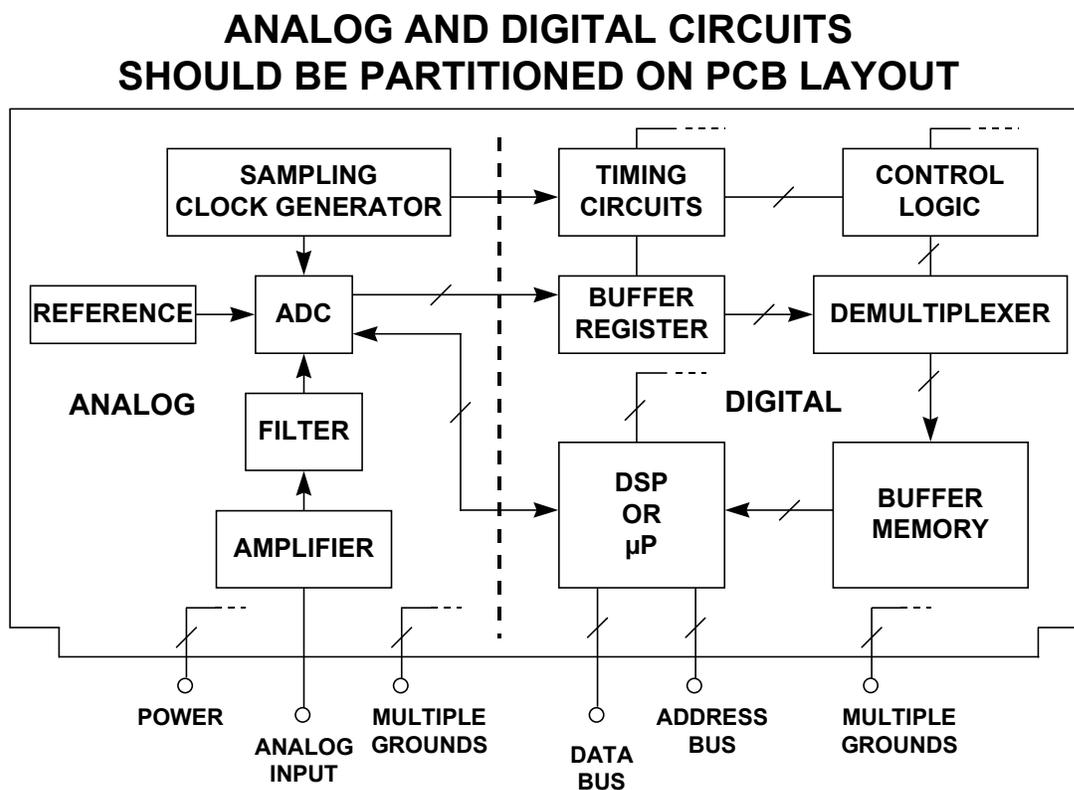


Figure 10.14

There are a number of important points to be considered when making signal and power connections. First of all a connector is one of the few places in the system where all signal conductors must run in parallel - it is therefore imperative to separate them with ground pins (creating a faraday shield) to reduce coupling between them.

Multiple ground pins are important for another reason: they keep down the ground impedance at the junction between the board and the backplane. The contact resistance of a single pin of a PCB connector is quite low (of the order of 10mΩ) when the board is new - as the board gets older the contact resistance is likely to

rise, and the board's performance may be compromised. It is therefore well worthwhile to allocate extra PCB connector pins so that there are many ground connections (perhaps 30-40% of all the pins on the PCB connector should be ground pins). For similar reasons there should be several pins for each power connection, although there is no need to have as many as there are ground pins.

Manufacturers of high performance mixed-signal ICs like Analog Devices offer evaluation boards to assist customers in their initial evaluations and layout. ADC evaluation boards generally contain an on-board low-jitter sampling clock oscillator, output registers, and appropriate power and signal connectors. They also may have additional support circuitry such as the ADC input buffer amplifier and external reference.

The layout of the evaluation board is optimized in terms of grounding, decoupling, and signal routing and can be used as a model when laying out the ADC PC board in the system. The actual layout is usually available from the ADC manufacturer in the form of computer CAD files (Gerber files).

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POWER SUPPLY NOISE REDUCTION AND FILTERING

Walt Jung, Walt Kester, Bill Chestnut

Precision analog circuitry has traditionally been powered from well regulated, low noise linear power supplies. During the last decade however, switching power supplies have become much more common in electronic systems. As a consequence, they also are being used for analog supplies. Good reasons for the general popularity include their high efficiency, low temperature rise, small size, and light weight.

In spite of these benefits, switchers *do* have drawbacks, most notably high output noise. This noise generally extends over a broad band of frequencies, resulting in both conducted and radiated noise, as well as unwanted electric and magnetic fields. Voltage output noise of switching supplies are short-duration voltage transients, or spikes. Although the fundamental switching frequency can range from 20kHz to 1MHz, the spikes can contain frequency components extending to 100MHz or more. While specifying switching supplies in terms of RMS noise is common vendor practice, as a user you should also specify the *peak* (or p-p) amplitudes of the switching spikes, at the output loading of your system.

The following section discusses filter techniques for rendering a switching regulator output *analog ready*, that is sufficiently quiet to power precision analog circuitry with relatively small loss of DC terminal voltage. The filter solutions presented are generally applicable to all power supply types incorporating switching element(s) in their energy path. This includes various DC-DC converters as well as popular 5V (PC type) supplies.

An understanding of the EMI process is necessary to understand the effects of supply noise on analog circuits and systems. Every interference problem has a *source*, a *path*, and a *receptor* [Reference 1]. In general, there are three methods for dealing with interference. First, source emissions can be minimized by proper layout, pulse-edge rise time control/reduction, filtering, and proper grounding. Second, radiation and conduction paths should be reduced through shielding and physical separation. Third, receptor immunity to interference can be improved, via supply and signal line filtering, impedance level control, impedance balancing, and utilizing differential techniques to reject undesired common-mode signals. This section focuses on reducing switching power supply noise with external post filters.

Tools useful for combating high frequency switcher noise are shown by Figure 10.15. They differ in electrical characteristics as well as practicality towards noise reduction, and are listed roughly in an order of priorities. Of these tools, L and C are the most powerful filter elements, and are the most cost-effective, as well as small in size.

SWITCHING REGULATOR NOISE REDUCTION TOOLS

- Capacitors
- Inductors
- Ferrites
- Resistors
- Linear Post Regulation
- Proper Layout and Grounding Techniques
- PHYSICAL SEPARATION FROM SENSITIVE ANALOG CIRCUITS!!

Figure 10.15

Capacitors are probably the single most important filter component for switchers. There are many different types of capacitors, and an understanding of their individual characteristics is absolutely mandatory to the design of effective practical supply filters. There are generally three classes of capacitors useful in 10kHz-100MHz filters, broadly distinguished as the generic dielectric types; *electrolytic*, *organic*, *film*, and *ceramic*. These can in turn can be further sub-divided. A thumbnail sketch of capacitor characteristics is shown in the chart of Figure 10.16.

TYPES OF CAPACITORS

	Aluminum Electrolytic (General Purpose)	Aluminum Electrolytic (Switching Type)	Tantalum Electrolytic	OS-CON Electrolytic	Polyester (Stacked Film)	Ceramic (Multilayer)
Size	100 μ F	120 μ F	120 μ F	100 μ F	1 μ F	0.1 μ F
Rated Voltage	25 V	25 V	20 V	20 V	400 V	50 V
ESR	0.6 Ω @ 100 kHz	0.18 Ω @ 100 kHz	0.12 Ω @ 100 kHz	0.02 Ω @ 100 kHz	0.11 Ω @ 1 MHz	0.12 Ω @ 1 MHz
Operating Frequency (*)	\cong 100 kHz	\cong 500 kHz	\cong 1 MHz	\cong 1 MHz	\cong 10 MHz	\cong 1 GHz

(*) Upper frequency strongly size and package dependent

Figure 10.16

With any dielectric, a major potential filter loss element is ESR (equivalent series resistance), the net parasitic resistance of the capacitor. ESR provides an ultimate limit to filter performance, and requires more than casual consideration, because it can vary both with frequency and temperature in some types. Another capacitor loss element is ESL (equivalent series inductance). ESL determines the frequency where the net impedance characteristic switches from capacitive to inductive. This varies from as low as 10kHz in some electrolytics to as high as 100MHz or more in chip ceramic types. Both ESR and ESL are minimized when a leadless package is used. All capacitor types mentioned are available in surface mount packages, preferable for high speed uses.

The *electrolytic* family provides an excellent, cost-effective low-frequency filter component, because of the wide range of values, a high capacitance-to-volume ratio, and a broad range of working voltages. It includes *general purpose aluminum electrolytic* types, available in working voltages from below 10V up to about 500V, and in size from 1 to several thousand μF (with proportional case sizes). All electrolytic capacitors are polarized, and thus cannot withstand more than a volt or so of reverse bias without damage. They also have relatively high leakage currents (up to tens of μA , and strongly dependent upon design specifics).

A subset of the general electrolytic family includes *tantalum* types, generally limited to voltages of 100V or less, with capacitance of up to 500 μF [Reference 3]. In a given size, tantalums exhibit a higher capacitance-to-volume ratios than do general purpose electrolytics, and have both a higher frequency range and lower ESR. They are generally more expensive than standard electrolytics, and must be carefully applied with respect to surge and ripple currents.

A subset of aluminum electrolytic capacitors is the *switching* type, designed for handling high pulse currents at frequencies up to several hundred kHz with low losses [Reference 4]. This capacitor type competes directly with tantalums in high frequency filtering applications, with the advantage of a broader range of values.

A more specialized high performance aluminum electrolytic capacitor type uses an organic semiconductor electrolyte [Reference 5]. The *OS-CON* capacitors feature appreciably lower ESR and higher frequency range than do other electrolytic types, with an additional feature of low low-temperature ESR degradation.

Film capacitors are available in a very broad range of values and an array of dielectrics, including polyester, polycarbonate, polypropylene, and polystyrene. Because of the low dielectric constant of these films, their volumetric efficiency is quite low, and a 10 μF /50V polyester capacitor (for example) is actually the size of your hand. Metalized (as opposed to foil) electrodes do help to reduce size, but even the highest dielectric constant units among film types (polyester, polycarbonate) are still larger than any electrolytic, even using the thinnest films with the lowest voltage ratings (50V). Where film types excel is in their low dielectric losses, a factor which may not necessarily be a practical advantage for filtering switchers. For example, ESR in film capacitors can be as low as 10m Ω or less, and the behavior of films generally is very high in terms of Q. In fact, this can cause problems of spurious resonance in filters, requiring damping components.

HARDWARE DESIGN TECHNIQUES

Film capacitors using a wound layer-type construction can be inductive. This can limit their effectiveness for high frequency filtering. Obviously, only non-inductively made film caps are useful for switching regulator filters. One specific style which is non-inductive is the *stacked-film* type, where the capacitor plates are cut as small overlapping linear sheet sections from a much larger wound drum of dielectric/plate material. This technique offers the low inductance attractiveness of a plate sheet style capacitor with conventional leads [see References 4, 5, 6]. Obviously, minimal lead length should be used for best high frequency effectiveness. Very high current polycarbonate film types are also available, specifically designed for switching power supplies, with a variety of low inductance terminations to minimize ESL [Reference 7].

Dependent upon their electrical and physical size, film capacitors can be useful at frequencies to well above 10MHz. At the highest frequencies, only stacked film types should be considered. Some manufacturers are now supplying film types in leadless surface mount packages, which eliminates the lead length inductance.

Ceramic is often the capacitor material of choice above a few MHz, due to its compact size, low loss, and availability up to several μF in the high-K dielectric formulations (X7R and Z5U), at voltage ratings up to 200V [see ceramic families of Reference 3]. NP0 (also called COG) types use a lower dielectric constant formulation, and have nominally zero TC, plus a low voltage coefficient (unlike the less stable high-K types). NP0 types are limited to values of $0.1\mu\text{F}$ or less, with $0.01\mu\text{F}$ representing a more practical upper limit.

Multilayer ceramic “chip caps” are very popular for bypassing/ filtering at 10MHz or higher, simply because their very low inductance design allows near optimum RF bypassing. For smaller values, ceramic chip caps have an operating frequency range to 1GHz. For high frequency applications, a useful selection can be ensured by selecting a value which has a self-resonant frequency *above* the highest frequency of interest.

All capacitors have some finite ESR. In some cases, the ESR may actually be helpful in reducing resonance peaks in filters, by supplying “free” damping. For example, in most electrolytic types, a nominally flat broad series resonance region can be noted by the impedance vs. frequency plot. This occurs where $|Z|$ falls to a minimum level, nominally equal to the capacitor’s ESR at that frequency. This low Q resonance can generally cover a relatively wide frequency range of several octaves. Contrasted to the very high Q sharp resonances of film and ceramic caps, the low Q behavior of electrolytics can be useful in controlling resonant peaks.

In most electrolytic capacitors, ESR degrades noticeably at low temperature, by as much as a factor of 4-6 times at -55°C vs. the room temperature value. For circuits where ESR is critical to performance, this can lead to problems. Some specific electrolytic types do address this problem, for example within the HFQ switching types, the -10°C ESR at 100kHz is no more than $2\times$ that at room temperature. The OSCON electrolytics have a ESR vs. temperature characteristic which is relatively flat.

As noted, all real capacitors have parasitic elements which limit their performance. The equivalent electrical network representing a real capacitor models both ESR and ESL as well as the basic capacitance, plus some shunt resistance (see Figure 10.17). In such a practical capacitor, at low frequencies the net impedance is almost purely capacitive. At intermediate frequencies, the net impedance is determined by ESR, for example about 0.12Ω to 0.4Ω at 125kHz , for several types. Above about 1MHz these capacitor types become inductive, with impedance dominated by the effect of ESL. All electrolytics will display impedance curves similar in general shape to that of Figure 10.18. The minimum impedance will vary with the ESR, and the inductive region will vary with ESL (which in turn is strongly effected by package style).

CAPACITOR EQUIVALENT CIRCUIT AND PULSE RESPONSE

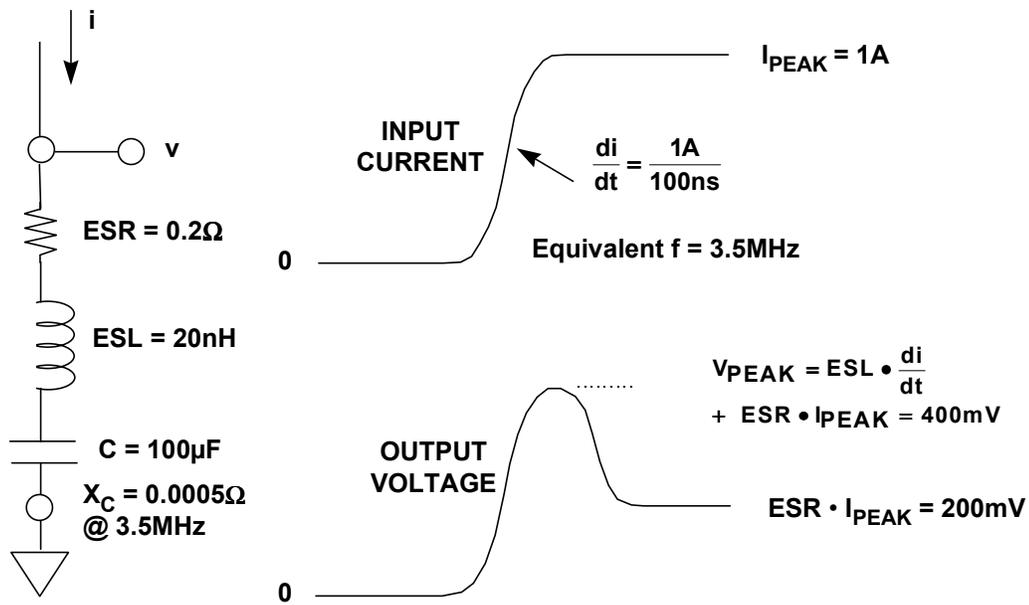


Figure 10.17

Regarding inductors, *Ferrites* (non-conductive ceramics manufactured from the oxides of nickel, zinc, manganese, or other compounds) are extremely useful in power supply filters [Reference 9]. At low frequencies ($<100\text{kHz}$), ferrites are inductive; thus they are useful in low-pass LC filters. Above 100kHz , ferrites become resistive, an important characteristic in high-frequency filter designs. Ferrite impedance is a function of material, operating frequency range, DC bias current, number of turns, size, shape, and temperature. Figure 10.19 summarizes a number of ferrite characteristics, and Figure 10.20 shows the impedance characteristic of several ferrite beads from Fair-Rite (<http://www.fair-rite.com>).

ELECTROLYTIC CAPACITOR IMPEDANCE VERSUS FREQUENCY

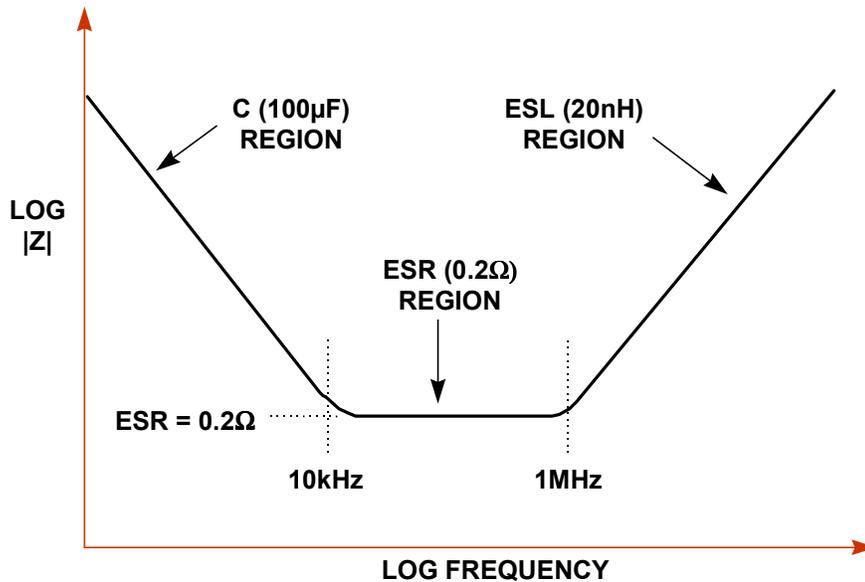


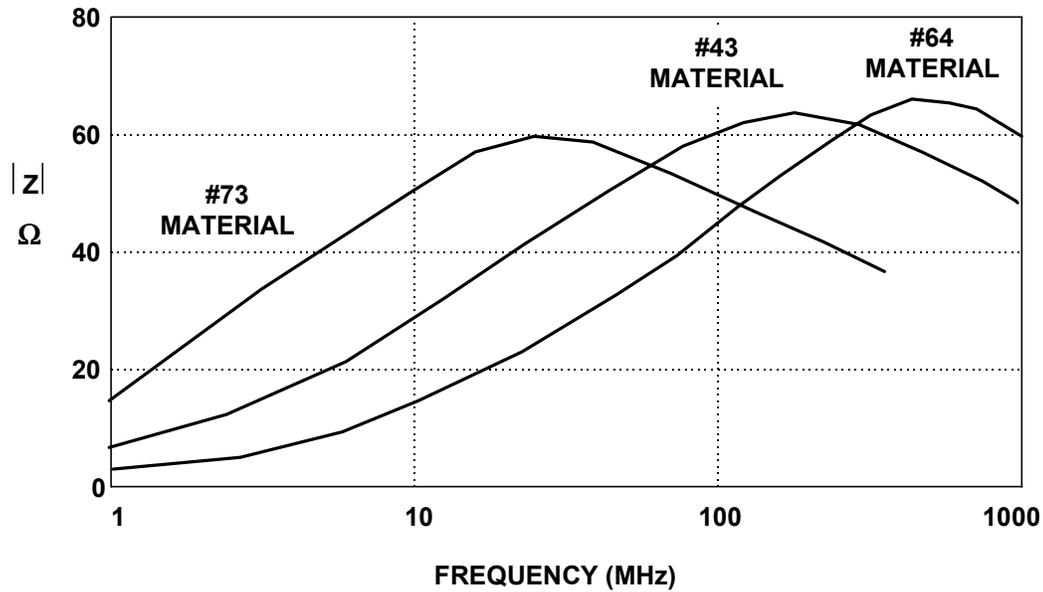
Figure 10.18

FERRITES SUITABLE FOR HIGH FREQUENCY FILTERS

- Ferrites Good for Frequencies Above 25kHz
- Many Sizes and Shapes Available Including Leaded "Resistor Style"
- Ferrite Impedance at High Frequencies Primarily Resistive -- Ideal for HF Filtering
- Low DC Loss: Resistance of Wire Passing Through Ferrite is Very Low
- High Saturation Current Versions Available
- Choice Depends Upon:
 - ◆ Source and Frequency of Interference
 - ◆ Impedance Required at Interference Frequency
 - ◆ Environmental: Temperature, AC and DC Field Strength, Size / Space Available
- Always Test the Design!

Figure 10.19

IMPEDANCE OF FERRITE BEADS



Courtesy: Fair-Rite Products Corp, Walkill, NY
<http://www.fair-rite.com>

Figure 10.20

Several ferrite manufacturers offer a wide selection of ferrite materials from which to choose, as well as a variety of packaging styles for the finished network (see References 10 and 11). A simple form is the *bead* of ferrite material, a cylinder of the ferrite which is simply slipped over the power supply lead to the decoupled stage. Alternately, the *leaded ferrite bead* is the same bead, pre-mounted on a length of wire and used as a component (see Reference 11). More complex beads offer multiple holes through the cylinder for increased decoupling, plus other variations. Surface mount beads are also available.

PSpice ferrite models for Fair-Rite materials are available, and allow ferrite impedance to be estimated [see Reference 12]. These models have been designed to match measured impedances rather than theoretical impedances.

A ferrite's impedance is dependent upon a number of inter-dependent variables, and is difficult to quantify analytically, thus selecting the proper ferrite is not straightforward. However, knowing the following system characteristics will make selection easier. First, determine the frequency range of the noise to be filtered. Second, the expected temperature range of the filter should be known, as ferrite impedance varies with temperature. Third, the peak DC current flowing through the ferrite must be known, to ensure that the ferrite does not saturate. Although models and other analytical tools may prove useful, the general guidelines given above, coupled with some experimentation with the actual filter connected to the supply output under system load conditions, should lead to a proper ferrite selection.

Using proper component selection, low and high frequency band filters can be designed to smooth a noisy switcher's DC output to produce an *analog ready* 5V supply. It is most practical to do this over two (and sometimes more) stages, each stage optimized for a range of frequencies. A basic stage can be used to carry all of the DC load current, and filter noise by 60dB or more up to a 1-10MHz range. This larger filter is used as a *card entry filter* providing broadband filtering for all power entering a PC card. Smaller, more simple local filter stages are also used to provide higher frequency decoupling right at the power pins of individual stages.

Switching Regulator Experiments

In order to better understand the challenge of filtering switching regulators, a series of experiments were conducted with a representative device, the ADP1148 synchronous buck regulator with a 9V input and a 3.3V/1A output.

In addition to observing typical input and output waveforms, the objective of these experiments was to reduce the output ripple to less than 10mV peak-to-peak, a value suitable for driving most analog circuits.

Measurements were made using a Tektronix wideband digitizing oscilloscope with the input bandwidth limited to 20MHz so that the ripple generated by the switching regulators could be more readily observed. In a system, power supply ripple frequencies above 20MHz are best filtered locally at each IC power pin with a low inductance ceramic capacitor and perhaps a series-connected ferrite bead.

Probing techniques are critical for accurate ripple measurements. A standard passive 10X probe was used with a "bayonet" probe tip adapter for making the ground connection as short as possible (see Figure 10.21). Use of the "ground clip lead" is not recommended in making this type of measurement because the lead length in the ground connection forms an unwanted inductive loop which picks up high frequency switching noise, thereby corrupting the signal being measured.

Note: Schematic representation of proper physical grounding is almost impossible. In all the following circuit schematics, the connections to ground are made to the ground plane using the shortest possible connecting path, regardless of how they are indicated in the actual circuit schematic diagram.

The circuit for the ADP1148 9V to 3.3V/1A buck regulator is shown in Figure 10.22. The output waveform of the ADP1148 buck regulator is shown in Figure 10.23. The fundamental switching frequency is approximately 150kHz, and the output ripple is approximately 40mV.

Adding an output filter consisting of a 50 μ H inductor and a 100 μ F leaded tantalum capacitor reduced the ripple to approximately 3mV.

PROPER PROBING TECHNIQUES

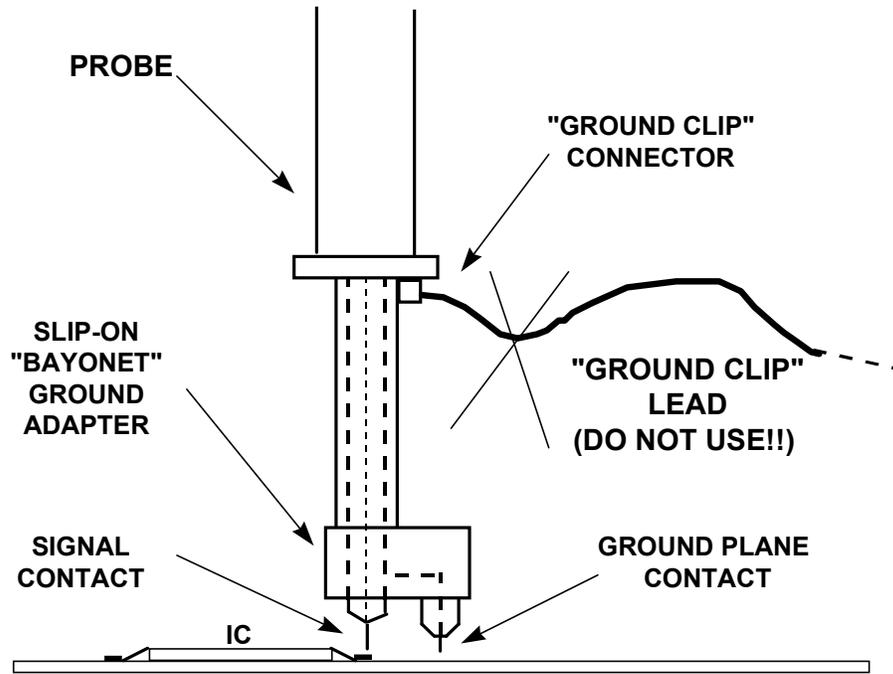


Figure 10.21

ADP1148 BUCK REGULATOR CIRCUIT

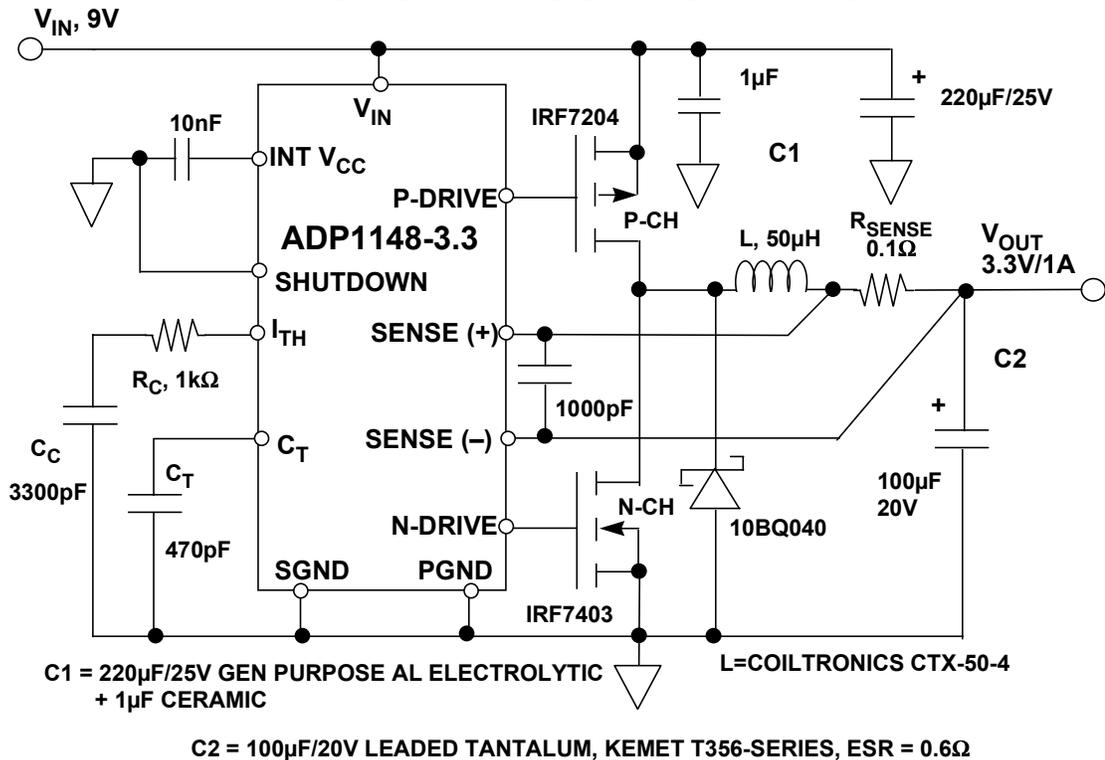
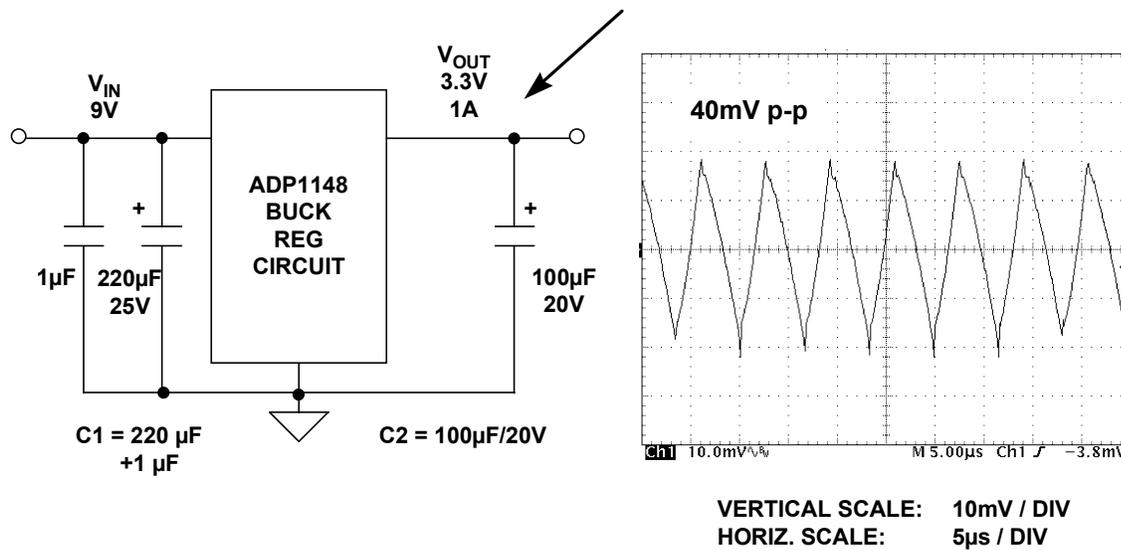


Figure 10.22

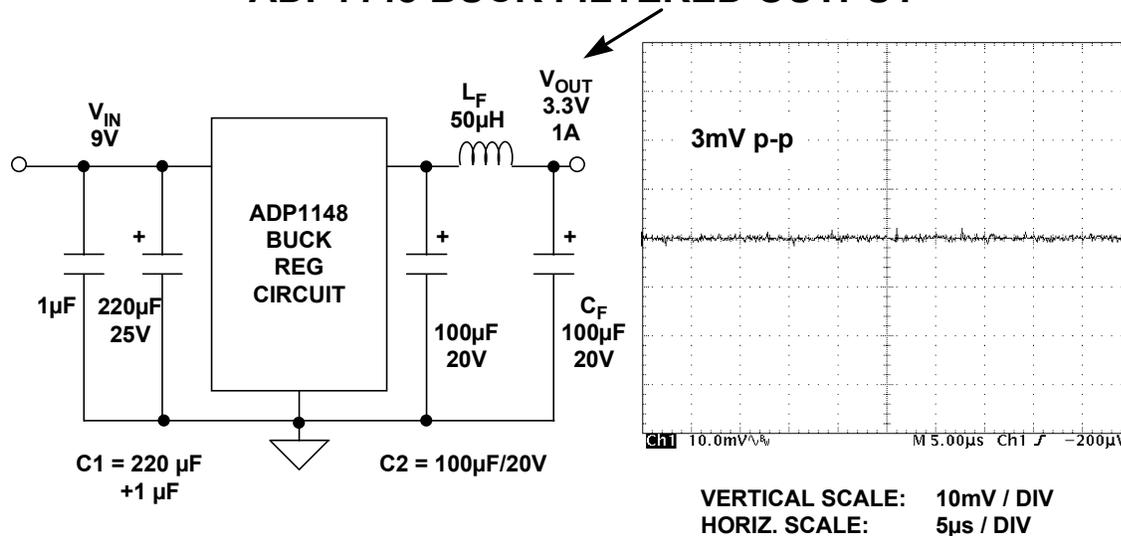
ADP1148 BUCK OUTPUT WAVEFORM



C1 = 1 μ F CERAMIC + 220 μ F/25V GENERAL PURPOSE AL ELECTROLYTIC
 C2 = 100 μ F/20V LEADED TANTALUM, KEMET T356-SERIES (ESR = 0.6 Ω)

Figure 10.23

ADP1148 BUCK FILTERED OUTPUT



C1 = 1 μ F CERAMIC + 220 μ F/25V GENERAL PURPOSE AL ELECTROLYTIC
 C2 = 100 μ F/20V LEADED TANTALUM, KEMET T356-SERIES (ESR = 0.6 Ω)

OUTPUT FILTER

L_F = COILTRONICS CTX-50-4

C_F = 100 μ F/20V LEADED TANTALUM, KEMET T356-SERIES

Figure 10.24

Linear regulators are often used following switching regulators for better regulation and lower noise. Low dropout (LDO) regulators such as the ADP3310 are desirable in these applications because they require only a small input-to-output series

voltage to maintain regulation. This minimizes power dissipation in the pass device and may eliminate the need for a heat sink. Figure 10.25 shows the ADP1148 buck regulator configured for a 9V input and a 3.75V/1A output. The output drives an ADP3310 linear LDO regulator configured for 3.75V input and 3.3V/1A output. The input and output of the ADP3310 is shown in Figure 10.26. Notice that the regulator reduces the ripple from 40mV to approximately 5mV.

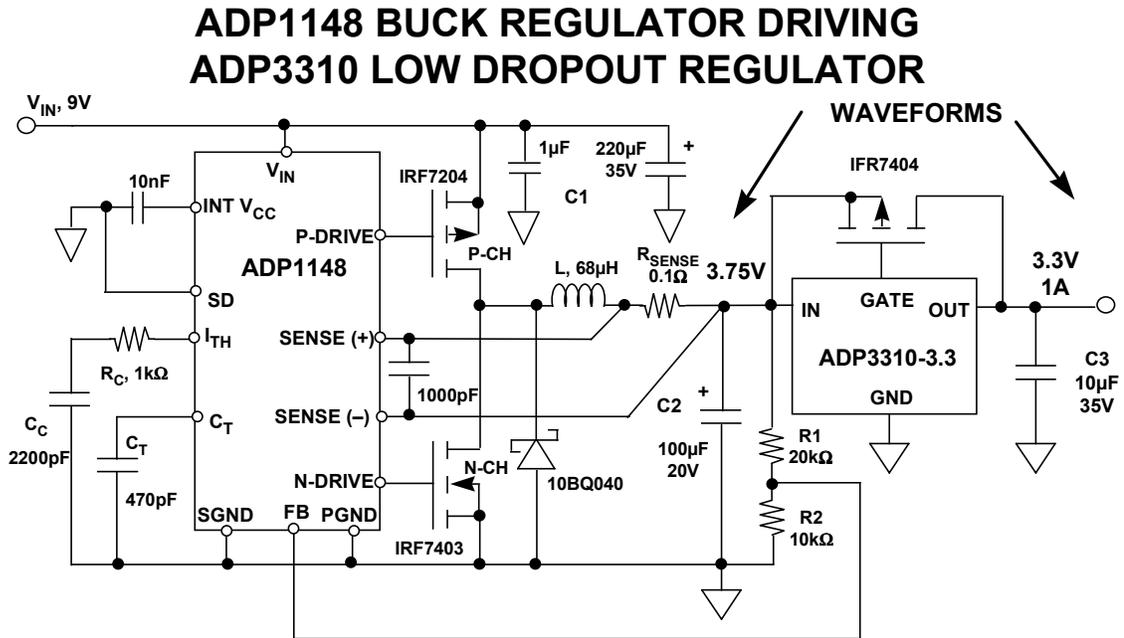


Figure 10.25

WAVEFORMS FOR ADP1148 BUCK REGULATOR DRIVING ADP3310 LOW DROPOUT REGULATOR

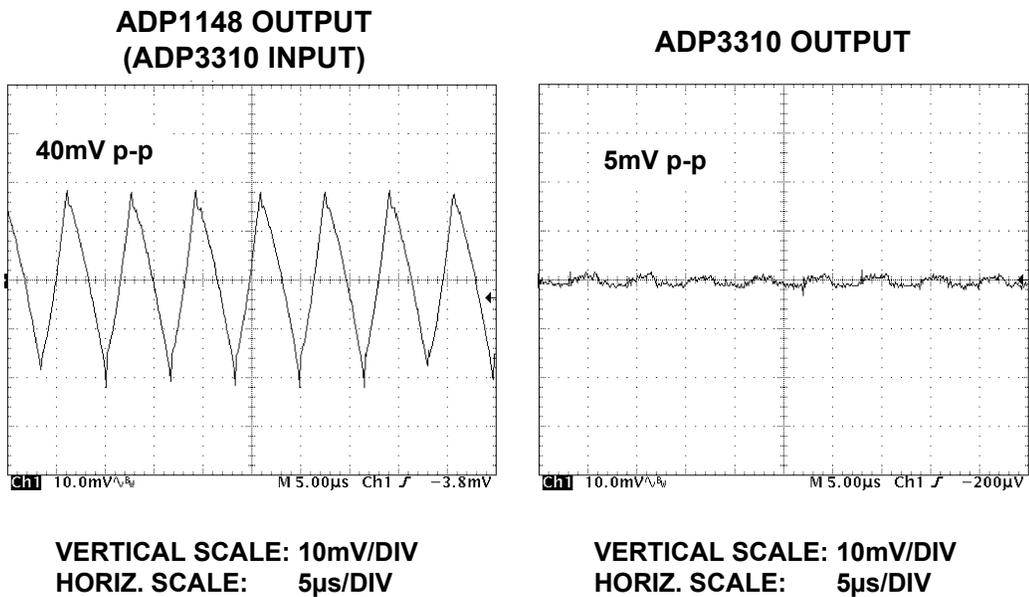


Figure 10.26

HARDWARE DESIGN TECHNIQUES

There are many tradeoffs in designing power supply filters. The success of any filter circuit is highly dependent upon a compact layout and the use of a large area ground plane. As has been stated earlier, all connections to the ground plane should be made as short as possible to minimize parasitic resistance and inductance.

Output ripple can be reduced by the addition of low ESL/ESR capacitors to the output. However, it may be more efficient to use an LC filter to accomplish the ripple reduction. In any case, proper component selection is critical. The inductor should not saturate under the maximum load current, and its DC resistance should be low enough as not to induce significant voltage drop. The capacitors should have low ESL and ESR and be rated to handle the required ripple current.

Low dropout linear post regulators provide both ripple reduction as well as better regulation and can be effective, provided the sacrifice in efficiency is not excessive.

Finally, it is difficult to predict the output ripple current analytically, and there is no substitute for a prototype using the real-world components. Once the filter is proven to provide the desired ripple attenuation (with some added safety margin), care must be taken that parts substitutions or vendor changes are not made in the final production units without first testing them in the circuit for equivalent performance.

SWITCHING SUPPLY FILTER SUMMARY

- **Proper Layout and Grounding (using Ground Plane) Mandatory**
- **Low ESL/ESR Capacitors Give Best Results**
- **Parallel Capacitors Lower ESR/ESL and Increase Capacitance**
- **External LC Filters Very Effective in Reducing Ripple**
- **Linear Post Regulation Effective for Noise Reduction and Best Regulation**
- **Completely Analytical Approach Difficult, Prototyping is Required for Optimum Results**
- **Once Design is Finalized, Do Not Switch Vendors or Use Parts Substitutions Without First Verifying Their Performance in Circuit**
- **High Frequency Localized Decoupling at IC Power Pins is Still Required**

Figure 10.27

Localized High Frequency Power Supply Filtering

The LC filters described in the previous section are useful in filtering switching regulator outputs. However, it may be desirable to place similar filters on the individual PC boards where the power first enters the board. Of course, if the switching regulator is placed on the PC board, then the LC filter should be an integral part of the regulator design.

Localized high frequency filters may also be required at each IC power pin (see Figure 10.28). Surface mount ceramic capacitors are ideal choices because of their low ESL. It is important to make the connections to the power pin and the ground plane as short as possible. In the case of the ground connection, a via directly to the ground plane is the shortest path. Routing the capacitor ground connection to another ground pin on the IC is not recommended due to the added inductance of the trace. In some cases, a ferrite bead in series with the power connection may also be desirable.

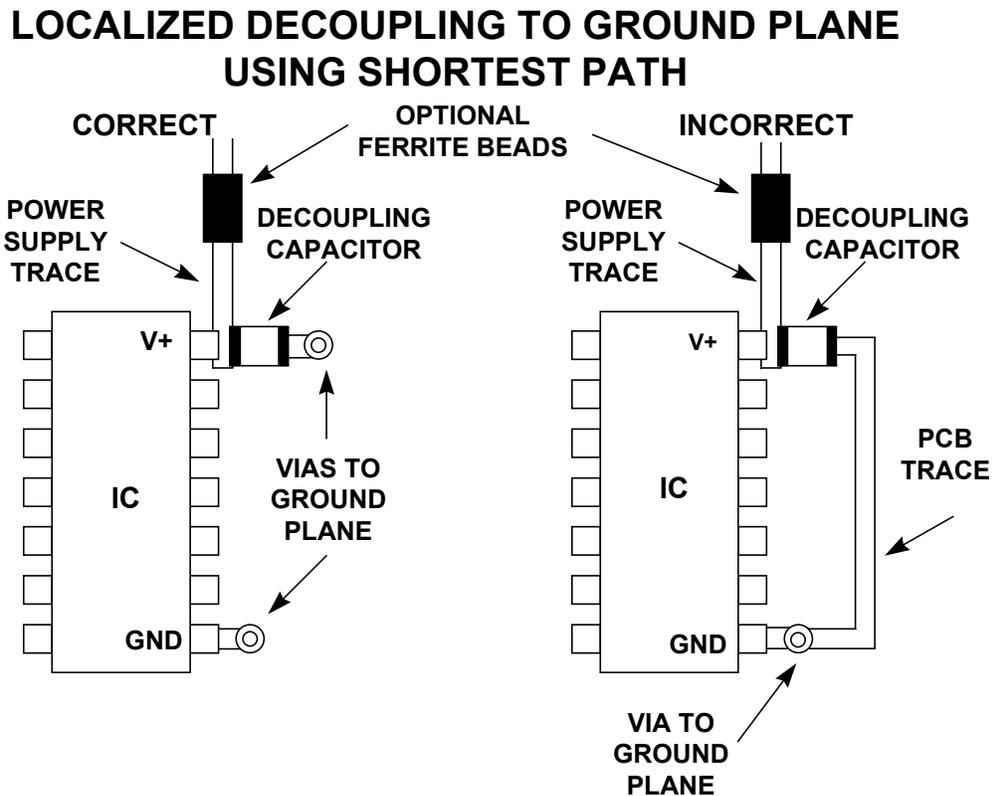


Figure 10.28

The following list summarizes the switching power supply filter layout/construction guidelines which will help ensure that the filter does the best possible job:

- (1) *Pick the highest electrical value and voltage rating for filter capacitors which is consistent with budget and space limits. This minimizes ESR, and maximizes filter performance. Pick chokes for low ΔL at the rated DC current, as well as low DCR.*
- (2) *Use short and wide PCB tracks to decrease voltage drops and minimize inductance. Make track widths at least 200 mils for every inch of track length for lowest DCR, and use 1 oz or 2 oz copper PCB traces to further reduce IR drops and inductance.*
- (3) *Use short leads or better yet, leadless components, to minimize lead inductance. This minimizes the tendency to add excessive ESL and/or ESR. Surface mount packages are preferred. Make all connections to the ground plane as short as possible.*

(4) Use a large-area ground plane for minimum impedance.

(5) Know what your components do over frequency, current and temperature variations! Make use of vendor component models for the simulation of prototype designs, and make sure that lab measurements correspond reasonably with the simulation. While simulation is not absolutely necessary, it does instill confidence in a design when correlation is achieved (see Reference 15).

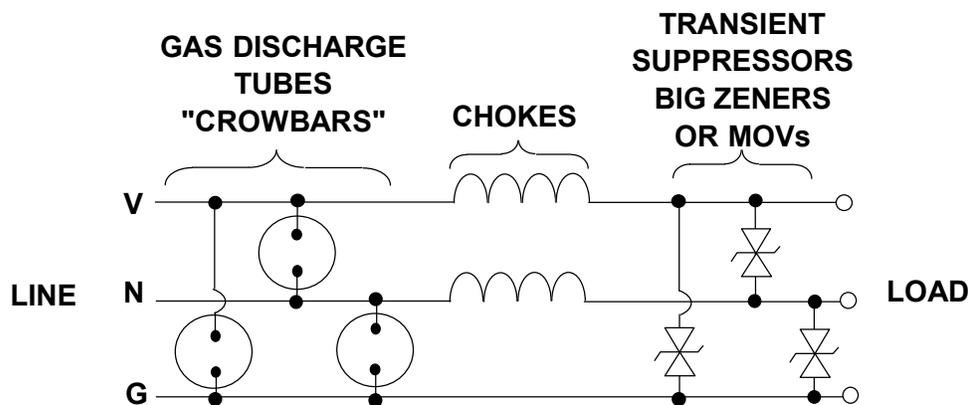
Filtering the AC Power Lines

The AC power line can also be an EMI entry/exit path! To remove this noise path and reduce emissions caused by the switching power supply or other circuits, a *power line filter* is required.

Figure 10.29 is an example of a hybrid power transient protection network commonly used in many applications where lightning transients or other power-line disturbances are prevalent. These networks can be designed to provide protection against transients as high as 10kV and as fast as 10ns. Gas discharge tubes (crowbars) and large geometry zener diodes or Transient Voltage Suppressors (TVSs) are used to provide both differential and common-mode protection. Metal-oxide varistors (MOVs) can be substituted for the zener diodes or TVSs in less critical, or in more compact designs. Chokes are used to limit the surge current until the gas discharge tubes fire.

POWER LINE DISTURBANCES CAN GENERATE EMI

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■ COMMON-MODE AND DIFFERENTIAL MODE PROTECTION

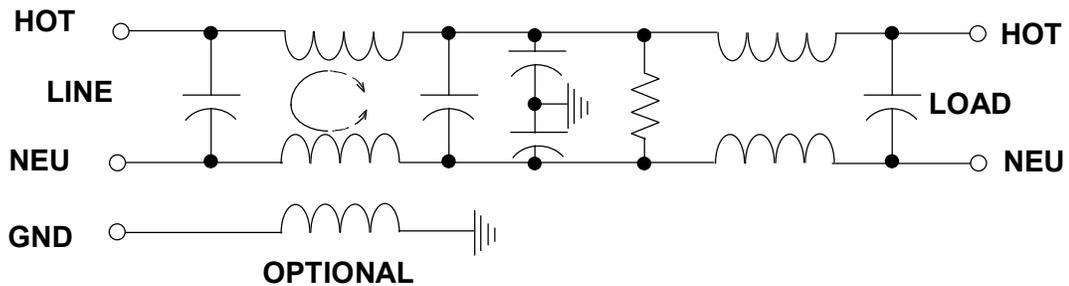
Figure 10.29

Commercial EMI filters, as illustrated in Figure 10.30, can be used to filter less catastrophic transients or high-frequency interference. These EMI filters provide both common-mode and differential mode filtering. An optional choke in the safety ground can provide additional protection against common-mode noise. The value of

this choke cannot be too large, however, because its resistance may affect power-line fault clearing. These filters work in both directions: they not only protect the equipment from surges on the power line but also prevent transients from the internal switching power supplies from corrupting the power line.

SCHEMATIC FOR A COMMERCIAL POWER LINE FILTER

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NOTE: OPTIONAL CHOKE ADDED FOR COMMON-MODE PROTECTION

Figure 10.30

Transformers provide the best common-mode power line isolation. They provide good protection at low frequencies (<1MHz), and for transients with rise and fall times greater than 300ns. Most motor noise and lightning transients are in this range, so isolation transformers work well for these types of disturbances. Although the isolation between input and output is galvanic, isolation transformers do not provide sufficient protection against extremely fast transients (<10ns) or those caused by high-amplitude electrostatic discharge (1 to 3ns). Isolation transformers can be designed for various levels of differential- or common-mode protection. For differential-mode noise rejection, the Faraday shield is connected to the neutral, and for common-mode noise rejection, the shield is connected to the safety ground.

It is important to remember that AC line power can potentially be lethal! Do not experiment without proper equipment and training! All components used in power line filters should be UL approved, and the best way to provide this is to specify a packaged UL approved filter. It should be installed in such a manner that it is the first circuit the AC line sees upon entering the equipment. Standard three wire IEC style line cords are designed to mate with three terminal male connectors integral to many line filters. This is the best way to achieve this function, as it automatically grounds the third wire to the shell of the filter and equipment chassis via a low inductance path.

HARDWARE DESIGN TECHNIQUES

Commercial power line filters are quite effective in reducing AC power-line noise. This noise generally has both common-mode and differential-mode components. Common-mode noise is noise that is found on any two of the three power connections (black, white, or green) with the same amplitude and polarity. In contrast, differential-mode noise is noise found only between two lines. By design, most commercially available filters address both noise modes (see Reference 16).

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3. Tantalum Electrolytic and Ceramic Capacitor Families, Kemet Electronics, Box 5928, Greenville, SC, 29606, (803) 963-6300.
4. Type HFQ Aluminum Electrolytic Capacitor and type V Stacked Polyester Film Capacitor, Panasonic, 2 Panasonic Way, Secaucus, NJ, 07094, (201) 348-7000.
5. OS-CON Aluminum Electrolytic Capacitor 93/94 Technical Book, Sanyo, 3333 Sanyo Road, Forrest City, AK, 72335, (501) 633-6634.
6. Ian Clelland, *Metalized Polyester Film Capacitor Fills High Frequency Switcher Needs*, **PCIM**, June 1992.
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9. Henry Ott, **Noise Reduction Techniques in Electronic Systems, 2d Ed.**, 1988, Wiley.
10. Fair-Rite Linear Ferrites Catalog, Fair-Rite Products, Box J, Wallkill, NY, 12886, (914) 895-2055, <http://www.fair-rite.com>.
11. Type EXCEL leaded ferrite bead EMI filter, and type EXC L leadless ferrite bead, Panasonic, 2 Panasonic Way, Secaucus, NJ, 07094, (201) 348-7000.
12. Steve Hageman, *Use Ferrite Bead Models to Analyze EMI Suppression*, **The Design Center Source**, MicroSim Newsletter, January, 1995.

HARDWARE DESIGN TECHNIQUES

13. Type 5250 and 6000-101K chokes, J. W. Miller, 306 E. Alondra Blvd., Gardena, CA, 90247, (310) 515-1720.
14. DIGI-KEY, PO Box 677, Thief River Falls, MN, 56701-0677, (800) 344-4539.
15. Tantalum Electrolytic Capacitor SPICE Models, Kemet Electronics, Box 5928, Greenville, SC, 29606, (803) 963-6300.
16. Eichhoff Electronics, Inc., 205 Hallene Road, Warwick, RI., 02886, (401) 738-1440, <http://www.eichhoff.com>.
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PREVENTING RFI RECTIFICATION

Walt Kester, Walt Jung, Chuck Kitchin

High frequency radio frequency interference (RFI) can seriously affect the DC performance of high accuracy circuits. Because of their relatively low bandwidth, precision operational amplifiers and instrumentation amplifiers will not accurately amplify RF signals in the MHz range. However, if these out-of-band signals are allowed to couple into the precision amplifier through either its input, output, or power supply pins, they can be rectified by various junctions in the amplifier and ultimately cause an unexplained and unwanted DC offset at the output. An excellent analysis of the phenomenon is found in Reference 1, but the purpose here is to show how proper filtering can be used to minimize or prevent these errors.

We have previously discussed how proper power supply decoupling techniques will minimize RFI on the IC power pins. Further discussion is required with respect to the amplifier inputs and outputs.

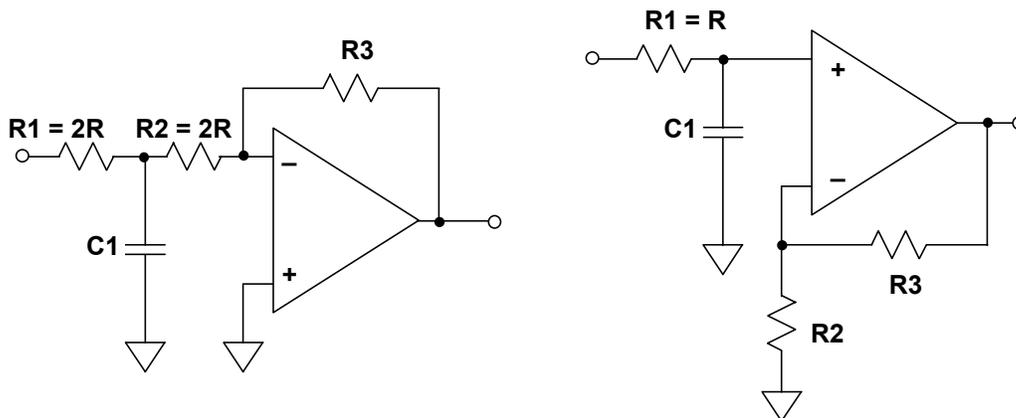
The best way to prevent rectification due to input RFI is to use a filter located close to the op amp input as shown in Figure 10.31. In the case of the inverting op amp, the filter capacitor C1 is placed between R1 and R2. The DC closed loop gain of the circuit is $-R3/(R1+R2)$. C1 is not connected directly to the inverting input of the op amp because that would result in instability. The filter bandwidth is chosen to be at least 100 times larger than the actual signal bandwidth to prevent signal attenuation. For the non-inverting configuration, the filter capacitor can be connected directly to the op amp input as shown.

It should be noted that a ferrite bead can be used instead of R1, however ferrite bead impedance is not well controlled and is generally no greater than 100Ω at 10MHz to 100MHz. This requires a large value capacitor to attenuate the lower frequencies.

Precision instrumentation amplifiers are particularly sensitive to common-mode RFI. Proper filtering is shown in Figure 10.32. Note that there is both common-mode filtering ($R1/C1$, $R2/C2$) and differential mode filtering ($R1+R2$, and C3). If $R1/R2$ and $C1/C2$ are not well matched, some of the input common-mode signal at V_{IN} will be converted to a differential one at the in-amp inputs. For this reason, C1 and C2 should be matched to within at least 5% of each other. R1 and R2 should be 1% metal film resistors to insure matching. Capacitor C3 attenuates the differential signal which can result from imperfect matching of the common-mode filters. In this type of filter, C3 should be much larger than C1 or C2 in order to ensure that any differential signal due to mismatching of the common-mode signals is sufficiently attenuated.

The overall filter bandwidth should be chosen to be at least 100 times the input signal bandwidth. The components should be symmetrically mounted on a PC board with a large area ground plane and placed very close to the in-amp input for optimum performance of the filter.

FILTERING AMPLIFIER INPUTS TO PREVENT RFI RECTIFICATION

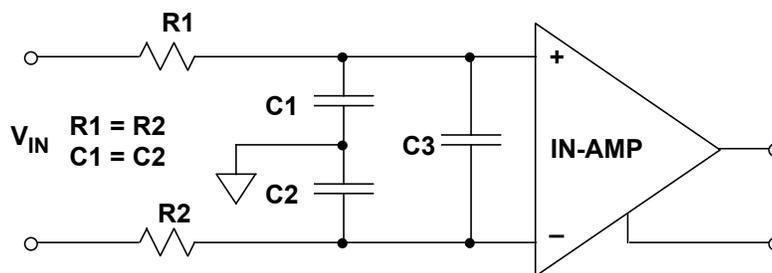


$$\text{FILTER BANDWIDTH} = \frac{1}{2\pi R C1}$$

> 100 × SIGNAL BANDWIDTH

Figure 10.31

FILTERING IN-AMP INPUTS



$$\tau_{\text{DIFF}} = (R1 + R2) C3$$

$$\tau_{\text{CM}} = R1 \cdot C1 = R2 \cdot C2 \quad \tau_{\text{DIFF}} \gg \tau_{\text{CM}}$$

R1·C1 SHOULD MATCH R2·C2

R1 = R2 SHOULD BE 1% RESISTORS
C1 = C2 SHOULD BE 5% CAPACITORS

$$\text{DIFFERENTIAL FILTER BANDWIDTH} = \frac{1}{2\pi (R1 + R2) \left[\frac{C1 \cdot C2}{C1 + C2} + C3 \right]}$$

Figure 10.32

Figure 10.33 shows an actual filter for use with the AD620 in-amp. The common-mode rejection was tested by applying a 1V p-p common-mode signal to the input resistors. The AD620 gain was 1000. The RTI offset voltage of the in-amp was measured as the frequency of the sinewave source was varied from DC to 20MHz. The maximum RTI input offset voltage shift was 1.5µV. The filter bandwidth was approximately 400Hz.

Common-mode chokes offer a simple, one component alternative to RC passive filters. Selecting the proper common-mode choke is critical, however. The choke used in the circuit of Figure 10.34 was a Pulse Engineering B4001 designed for XDSL data receivers (through-hole mount). The B4003 is an equivalent surface mount choke. The maximum RTI offset shift measured from DC to 20MHz was 4.5µV. Unlike the RC filter of Figure 10.32, the choke-based filter offers no differential mode filtration, as shown.

COMMON AND DIFFERENTIAL MODE FILTER WITH AD620

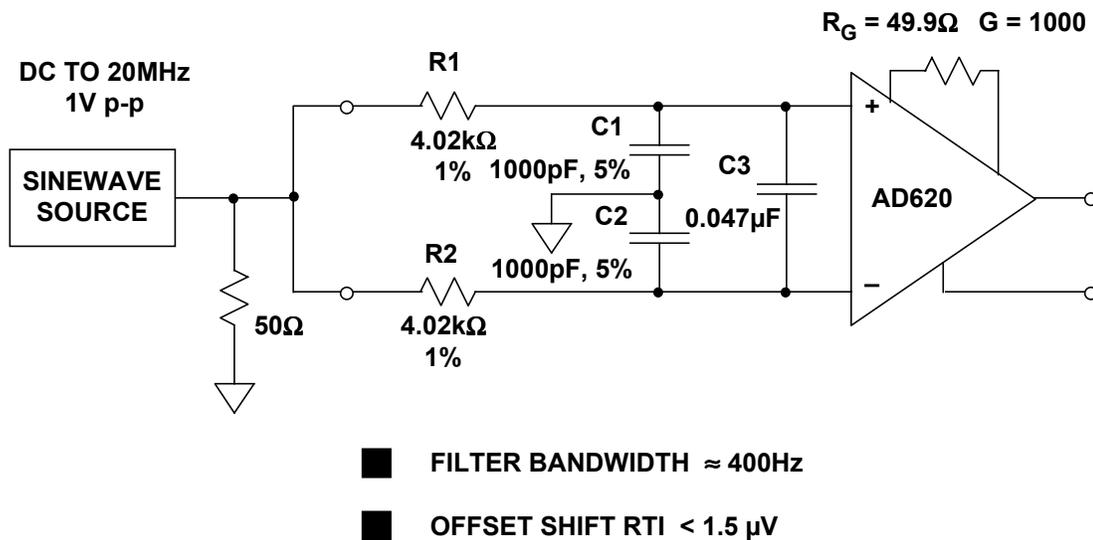


Figure 10.33

In addition to filtering the inputs and the power pins, amplifier outputs need to be protected from RFI, especially if they must drive long lengths of cable. RFI on the output can couple into the amplifier where it is rectified and appears again on the output as a DC offset shift. A resistor or ferrite bead in series with the output is the simplest output filter. Adding a capacitor as shown in Figure 10.35 improves this filter, but the capacitor should not be connected to the op-amp side of the resistor because it may cause the amplifier to become unstable. Many amplifiers are sensitive to direct output capacitive loads, so this condition should be avoided unless the amplifier data sheet clearly specifies that the output is insensitive to capacitive loading.

COMMON MODE CHOKE WITH AD620

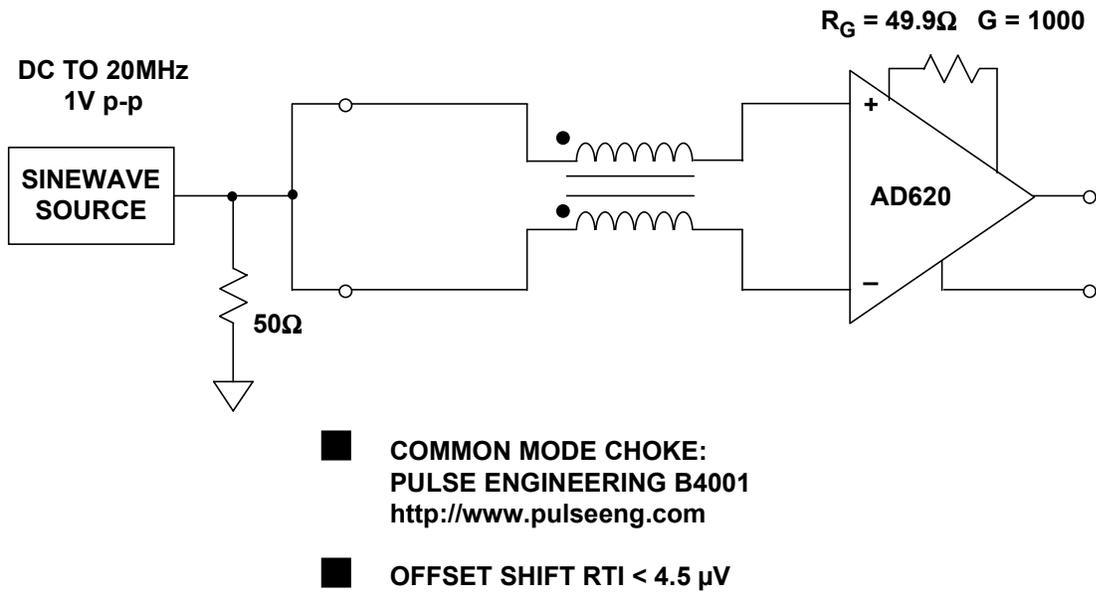


Figure 10.34

FILTERING AMPLIFIER OUTPUTS PROTECTS AGAINST EMI/RFI EMISSION AND SUSCEPTIBILITY

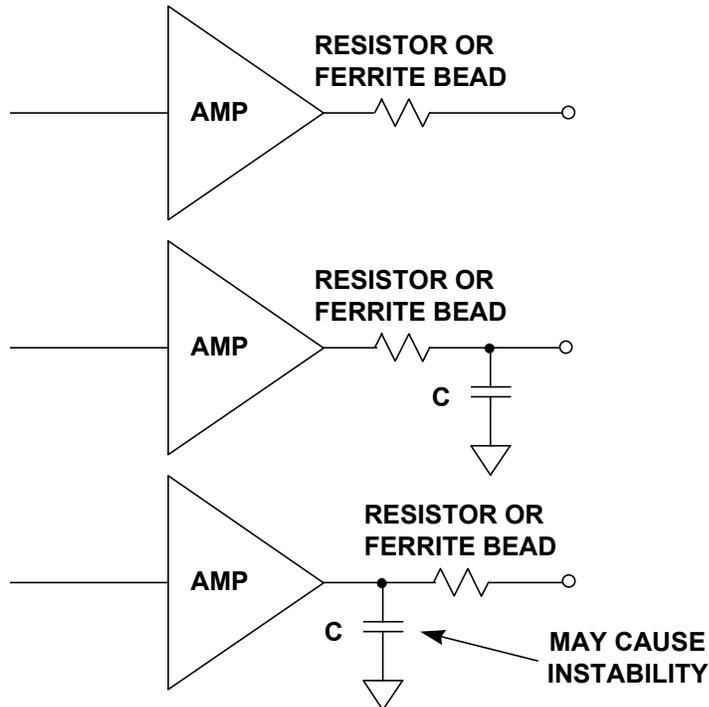


Figure 10.35

REFERENCES ON RFI RECTIFICATION

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DEALING WITH HIGH SPEED LOGIC

Much has been written about terminating printed circuit board traces in their characteristic impedance to avoid reflections. A good rule-of-thumb to determine when this is necessary is as follows: *Terminate the line in its characteristic impedance when the one-way propagation delay of the PCB track is equal to or greater than one-half the applied signal rise/fall time (whichever edge is faster)*. A conservative approach is to use a 2 inch (PCB track length)/nanosecond (rise-, fall-time) criterion. For example, PCB tracks for high-speed logic with rise/fall time of 5ns should be terminated in their characteristic impedance if the track length is equal to or greater than 10 inches (including any meanders). The 2 inch/nanosecond track length criterion is summarized in Figure 10.36 for a number of logic families.

LINE TERMINATION SHOULD BE USED WHEN LENGTH OF PCB TRACK EXCEEDS 2 inches/ns

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DIGITAL IC FAMILY	t _r , t _s (ns)	PCB TRACK LENGTH (inches)	PCB TRACK LENGTH (cm)
GaAs	0.1	0.2	0.5
ECL	0.75	1.5	3.8
Schottky	3	6	15
FAST	3	6	15
AS	3	6	15
AC	4	8	20
ALS	6	12	30
LS	8	16	40
TTL	10	20	50
HC	18	36	90

t_r = rise time of signal in ns

t_f = fall time of signal in ns

For analog signals @ f_{max}, calculate t_r = t_f = 0.35 / f_{max}

Figure 10.36

This same 2 inch/nanosecond rule of thumb should be used with analog circuits in determining the need for transmission line techniques. For instance, if an amplifier must output a maximum frequency of f_{max}, then the equivalent risetime, t_r, can be calculated using the equation t_r = 0.35/f_{max}.

The maximum PCB track length is then calculated by multiplying the risetime by 2 inch/nanosecond. For example, a maximum output frequency of 100MHz corresponds to a risetime of 3.5ns, and a track carrying this signal greater than 7 inches should be treated as a transmission line.

Equation 10.1 can be used to determine the characteristic impedance of a PCB track separated from a power/ground plane by the board's dielectric (microstrip transmission line):

$$Z_0(\Omega) = \frac{87}{\sqrt{\epsilon_r + 1.41}} \ln \left[\frac{5.98d}{0.89w + t} \right] \quad \text{Eq. 10.1}$$

where ϵ_r = dielectric constant of printed circuit board material;
d = thickness of the board between metal layers, in mils;
w = width of metal trace, in mils; and
t = thickness of metal trace, in mils.

The one-way transit time for a single metal trace over a power/ground plane can be determined from Eq.10.2:

$$t_{pd}(\text{ns / ft}) = 1.017\sqrt{0.475\epsilon_r + 0.67} \quad \text{Eq. 10.2}$$

For example, a standard 4-layer PCB board might use 8-mil wide, 1 ounce (1.4 mils) copper traces separated by 0.021" FR-4 ($\epsilon_r=4.7$) dielectric material. The characteristic impedance and one-way transit time of such a signal trace would be 88 Ω and 1.7ns/ft (7"/ns), respectively.

The best ways to keep sensitive analog circuits from being affected by fast logic are to physically separate the two and to use no faster logic family than is dictated by system requirements. In some cases, this may require the use of several logic families in a system. An alternative is to use series resistance or ferrite beads to slow down the logic transitions where the speed is not required. Figure 10.37 shows two methods. In the first, the series resistance and the input capacitance of the gate form a lowpass filter. Typical CMOS input capacitance is 10pF. Locate the series resistor close to the driving gate. The resistor minimizes transient currents and may eliminate the necessity of using transmission line techniques. The value of the resistor should be chosen such that the rise and fall times at the receiving gate are fast enough to meet system requirement, but no faster. Also, make sure that the resistor is not so large that the logic levels at the receiver are out of specification because of the source and sink current which must flow through the resistor.

SLOW DOWN FAST LOGIC EDGES TO MINIMIZE EMI/RFI PROBLEMS

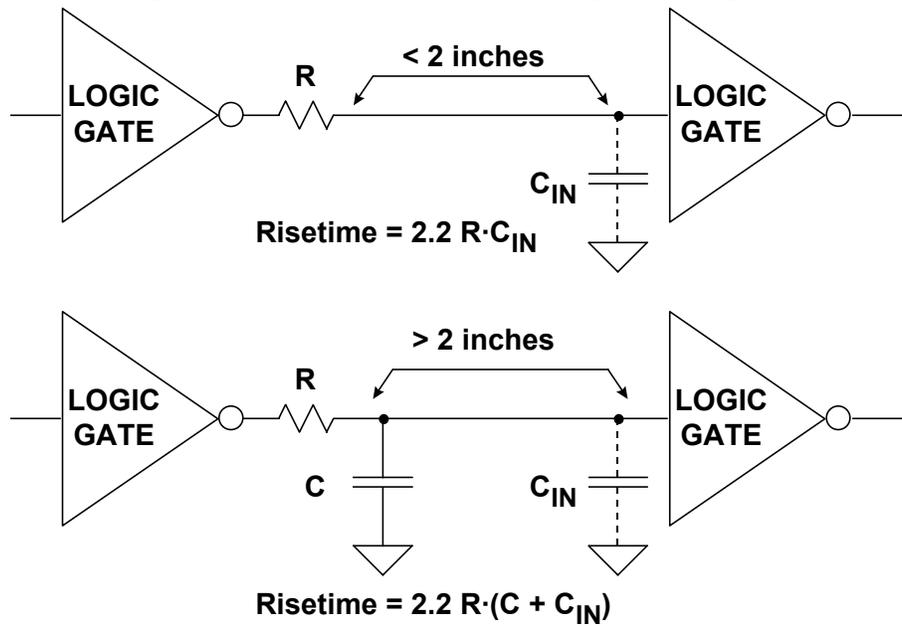


Figure 10.37

A REVIEW OF SHIELDING CONCEPTS

The concepts of shielding effectiveness presented next are background material. Interested readers should consult References 1,3, and 4 cited at the end of the section for more detailed information.

Applying the concepts of shielding requires an understanding of the source of the interference, the environment surrounding the source, and the distance between the source and point of observation (the receptor or victim). If the circuit is operating close to the source (in the near-, or induction-field), then the field characteristics are determined by the source. If the circuit is remotely located (in the far-, or radiation-field), then the field characteristics are determined by the transmission medium.

A circuit operates in a near-field if its distance from the source of the interference is less than the wavelength (λ) of the interference divided by 2π , or $\lambda/2\pi$. If the distance between the circuit and the source of the interference is larger than this quantity, then the circuit operates in the far field. For instance, the interference caused by a 1ns pulse edge has an upper bandwidth of approximately 350MHz. The wavelength of a 350MHz signal is approximately 32 inches (the speed of light is approximately 12"/ns). Dividing the wavelength by 2π yields a distance of approximately 5 inches, the boundary between near- and far-field. If a circuit is within 5 inches of a 350MHz interference source, then the circuit operates in the near-field of the interference. If the distance is greater than 5 inches, the circuit operates in the far-field of the interference.

Regardless of the type of interference, there is a characteristic impedance associated with it. The characteristic, or wave impedance of a field is determined by the ratio of its electric (or E-) field to its magnetic (or H-) field. In the far field, the ratio of the electric field to the magnetic field is the characteristic (wave impedance) of free space, given by $Z_0 = 377\Omega$. In the near field, the wave-impedance is determined by the nature of the interference and its distance from the source. If the interference source is high-current and low-voltage (for example, a loop antenna or a power-line transformer), the field is predominately magnetic and exhibits a wave impedance which is less than 377Ω . If the source is low-current and high-voltage (for example, a rod antenna or a high-speed digital switching circuit), then the field is predominately electric and exhibits a wave impedance which is greater than 377Ω .

Conductive enclosures can be used to shield sensitive circuits from the effects of these external fields. These materials present an impedance mismatch to the incident interference because the impedance of the shield is lower than the wave impedance of the incident field. The effectiveness of the conductive shield depends on two things: First is the loss due to the *reflection* of the incident wave off the shielding material. Second is the loss due to the *absorption* of the transmitted wave *within* the shielding material. Both concepts are illustrated in Figure 10.38. The amount of reflection loss depends upon the type of interference and its wave impedance. The amount of absorption loss, however, is independent of the type of interference. It is the same for near- and far-field radiation, as well as for electric or magnetic fields.

REFLECTION AND ABSORPTION ARE THE TWO PRINCIPAL SHIELDING MECHANISMS

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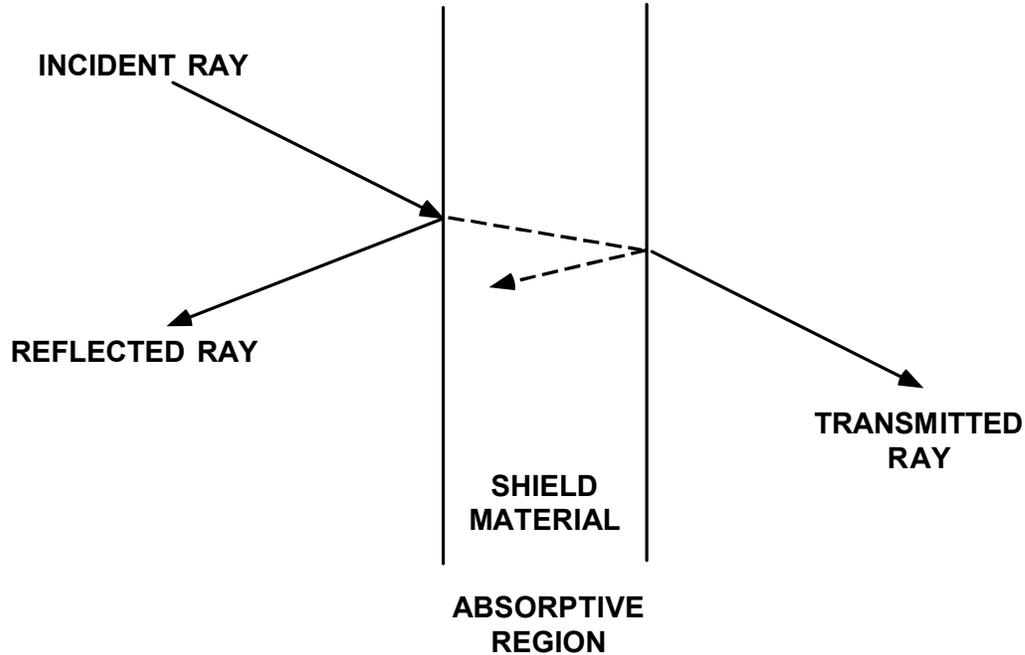


Figure 10.38

Reflection loss at the interface between two media depends on the difference in the characteristic impedances of the two media. For electric fields, reflection loss depends on the frequency of the interference and the shielding material. This loss can be expressed in dB, and is given by:

$$R_e(\text{dB}) = 322 + 10\log_{10} \left[\frac{\sigma_r}{\mu_r f^3 r^2} \right] \quad \text{Eq. 10.3}$$

where σ_r = relative conductivity of the shielding material, in Siemens per meter;
 μ_r = relative permeability of the shielding material, in Henries per meter;
 f = frequency of the interference, and
 r = distance from source of the interference, in meters

For magnetic fields, the loss depends also on the shielding material and the frequency of the interference. Reflection loss for magnetic fields is given by:

$$R_m(\text{dB}) = 14.6 + 10\log_{10} \left[\frac{f r^2 \sigma_r}{\mu_r} \right] \quad \text{Eq. 10.4}$$

and, for plane waves ($r > \lambda/2\pi$), the reflection loss is given by:

$$R_{pw}(\text{dB}) = 168 + 10\log_{10} \left[\frac{\sigma_r}{\mu_r f} \right] \quad \text{Eq. 10.5}$$

Absorption is the second loss mechanism in shielding materials. Wave attenuation due to absorption is given by:

$$A(\text{dB}) = 3.34 t \sqrt{\sigma_r \mu_r f} \quad \text{Eq. 10.6}$$

where t = thickness of the shield material, in inches. This expression is valid for plane waves, electric and magnetic fields. Since the intensity of a transmitted field decreases exponentially relative to the thickness of the shielding material, the absorption loss in a shield one skin-depth (δ) thick is 9dB. Since absorption loss is proportional to thickness and inversely proportional to skin depth, increasing the thickness of the shielding material improves shielding effectiveness at high frequencies.

Reflection loss for plane waves in the far field decreases with increasing frequency because the shield impedance, Z_s , increases with frequency. Absorption loss, on the other hand, increases with frequency because skin depth decreases. For electric fields and plane waves, the primary shielding mechanism is reflection loss, and at high frequencies, the mechanism is absorption loss. For these types of interference, high conductivity materials, such as copper or aluminum, provide adequate shielding. At low frequencies, both reflection and absorption loss to magnetic fields is low; thus, it is very difficult to shield circuits from low-frequency magnetic fields. In these applications, high-permeability materials that exhibit low-reluctance provide the best protection. These low-reluctance materials provide a magnetic shunt path that diverts the magnetic field away from the protected circuit. Some characteristics of metallic materials commonly used for shielded enclosures are shown in Figure 10.39.

A properly shielded enclosure is very effective at preventing external interference from disrupting its contents as well as confining any internally-generated interference. However, in the real world, openings in the shield are often required to accommodate adjustment knobs, switches, connectors, or to provide ventilation. Unfortunately, these openings may compromise shielding effectiveness by providing paths for high-frequency interference to enter the instrument.

**CONDUCTIVITY AND PERMEABILITY FOR
VARIOUS SHIELDING MATERIALS**

MATERIAL	RELATIVE CONDUCTIVITY	RELATIVE PERMEABILITY
Copper	1	1
Aluminum	1	0.61
Steel	0.1	1,000
Mu-Metal	0.03	20,000

Conductivity: Ability to Conduct Electricity

Permeability: Ability to Absorb Magnetic Energy

Figure 10.39

The longest dimension (not the total area) of an opening is used to evaluate the ability of external fields to enter the enclosure, because the openings behave as slot antennas. Equation 10.7 can be used to calculate the shielding effectiveness, or the susceptibility to EMI leakage or penetration, of an opening in an enclosure:

$$\text{Shielding Effectiveness (dB)} = 20 \log_{10} \left(\frac{\lambda}{2 \cdot L} \right) \quad \text{Eq. 10.7}$$

where λ = wavelength of the interference and
L = maximum dimension of the opening

Maximum radiation of EMI through an opening occurs when the longest dimension of the opening is equal to one half-wavelength of the interference frequency (0dB shielding effectiveness). A rule-of-thumb is to keep the longest dimension less than 1/20 wavelength of the interference signal, as this provides 20dB shielding effectiveness. Furthermore, a few small openings on each side of an enclosure is preferred over many openings on one side. This is because the openings on different sides radiate energy in different directions, and as a result, shielding effectiveness is not compromised. If openings and seams cannot be avoided, then conductive gaskets, screens, and paints alone or in combination should be used judiciously to limit the longest dimension of any opening to less than 1/20 wavelength. Any cables, wires, connectors, indicators, or control shafts penetrating the enclosure should have circumferential metallic shields physically bonded to the enclosure at the point of entry. In those applications where unshielded cables/wires are used, then filters are recommended at the point of shield entry.

General Points on Cables and Shields

Although covered in more detail later, the improper use of cables and their shields is a significant contributor to both radiated and conducted interference. Rather than developing an entire treatise on these issues, the interested reader should consult References 1,2, 4, and 5. As illustrated in Figure 10.40, effective cable and enclosure shielding confines sensitive circuitry and signals within the entire shield without compromising shielding effectiveness. As shown in the diagram, the enclosures and the shield must be grounded properly, otherwise they will act as an antenna and make the radiated and conducted interference problem worse.

**"ELECTRICALLY LONG" OR "ELECTRICALLY SHORT"
APPLICATION**

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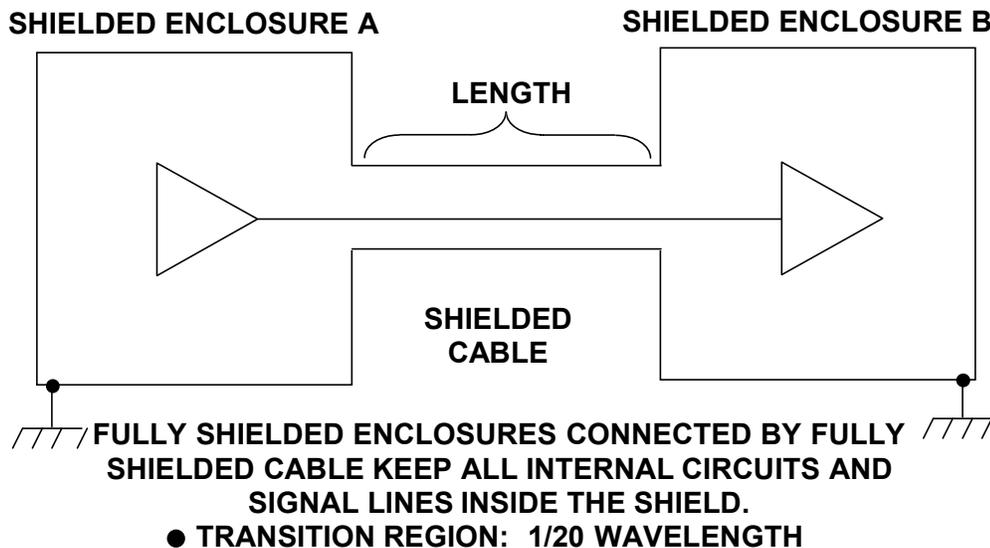


Figure 10.40

Depending on the type of interference (pickup/radiated, low/high frequency), proper cable shielding is implemented differently and is very dependent on the length of the cable. The first step is to determine whether the length of the cable is *electrically short* or *electrically long* at the frequency of concern. A cable is considered *electrically short* if the length of the cable is less than 1/20 wavelength of the highest frequency of the interference, otherwise it is *electrically long*. For example, at 50/60Hz, an *electrically short* cable is any cable length less than 150 miles, where the primary coupling mechanism for these low frequency electric fields is capacitive. As such, for any cable length less than 150 miles, the amplitude of the interference will be the same over the entire length of the cable.

In those applications where the length of the cable is *electrically long*, or protection against high-frequency interference is required, then the preferred method is to connect the cable shield to low-impedance points at both ends (direct connection at the driving end, and capacitive connection at the receiver). Otherwise, unterminated

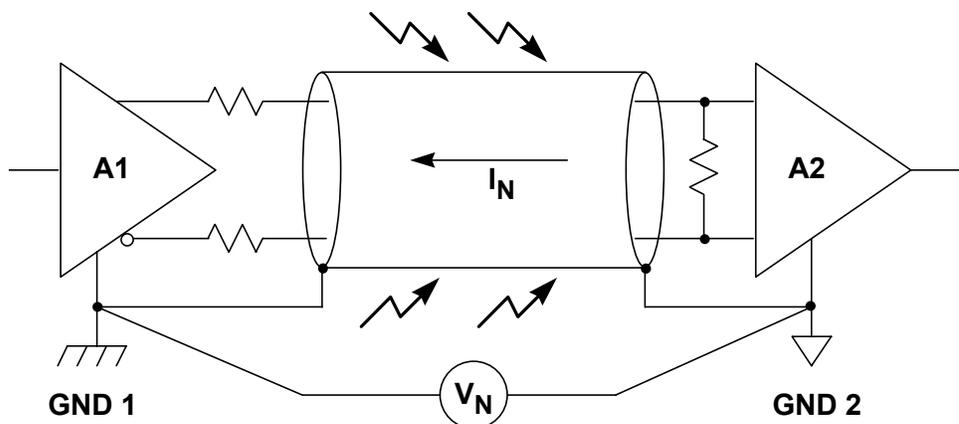
HARDWARE DESIGN TECHNIQUES

transmission lines effects can cause reflections and standing waves along the cable. At frequencies of 10MHz and above, circumferential (360°) shield bonds and metal connectors are required to main low-impedance connections to ground.

In summary, for protection against low-frequency (<1MHz), electric-field interference, grounding the shield at one end is acceptable. For high-frequency interference (>1MHz), the preferred method is grounding the shield at both ends, using 360° circumferential bonds between the shield and the connector, and maintaining metal-to-metal continuity between the connectors and the enclosure.

Grounding the shield at both ends, however, can create a low frequency ground loop in a practical situation as shown in Figure 10.41.

GROUND LOOPS IN SHIELDED TWISTED PAIR CABLE



■ V_N Causes Current in Shield (Usually 50/60Hz)

■ Differential Error Voltage is Produced at Input of A2 Unless:

- ◆ A1 Output is Perfectly Balanced and
- ◆ A2 Input is Perfectly Balanced and
- ◆ Cable is Perfectly Balanced

Figure 10.41

As discussed above, cable shields can be subjected to both low and high frequency interference. Good design practice requires that the shield be grounded at both ends if the cable is electrically long to the interference frequency, as is usually the case with RF interference.

When two systems A1 and A2 are remote from each other, however, there is usually a difference in the ground potentials at each system. The frequency of this potential difference is generally the line frequency (50Hz or 60Hz) and multiples thereof. If the shield is grounded at both ends as shown, however, a noise current flows through the shield. In a perfectly balanced system, the common-mode rejection of the system is infinite, and this current produces no differential error at the receiver A2. However, perfect balance is never achieved in the driver, its impedance, the cable, or the receiver, so a certain portion of the shield current will appear as a

differential signal at the input of A2. The following examples illustrate the correct way to ground the shield under various conditions.

Figure 10.42 shows a remote passive RTD sensor connected to a bridge and conditioning circuit by a shielded cable. The proper grounding method is shown in the upper part of the figure, where the shield is grounded at the receiving end. However, safety considerations may require that the remote end of the shield be grounded. If this is the case, the receiving end can be grounded with a low inductance ceramic capacitor ($0.01\mu\text{F}$ to $0.1\mu\text{F}$). The capacitor acts as a ground to RF signals on the shield but blocks line frequency current to flow in the shield. This technique is often referred to as a *hybrid ground*.

In the case of an active remote sensor (Figure 10.43), the hybrid ground is also appropriate, either for a balanced or single-ended driver. The capacitor breaks the DC ground loop in both cases. In both cases, the line is driven from an impedance of R_S , split between legs. In the case of the bottom diagram, the $R_S/2$ resistor in the return leg can only be used for applications with a balanced receiver, as shown.

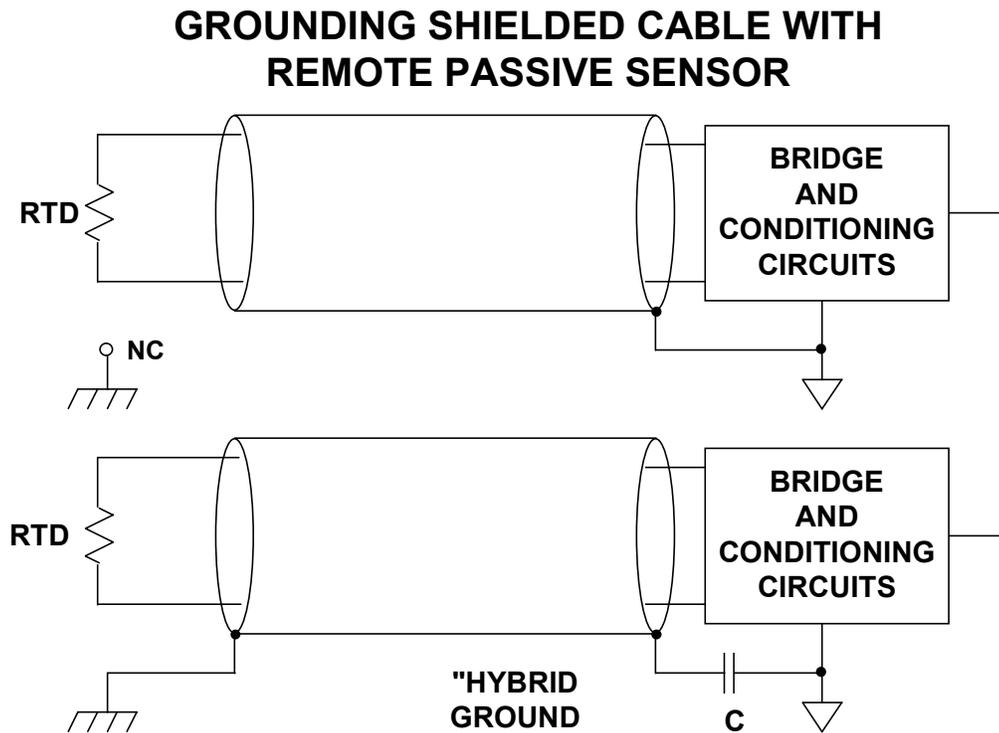


Figure 10.42

Coaxial cables are different from shielded twisted pair cables in that the signal return current path is through the shield. For this reason, the ideal situation is to ground the shield at the driving end and allow the shield to float at the differential receiver (A2) as shown in Figure 10.44. For this technique to work, however, the receiver must be differential and have good high frequency common mode rejection. If the receiver is a single-ended type, there is no choice but to ground the coaxial cable shield at both ends.

GROUNDING SHIELDED CABLE WITH REMOTE ACTIVE SENSOR

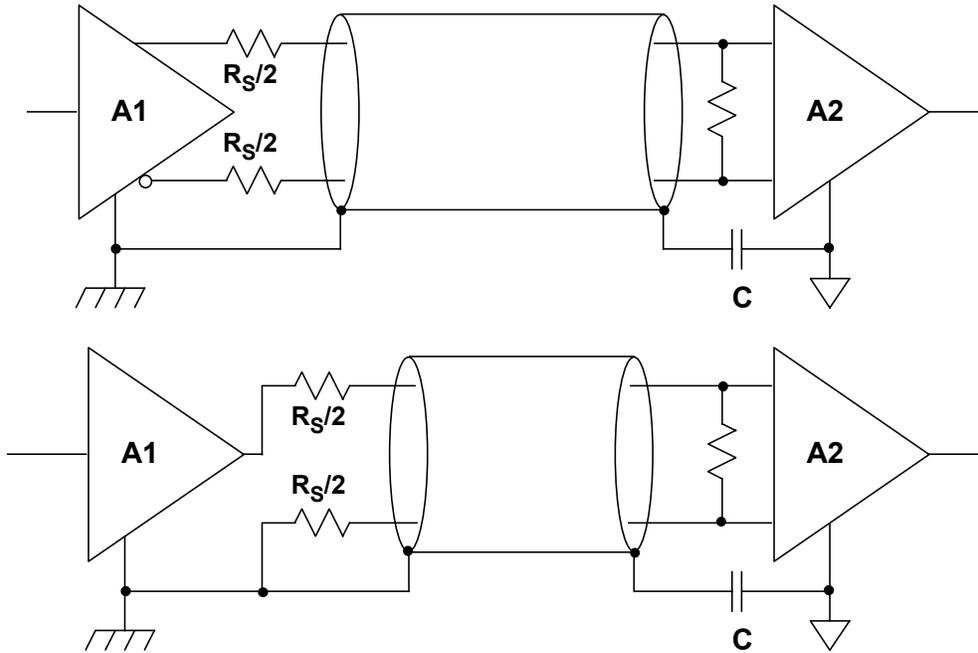


Figure 10.43

COAXIAL CABLE GROUNDING

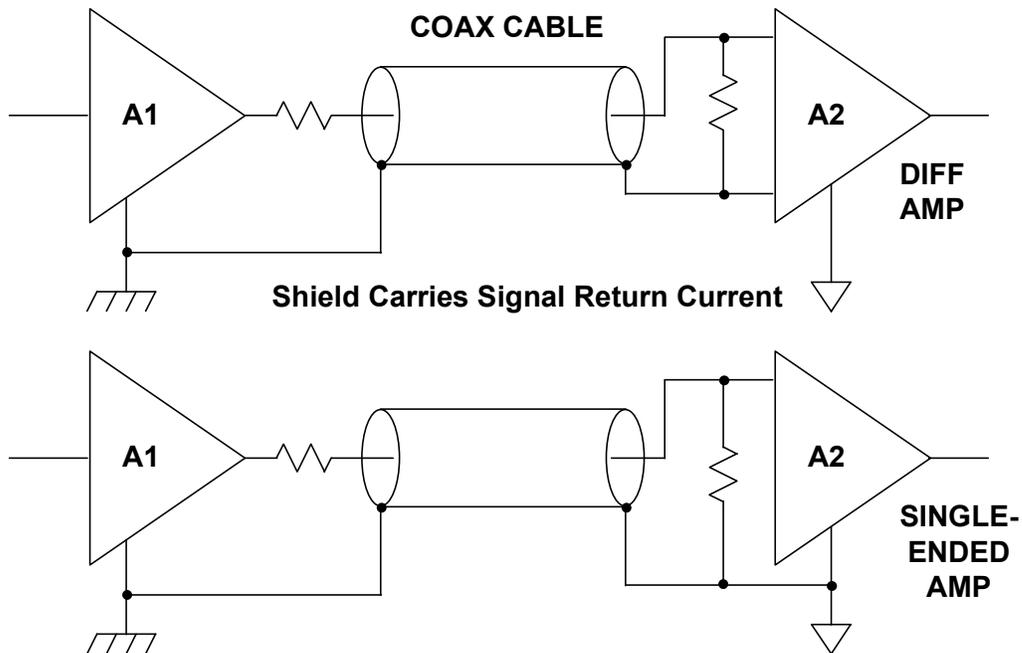


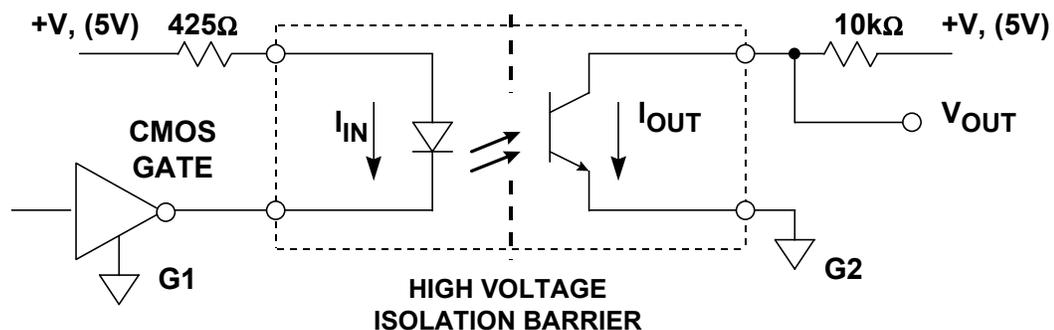
Figure 10.44

Digital Isolation Techniques

Another way to break ground loops is to use isolation techniques. Analog isolation amplifiers find many applications where a high degree of isolation is required, such as in medical instrumentation. Digital isolation techniques offer a reliable method of transmitting digital signals over interfaces without introducing ground noise.

Optoisolators are useful and available in a wide variety of styles and packages. Current is applied to an LED transmitter as shown in Figure 10.45. The light output is received by a phototransistor. Isolation voltages range from 5000V to 7000V. In the circuit, the LED is driven with a current of approximately 10mA. This produces a light output sufficient to saturate the phototransistor. Although excellent for digital signals, optoisolators are too nonlinear for most analog applications. One should realize that since the phototransistor is operated in a saturated mode, rise and fall-times can range from 10 μ s to 20 μ s in some slower devices, so the proper optoisolator for the application must be selected.

ISOLATION USING OPTOISOLATORS



- Uses Light for Transmission Over a High Voltage Barrier
- The LED is the Transmitter, and the Phototransistor is the Receiver
- High Voltage Isolation: 5000V to 7000V
- Non-Linear -- Best for Digital or Frequency Information
- Rise and Fall-times can be 10 to 20 μ s in Slower Devices
- Example: Siemens IL-1 (<http://www.siemens.com>)

Figure 10.45

The AD260/AD261 family of digital isolators isolates five digital control signals to/from high speed DSPs, microcontrollers, or microprocessors. The AD260 also has a 1.5W transformer for a 3.5kV isolated external DC/DC power supply circuit.

HARDWARE DESIGN TECHNIQUES

Each line of the AD260 can handle digital signals up to 20MHz with a propagation delay of only 14ns which allows for extremely fast data transmission. Output waveform symmetry is maintained to within ± 1 ns of the input so the AD260 can be used to accurately isolate time-based pulse width modulator (PWM) signals.

A simplified schematic of one channel of the AD260/AD261 is shown in Figure 10.46. The data input is passed through a schmitt trigger circuit, through a latch, and a special transmitter circuit which differentiates the edges of the digital input signal and drives the primary winding of a proprietary transformer with a "set-high/set-low" signal. The secondary of the isolation transformer drives a receiver with the same "set-hi/set-low" data which regenerates the original logic waveform. An internal circuit operates in the background which interrogates all inputs about every $5\mu\text{s}$ and in the absence of logic transitions, sends appropriate "set-hi/set-low" data across the interface. Recovery time from a fault condition or at power-up is thus between $5\mu\text{s}$ and $10\mu\text{s}$.

The power transformer (available on the AD260) is designed to operate between 150kHz and 250kHz and will easily deliver more than 1W of isolated power when driven push-pull (5V) on the transmitter side. Different transformer taps, rectifier and regulator schemes will provide combinations of $\pm 5\text{V}$, 15V, 24V, or even 30V or higher. The output voltage when driven with a low voltage-drop drive will be 37V p-p across the entire secondary with a 5V push-pull drive.

AD260/AD261 DIGITAL ISOLATORS

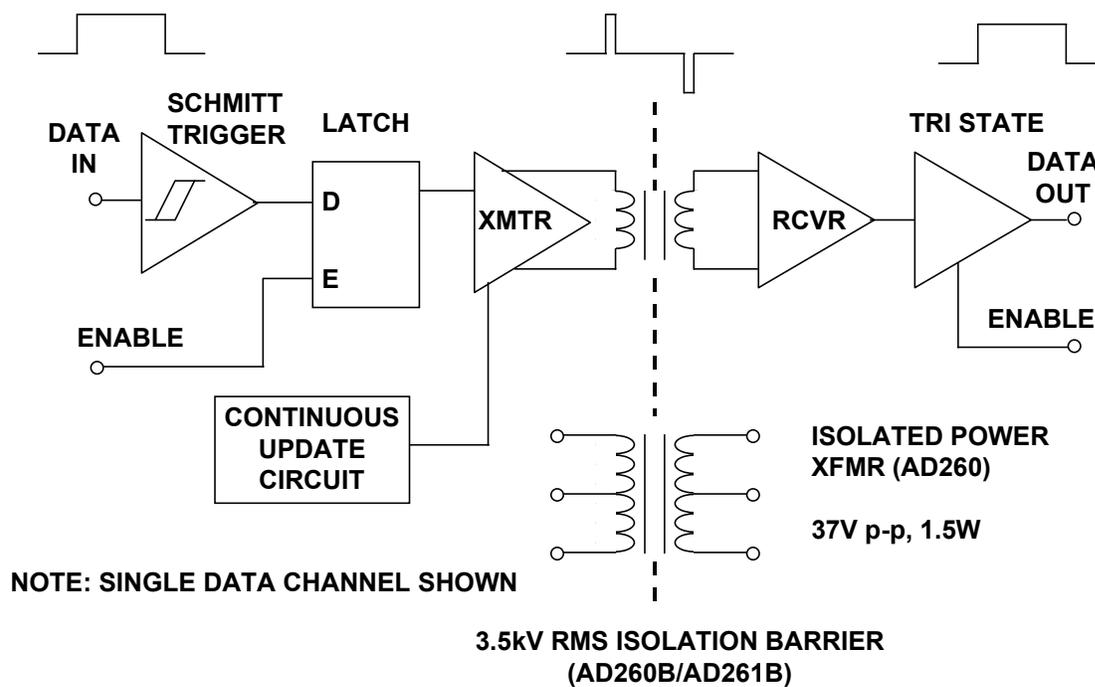


Figure 10.46

AD260/AD261 DIGITAL ISOLATOR KEY SPECIFICATIONS

- Isolation Test Voltage to 3.5kV RMS (AD260B/AD261B)
- Five Isolated Digital Lines Available in 6 Input/Output Configurations
- Logic Signal Frequency: 20MHz Max.
- Isolated Power Transformer: 37V p-p, 1.5W (AD260)
- Waveform Edge Transmission Symmetry: ± 1 ns
- Propagation Delay: 14ns
- Rise and Fall-Times < 5ns

Figure 10.47

REFERENCES ON EMI/RFI AND SHIELDING

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5. Ralph Morrison, **Grounding And Shielding Techniques In Instrumentation, Fourth Edition**, New York, John Wiley & Sons, 1998.
6. **Amplifier Applications Guide**, Chapter XI, pg. 61, Analog Devices, Incorporated, Norwood, MA, 1992.
7. B.Slattery and J.Wynne, *Design and Layout of a Video Graphics System for Reduced EMI*, Analog Devices Application Note AN-333.

HARDWARE DESIGN TECHNIQUES

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15. Neil Muncy, *Noise Susceptibility in Analog and Digital Signal Processing Systems*, presented at 97th **Audio Engineering Society Convention**, Nov. 1994.
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OVERVOLTAGE PROTECTION

Walt Kester, Wes Freeman, Joe Buxton

Op amps and instrumentation amplifiers must often interface to the outside world, which may entail handling voltages that exceed their absolute maximum ratings. Sensors are often placed in an environment where a fault may connect the sensor to high voltages: if the sensor is connected to an amplifier, the amplifier inputs may see voltages exceeding its power supplies. Whenever its input voltage goes outside its supply range, an op amp may be damaged, even when they are turned off. Almost all op amps' input absolute maximum ratings limit the maximum allowable input voltage to the positive and negative supplies or possibly 0.3V outside these supplies. A few exceptions to this rule do exist, which can be identified from individual data sheets, but the vast majority of amplifiers require input protection if over-voltage can possibly occur.

Any op amp input will break down to the positive rail or the negative rail if it encounters sufficient over-voltages. The breakdown voltage is entirely dependent on the structure of the input stage. It may be equivalent to a diode drop of 0.7V or to a process breakdown voltage of 50V or more. The danger of an over-voltage is that when conduction occurs large currents may flow, which can destroy the device. In many cases, over-voltage results in current well in over 100mA, which can destroy a part almost instantly.

To avoid damage, input current should be limited to less than 5mA unless otherwise stated on the relevant data sheet. This value is a conservative rule of thumb based on metal trace widths in a typical op amp input stage. Higher levels of current can cause metal migration, which will eventually lead to an open trace. Migration is a cumulative effect that may not result in a failure for a long period of time. Failure may occur due to multiple over-voltages, which is a difficult failure mode to identify. Thus, even though an amplifier may appear to withstand over-voltage currents well above 5mA for a short period of time, it is important to limit the current to guarantee long term reliability.

Two types of conduction occur in over-voltage conditions, forward biasing of PN junctions inherent in the structure of the input stage or, given enough voltage, reverse junction breakdown. The danger of forward biasing a PN-junction is that excessive current will flow and damage the part. As long as the current is limited no damage should occur. However, when the conduction is due to the reverse breakdown of a PN junction, the problem can be more serious. In the case of a base-emitter junction break down, even small amounts of current can cause degradation in the beta of the transistor. After a breakdown occurs, input parameters such as offset and bias current may be well out of specification. Diode protection is needed to prevent base-emitter junction breakdown. Other junctions, such as base-collector junctions and JFET gate-source junctions do not exhibit the same degradation in performance on break down, and for these the input current should be limited to 5mA, unless the data sheet specifies a larger value.

INPUT OVERVOLTAGE

- **INPUT SHOULD NOT EXCEED ABSOLUTE MAXIMUM RATINGS**
(Usually Specified With Respect to Supply Voltages)
- **A Common Specification Requires the Input Signal Remain Within 0.3V of the Supply Rails**
- **Input Stage Conduction Current Should Be Limited**
(Rule of Thumb: $\leq 5\text{mA}$ Unless Otherwise Specified)
- **Avoid Reverse Bias Junction Breakdown in Input Stage Junctions**
- **Differential and Common Mode Ratings May Differ**
- **No Two Amplifiers are Exactly the Same**
- **Some ICs Contain Input Protection (Voltage Clamps, Current Limits, or Both), but Absolute Maximum Ratings Must Still Be Observed**

Figure 10.48

A generalized external protection circuit using two Schottky diodes and an external current limiting resistor can be used to ensure input protection as shown in Figure 10.49. If the op amp has internal protection diodes to the supplies, they will conduct at about 0.6V forward drop above or below the supply rails. The external current limit resistor must be chosen so that the maximum amount of input current is limited to 5mA. This can result in large values of R_{LIMIT} , and the resulting increase in noise and offset voltage may not be acceptable. For instance, to protect against a 100V input at V_{IN} , R_{LIMIT} must be greater than 20k Ω (assuming a worst case condition where the supply voltages are at zero volts). The external Schottky protection diodes will begin to conduct at about 0.3V, and overvoltage current is shunted through them to the supply rails rather than through the internal ones. This allows R_{LIMIT} to be set by the maximum allowable diode current, which can be much larger than the internal limit of 5mA. For instance, a 500 Ω R_{LIMIT} resistor would limit the diode current to 200mA for a V_{IN} of 100V.

A protection resistor in series with an amplifier input will also produce a voltage drop due to the amplifier bias current flowing through it. This drop appears as an increase in the circuit offset voltage (and, if the bias current changes with temperature, offset drift). In amplifiers where bias currents are approximately equal, a resistor in series with each input will tend to balance the effect and reduce the error.

When using external Schottky clamp diodes to protect operational amplifier inputs, the effects of diode junction capacitance and leakage current should be evaluated in the application. Diode junction capacitance and R_{LIMIT} will add an additional pole in the signal path, and diode leakage currents will double for every 10 $^{\circ}\text{C}$ rise in ambient temperature. Therefore, low leakage diodes should be used such that, at the highest ambient temperature for the application, the total diode leakage current is less than one-tenth of the input bias current for the device at that temperature. Another issue with regard to the use of Schottky diodes is the change in their

forward voltage drop as a function of temperature. These diodes do not, in fact, limit the signal to $\pm 0.3V$ at all ambient temperatures, but if the Schottky diodes are at the same temperature as the op amp, they will limit the voltage to a safe level, even if they do not limit it at all times to within the data sheet rating. This is true if over-voltage is only possible at turn-on, when the diodes and the op amp will always be at the same temperature. If the op amp is warm when it is repowered, however, steps must be taken to ensure that diodes and op amp are at the same temperature.

GENERALIZED EXTERNAL OVERVOLTAGE PROTECTION CIRCUIT FOR OP AMPS

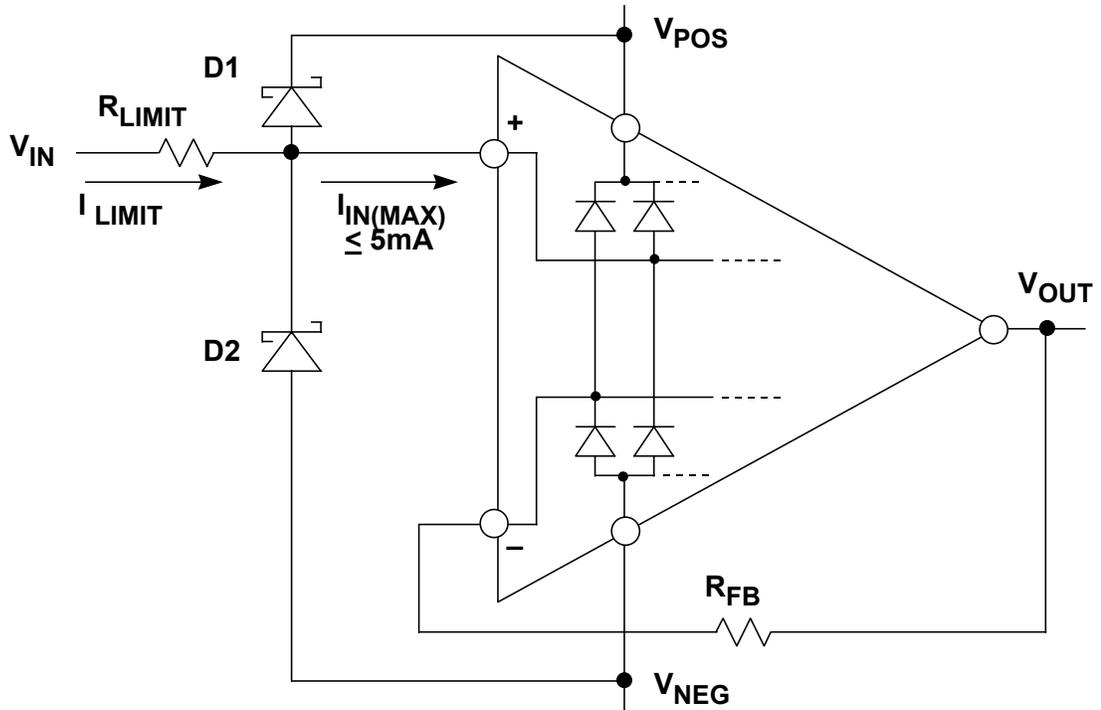


Figure 10.49

A simplified schematic of the AD620 instrumentation amplifier is shown in Figure 10.50. The 400Ω input resistors are thin-film, and therefore do not behave as junctions, as would be the case with diffused resistors. The input transistors Q1 and Q2 have diodes D1 and D2 across their base-emitter junctions to prevent reverse breakdown. Figure 10.51 shows an equivalent input circuit for an overvoltage condition. The common-mode voltage at $+V_{IN}$ or $-V_{IN}$ should be limited to $0.3V$ above V_{POS} and $0.3V$ below V_{NEG} . In addition, the differential input voltage should be limited to a value which limits the input current to $10mA$ maximum. The equivalent circuit shows that the input current flows through the two external R_{LIMIT} resistors, the two internal R_S resistors, the gain-setting resistor R_G , and two diode drops (Q2 and D1). For a given differential input voltage, the input current is a function of R_G and hence the gain. For a gain of 1000, $R_G = 49.9\Omega$, and therefore has more of an impact on the input current than for a gain of 10, where $R_G = 5.49k\Omega$.

AD620 SIMPLIFIED SCHEMATIC

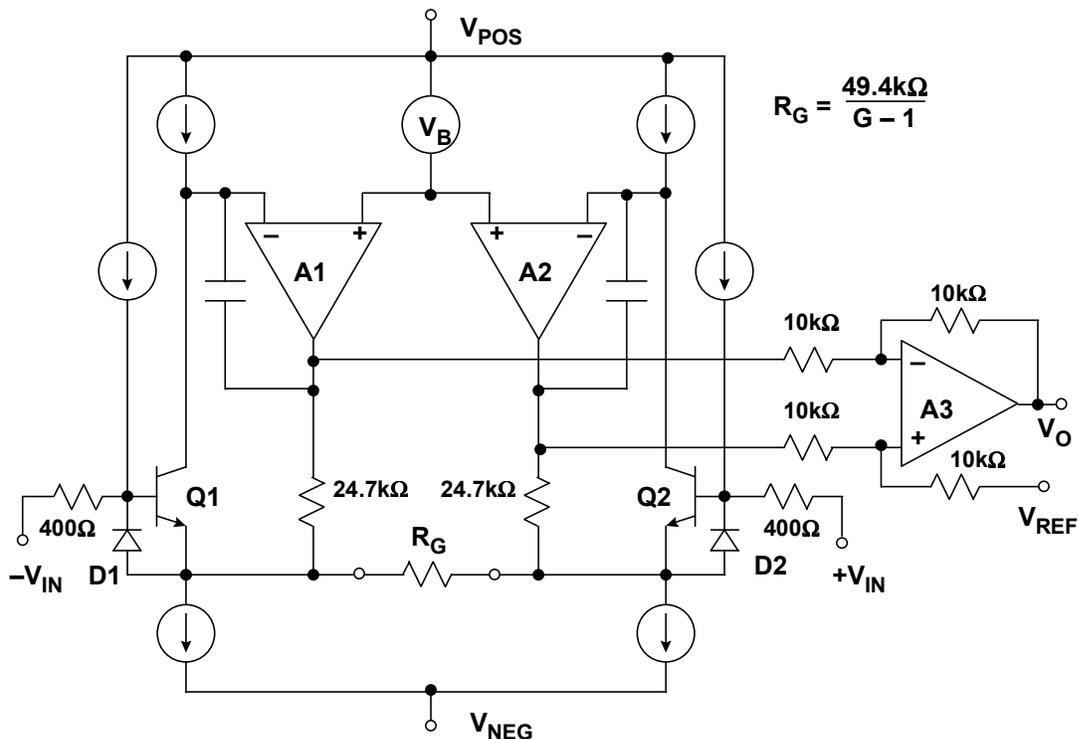


Figure 10.50

AD620 EQUIVALENT INPUT CIRCUIT WITH OVERVOLTAGE

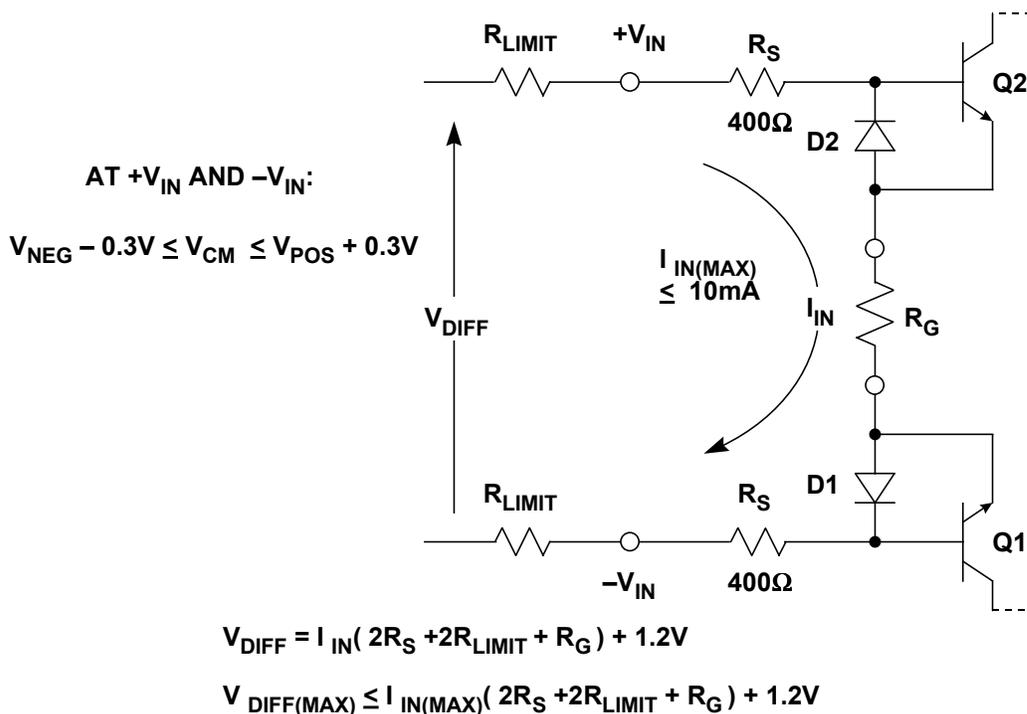


Figure 10.51

A generalized external voltage protection circuit for an in-amp is shown in Figure 10.52. The R_{LIMIT} resistors are chosen to limit the maximum current through the diodes connected to V_{POS} and V_{NEG} . The Zener diodes or Transient Voltage Suppressors (TVSs, or TransZorbs™) are selected to limit the maximum differential input voltage to less than $|V_{POS} - V_{NEG}|$ if required.

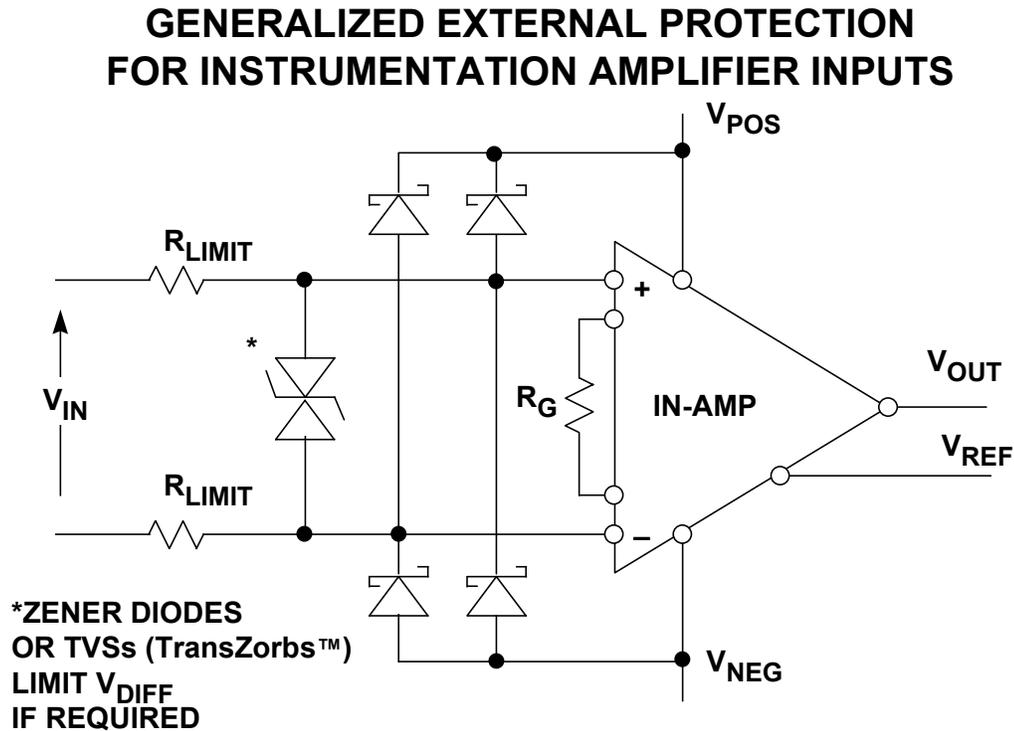


Figure 10.52

The two op amp instrumentation (see Figure 10.53) can generally be protected with external Schottky diodes to the supplies and current limit resistors. The input current is not a function of the gain-setting resistor as in the case of the three op amp in-amp configuration.

ADCs whose input range falls between the supply rails can generally be protected with external Schottky diodes and a current limit resistor as shown in Figure 10.54. Even if internal ESD protection diodes are provided, the use of the external ones allows smaller values of R_{LIMIT} and lower noise and offset errors. ADCs with thin-film input attenuators, such as the AD7890-10 (see Figure 10.55), can be protected with Zener diodes or TVSs with an R_{LIMIT} resistor to limit the current through them.

INPUT PROTECTION FOR TWO OP AMP IN-AMP (AD627)

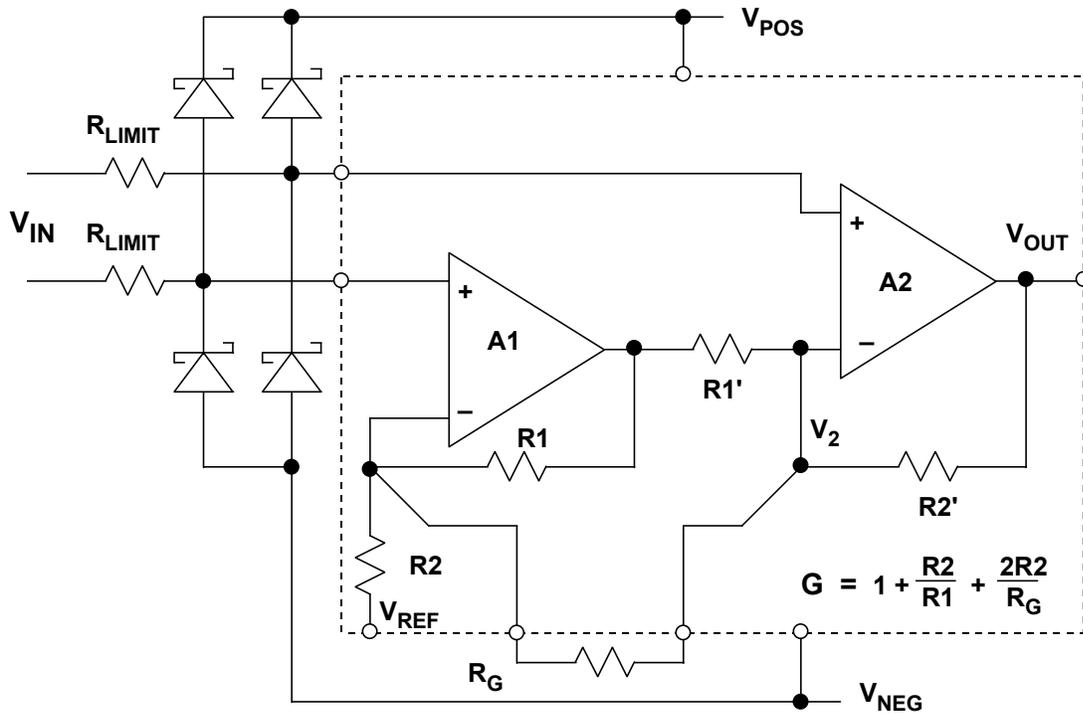
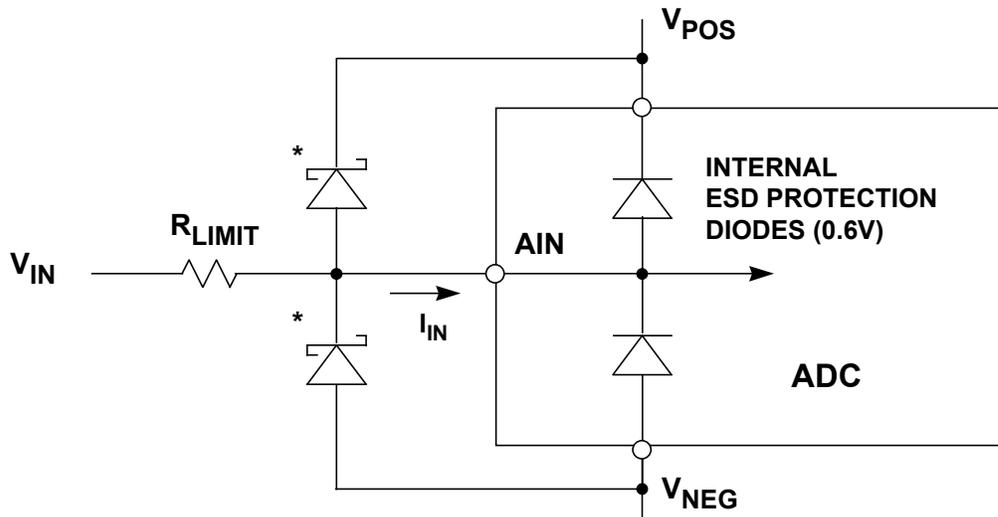


Figure 10.53

INPUT PROTECTION FOR ADCs WITH INPUT RANGES WITHIN SUPPLY VOLTAGES



- Choose R_{LIMIT} to Limit I_{IN} Current to 5mA
- *Additional External Schottky Diodes Allow Lower Values of R_{LIMIT}

Figure 10.54

INPUT PROTECTION FOR SINGLE-SUPPLY ADCs WITH THIN FILM RESISTOR INPUT ATTENUATORS

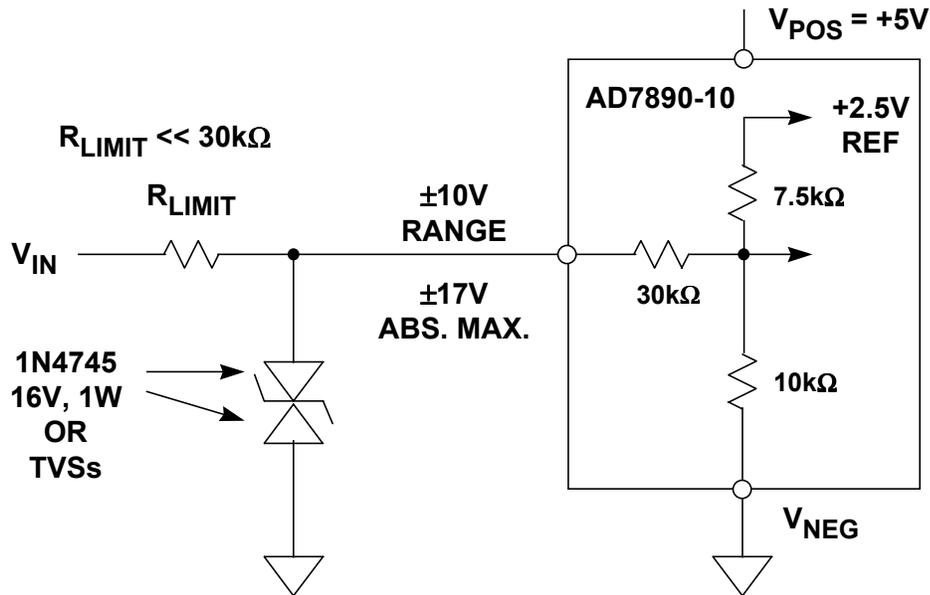


Figure 10.55

Overvoltage Protection Using CMOS Channel Protectors

The ADG465/ADG466/ADG467 are CMOS channel protectors which are placed in series with the signal path. The channel protector will protect sensitive components from voltage transients whether the power supplies are present or not. Because the channel protection works whether the supplies are present or not, the channel protectors are ideal for use in applications where correct power sequencing cannot always be guaranteed (e.g., hot-insertion rack systems) to protect analog inputs.

Each channel protector (see Figure 10.56) has an independent operation and consists of four MOS transistors - two NMOS and two PMOS. One of the PMOS devices does not lie directly in the signal path but is used to connect the source of the second PMOS device to its backgate. This has the effect of lowering the threshold voltage and so increasing the input signal range of the channel for normal operation. The source and backgate of the NMOS devices are connected for the same reason.

The channel protector behaves just like a series resistor (60Ω to 80Ω) during normal operation, i.e., $(V_{SS} + 2V) < V_D < (V_{DD} - 1.5V)$. When a channel's analog input voltage exceeds this range, one of the MOSFETs will switch off, clamping the output at either $V_{SS} + 2V$ or $V_{DD} - 1.5V$. Circuitry and signal source protection is provided in the event of an overvoltage or power loss. The channel protectors can withstand overvoltage inputs from $V_{SS} - 20V$ to $V_{DD} + 20V$ with power on ($V_{DD} - V_{SS} = 44V$ maximum). With power off ($V_{DD} = V_{SS} = 0V$), maximum input voltage is $\pm 35V$. The channel protectors are very low power devices, and even under fault conditions, the supply current is limited to sub microampere levels. All transistors

are dielectrically isolated from each other using a trench isolation method thereby ensuring that the channel protectors cannot latch up.

Figure 10.58 shows a typical application that requires overvoltage and power supply sequencing protection. The application shows a hot-insertion rack system. This involves plugging a circuit board or module into a live rack via an edge connector. In this type of application it is not possible to guarantee correct power supply sequencing. Correct power supply sequencing means that the power supplies should be connected before any external signals. Incorrect power sequencing can cause a CMOS device to latch up. This is true of most CMOS devices regardless of the functionality. RC networks are used on the supplies of the channel protector to ensure that the rest of the circuit is powered up before the channel protectors. In this way, the outputs of the channel protectors are clamped well below V_{DD} and V_{SS} until the capacitors are charged. The diodes ensure that the supplies on the channel protector never exceed the supply rails when it is being disconnected. Again this ensures that signals on the inputs of the CMOS devices never exceed the supplies.

ADG465, ADG466, and ADG467 SINGLE, TRIPLE, AND OCTAL CHANNEL PROTECTORS

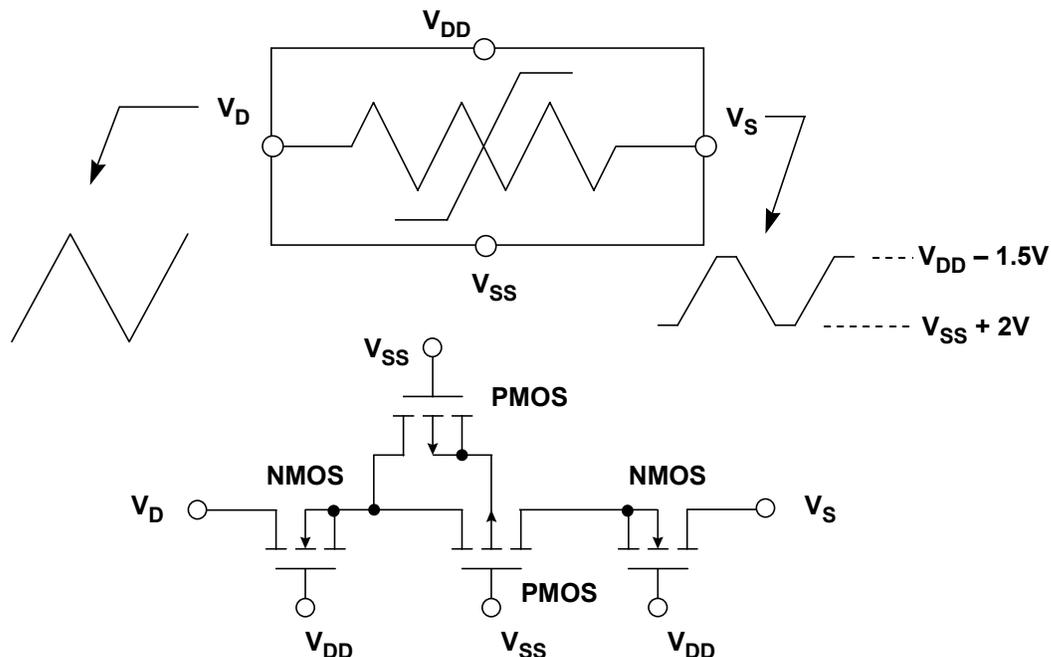


Figure 10.56

ADG465, ADG466, and ADG467 CHANNEL PROTECTORS KEY SPECIFICATIONS

- Low On-Resistance (50Ω for ADG465, 80Ω for ADG466/467)
- On-Resistance Match: 3%
- 44V Maximum Supply Voltage, $V_{DD} - V_{SS}$
- Fault and Overvoltage Protection up to $\pm 40V$
- Positive Overvoltages Clamped at $V_{DD} - 1.5V$
- Negative Overvoltages Clamped at $V_{SS} + 2V$
- Signal Paths Open-Circuit with Power Off
- Latch-Up Proof Construction

Figure 10.57

OVERVOLTAGE AND POWER SUPPLY SEQUENCING PROTECTION USING THE ADG466

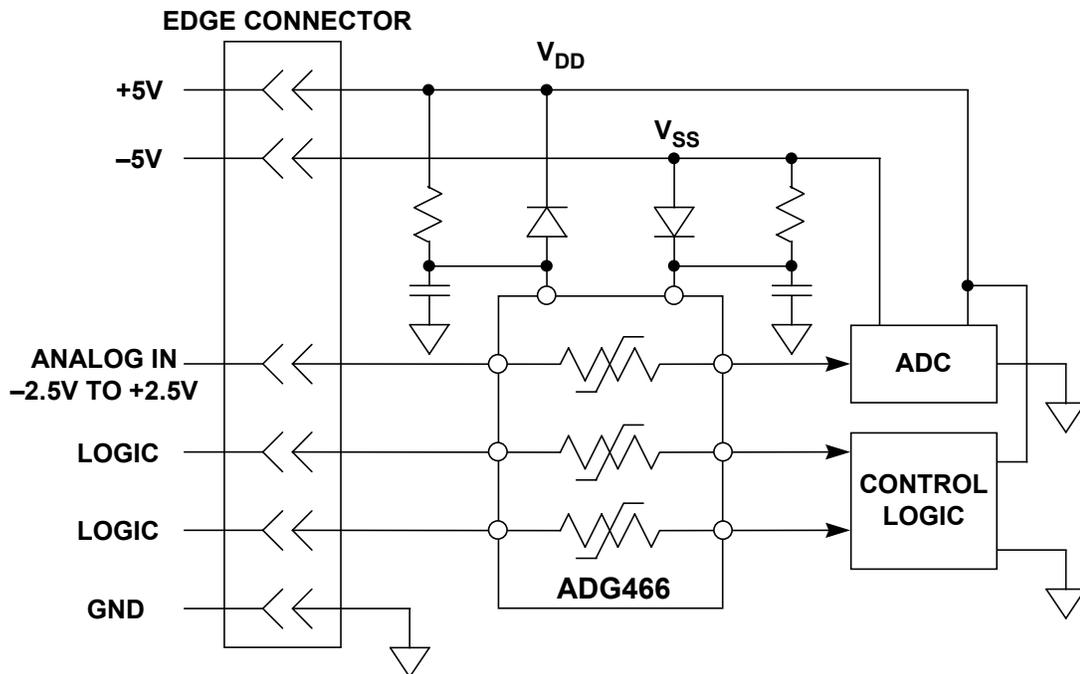


Figure 10.58

ELECTROSTATIC DISCHARGE

Walt Kester, Wes Freeman, James Bryant

Electrostatic discharge is a single, fast, high current transfer of electrostatic charge that results from:

- (1) *Direct contact transfer between two objects at different potentials (sometimes called contact discharge), or*
- (2) *A high electrostatic field between two objects when they are in close proximity (sometimes called air discharge)*

The prime sources of static electricity are mostly insulators and are typically synthetic materials, e.g., vinyl or plastic work surfaces, insulated shoes, finished wood chairs, Scotch tape, bubble pack, soldering irons with ungrounded tips, etc. Voltage levels generated by these sources can be extremely high since their charge is not readily distributed over their surfaces or conducted to other objects.

The generation of static electricity caused by rubbing two substances together is called the *triboelectric* effect. Examples are shown in Figure 10.59.

EXAMPLES OF ELECTROSTATIC CHARGE GENERATION

- **Walking Across a Carpet**
 - ◆ **1000V - 1500V Generated**
- **Walking Across a Vinyl Floor**
 - ◆ **150V - 250V Generated**
- **Handling Material Protected by Clear Plastic Covers**
 - ◆ **400V - 600V Generated**
- **Handling Polyethylene Bags**
 - ◆ **1000V - 2000V Generated**
- **Pouring Polyurethane Foam Into a Box**
 - ◆ **1200V - 1500V Generated**
- **Note: Assume 60% RH. For Low RH (30%), Generated Voltages Can Be >10 Times Those Listed Above**

Figure 10.59

Integrated circuits can be damaged by the high voltages and high peak currents that can be generated by electrostatic discharge. Precision analog circuits, which often feature very low bias currents, are more susceptible to damage than common digital circuits, because the traditional input-protection structures which protect against ESD damage also increase input leakage.

For the design engineer or technician, the most common manifestation of ESD damage is a catastrophic failure of the IC. However, exposure to ESD can also cause increased leakage or degrade other parameters. If a device appears to not meet a data sheet specification during evaluation, the possibility of ESD damage should be considered.

UNDERSTANDING ESD DAMAGE

■ ESD Failure Mechanisms:

- ◆ Dielectric or junction damage
- ◆ Surface charge accumulation
- ◆ Conductor fusing

■ ESD Damage Can Cause:

- ◆ Increased leakage
- ◆ Degradation in performance
- ◆ Functional failures of ICs.

■ ESD Damage is often Cumulative:

- ◆ For example, each ESD "zap" may increase junction damage until, finally, the device fails.

Figure 10.60

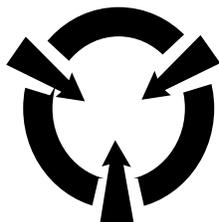
All ESD sensitive devices are shipped in protective packaging. ICs are usually contained in either conductive foam or antistatic tubes. Either way, the container is then sealed in a static-dissipative plastic bag. The sealed bag is marked with a distinctive sticker, such as that shown in Figure 10.61, which outlines the appropriate handling procedures. In addition, the data sheets for ESD sensitive ICs generally have a statement to that effect (see Figure 10.62).

Once ESD-sensitive devices are identified, protection is relatively easy. Obviously, keeping ICs in their original protective packaging as long as possible is the first step. The second step is to discharge potential ESD sources before damage to the IC can occur. Discharging a potentially dangerous voltage can be done quickly and safely through a high impedance.

The key component required for safe ESD handling is a workbench with a static-dissipative surface, as shown in Figure 10.63. This surface is connected to ground through a 1M Ω resistor, which dissipates static charge while protecting the user from electrical shock hazards caused by ground faults. If existing bench tops are nonconductive, a static-dissipative mat should be added, along with a discharge resistor.

RECOGNIZING ESD SENSITIVE DEVICES

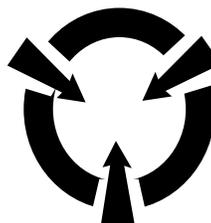
All static sensitive devices are sealed in protective packaging and marked with special handling instructions



CAUTION

SENSITIVE ELECTRONIC DEVICES

DO NOT SHIP OR STORE NEAR STRONG
ELECTROSTATIC, ELECTROMAGNETIC,
MAGNETIC, OR RADIOACTIVE FIELDS



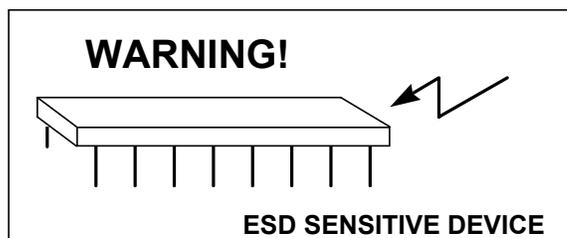
CAUTION

SENSITIVE ELECTRONIC DEVICES

DO NOT OPEN EXCEPT AT
APPROVED FIELD FORCE
PROTECTIVE WORK STATION

Figure 10.61

ESD STATEMENT ON DATA SHEETS OF MOST LINEAR AND MIXED-SIGNAL ICs

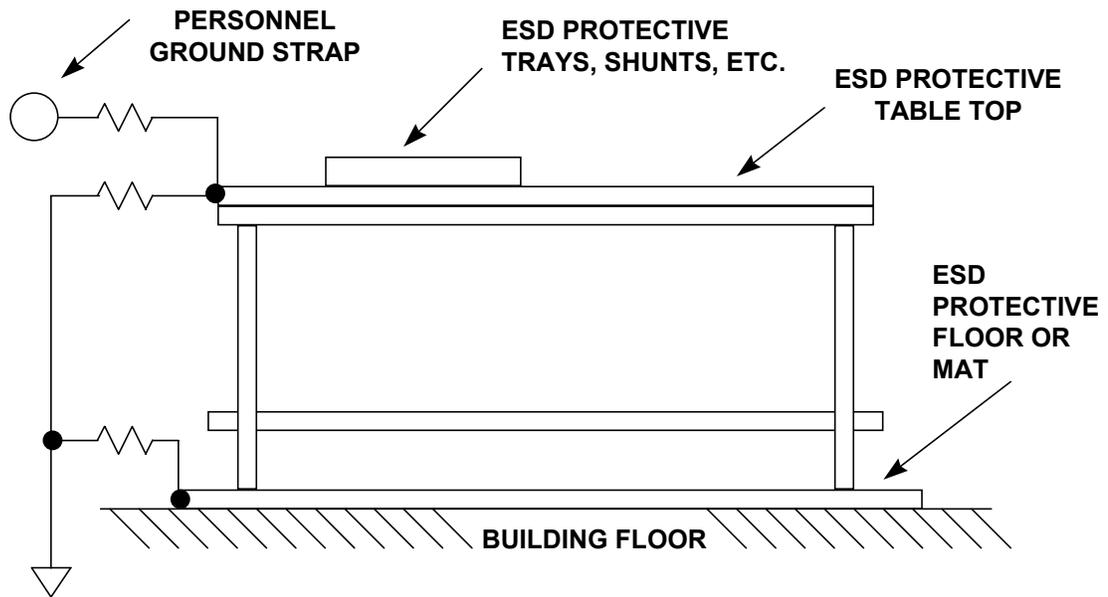


CAUTION

ESD (Electrostatic Discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADXXX features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Figure 10.62

WORKSTATION FOR HANDLING ESD-SENSITIVE DEVICES



Note: Conductive Table Top Sheet Resistance $\approx 1\text{M}\Omega / \square$

Figure 10.63

Notice that the surface of the workbench has a moderately high sheet resistance. It is neither necessary nor desirable to use a low-resistance surface (such as a sheet of copper-clad PC board) for the work surface. Remember, a high peak current may flow if a charged IC is discharged through a low impedance. This is precisely what happens when a charged IC contacts a grounded copper clad board. When the same charged IC is placed on the surface shown in Figure 10.63, however, the peak current is not high enough to damage the device.

A conductive wrist strap is also recommended while handling ESD-sensitive devices. The wrist strap ensures that normal tasks, such as peeling tape off of packages, will not cause damage to ICs. Again, a $1\text{M}\Omega$ resistor, from the wrist strap to ground, is required for safety.

When building prototype breadboards or assembling PC boards which contain ESD-sensitive devices, all passive components should be inserted and soldered before the ICs. This procedure minimizes the ESD exposure of the sensitive devices. The soldering iron must, of course, have a grounded tip.

Protecting ICs from ESD requires the participation of both the IC manufacturer and the customer. IC manufacturers have a vested interest in providing the highest possible level of ESD protection for their products. IC circuit designers, process engineers, packaging specialists and others are constantly looking for new and improved circuit designs, processes, and packaging methods to withstand or shunt ESD energy.

A complete ESD protection plan, however, requires more than building-ESD protection into ICs. Users of ICs must also provide their employees with the necessary knowledge of and training in ESD handling procedures (Figure 10.64).

ESD PROTECTION REQUIRES A PARTNERSHIP BETWEEN THE IC SUPPLIER AND THE CUSTOMER

ANALOG DEVICES:

- **Circuit Design and Fabrication -**
 - ↓ **Design and manufacture products with the highest level of ESD protection consistent with required analog and digital performance.**
 - ↓
- **Pack and Ship -**
 - ↓ **Pack in static dissipative material. Mark packages with ESD warning.**

CUSTOMERS:

- **Incoming Inspection -**
 - ↓ **Inspect at grounded workstation. Minimize handling.**
- **Inventory Control -**
 - ↓ **Store in original ESD-safe packaging. Minimize handling.**
- **Manufacturing -**
 - ↓ **Deliver to work area in original ESD-safe packaging. Open packages only at grounded workstation. Package subassemblies in static dissipative packaging.**
 - ↓
- **Pack and Ship -**
 - ↓ **Pack in static dissipative material if required. Replacement or optional boards may require special attention.**

Figure 10.64

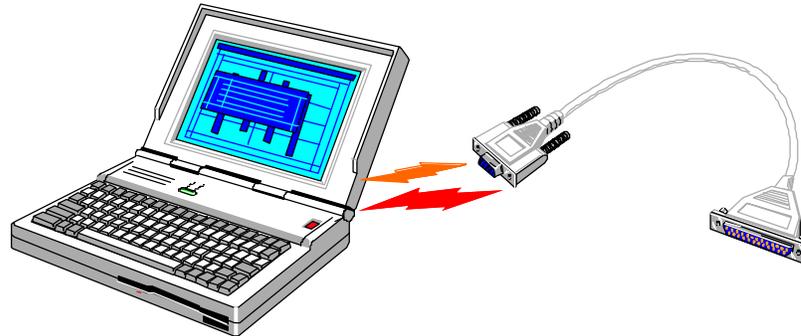
Special care should be taken when breadboarding and evaluating ICs. The effects of ESD damage can be cumulative, so repeated mishandling of a device can eventually cause a failure. Inserting and removing ICs from a test socket, storing devices during evaluation, and adding or removing external components on the breadboard should all be done while observing proper ESD precautions. Again, if a device fails during a prototype system development, repeated ESD stress may be the cause.

The key word to remember with respect to ESD is *prevention*. There is no way to undo ESD damage, or to compensate for its effects.

ESD Models and Testing

Some applications have higher ESD sensitivity than others. ICs which are located on a PC board surrounded by other circuits are generally much less susceptible to ESD damage than circuits which must interface with other PC boards or the outside world. These ICs are generally not specified or guaranteed to meet any particular ESD specification (with the exception of MIL-STD-883 Method 3015 classified devices). A good example of an ESD-sensitive interface is the RS-232 port on a computer (see Figure 10.65). The RS-232 driver and receiver ICs are directly in the firing line for voltage transients as well as ESD. In order to guarantee ESD performance for such devices, the test methods and limits must be specified.

RS-232 PORT IS VERY SUSCEPTIBLE TO ESD



- I-O Transceiver Is Directly in the Firing Line for Transients - RS-232 Port Is Particularly Vulnerable
- I-O Port Is an Open Gateway in the Enclosure
- Harmonised Standards Are Now Mandatory Requirements in European Community

Figure 10.65

A host of test waveforms and specifications have been developed to evaluate the susceptibility of devices to ESD. The three most prominent of these waveforms currently in use for semiconductor or discrete devices are: The Human Body Model (HBM), the Machine Model (MM), and the Charged Device Model (CDM). Each of these models represents a fundamentally different ESD event, consequently, correlation between the test results for these models is minimal.

Since 1996, all electronic equipment sold to or within the European Community must meet Electromechanical Compatibility (EMC) levels as defined in specification IEC1000-4-x. This does not apply to individual ICs, but to the end equipment. These standards are defined along with test methods in the various IEC1000 specifications shown in Figure 10.66.

IEC1000-4-2 specifies compliance testing using two coupling methods, *contact discharge* and *air-gap discharge*. Contact discharge calls for a direct connection to the unit being tested. Air-gap discharge uses a higher test voltage, but does not make direct contact with the unit under test. With air discharge, the discharge gun is moved toward the unit under test, developing an arc across the air gap, hence the term air discharge. This method is influenced by humidity, temperature, barometric pressure, distance and rate of closure of the discharge gun. The contact-discharge method, while less realistic, is more repeatable and is gaining acceptance in preference to the air-gap method.

IEC 1000-4-x BASIC IMMUNITY STANDARDS FOR ELECTRONIC EQUIPMENT (NOT ICs!)

- IEC1000-4 Electromagnetic Compatibility EMC
- IEC1000-4-1 Overview of Immunity Tests
- IEC1000-4-2 Electrostatic Discharge Immunity (ESD)
- IEC1000-4-3 Radiated Radio-Frequency Electromagnetic Field Immunity
- IEC1000-4-4 Electrical Fast Transients (EFT)
- IEC1000-4-5 Lightning Surges
- IEC1000-4-6 Conducted Radio Frequency Disturbances above 9kHz
- Compliance Marking:



Figure 10.66

Although very little energy is contained within an ESD pulse, the extremely fast risetime coupled with high voltages can cause failures in unprotected ICs. Catastrophic destruction can occur immediately as a result of arcing or heating. Even if catastrophic failure does not occur immediately, the device may suffer from parametric degradation, which may result in degraded performance. The cumulative effects of continuous exposure can eventually lead to complete failure.

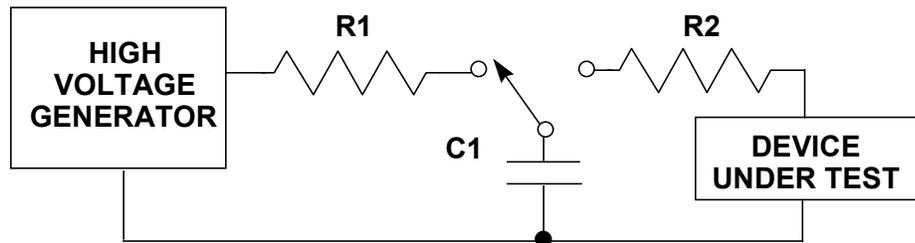
I-O lines are particularly vulnerable to ESD damage. Simply touching or plugging in an I-O cable can result in a static discharge that can damage or completely destroy the interface product connected to the I-O port (such as RS-232 line drivers and receivers). Traditional ESD test methods such as MIL-STD-883B Method 3015.7 do not fully test a product's susceptibility to this type of discharge. This test was intended to test a product's susceptibility to ESD damage during handling. Each pin is tested with respect to all other pins. There are some important differences between the MIL-STD-883B Method 3015.7 test and the IEC test:

- (1) *The IEC test is much more stringent in terms of discharge energy. The peak current injected is over four times greater.*
- (2) *The current risetime is significantly faster in the IEC test.*
- (3) *The IEC test is carried out while power is applied to the device.*

It is possible that ESD discharge could induce latch-up in the device under test. This test is therefore more representative of a real-world I-O discharge where the equipment is operating normally with power applied. For maximum confidence, however, both tests should be performed on interface devices, thus ensuring maximum protection both during handling, and later, during field service.

A comparison of the test circuit values for the IEC1000-4-2 model versus the MIL-STD-883B Method 3015.7 Human Body Model is shown in Figure 10.67, and the ESD waveforms are compared in Figure 10.68.

**MIL STD 883B METHOD 3015.7 HUMAN BODY MODEL
VERSUS IEC 1000-4-2 ESD TESTING**



ESD TEST METHOD	R2	C1
Human Body Model MIL STD 883B Method 3015.7	1.5kΩ	100pF
IEC 1000-4-2	330Ω	150pF

NOTE: CONTACT DISCHARGE VOLTAGE SPEC FOR IEC 1000-4-2 IS ±8kV

Figure 10.67

Suitable ESD-protection design measures are relatively easy to incorporate, and most of the over-voltage protection methods previously discussed in this section will help. Additional protection can be obtained by the addition of TransZorbs at appropriate places in the system. For RS-232 and RS-485 line drivers and receivers, the ADMXXX-E series is supplied with guaranteed 15kV (HBM) ESD specifications.

MIL-STD-883B, METHOD 3015.7 HUMAN BODY MODEL AND IEC 1000-4-2 ESD WAVEFORMS

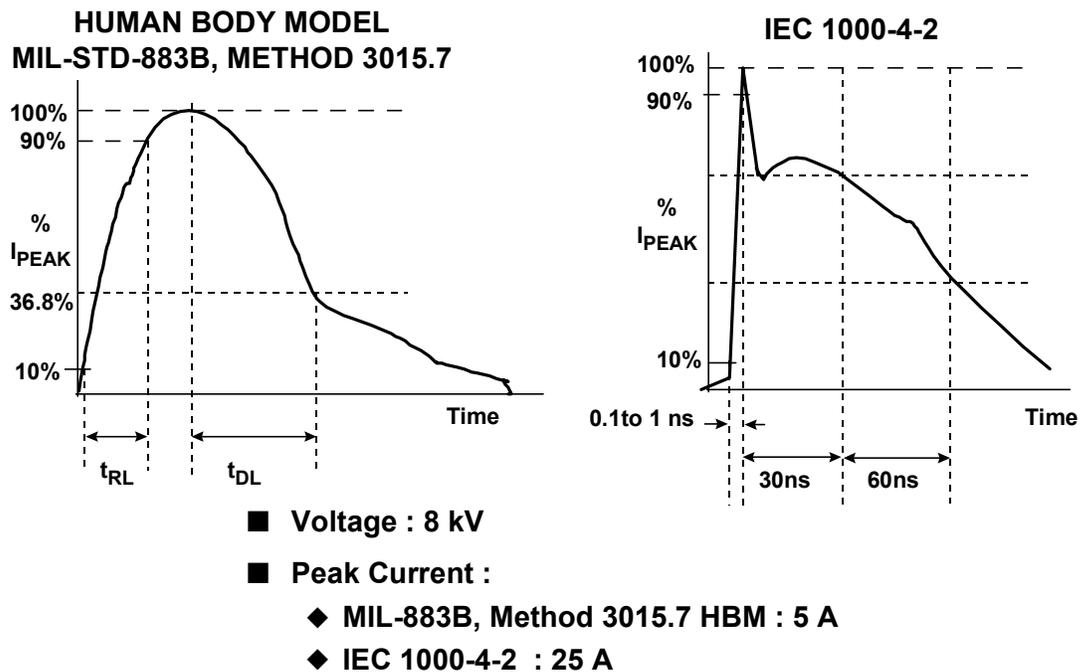


Figure 10.68

CUSTOMER DESIGN PRECAUTIONS FOR ICs WHICH MUST OPERATE AT ESD-SUSCEPTIBLE INTERFACES

- Observe all Absolute Maximum Ratings on Data Sheet!
- Follow General Overvoltage Protection Recommendations
 - ◆ Add Series Resistance to Limit Currents
 - ◆ Add Zeners or Transient Voltage Suppressors (TVS) TransZorbs™ for Extra Protection (<http://www.gensemi.com>)
- Purchase ESD-Specified Digital Interface Devices Such as
 - ◆ ADMXXX-E Series of RS-232 / RS-485 Drivers / Receivers (MIL-883B, Method 3015.7: 15kV, IEC 1000-4-2: 8kV)
- Read AN-397, "Electrically Induced Damage to Standard Linear Integrated Circuits: The Most Common Causes and the Associated Fixes to Prevent Recurrence," by Niall Lyne - Available from Analog Devices, <http://www.analog.com>

Figure 10.69

REFERENCES ON ESD AND OVERVOLTAGE:

1. **Amplifier Applications Guide**, Section XI, pp. 1-10, Analog Devices, Incorporated, Norwood, MA, 1992.
2. **Systems Applications Guide**, Section 1, pp. 56-72, Analog Devices, Incorporated, Norwood, MA, 1993.
3. **Linear Design Seminar**, Section 1, pp. 19-22, Analog Devices, Incorporated, Norwood, MA, 1994.
4. **ESD Prevention Manual**, Analog Devices, Inc.
5. *MIL-STD-883 Method 3015, Electrostatic Discharge Sensitivity Classification*. Available from Standardization Document Order Desk, 700 Robbins Ave., Building #4, Section D, Philadelphia, PA 19111-5094.
6. *EIAJ ED-4701 Test Method C-111, Electrostatic Discharges*. Available from the Japan Electronics Bureau, 250 W 34th St., New York NY 10119, Attn.: Tomoko.
7. *ESD Association Standard S5.2 for Electrostatic Discharge (ESD) Sensitivity Testing -Machine Model (MM)- Component Level*. Available from the ESD Association, Inc., 200 Liberty Plaza, Rome, NY 13440.
8. *ESD Association Draft Standard DS5.3 for Electrostatic Discharge (ESD) Sensitivity Testing - Charged Device Model (CDM) Component Testing*. Available from the ESD Association, Inc., 200 Liberty Plaza, Rome, NY 13440.
9. Niall Lyne, *Electrical Overstress Damage to CMOS Converters*, **Application Note AN-397**, Analog Devices, 1995, <http://www.analog.com>.
10. *How to Reliably Protect CMOS Circuits Against Power Supply Overvoltage*, **Application Note AN-311**, Analog Devices, <http://www.analog.com>
11. ADM3311E RS-232 Port Transceiver Data Sheet, Analog Devices, Inc., <http://www.analog.com>.
12. TransZorbs Available from General Semiconductor, Inc., 10 Melville Park Road, Melville, NY, 11747-3113, 516-847-3000, <http://www.gensemi.com>.