SECTION 7

OVERVOLTAGE EFFECTS ON ANALOG INTEGRATED CIRCUITS

- Amplifier Input Stage Overvoltage
- Amplifier Output Voltage Phase Reversal
- Understanding and Protecting Integrated Circuits from Electrostatic Discharge (ESD)

SECTION 7

OVERVOLTAGE EFFECTS ON ANALOG INTEGRATED CIRCUITS

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One of the most commonly asked applications questions is: "What happens if external voltages are applied to an analog integrated circuit with the supplies turned off?" This question describes situations that can take on many different forms: from lightning strikes on cables which propagate very high transient voltages into signal conditioning circuits, to walking across a carpet and then touching a printed circuit board full of sensitive precision circuits. Regardless of the situation, the general issue is the effect of overvoltage stress (and, in some cases, abuse) on analog integrated circuits. The discussion which follows will be limited in general to operational amplifiers, because it is these devices that most often interface to the outside world. The principles developed here can and should be applied to all analog integrated circuits which are required to condition or digitize analog waveforms. These devices include (but are not limited to) instrumentation amplifiers, analog comparators, sample-and-hold amplifiers, analog switches and multiplexers, and analog-to-digital converters.

AMPLIFIER INPUT STAGE OVERVOLTAGE

In real world signal conditioning, sensors are often used in hostile environments where faults can and do occur. When these faults take place, signal conditioning circuitry can be exposed to large voltages which exceed the power supplies. The likelihood for damage is quite high, even though the components' power supplies may be turned on. Published specifications for operational amplifier absolute maximum ratings state that applied input signal levels should never exceed the power supplies by more than 0.3V or, in some devices, 0.7V. Exceeding these levels exposes amplifier input stages to potentially destructive fault currents which flow through internal metal traces and parasitic p-n junctions to the supplies. Without some type of current limiting, unprotected input differential pairs (BJTs or FETs) can be destroyed in a matter of microseconds. There are, however, some devices with built-in circuitry that can provide protection beyond the supply voltages, but in general, absolute maximum ratings must still be observed.

INPUT STAGE OVERVOLTAGE

- **INPUT SHOULD NOT EXCEED ABSOLUTE MAXIMUM RATINGS (Usually Specified With Respect to Supply Voltages)**
- **A Common Specification Requires the Input Signal $<|V_s| \pm 0.3V$**
- **Input Voltage Should be Held Near Zero in the Absence of Supplies**
- **Input Stage Conduction Current Needs to be Limited (Rule of Thumb: ≤ 5mA)**
- **Avoid Reverse Bias Junction Breakdown in Input Stage Base-Emitter Junctions**
- **Differential and Common-Mode Ratings may Differ**
- **No Two Amplifiers are exactly the Same**
- **Some Op Amps Contain Input Protection (Voltage Clamps, Current Limits, or Both), but Absolute Maximum Ratings Must Still be Observed**

Figure 7.1

Although more recent vintage operational amplifiers designed for single-supply or rail-to-rail operation are now including information with regard to input stage overvoltage effects, there are very many amplifiers available today without such information provided by the manufacturer. In those cases, the circuit designer using these components must ascertain the input stage current-voltage characteristic of the device in question before steps can be taken to protect it. All amplifiers will conduct current to the positive/negative supply, provided the applied input voltage exceeds some internal threshold. This threshold is device dependent, and can range from 0.7V to 30V, depending on the internal construction of the input stage. Regardless of the threshold level, externally generated fault currents should be limited to no more than ±5mA.

Many factors contribute to the current-voltage characteristic of an amplifier's input stage: internal differential clamping diodes, current-limiting series resistances, substrate potential connections, and differential input stage topologies (BJTs or FETs). Input protection diodes used as differential input clamps are typically constructed from the base-emitter junctions of NPN transistors. These diodes usually form a parasitic p-n-junction to the negative supply when the applied input voltage exceeds the negative supply. Current-limiting series resistances used in the input stages of operational amplifiers can be fabricated from three types of material: n- or p-type diffusions, polysilicon, or thin-films (SiCr, for example). Polysilicon and thin-film resistors are fabricated over thin layers of oxide which provide an insulating barrier to the substrate; as such, they do not exhibit any parasitic p-n junctions to either supply. Diffused resistors, on the other hand, exhibit p-n

junctions to the supplies because they are constructed from either p- or n-type diffusion regions. The substrate potential of the amplifier is the most critical component, for it will determine the sensitivity of an amplifier's input current-voltage characteristic to supply voltage.

The configuration of the amplifier's input stage also plays a large role in the current-voltage characteristic of the amplifier. Input differential pairs of operational amplifiers are constructed from either bipolar transistors (NPN or PNP) or field-effect transistors (junction or MOS, N- or P-channel). While the bipolar input differential pairs do not have any direct path to either supply, FET differential pairs do. For example, an n-channel JFET forms a parasitic p-n junction between its backgate and the p-substrate that energizes when $V_{IN} + 0.7V < V_{NEG}$. As mentioned previously, many manufacturers of analog integrated circuits do not provide any details with regard to the behavior of the device's input structure. Either simplified schematics are not provided or, if they are shown, the behavior of the input stage under an overvoltage condition is omitted. Therefore, other measures must be taken in order to identify the conduction paths.

A standard transistor curve tracer can be configured to determine the current-voltage characteristic of any amplifier regardless of input circuit topology. As shown in Figure 7.2, both amplifier supply pins are connected to ground, and the collector output drive is connected to one of the amplifier's inputs. The curve tracer applies a DC ramp voltage and measures the current flowing through the input stage. In the event that a transistor curve tracer is not available, a DC voltage source and a multimeter can be substituted for the curve tracer. A 10kohm resistor should be used between the DC voltage source and the amplifier input for additional protection. Ammeter readings from the multimeter at each applied DC voltage will yield the same result as that produced by the curve tracer. Although either input can be tested (both inputs should), it is recommended that the unused input is left open; otherwise, additional junctions could come into play and would complicate matters further. Evaluations of current feedback amplifier input stages are more difficult because of the lack of symmetry between the inputs. As a result, both inputs should be characterized for their individual current-voltage characteristics.

OVER-VOLTAGE CURVE TRACER TEST SETUP

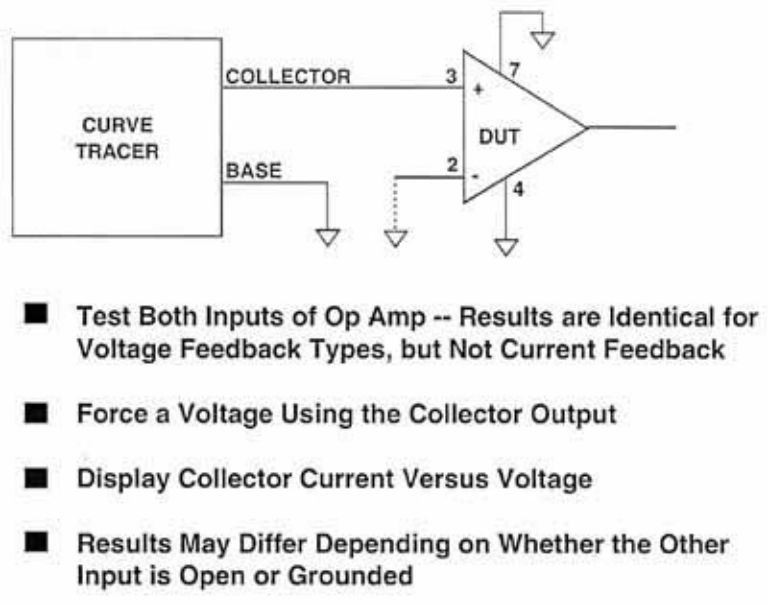

Figure 7.2

Once the input current-voltage characteristic has been determined for the device in question, the next step is to determine the minimum level of resistance required to limit fault currents to ±5mA. Equation 7.1 illustrates the computation for R_S when the input overvoltage level is known:

$$R_S = \frac{V_{IN(MAX)} - V_{SUPPLY}}{5\ mA} \qquad \text{Eq. 7.1}$$

The worst case condition for overvoltage would be when the power supplies are initially turned off or disconnected. In this case, V_{SUPPLY} is equal to zero. For example, if the input overvoltage could reach 100V under some type of fault condition, then the external resistor should be no smaller than 20kohms. Most operational amplifier applications only require protection at one input; however, there are a few configurations (difference amplifiers, for example) where both inputs can be subjected to overvoltage and both must be protected. The need for protection on both inputs is much more common with instrumentation amplifiers.

OVERVOLTAGE EFFECTS

- **Junctions may be Forward Biased if the Current is Limited**
- **In General a Safe Current Limit is 5mA**
- **Reverse Bias Junction Breakdown is Damaging Regardless of the Current Level**
- **When in Doubt, Protect with External Diodes and Series Resistances**
- **Curve Tracers Can be Used to Check the Overvoltage Characteristics of a Device**
- **Simplified Equivalent Circuits in Data Sheets do not tell the Entire Story!!!**

Figure 7.3

AMPLIFIER OUTPUT VOLTAGE PHASE REVERSAL

Some operational amplifiers exhibit output voltage phase reversal when one or both of their inputs exceeds their input common-mode voltage range. Phase reversal is usually associated with JFET (n- or p-channel) input amplifiers, but some bipolar devices (especially single-supply amplifiers operating as unity-gain followers) may also be susceptible. In the vast majority of applications, output voltage phase reversal does not harm the amplifier nor the circuit in which the amplifier is used. Although a number of operational amplifiers suffer from phase reversal, it is rarely a problem in system design. However, in servo loop applications, this effect can be quite hazardous. Fortunately, this is only a temporary condition. Once the amplifier's inputs return to within its normal operating common-mode range, output voltage phase reversal ceases. It may still be necessary to consult the amplifier manufacturer, since phase reversal information rarely appears on device data sheets. Summarized as follows is a list of recent vintage Analog Devices amplifier products that are now including output voltage phase reversal characterization/commentary:

Single-Supply/ Rail-to-Rail	Dual Supply
OP295/OP495	OP282/OP482
OP113/OP213/OP413	OP285
OP183/OP283	OP467
OP292/OP492	OP176
OP191/OP291/OP491	BUF04
OP279	
AD820/AD822/AD824	
OP193/OP293/OP493	

In BiFET operational amplifiers, phase reversal may be prevented by adding an appropriate resistance in series with the amplifier's input to limit the current. Bipolar input devices can be protected by using a Schottky diode to clamp the input to within a few hundred millivolts of the negative rail. For a complete description of the output voltage phase reversal effect, please consult Reference 1.

BEWARE OF AMPLIFIER OUTPUT PHASE REVERSAL

- **Sometimes Occurs in FET and Bipolar Input (Especially Single-Supply) Op Amps when Input Exceeds Common Mode Range**
- **Does Not Harm Amplifier, but may be Disastrous in Servo Systems!**
- **Not Usually Specified on Data Sheet, so Amplifier Must be Checked**
- **Easily Prevented:**

BiFETs: **Add Appropriate Input Series Resistance (Determined Empirically, Unless Provided in Data Sheet)**

Bipolars: **Use Schlottky Diode Clamps to the Supply Rails.**

Figure 7.4

Rail-to-rail operational amplifiers present a special class of problems to the integrated circuit designer, because these types of devices should not exhibit any abnormal behavior throughout the entire input common-mode range. In fact, it is desirable that devices used in these applications also not exhibit any abnormal behavior if the applied input voltages exceed the power supply range. One of the more recent vintage rail-to-rail input/output operational amplifiers, the OPX91 family (the OP191, the OP291, and the OP491), includes additional components that prevent overvoltage and damage to the device. As shown in Figure 7.5, the input stage of the OPX91 devices use six diodes and two resistors to clamp the input terminals to each other and to the supplies. D1 and D2 are base-emitter NPN diodes which are used to protect the bases of Q1-Q2 and Q3-Q4 against avalanche breakdown when the applied differential input voltage to the device exceeds 0.7V. Diodes D3-D6 are diodes formed from substrate PNP transistors that clamp the applied input voltages on the OPX91 to the supply rails.

A CLOSER LOOK AT THE OP-X91 INPUT STAGE REVEALS ADDITIONAL DEVICES

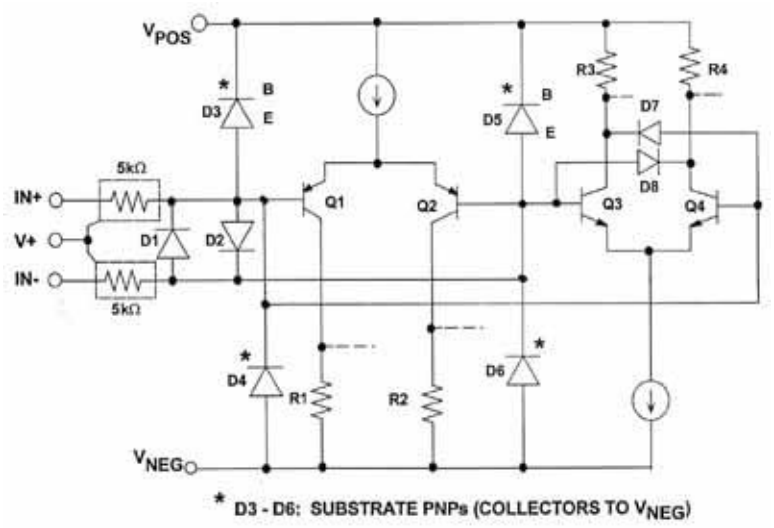

Figure 7.5

An interesting benefit from using substrate PNPs as clamp diodes is that their collectors are connected to the negative supply; thus, when the applied input voltage exceeds either supply rail, the diodes energize, and the fault currents are diverted directly to the supply and not through or into the device's input stage. There are also 5kohm resistors in series with each of the inputs to the OPX91 to limit the fault current through D1 and D2 when the differential input voltage exceeds 0.7V. Note that these 5kohm resistors are p-type diffusions placed inside an n-well, which is then connected to the positive supply. When the applied input voltage exceeds the positive supply, some of the fault current generated is also diverted to V_{POS} and away from the input stage. As a result of these measures, the input overvoltage characteristic of the OPX91 is well behaved as shown in Figure 7.6. Note that the combination of the 5kohm resistors and clamp diodes safely limits the input current to less than 2mA, even when the inputs of the device exceed the supply rails by 10V.

INTERNAL 5kΩ RESISTORS PLUS IINPUT CLAMP DIODES COMBINE TO PROTECT OP-X91 DEVICES AGAINST OVERVOLTAGE

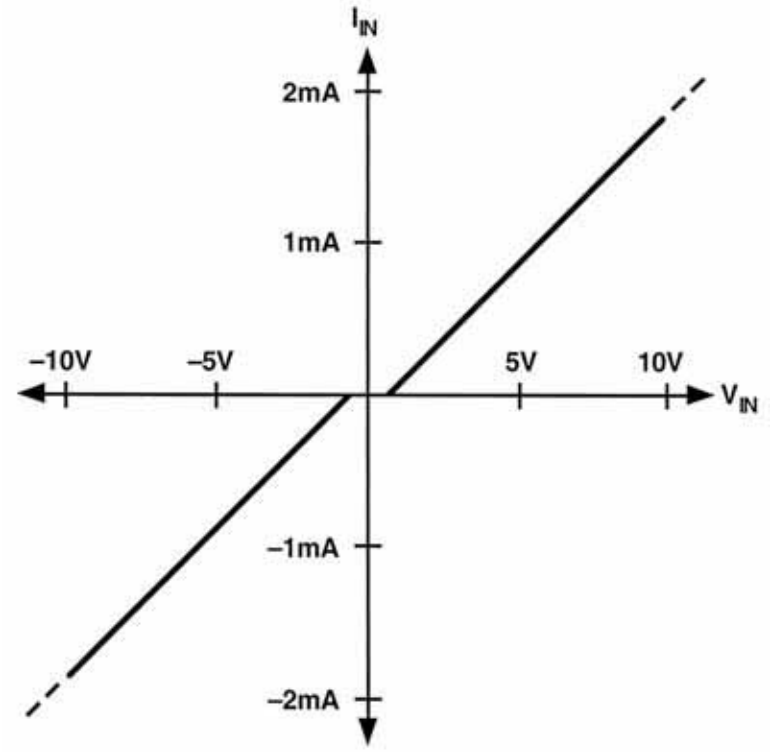

Figure 7.6

As an added safety feature, an additional pair of diodes is used in the input stage across Q3 and Q4 to prevent subsequent stages internal to the OPX91 from collapsing (that is, forced into cutoff). If these stages were forced into cutoff, then the amplifier would undergo output voltage phase reversal when the inputs exceeded the positive input common mode voltage. An illustration of the diodes' effectiveness is shown in Figure 7.7. Here, the OPX91 family can safely handle a 20Vp-p input signal on ±5V supplies without exhibiting any sign of output voltage phase reversal or other anomalous behavior. With these amplifiers, no external clamping diodes are required.

ADDITION OF TWO CLAMP DIODES PROTECTS OP-X91 DEVICES AGAINST OUTPUT PHASE REVERSAL

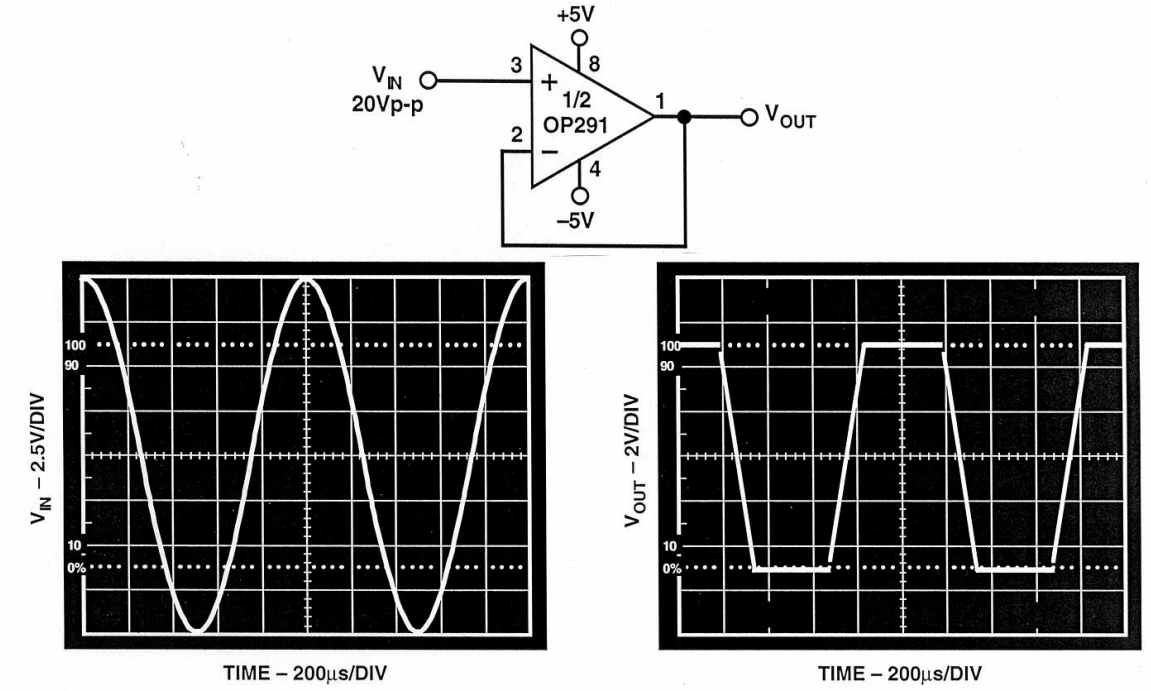

Figure 7.7

For those amplifiers where external protection is clearly required against both overvoltage abuse and output phase reversal, a common technique is to use a series resistance, R_S, to limit fault current, and Schottky diodes to clamp the input signal to the supplies, as shown in Figure 7.8.

GENERALIZED EXTERNAL PROTECTION SCHEME AGAINST INPUT OVERVOLTAGE ABUSE AND OUTPUT VOLTAGE PHASE REVERSAL IN SINGLE-SUPPLY OP AMPS

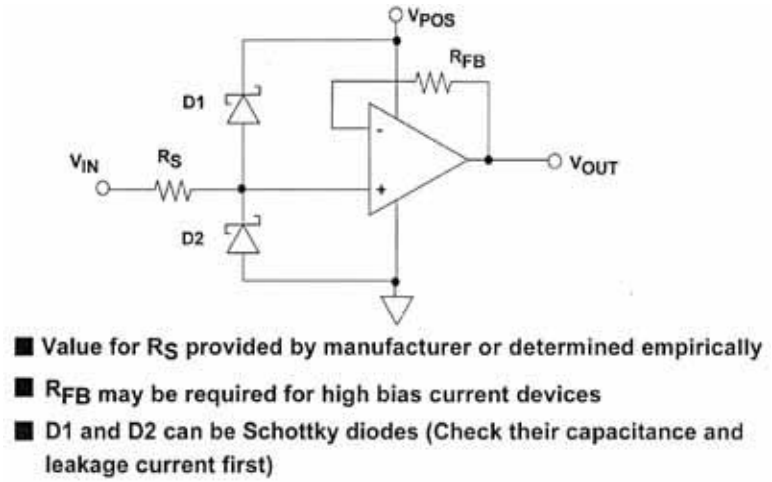

Figure 7.8

The external input series resistance, R_S, will be provided by the manufacturer of the amplifier, or determined empirically by the user with the method previously shown in Figure 7.2 and Eq. 7.1. More often than not, the value of this resistor will provide enough protection against output voltage phase reversal, as well as limiting the fault current through the Schottky diodes.

It is evident that whenever resistance is added in series with an amplifier's input, its offset and noise performance will be affected. The effects of this series resistance on circuit noise can be calculated using the following equation.

$$E_{n,total} = \sqrt{\left(e_{n,op\ amp}\right)^2 + \left(e_{n,R_S}\right)^2 + \left(R_S \ \ i_{n,op\ amp}\right)^2}$$

The thermal noise of the resistor, the voltage noise due to amplifier noise current flowing through the resistor, and the input noise voltage of the amplifier are added together (in root-sum-square manner, since the noise voltages are uncorrelated) to determine the total input noise and may be compared with the input voltage noise in the absence of the protection resistor.

A protection resistor in series with an amplifier input will also produce a voltage drop due to the amplifier bias current flowing through it. This drop appears as an increase in the circuit offset voltage (and, if the bias current changes with temperature, offset drift). In amplifiers where bias currents are approximately equal, a resistor in series with each input will tend to balance the effect and reduce the error. The effects of this additional series resistance on the circuit's overall offset voltage can be calculated:

$$V_{os(total)} = V_{os} + I_b R_s$$

For the case where $R_{FB} = R_S$ or where the source impedance levels are balanced, then the total circuit offset voltage can be expressed as:

$$V_{os(total)} = V_{os} + I_{os} R_s$$

To limit the additional noise of R_{FB}, it can be shunted with a capacitor.

When using external clamp diodes to protect operational amplifier inputs, the effects of diode junction capacitance and leakage current should be evaluated in the application. Diode junction capacitance and R_S will add an additional pole in the signal path, and diode leakage currents will double for every 10°C rise in ambient temperature. Therefore, low leakage diodes should be used such that, at the highest ambient temperature for the application, the total diode leakage current is less than one-tenth of the input bias current for the device at that temperature. Another issue with regard to the use of Schottky diodes is the change in their forward voltage drop as a function of temperature. These diodes do not, in fact, limit the signal to ±0.3V at all ambient temperatures, but if the Schottky diodes are at the same temperature as the op amp, they will limit the voltage to a safe level, even if they do not limit it at all times to within the data sheet rating. This is true if over-voltage is only possible at turn-on, when the diodes and the op amp will always be at the same temperature. If the op amp is warm when it is repowered, however, steps must be taken to ensure that diodes and op amp are at the same temperature.

UNDERSTANDING AND PROTECTING INTEGRATED CIRCUITS FROM ELECTROSTATIC DISCHARGE (ESD)

Wes Freeman

Integrated circuits can be damaged by the high voltages and high peak currents that can be generated by electrostatic discharge. Precision analog circuits, which often feature very low bias currents, are more susceptible to damage than common digital circuits, because the traditional input-protection structures which protect against ESD damage also increase input leakage.

The keys to eliminating ESD damage are: (1) awareness of the sources of ESD voltages, and (2) understanding the simple handling steps that will discharge potential voltages safely.

The basic definitions relating to ESD are given in Figure 7.9. Notice that the *ESD Failure Threshold* level relates to any of the IC data sheet limits, and not simply to a *catastrophic failure* of the device. Also, the limits apply to each pin of the IC, not just to the input and output pins.

ESD DEFINITIONS

- **ESD (Electrostatic Discharge):**
  - **A single fast, high current transfer of electrostatic charge.**
    - **Direct contact between two objects at different potentials.**
    - **A high electrostatic field between two objects when they are close in proximity.**

- **ESD Failure Threshold:**
  - **The highest voltage level at which all pins on a device can be subjected to ESD zaps without failing any 25°C data sheet limits**

Figure 7.9

The generation of static electricity caused by rubbing two substances together is called the *triboelectric effect*. Static charge can be generated either by dissimilar materials (for example, rubber-soled shoes moving across a rug) or by separating similar materials (for example, pulling transparent tape off of a roll).

A wide variety of common human activities can create high electrostatic charge. Some examples are given in Figure 7.10. The values shown will occur with a fairly high relative humidity. Low humidity, such as can occur indoors during cold weather, can generate voltages 10 times (or more) greater than the values shown.

EXAMPLES OF ELECTROSTATIC CHARGE GENERATION

- **Person walks across a typical carpet.**
  - **1000-1500V generated**
- **Person walks across a typical vinyl floor.**
  - **150 - 250V generated**
- **Person handles instructions protected by clear plastic covers.**
  - **400 - 600V generated**
- **Person handles polyethylene bags.**
  - **1000 - 1200V generated**
- **Person pours polyurethane foam into a box.**
  - **1200 - 1500V generated**
- **An IC slides down a grounded handler chute.**
  - **50 - 500V generated**
- **An IC slides down an open conductive shipping tube.**
  - **25 - 250V generated**

Note:

Above values can occur in a high (≈60%) RH environment. For low RH (≈30%), generated voltages can be >10 times those listed above!

Figure 7.10

In an effort to standardize the testing and classification of integrated circuits for ESD robustness, ESD models have been developed (Figure 7.11). These models attempt to simulate the source of ESD voltage. The assumptions underlying the three commonly-used models are different, so results are not directly comparable.

MODELING ELECTRONIC POTENTIAL

- **Three Models:**
  1. **Human Body Model (HBM)**
  2. **Machine Model (MM)**
  3. **Charged Device Model (CDM)**
- **Model Correlation:**
  - **Low - Assumptions are Different**

Figure 7.11

The most-often encountered ESD model is the Human Body Model (HBM). This model simulates the approximate resistance and capacitance of a human body with a simple RC network. The capacitor is charged through a high voltage power supply (HVPS) and then discharged (using a high voltage switch) through a series resistor.

The RC values for different individuals will, of course, vary. However, the HBM has been standardized by MIL-STD-883 Method 3015 Electrostatic Discharge Sensitivity Classification, which specifies R-C combinations of 1.5kohm and 100pF. (R, C, and L values for all three ESD models are shown in Figure 7.12.)

ESD MODELS APPLICABLE TO ICs

- **Human Body Model (HBM)**

  Simulates the discharge event that occurs when a person charged to either a positive or negative potential touches an IC at different potential.

  RLC: R = 1.5kΩ, L ≈ 0nH, C = 100pF

- **Machine Model (MM)**

  Non-real-world Japanese model based on worst-case HBM.

  RLC: R ≈ 0Ω, L ≈ 500nH, C = 200pF

- **Charged Device Model (CDM)**

  Simulates the discharge that occurs when a pin on an IC, charged to either a positive or negative potential, contacts a conductive surface at a different (usually ground) potential.

  RLC: R = 1Ω, L ≈ 0nH, C= 1 - 20pF

Figure 7.12

The Machine Model (MM) is a worst-case Human Body Model. Rather than using an *average* value for resistance and capacitance of the human body, the MM assumes a worst-case value of 200pF and 0ohms. The 0ohm output resistance of the MM is also intended to simulate the discharge from a charged conductive object (for example, a charged DUT socket on an automatic test system) to an IC pin, which is how the Machine Model earned its name. However, the MM does not simulate many known real-world ESD events. Rather, it models the ESD event resulting from a ideal voltage source (in other words, with no resistance in the discharge path). EIAJ Specification ED-4701 Test Method C-111 Condition A and ESD Association Specification S5.2 provide guidelines for MM testing.

The Charged Device Model (CDM) originated at AT&T. This model differs from the HBM and the MM, in that the source of the ESD energy is the IC itself. The CDM assumes that the integrated circuit die, bond wires, and lead frame are charged to some potential (usually positive with respect to ground). One or more of the IC pins then contacts ground, and the stored charge rapidly discharges through the leadframe and bond wires. Typical examples of triboelectric charging followed by a CDM discharge include:

1. An IC slides down a handler chute and then a corner pin contacts a grounded stop bar.

2. An IC slides down an open conductive shipping tube and then a corner pin contacts a conductive surface.

The basic concept of the CDM is different than the HBM and MM in two ways. First, the CDM simulates a charged IC discharging to ground, while the HBM and MM both simulate a charged source discharging into the IC. Thus, current flows out of the IC during CDM testing, and into the IC during HBM and MM testing. The second difference is that the capacitor in the CDM is the capacitance of the package, while the HBM and MM use a fixed external capacitor.

Unlike the HBM and MM, CDM ESD thresholds may vary for the same die in different packages. This occurs because the device under test (DUT) capacitance is a function of the package. For example, the capacitance of an 8-pin package is different than the capacitance of a 14-pin package. CDM capacitance values can vary from about 1 to 20pF. The device capacitance is discharged through a 1ohm resistor.

Schematic representations of the three models are shown in Figure 7.13. Notice that C1 in the HBM and MM are external capacitors, while C_{PKG} in the CDM is the internal capacitance of the DUT.

The HBM discharge waveform is a predicable unipolar RC pulse, while the MM discharge shows ringing because of the parasitic inductance in the discharge path (typically 500nH.). Ideally, the CDM waveform is also a single unipolar pulse, but the parasitic inductance in series with the 1ohm resistor slows the rise time and introduces some ringing.

SCHEMATIC RESPRESENTATION OF ESD MODELS AND TYPICAL DISCHARGE WAVEFORMS

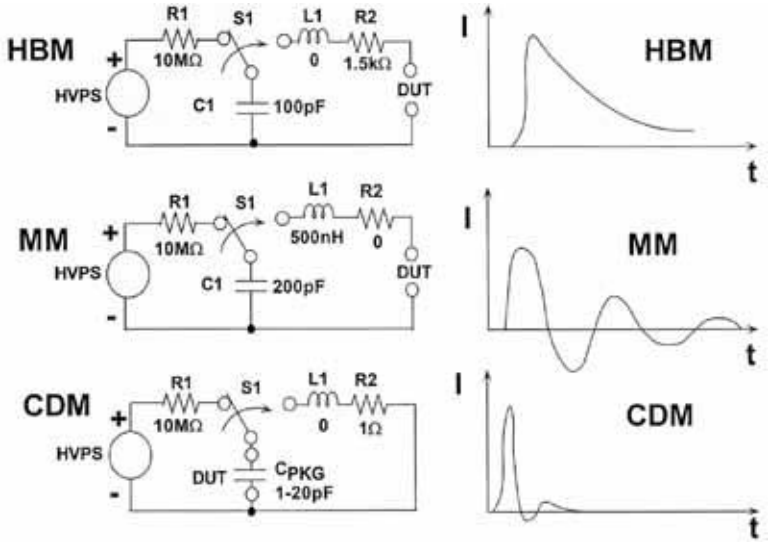

Figure 7.13

The significant features of each ESD model are summarized in Figure 7.14. The peak currents shown for each model are based on a test voltage of 400V. Peak current is lowest for the HBM because of the relatively high discharge resistance. The CDM discharge has low energy because device capacitance is only in the range of 1pF to 20pF, but peak current is high. The MM has the highest energy discharge, because it has the highest capacitance value (Power = 0.5 CV^2).

COMPARISON OF HBM, MM, AND CDM ESD MODELS

MODEL:	HBM	MM	SOCKETED CDM
Simulate:	Human Body	Machine	Charged Device
Origin:	US Military, Late 1960s	Japan, 1978	AT&T,1974
Real World?	Yes	Generally	Yes
RC:	1.5kΩ, 100pF	0Ω, 200pF	1Ω, 1 - 20pF
Rise Time	<10ns (6-9ns typ)	14ns*	400ps**
Ipeak at 400V	0.27A	5.8A*	2.1A**
Energy:	Moderate	High	Low
Package Dependent:	No	No	Yes
Standard:	MIL-STD-883 Method 3015	ESD Association Std S5.2; EIAJ Std. ED-4701, Method C-111	ESD Association Draft Std. DS5.3

* These values per ESD Association Std. S5.2.
EIAJ Std. ED-4701 Method C-111 includes no waveform specifications.
** These values are for the direct charging (socketed) method.

Figure 7.14

Figure 7.15 compares 400V discharge waveforms of the CDM, MM, and HBM, with the same current and time scales.

RELATIVE COMPARISON OF 400V HBM, MM, AND CDM DISCHARGES

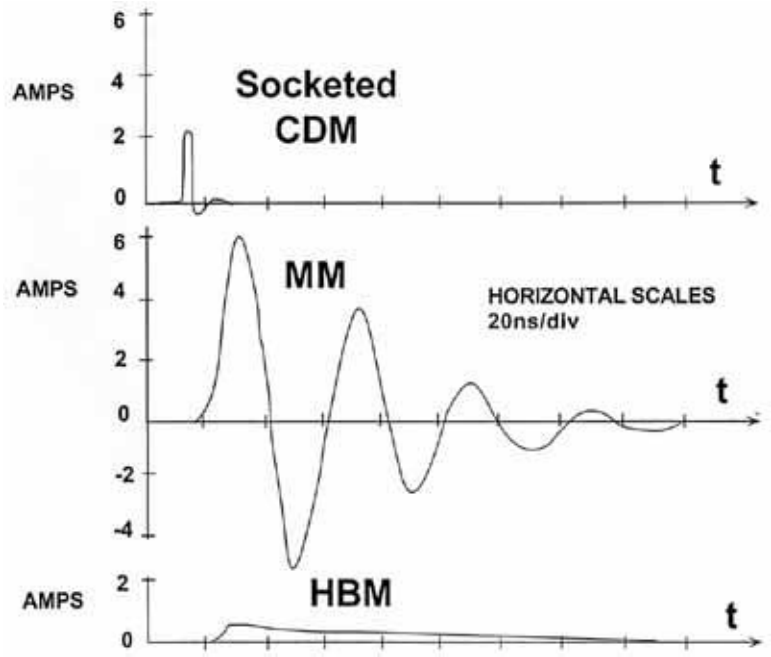

Figure 7.15

The CDM waveform corresponds to the shortest known real-world ESD event. The waveform has a rise time of <1ns, with the total duration of the CDM event only about 2ns. The CDM waveform is essentially unipolar, although some ringing occurs at the end of the pulse that results in small negative-going peaks. The very short duration of the overall CDM event results in an overall discharge of relatively low energy, but peak current is high.

The MM waveform consists of both positive- and negative-going sinusoidal peaks, with a resonance frequency of 10MHz to 15MHz. The initial MM peak has a typical rise time of 14ns, and the total pulse duration is about 150ns. The multiple high current, moderate duration peaks of the MM result in an overall discharge energy that is by far the highest of the three models for a given test voltage.

The risetime for the unipolar HBM waveform is typically 6-9ns, and the waveform decays exponentially towards 0V with a fall time of approximately 150ns. (Method 3015 requires a rise time of <10ns and a delay time of 150ns ± 20ns, with decay time defined as the time for the waveform to drop from 100% to 36.8% of peak current). The peak current for the HBM is 400V/1500ohms, or 0.267A, which is much lower than is produced by 400V CDM and MM events. However, the relatively long duration of the total HBM event still results in an overall discharge of moderately high energy.

As previously noted, the MM waveform is bipolar while HBM and CDM waveforms are primarily unipolar. However, HBM and CDM testing is done with both positive and negative polarity pulses. Thus all three models stress the IC in both directions.

MIL-STD-883 Method 3015 classifies ICs for ESD failure threshold. The classification limits, shown in Figure 7.16, are derived using the HBM shown in Figure 7.13. Method 3015 also mandates a marking method to denote the ESD classification. All military grade Class 1 and 2 devices have their packages marked with one or two "Delta" symbols, respectively, while class 3 devices (with a failure threshold >4kV) do not have any ESD marking. Commercial and industrial grade IC packages may not be marked with any ESD classification symbol.

CLASSIFYING AND MARKING ICs FOR ESD
PER MIL-883C, METHOD 3015

HBM ESD CLASS	FAILURE THRESHOLD	MARKING
1	<2kV	Δ
2	2kV - <4kV	Δ Δ
3	>4kV	None

Note: Commercial and Industrial Grade ICs are not marked for ESD

Figure 7.16

Notice that the Class 1 limit includes all devices which do not pass a 2kV threshold. However, a Class 1 rating does not imply that all devices within that class will pass 1,999V. In any event, the emphasis must be placed on eliminating ESD exposure, not on attempting to decide how much ESD exposure is 'safe.'

A detailed discussion of IC failure mechanisms is beyond the scope of this seminar, but some typical ESD effects are shown in Figure 7.17.

UNDERSTANDING ESD DAMAGE

- **ESD Failure Mechanisms:**
  - **Dielectric or junction damage**
  - **Surface charge accumulation**
  - **Conductor fusing.**
- **ESD Damage Can Cause:**
  - **Increased leakage**
  - **Reduced performance**
  - **Functional failures of ICs.**
- **ESD Damage is often Cumulative:**
  - **For example, each ESD "zap" may increase junction damage until, finally, the device fails.**

Figure 7.17

For the design engineer or technician, the most common manifestation of ESD damage is a catastrophic failure of the IC. However, exposure to ESD can also cause increased leakage or degrade other parameters. If a device appears to not meet a data sheet specification during evaluation, the possibility of ESD damage should be considered.

Special care should be taken when breadboarding and evaluating ICs. The effects of ESD damage can be cumulative, so repeated mishandling of a device can eventually cause a failure. Inserting and removing ICs from a test socket, storing devices during evaluation, and adding or removing external components on the breadboard should all be done while observing proper ESD precautions. Again, if a device fails during a prototype system development, repeated ESD stress may be the cause.

The key word to remember with respect to ESD is *prevention*. There is no way to un-do ESD damage, or to compensate for its effects.

THE MOST IMPORTANT THING TO REMEMBER ABOUT ESD DAMAGE

- **ESD DAMAGE *CANNOT* BE "CURED"!**
- **Circuits cannot be *tweaked, nulled, adjusted,* etc., to compensate for ESD damage.**

ESD DAMAGE MUST BE *PREVENTED!*

Figure 7.18

Since ESD damage can not be undone, the only cure is prevention. Luckily, prevention is a simple two-step process. The first step is recognizing ESD-sensitive products, and the second step is understanding how to handle these products.

PREVENTING ESD DAMAGE TO ICs

Two key elements in protecting circuits from ESD damage are:

- **Recognizing ESD-sensitive products**
- **Always handling ESD-sensitive products at a *grounded* workstation.**

Figure 7.19

All static sensitive devices are shipped in protective packaging. ICs are usually contained in either conductive foam or in antistatic tubes. Either way, the container is then sealed in a static-dissipative plastic bag. The sealed bag is marked with a distinctive sticker, such as is shown in Figure 7.20, which outlines the appropriate handling procedures.

RECOGNiZING ESD-SENSITIVE DEVICES

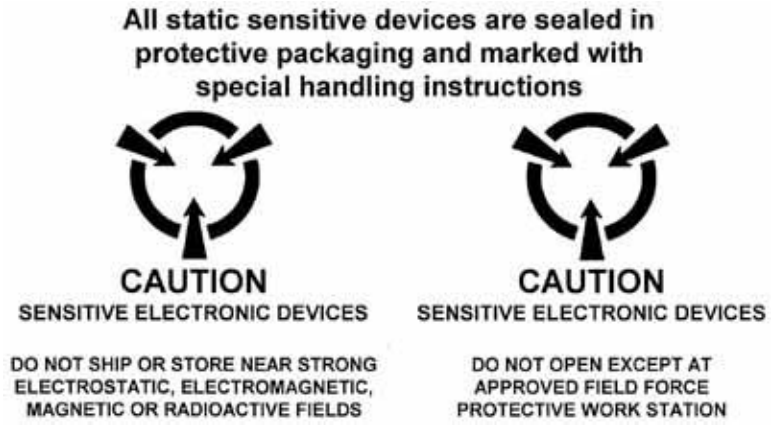

Figure 7.20

Once ESD-sensitive devices are identified, protection is easy. Obviously, keeping ICs in their original protective packaging as long as possible is the first step. The second step is to discharge potential ESD sources before damage to the IC can occur. The HBM capacitance is only 100pF, so discharging a potentially dangerous voltage can be done quickly and safely through a high impedance. Even with a source resistance of 10Megohms, the 100pF will be discharged in less than 100milliseconds.

The key component required for safe ESD handling is a workbench with a static-dissipative surface, as shown in Figure 7.21. This surface is connected to ground through a 1Megohm resistor, which dissipates static charge while protecting the user from electrical shock hazards caused by ground faults. If existing bench tops are nonconductive, a static-dissipative mat should be added, along with a discharge resistor.

WORKSTATION FOR HANDLING ESD-SENSITIVE DEVICES

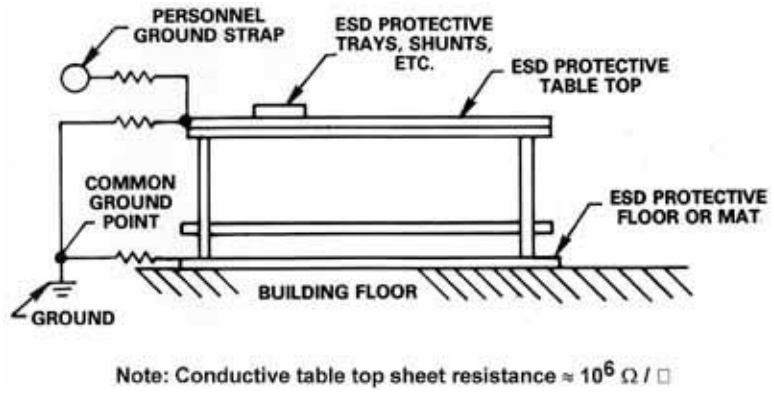

Figure 7.21

Notice that the surface of the workbench has a moderately high sheet resistance. It is neither necessary nor desirable to use a low-resistance surface (such as a sheet of copper-clad PC board) for the work surface. Remember, the CDM assumes that a high peak current will flow if a charged IC is discharged through a low impedance. This is precisely what happens when a charged IC contacts a grounded copper clad board. When the same charged IC is placed on the surface shown in Figure 7.21, however, the peak current is not high enough to damage the device.

A conductive wrist strap is also recommended while handling ESD-sensitive devices. The wrist strap ensures that normal tasks, such as peeling tape off of packages, will not cause damage to ICs. Again, a 1Megohm resistor, from the wrist strap to ground, is required for safety.

When building prototype breadboards or assembling PC boards which contain ESD-sensitive devices, all passive components should be inserted and soldered before the ICs. This procedure minimizes the ESD exposure of the sensitive devices. The soldering iron must, of course, have a grounded tip.

Protecting ICs from ESD requires the participation of both the IC manufacturer and the customer. IC manufacturers have a vested interest in providing the highest possible level of ESD protection for their products. IC circuit designers, process engineers, packaging specialists and others are constantly looking for new and improved circuit designs, processes, and packaging methods to withstand or shunt ESD energy (Figure 7.22)

ANALOG DEVICES' COMMITMENT

- **Analog Devices is committed to helping our customers *prevent* ESD damage by:**
  - **Building products with the highest level of ESD protection commensurate with performance requirements**
  - **Protecting products from ESD during shipment**
  - **Helping customers to avoid ESD exposure during manufacture**

Figure 7.22

A complete ESD protection plan, however, requires more than building-ESD protection into ICs. Users of ICs must also provide their employees with the necessary knowledge of and training in ESD handling procedures (Figure 7.23).

ESD PROTECTION REQUIRES A PARTNERSHIP BETWEEN THE IC SUPPLIER AND THE CUSTOMER

ANALOG DEVICES:

- **Circuit Design and Fabrication -**
  - **Design and manufacture products with the highest level of ESD protection consistent with required analog and digital performance.**
- **Pack and Ship -**
  - **Pack in static dissipative material. Mark packages with ESD warning.**

CUSTOMERS:

- **Incoming Inspection -**
  - **Inspect at grounded workstation. Minimize handling.**
- **Inventory Control -**
  - **Store in original ESD-safe packaging. Minimize Handling.**
- **Manufacturing -**
  - **Deliver to work are in original ESD-safe packaging. Open packages only at grounded workstation. Package subassemblies in static dissipative packaging.**
- **Pack and Ship -**
  - **Pack in static dissipative material if required. Replacement or optional boards may require special attention.**

Figure 7.23

The **ESD Protection Manual** is available from Analog Devices' literature department. This manual provides additional information on static-dissipative work surfaces, packaging materials, protective clothing, ESD training, and other subjects.

ESD PROTECTION MANUAL

Contact Analog Devices' literature department for a copy of the ESD Prevention Manual, which has further information on:

- **Handling Instructions**
- **Packaging**
- **Static-Safe Facilities**
- **Other ESD Issues**

Figure 7.24

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4. **ESD Prevention Manual**, Analog Devices, Inc.

5. *MIL-STD-883 Method 3015, Electrostatic Discharge Sensitivity Classification*. Available from Standardization Document Order Desk, 700 Robbins Ave., Building #4, Section D, Philadelphia, PA 19111-5094.

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7. *ESD Association Standard S5.2 for Electrostatic Discharge (ESD) Sensitivity Testing -Machine Model (MM)- Component Level*. Available from the ESD Association, Inc., 200 Liberty Plaza, Rome, NY 13440.

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