

SECTION 5

UNDERSAMPLING APPLICATIONS

- Fundamentals of Undersampling
- Increasing ADC SFDR and ENOB using External SHAs
- Use of Dither Signals to Increase ADC Dynamic Range
- Effect of ADC Linearity and Resolution on SFDR and Noise in Digital Spectral Analysis Applications
- Future Trends in Undersampling ADCs

SECTION 5

UNDERSAMPLING APPLICATIONS

Walt Kester

An exciting new application for wideband, low distortion ADCs is called *undersampling, harmonic sampling, bandpass sampling, or Super-Nyquist Sampling*. To understand these applications, it is necessary to review the basics of the sampling process.

The concept of discrete time and amplitude sampling of an analog signal is shown in Figure 5.1. The continuous analog data must be sampled at discrete intervals, t_s , which must be carefully chosen to insure an accurate representation of the original analog signal. It is clear that the more samples taken (faster sampling rates), the more accurate the digital representation, but if fewer samples are taken (lower sampling rates), a point is reached where critical information about the signal is actually lost. This leads us to the statement of Shannon's Information Theorem and Nyquist's Criteria given in Figure 5.2. Most textbooks state the Nyquist theorem along the following lines: *A signal must be sampled at a rate greater than twice its maximum frequency in order to ensure unambiguous data*. The general assumption is that the signal has frequency components from dc to some upper value, f_a . The Nyquist Criteria thus requires sampling at a rate $f_s > 2f_a$ in order to avoid overlapping aliased components. For signals which do not extend to dc, however, the minimum required sampling rate is a function of the *bandwidth* of the signal as well as its position in the frequency spectrum.

SAMPLING AN ANALOG SIGNAL

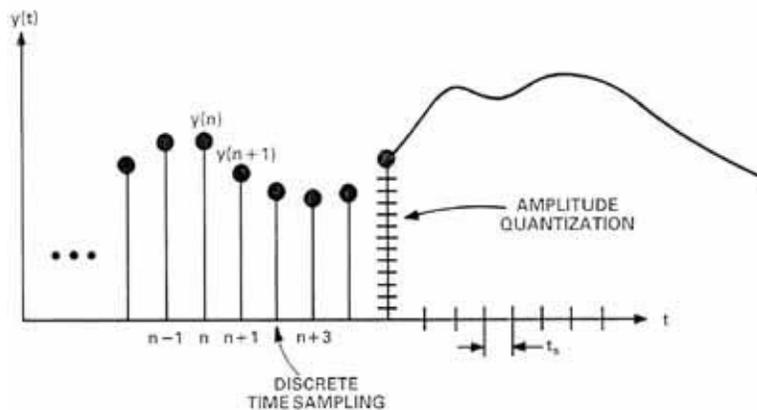


Figure 5.1

SHANNON'S INFORMATION THEOREM AND NYQUIST'S CRITERIA

■ Shannon:

- ◆ An Analog Signal with a *Bandwidth* of f_a Must be Sampled at a Rate of $f_s > 2f_a$ in Order to Avoid the Loss of Information.
- ◆ The signal bandwidth may extend from DC to f_a (*Baseband Sampling*) or from f_1 to f_2 , where $f_a = f_2 - f_1$ (*Undersampling, Bandpass Sampling, Harmonic Sampling, Super-Nyquist*)

■ Nyquist:

- ◆ If $f_s < 2f_a$, then a Phenomena Called *Aliasing* Will Occur.
- ◆ Aliasing is used to advantage in undersampling applications.

Figure 5.2

In order to understand the implications of *aliasing* in both the time and frequency domain, first consider the four cases of a time domain representation of a sampled sinewave signal shown in Figure 5.3. In Case 1, it is clear that an adequate number of samples have been taken to preserve the information about the sinewave. In Case 2 of the figure, only four samples per cycle are taken; still an adequate number to preserve the information. Case 3 represents the ambiguous limiting condition where $f_s = 2f_a$. If the relationship between the sampling points and the sinewave were such that the sinewave was being sampled at precisely the zero crossings (rather than at the peaks, as shown in the illustration), then all information regarding the sinewave would be lost. Case 4 of Figure 5.3 represents the situation where $f_s < 2f_a$, and the information obtained from the samples indicates a sinewave having a frequency which is lower than $f_s/2$, i.e. the out-of-band signal is *aliased* into the Nyquist bandwidth between dc and $f_s/2$. As the sampling rate is further decreased, and the analog input frequency f_a approaches the sampling frequency f_s , the aliased signal approaches dc in the frequency spectrum.

TIME DOMAIN EFFECTS OF ALIASING

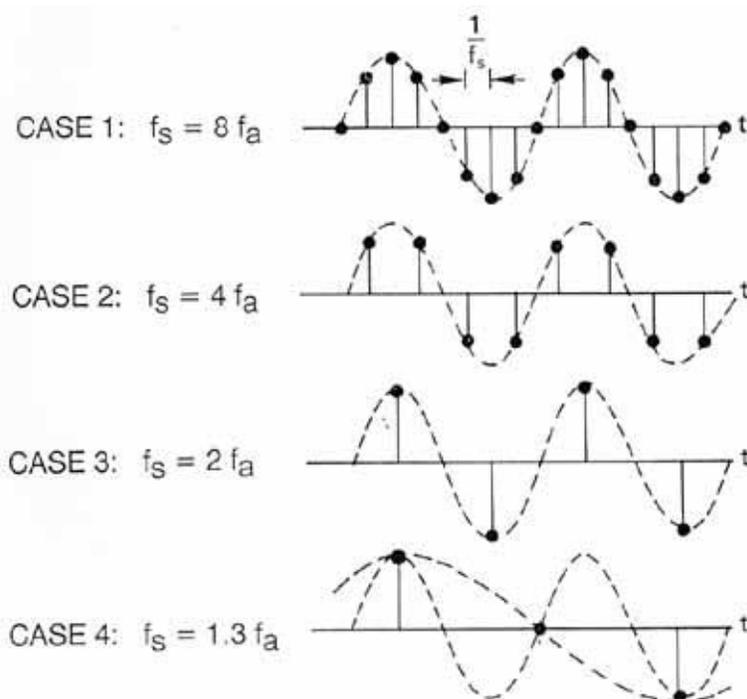


Figure 5.3

The corresponding frequency domain representation of the above scenario is shown in Figure 5.4. Note that sampling the analog signal f_a at a sampling rate f_s actually produces two alias frequency components, one at $f_s + f_a$, and the other at $f_s - f_a$. The upper alias, $f_s + f_a$, seldom presents a problem, since it lies outside the Nyquist bandwidth. It is the lower alias component, $f_s - f_a$, which causes problems when the input signal exceeds the Nyquist bandwidth, $f_s/2$.

FREQUENCY DOMAIN EFFECTS OF ALIASING

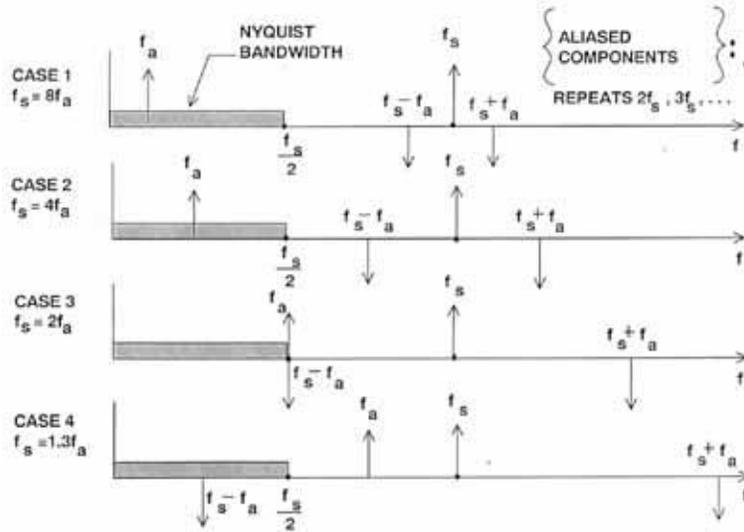


Figure 5.4

From Figure 5.4, we make the extremely important observation that *regardless of where the analog signal being sampled happens to lie in the frequency spectrum (as long as it does not lie on multiples of $f_s/2$), the effects of sampling will cause either the actual signal or an aliased component to fall within the Nyquist bandwidth between dc and $f_s/2$* . Therefore, any signals which fall outside the bandwidth of interest, whether they be spurious tones or random noise, must be adequately filtered *before* sampling. If unfiltered, the sampling process will alias them back within the Nyquist bandwidth where they can corrupt the wanted signals.

Methods exist which use aliasing to our advantage in signal processing applications. Figure 5.5 shows four cases where a signal having a 1MHz bandwidth is located in different portions of the frequency spectrum. The sampling frequency must be chosen such that there is no overlapping of the aliased components. In general, the sampling frequency must be at least twice the signal bandwidth, and the sampled signal must not cross an integer multiple of $f_s/2$.

MINIMUM SAMPLING RATE REQUIRED FOR NON-OVERLAPPING ALIASING OF A 1MHz BANDWIDTH SIGNAL

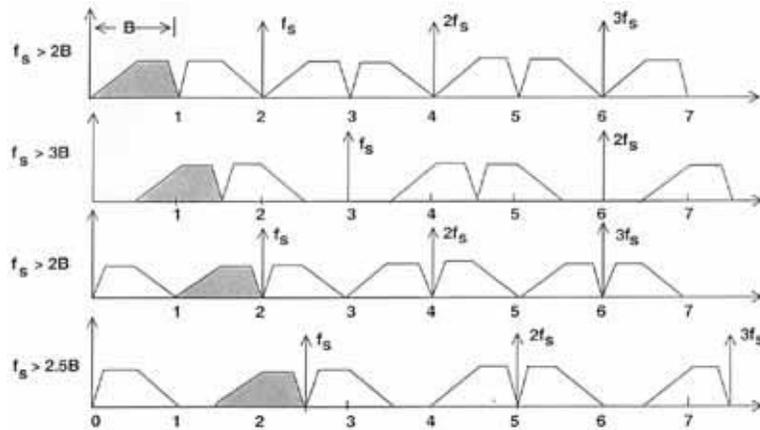


Figure 5.5

In the first case, the signal occupies a band from dc to 1MHz, and therefore must be sampled at greater than 2MSPS. The second case shows a 1MHz signal which occupies the band from 0.5 to 1.5MHz. Notice that this signal must be sampled at a minimum of 3MSPS in order to avoid overlapping aliased components. In the third case, the signal occupies the band from 1 to 2MHz, and the minimum required sampling rate for no overlapping aliased components drops back to 2MSPS. The last case shows a signal which occupies the band from 1.5 to 2.5MHz. This signal must be sampled at a minimum of 2.5MSPS to avoid overlapping aliased components.

This analysis can be generalized as shown in Figure 5.6. The actual minimum required sampling rate is a function of the ratio of the highest frequency component, f_{MAX} , to the total signal bandwidth, B. Notice for large ratios of f_{MAX} to the bandwidth, B, the minimum required sampling frequency approaches 2B.

**MINIMUM REQUIRED SAMPLING RATE AS A FUNCTION OF
THE RATIO OF THE HIGHEST FREQUENCY COMPONENT
TO THE TOTAL SIGNAL BANDWIDTH**

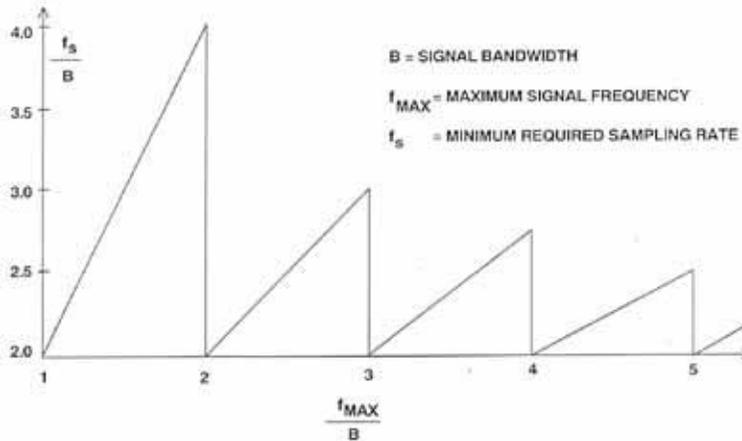


Figure 5.6

Let us consider the case of a signal which occupies a *bandwidth* of 1MHz and lies between 6 and 7MHz as shown in Figure 5.7. Shannon's Information Theorem states that the signal (bandwidth = 1MHz) must be sampled at least at 2MSPS in order to retain all the information (avoid overlapping aliased components). Assuming that the ADC sampling rate, f_s , is 2MSPS, additional sampling frequencies are generated at all integer multiples of f_s : 4MHz, 6MHz, 8MHz, etc. The actual signal between 6 and 7MHz is aliased around each of these sampling frequency harmonics, f_s , $2f_s$, $3f_s$, $4f_s$, ..., hence the term *harmonic sampling*. Notice that any one of the aliased components is an accurate representation of the original signal (the frequency inversion which occurs for one-half of the aliased components can be removed in software). In particular, the component lying in the baseband region between dc and 1MHz is the one calculated using a Fast Fourier Transform, and is also an accurate representation of the original signal, assuming no ADC conversion errors. The FFT output tells us all the characteristics of the signal except for its original position in the frequency spectrum, which was a priori knowledge.

INTERMEDIATE FREQUENCY (IF) SIGNAL BETWEEN 6 AND 7 MHz IS ALIASED BETWEEN DC AND 1MHz BY SAMPLING AT 2MSPS

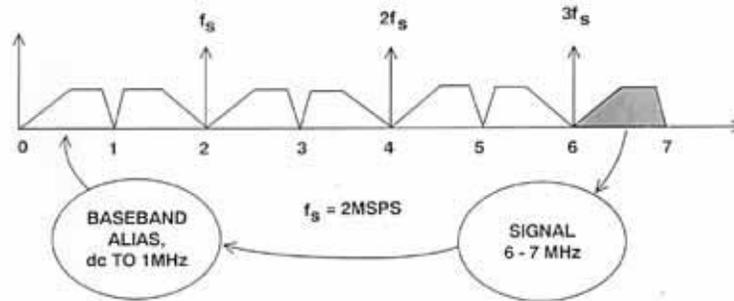


Figure 5.7

A popular application of undersampling is in digital receivers. A simplified block diagram of a traditional digital receiver using *baseband* sampling is shown in Figure 5.8. The mixer in the RF section of the receiver mixes the signal from the antenna with the RF frequency of the local oscillator. The desired information is contained in relatively small bandwidth of frequencies Δf . In actual receivers, Δf may be as high as a few megahertz. The local oscillator frequency is chosen such that the Δf band is centered about the IF frequency at the bandpass filter output. Popular IF frequencies are generally between 10 and 100MHz. The detector then translates the Δf frequency band down to baseband where it is filtered and processed by a baseband ADC. Actual receivers can have several stages of RF and IF processing, but the simple diagram serves to illustrate the concepts.

SIMPLIFIED DIGITAL RECEIVER USING BASEBAND SAMPLING

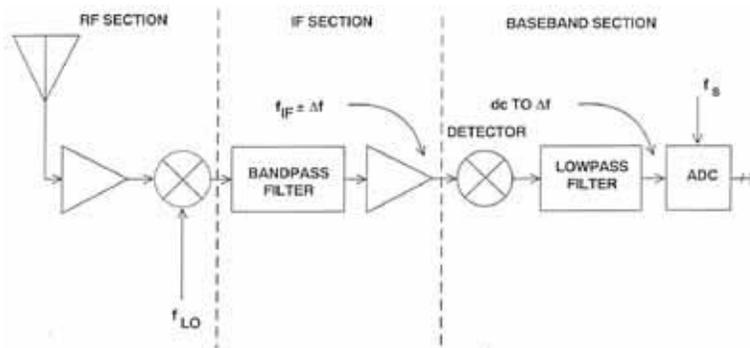


Figure 5.8

In a receiver which uses direct IF-to-digital techniques (often called *undersampling*, *harmonic*, *bandpass*, or *IF sampling*), the IF signal is applied directly to a wide bandwidth ADC as shown in Figure 5.9. The ADC sampling rate is chosen to be at least $2 \Delta f$. The process of sampling the IF frequency at the proper rate causes one of the aliased components of Δf to appear in the dc to $f_s/2$ Nyquist

bandwidth of the ADC output. DSP techniques can now be used to process the digital baseband signal. This approach eliminates the detector and its associated noise and distortion. There is also more flexibility in the DSP because the ADC sampling rate can be shifted to tune the exact position of the f signal within the baseband.

The obvious problem with this approach is that the ADC must now be able to accurately digitize signals which are well outside the dc to $f_s/2$ Nyquist bandwidth which most ADCs were designed to handle. Special techniques are available, however, which can extend the dynamic range of ADCs to include IF frequencies.

SIMPLIFIED DIGITAL RECEIVER USING IF SAMPLING

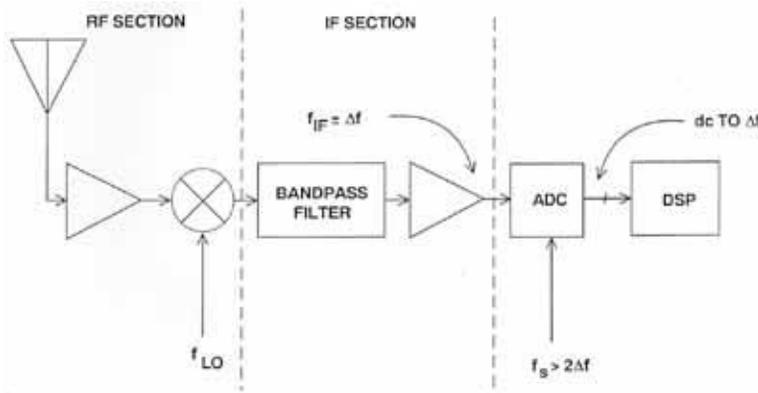


Figure 5.9

Let us consider a typical example, where the IF frequency is 72.5MHz, and the desired signal occupies a bandwidth of 4MHz ($B=4\text{MHz}$), centered on the IF frequency (see Figure 5.10). We know from the previous discussion that the minimum sampling rate must be greater than 8MHz, probably on the order of 10MHz in order to prevent dynamic range limitations due to aliasing. If we place the sampling frequency at the lower band-edge of 70MHz ($72.5-2.5$), we will definitely recover the aliased component of the signal in the dc to 5MHz baseband. There is, however, no need to sample at this high rate, so we may choose any sampling frequency 10MHz or greater which is an integer sub-multiple of 70MHz, i.e., $70 \div 2 = 35.000\text{MHz}$, $70 \div 3 = 23.333\text{MHz}$, $70 \div 4 = 17.500\text{MHz}$, $70 \div 5 = 14.000\text{MHz}$, $70 \div 6 = 11.667\text{MHz}$, or $70 \div 7 = 10.000\text{MHz}$. We will therefore choose the lowest possible sampling rate of 10.000MHz ($70 \div 7$).

**INTERMEDIATE FREQUENCY (IF) SIGNAL
AT 72.5MHz (± 2 MHz) IS ALIASED BETWEEN
DC AND 5MHz BY SAMPLING AT 10MSPS**

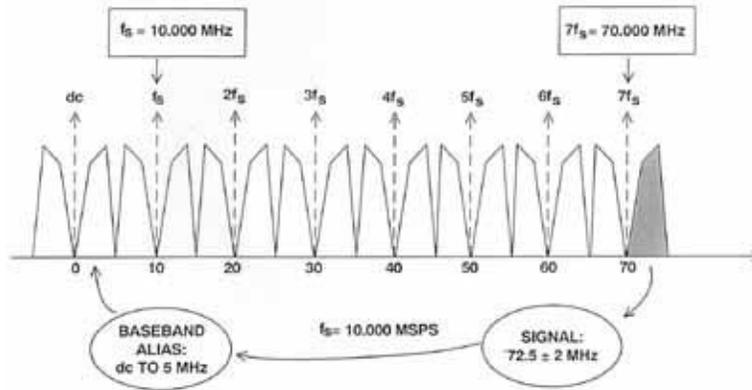


Figure 5.10

There is an advantage in choosing a sampling frequency which is a sub-multiple of the lower band-edge in that there is no frequency inversion in the baseband alias as would be the case for a sampling frequency equal to a sub-multiple of the upper band-edge. (Frequency inversion can be easily dealt with in the DSP software should it occur, so the issue is not very important).

Undersampling applications such as the one just described generally require sampling ADCs which have low distortion at the high input IF input frequency. For instance, in the example just discussed, the ADC sampling rate requirement is only 10MSPS, but low distortion is required (preferably 60 to 80dB SFDR) at the IF frequency of 72.5MHz.

A large opportunity for bandpass sampling is in digital cellular radio base stations. For systems which have RF frequencies at 900MHz, 70MHz is a popular first-IF frequency. For systems using an RF frequency of 1.8GHz, first-IF frequencies between 200 and 240MHz are often used.

In broadband receiver applications, one ADC digitizes multiple channels in the receive path. Individual channel selection and filtering is done in the digital domain. Narrowband channel characteristics such as bandwidth, passband ripple, and adjacent channel rejection can be controlled with changes to digital parameters (i.e. filter coefficients). Such flexibility is not possible when narrowband analog filters are in the receive path.

Figure 5.11 illustrates the kind of input spectrum an ADC must digitize in a multichannel design. The spectral lines represent narrowband signal inputs from a variety of signal sources at different received power levels. Signal "C" could represent a transmitter located relatively far away from the signal sources "A" and "B". However, the receiver must recover all of the signals with equal clarity. This requires that distortion from the front-end RF and IF signal processing components,

including the ADC, not exceed the minimum acceptable level required to demodulate the weakest signal of interest. Clearly, third-order intermodulation distortion generated by "A" and "B" ($2B - A$, and $2A - B$) will distort signals C and D if the nonlinearities in the front-end are severe. Strong out-of-band signals can also introduce distortion; signal "E" in Figure 5.11 shows a large signal that is partially attenuated by the antialiasing filter. In many systems, the power level of the individual transmitters is under control of the base station. This capability helps to reduce the total dynamic range required.

BROADBAND DIGITAL RECEIVER ADC INPUT

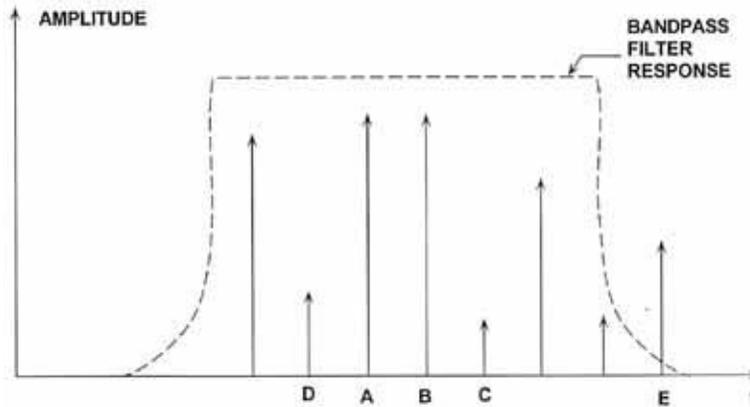


Figure 5.11

In broadband receiver applications (using an RF frequency of approximately 900MHz, and a first-IF frequency of 70MHz), SFDR requirements for the ADC are typically 70 to 80dBc. Signal bandwidths between 5MHz and 10MHz are common, requiring corresponding sampling rates of 10MSPS to 20MSPS.

Sampling ADCs are generally designed to process signals up to Nyquist ($f_s/2$) with a reasonable amount of dynamic performance. As we have seen, however, even though the input bandwidth of a sampling ADC is usually much greater than its maximum sampling rate, the SFDR and effective bit (ENOB) performance usually decreases dramatically for full scale input signals much above $f_s/2$. This implies that the selection criteria for ADCs used in undersampling applications is SFDR or ENOB at the IF frequency, rather than sampling rate.

The general procedure for selecting an ADC for an undersampling application is not straightforward. The signal bandwidth and its location within the frequency spectrum must be known. The bandwidth of the signal determines the minimum sampling rate required, and in order to ease the requirement on the antialiasing filter, a sampling rate of 2.5 times the signal bandwidth works well. After determining the approximate sampling frequency needed, select the ADC based on the required SFDR, $S/(N+D)$, or ENOB at the IF frequency. This is where the dilemma usually occurs. You will find that an ADC specified for a maximum sampling rate of 10MSPS, for instance, will not have adequate SFDR at the IF frequency (72.5MHz in the example above), even though its performance is excellent up to its Nyquist frequency of 5Mhz. In order to meet the SFDR, $S/(N+D)$, or ENOB

requirement, you will generally require an ADC having a much higher sampling rate than is actually needed.

Figure 5.12 shows the approximate SFDR versus input frequency for the AD9022/AD9023 (20MSPS), AD9026/AD9027 (31MSPS), and the AD9042 (40MSPS) series of low distortion ADCs. Notice that the AD9042 has superior SFDR performance.

SFDR COMPARISON BETWEEN 12-BIT SAMPLING ADCs

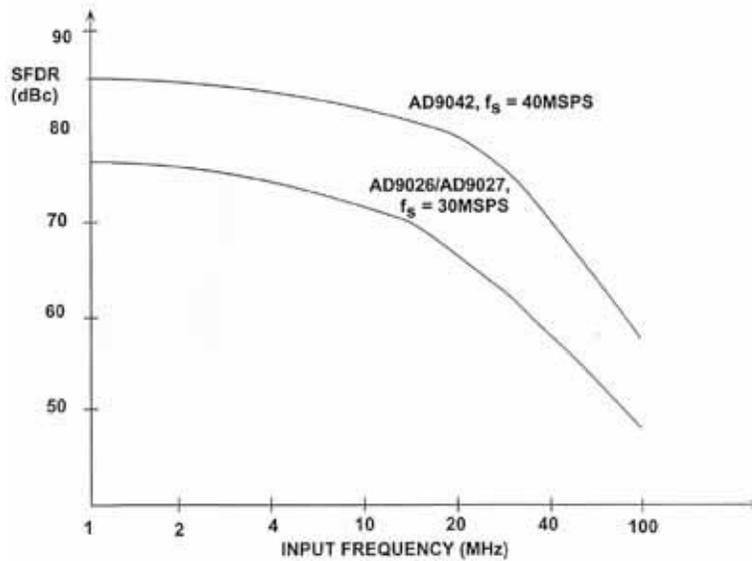


Figure 5.12

The AD9042 is a state-of-the-art 12-bit, 40MSPS two stage subranging ADC consisting of a 6-bit coarse ADC and a 7-bit residue ADC with one bit of overlap to correct for any DNL, INL, gain or offset errors of the coarse ADC, and offset errors in the residue path. A block diagram is shown in Figure 5.13. A proprietary gray-code architecture is used to implement the two internal ADCs. The gain alignments of the coarse and residue, likewise the subtraction DAC, rely on the statistical matching of the process. As a result, 12-bit integral and differential linearity is obtained without laser trim. The internal DAC consists of 126 interdigitated current sources. Also on the DAC reference are an additional 20 interdigitated current sources to set the coarse gain, residue gain, and full scale gain. The interdigitization removes the requirement for laser trim. The AD9042 is fabricated on a high speed dielectrically isolated complementary bipolar process. The total power dissipation is only 575mW when operating on a single +5V supply.

BLOCK DIAGRAM OF AD9042 12-BIT, 40MSPS ADC

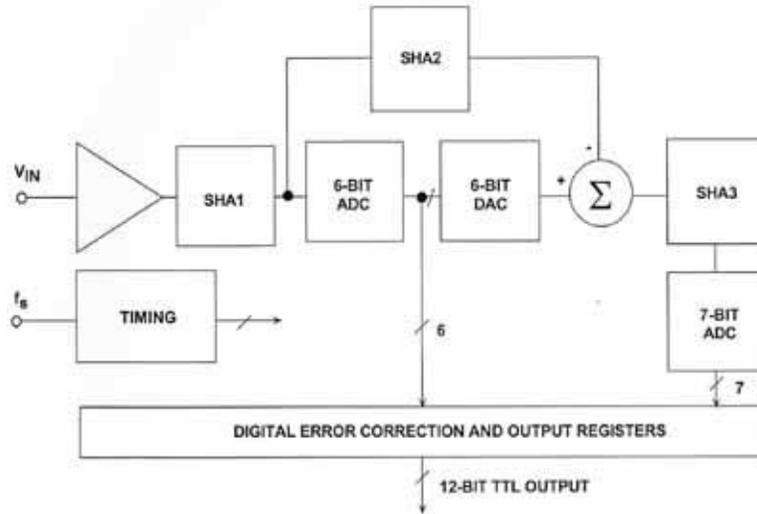


Figure 5.13

AD9042 12-BIT, 40MSPS ADC KEY SPECIFICATIONS

- Input Range: 1V peak-to-peak, $V_{cm} = +2.4V$
- Input Impedance: 250Ω to V_{cm}
- Effective Input Noise: 0.33LSBs rms
- SFDR at 20MHz Input: 80dB
- $S/(N+D)$ at 20MHz Input = 66dB
- Digital Outputs: TTL Compatible
- Power Supply: Single +5V
- Power Dissipation: 575mW
- Fabricated on High Speed Dielectrically Isolated Complementary Bipolar Process

Figure 5.14

The outstanding performance of the AD9042 is partly due to the use of differential techniques throughout the device. The low distortion input amplifier converts the single-ended input signal into a differential one. If maximum SFDR performance is desired, the signal source should be coupled directly into the input of the AD9042 without using a buffer amplifier. Figure 5.15 shows a method using capacitive coupling.

**INPUT STRUCTURE OF AD9042 ADC IS
DESIGNED TO BE DRIVEN DIRECTLY FROM 50Ω
SOURCE FOR BEST SFDR**

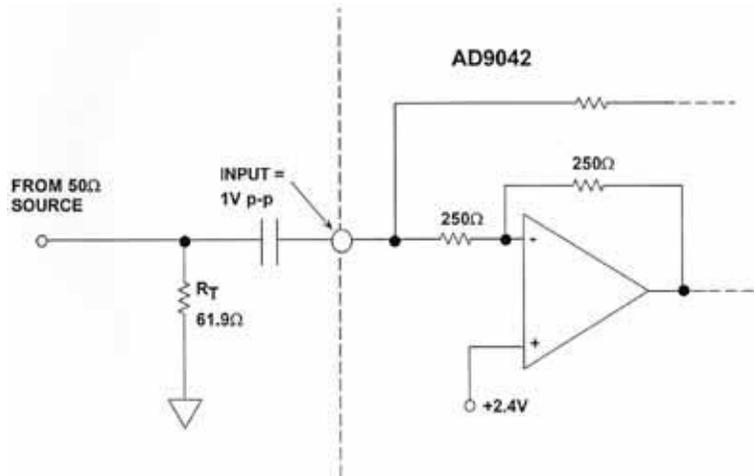


Figure 5.15

INCREASING ADC SFDR AND ENOB USING EXTERNAL SHAS

An external SHA can increase the SFDR and ENOB of a sampling ADC for undersampling applications if properly selected and interfaced to the ADC. The SHA must have low hold-mode distortion at the frequency of interest. In addition, the acquisition time must be short enough to operate at the required sampling frequency. Figure 5.17 shows the effects of adding a SHA to an 8-bit flash converter. The ADC is clocked at 20MSPS, and the input frequency to the ADC is 19.98MHz. The scope photo shows the "beat" frequency of 2kHz reconstructed with an 8-bit DAC. Notice that without the SHA, the ADC has non-linearities and missing codes. The addition of the SHA (properly selected and timed) greatly improves the linearity and reduces the distortion.

THE ADDITION OF AN EXTERNAL WIDEBAND LOW DISTORTION SHA EXTENDS THE LOW FREQUENCY PERFORMANCE OF THE ADC TO HIGHER FREQUENCIES

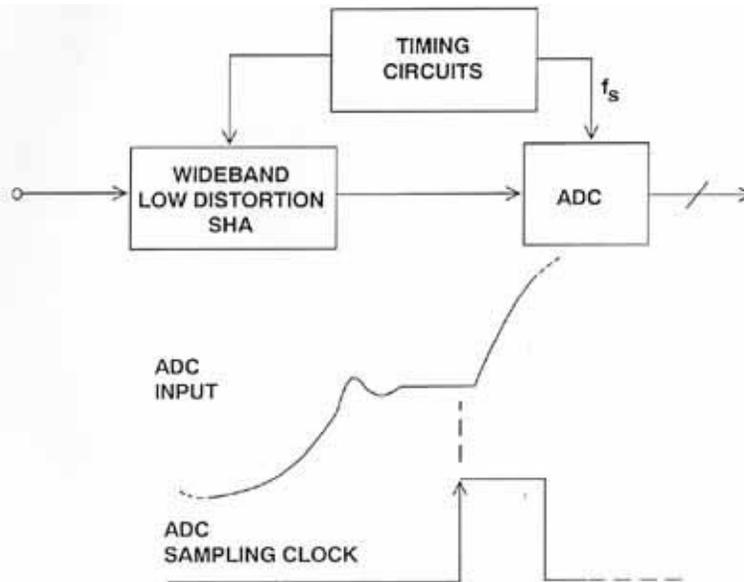


Figure 5.16

EFFECTS OF EXTERNAL SHA ON FLASH ADC PERFORMANCE FOR $f_{in} = 19.98\text{MHz}$, $f_s = 20.00\text{MSPS}$

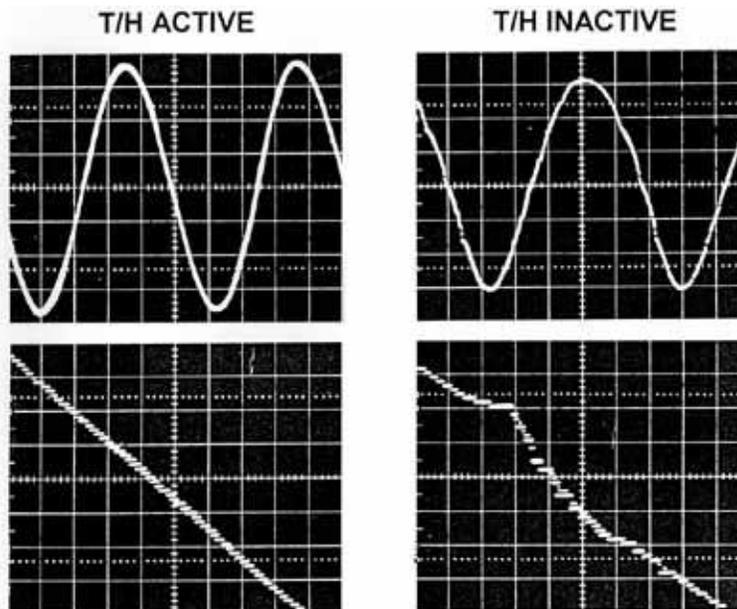


Figure 5.17

Most SHAs are specified for distortion when operating in the track mode. What is of real interest, however, is the signal distortion in the hold mode when the SHA is operating dynamically. The AD9100 (30MSPS) and AD9101(125MSPS) are ultra-fast SHAs and are specified in terms of hold-mode distortion. The measurement is done using a high performance low distortion ADC (such as the AD9014 14-bit, 10MSPS) to digitize the held value of the SHA output. An FFT is performed on the ADC output, and the distortion is measured digitally. For sampling rates greater than 10MSPS, the ADC is clocked at an integer sub-multiple of the SHA sampling frequency. This causes a frequency translation in the FFT output because of undersampling, but the distortion measurement still represents that of the SHA which is operating at the higher sampling rate. The AD9100 is optimized for low distortion up to 30MSPS, while the AD9101 will provide low distortion performance up to a sampling rate of 125MSPS. The low distortion performance of these SHAs is primarily due to the architecture which differs from the classical open-loop SHA architecture shown in Figure 5.18.

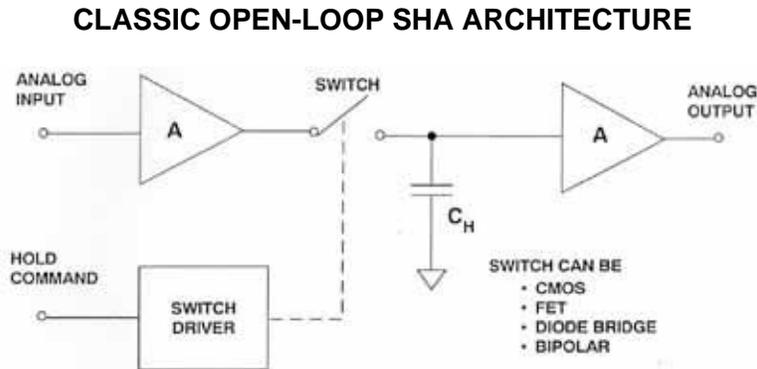


Figure 5.18

The sampling switch in the classic open-loop architecture is not within a feedback loop, and therefore distortion is subject to the non-linearity of the switch. The AD9100/AD9101 architecture shown in Figure 5.19 utilizes switches inside the feedback loop to achieve better than 12-bit AC and DC performance. The devices are fabricated on a high speed complementary bipolar process. In the track mode, S1 applies the buffered input signal to the hold capacitor, C_H , and S2 provides negative feedback to the input buffer. In the hold mode, both switches are disconnected from the hold capacitor, and negative feedback to the input buffer is supplied by S1. This architecture provides extremely low hold-mode distortion by maintaining high loop gains at high frequency. The output buffer can be configured to provide voltage gain (AD9101), which allows the switches to operate on lower common-mode voltage, thereby giving lower overall distortion.

**CLOSED-LOOP SHA ARCHITECTURE
PROVIDES LOW DISTORTION AND HIGH SPEED
(AD9100, AD9101)**

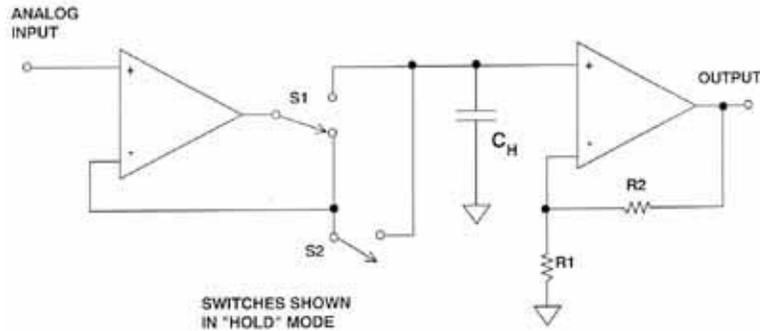


Figure 5.19

The hold-mode SFDR of the AD9100 is a function of the peak-to-peak input signal level and frequency as shown in Figure 5.20. Notice the data was taken as a sampling frequency of 10MSPS for three input amplitudes. The test configuration of Figure 5.21 was used to collect the data. For each input amplitude, the gain of the op amp between the AD9100 and the AD9014 ADC was adjusted such that the signal into the AD9014 was always full scale (2V peak-to-peak). Notice that optimum SFDR was obtained with a 200mV p-p input signal. Timing between the SHA and the ADC is critical. The SHA acquisition time should be long enough to achieve the desired accuracy, but short enough to allow sufficient hold-time for the ADC front-end to settle and yield a low-distortion conversion. For the test configuration shown, the optimum performance was achieved using an acquisition time of 20ns and a hold time of 80ns. The ADC is clocked close to the end of the SHA's hold time. Best performance in this type of application is always achieved by optimizing the timing in the actual circuit.

**AD9100 HOLD-MODE SFDR MEASURED AT
A SAMPLING RATE OF 10MSPS**

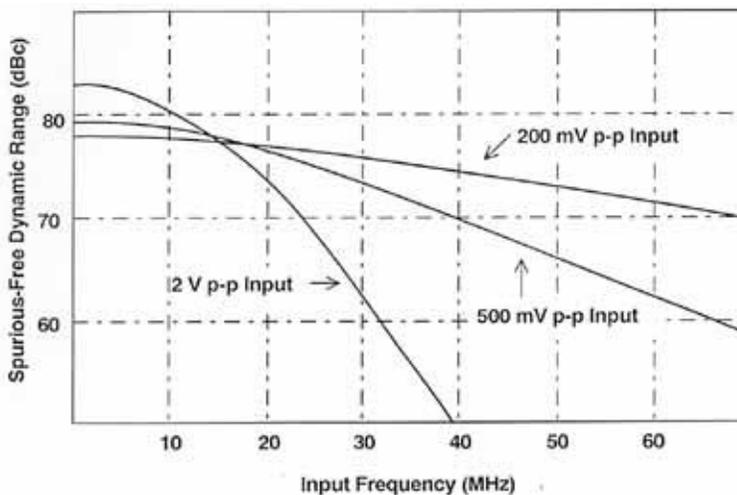


Figure 5.20

**TEST CONFIGURATION AND TIMING FOR
MEASURING AD9100 SFDR AT 10MSPS**

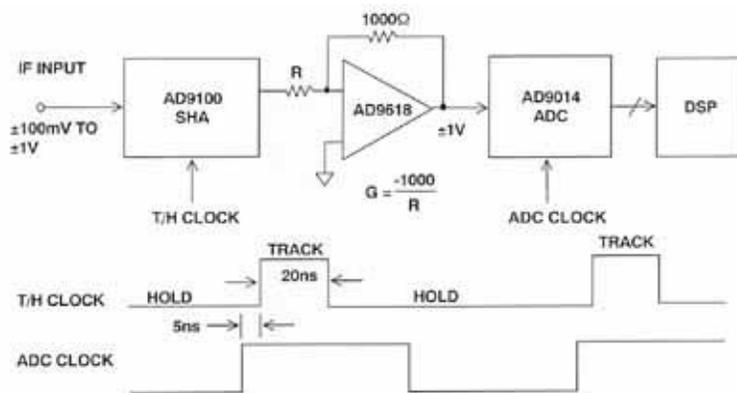


Figure 5.21

Figure 5.22 shows the SFDR of the AD9100 superimposed on the SFDR of the AD9026/AD9027 and the AD9042 ADCs. These data indicate that the AD9100 will significantly improve the SFDR of the AD9026/AD9027 ADC at the higher input frequencies. The performance of the AD9042 indicates that SFDR improvements will only occur at input frequencies above 40MHz.

**SFDR PERFORMANCE OF AD9100 SHA,
AD9026/AD9027 ADC, AND AD9042 ADC**

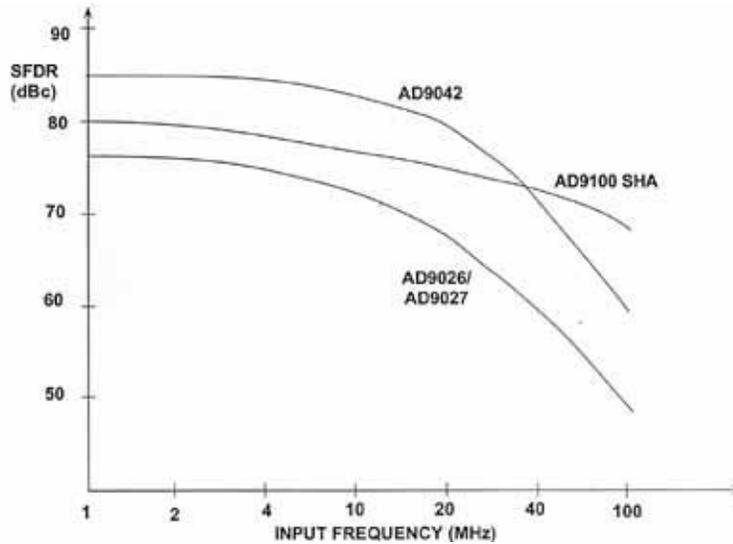


Figure 5.22

The performance of the AD9100 SHA driving the AD9026/AD9027 ADC at a sampling frequency of 10MSPS is shown in Figure 5.23. The input signal is a 200mV peak-to-peak 71.4MHz sinewave. The amplifier between the SHA and the ADC is adjusted for a gain of 10. The SFDR is 72dBc, and the SNR is 62dB.

**FFT OUTPUT FOR AD9100 SHA DRIVING AD9026 ADC:
INPUT = 200mV p-p, G = 10, f_s = 10MSPS, f_{in} = 71.4MHz**

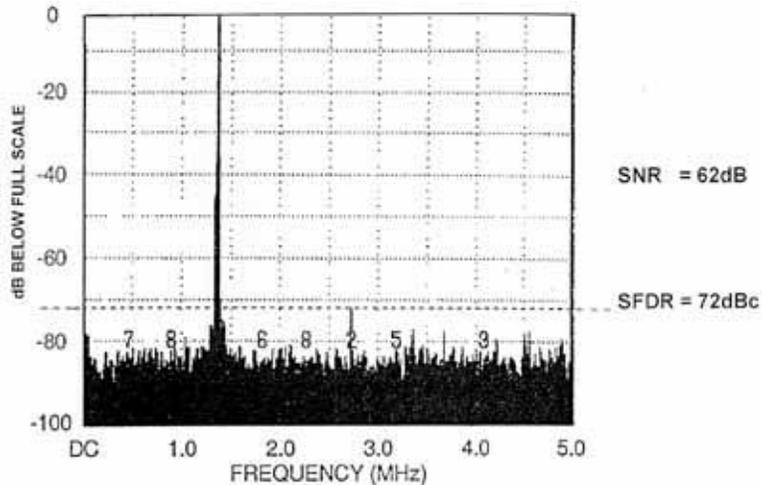


Figure 5.23

Similar dynamic range improvements can be achieved with high speed flash converters at higher sampling rates with the AD9101 SHA. The architecture is

similar to the AD9100, but the output buffer amplifier is optimized for a gain of 4 (see Figure 5.24). This configuration allows the front end sampler to operate at relatively low signal amplitudes, resulting in dramatic improvement in hold-mode distortion at high input frequencies and sampling rates up to 125MSPS. The AD9101 has an input bandwidth of 350MHz and an acquisition time of 7ns to 0.1% and 11ns to 0.01%.

AD9101 125MSPS SHA

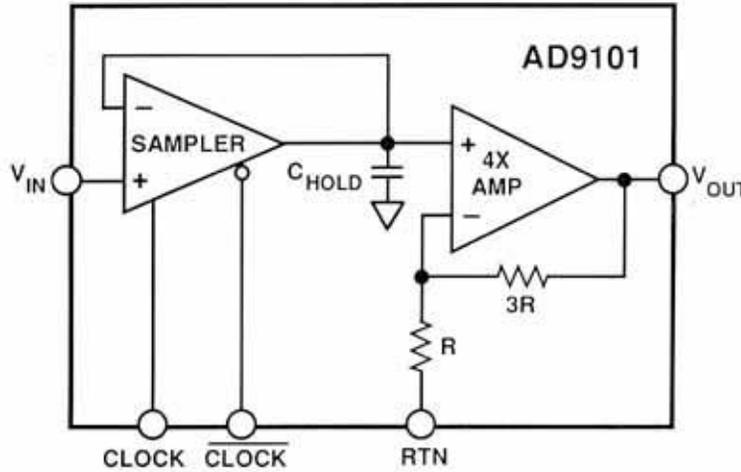


Figure 5.24

A block diagram and a timing diagram is shown for the AD9101 driving the AD9002 8 bit flash converter at 125MSPS (Figure 5.25). The corresponding dynamic range with and without the AD9101 is shown in Figure 5.26.

**AD9101 SHA DRIVING AD9002 8-BIT, 125MSPS
FLASH CONVERTER FOR IMPROVED DYNAMIC RANGE**

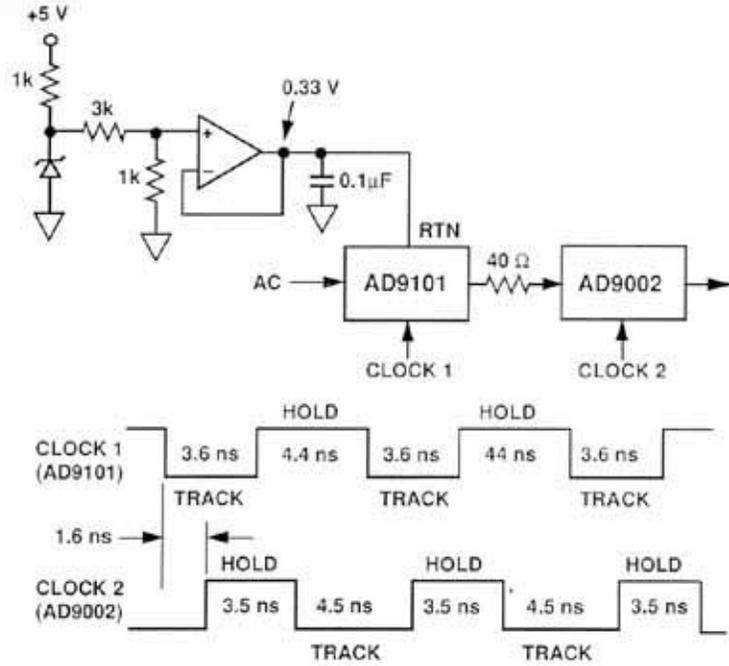


Figure 5.25

**AD9002 DYNAMIC PERFORMANCE
WITH AND WITHOUT AD9101 SHA**

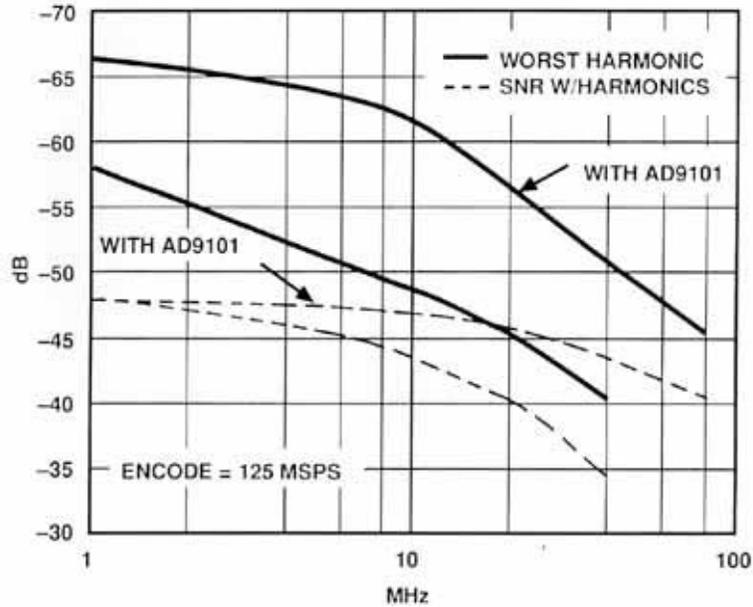


Figure 5.26

USE OF DITHER SIGNALS TO INCREASE ADC DYNAMIC RANGE

In the development of classical ADC quantization noise theory, the assumption is usually made that the quantization error signal is uncorrelated with the ADC input signal. If this is true, then the quantization noise appears as random noise spread uniformly over the Nyquist bandwidth, dc to $f_s/2$, and it has an rms value equal to $q/(\sqrt{12})$. If, however, the input signal is locked to a non-prime integer sub-multiple of f_s , the quantization noise will no longer appear as uniformly distributed random noise, but instead will appear as harmonics of the fundamental input sine wave. This is especially true if the input is an exact even submultiple of f_s . Figure 5.27 illustrates the point using FFT simulation for an ideal 12 bit ADC. The FFT record length was chosen to be 4096. The spectrum on the left shows the FFT output when the input signal is an exact even submultiple ($1/32$) of the sampling frequency (the frequency was chosen so that there were exactly 128 cycles per record). The SFDR is approximately 78dBc. The spectrum on the right shows the output when the input signal is such that there are exactly 127 cycles per record. The SFDR is now about 92dBc which is an improvement of 14dB. Signal-correlated quantization noise is highly undesirable in spectral analysis applications, where it becomes difficult to differentiate between real signals and system-induced spurious components, especially when searching the spectrum for the presence of low-level signals in the presence of large signals.

EFFECTS OF SAMPLING A SIGNAL WHICH IS AN EXACT EVEN SUB-MULTIPLE OF THE ADC SAMPLING FREQUENCY (M = 4096, IDEAL 12-BIT ADC SIMULATION)

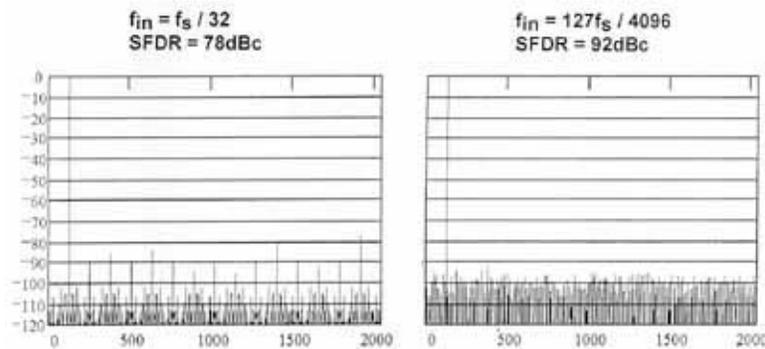


Figure 5.27

There are a number of ways to reduce this effect, but the easiest way is to add a small amount of broadband rms noise to the ADC input signal as shown in Figure 5.28. The rms value of this noise should be equal to about $1/2$ LSB. The effect of this is to randomize the quantization noise and eliminate its possible signal-dependence. In most systems, there is usually enough random noise present on the input signal so that this happens automatically. This is especially likely when using high speed ADCs which have 12 or more bits of resolution and a relatively small input range of 2V p-p or less. The total noise at the ADC is composed of the noise of the input signal, the effective input noise of the ADC, and an additional component caused by

the effects of the sampling clock jitter. In most cases, the rms value of the total ADC input noise is greater than 1/2 LSB.

THE ADDITION OF WIDEBAND GAUSSIAN NOISE TO THE ADC INPUT RANDOMIZES QUANTIZATION NOISE AND REMOVES INPUT SIGNAL DEPENDENCE

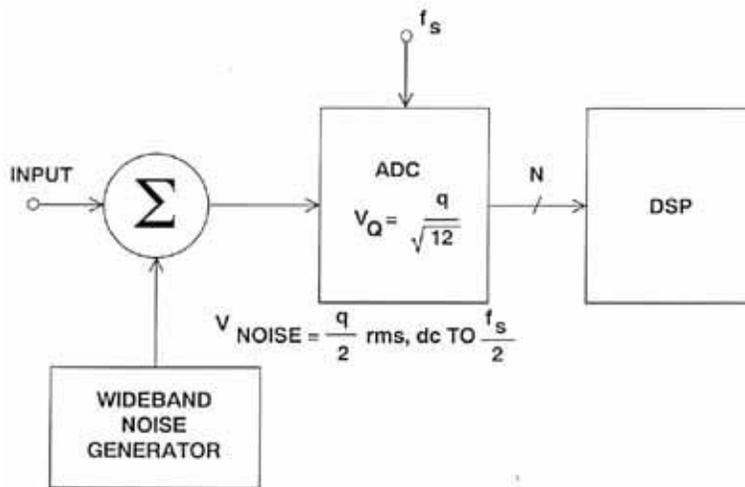


Figure 5.28

EFFECT OF ADC LINEARITY AND RESOLUTION ON SFDR AND NOISE IN DIGITAL SPECTRAL ANALYSIS APPLICATIONS

In order to understand the relationships between ADC resolution, noise, and Spurious Free Dynamic Range (SFDR), it is first necessary to review the some of the issues relating to digital spectral analysis, specifically the FFT. The FFT takes a discrete number of time samples, M, and converts them into M/2 discrete spectral components. The spacing between the spectral lines is $\Delta f = f_s/M$. When a full scale sinewave signal is applied to an ADC having a resolution of N bits, the theoretical rms signal to rms noise ratio is $6.02N + 1.76\text{dB}$. If the quantization noise is uncorrelated with the signal, it appears as gaussian noise spread uniformly over the bandwidth dc to $f_s/2$. The FFT acts as a narrowband filter with a bandwidth of Δf , and the FFT noise floor is therefore $10\log_{10}(M/2)$ dB below the broadband quantization noise level ($6.02N + 1.76\text{dB}$). The FFT noise floor is pushed down by 3dB each time the FFT record length, M, is doubled (see Figure 5.29). This reduction in the noise floor is the same effect achieved by narrowing the bandwidth of an analog spectrum analyzer to a bandwidth of f_s/M .

For example, a 4096 point FFT has a noise floor which is 33dB below the theoretical broadband rms quantization noise floor of 74dB for a 12-bit ADC as shown in Figure 5.30 (where the average noise floor is about $74 + 33 = 107\text{dB}$ below full scale). Notice that there are random peaks and valleys around the average FFT noise floor. These

peaks (due to quantization noise, FFT artifacts, and roundoff error) limit the ideal SFDR to about 92dBc.

RELATIONSHIP BETWEEN AVERAGE NOISE IN FFT BINS AND BROADBAND RMS QUANTIZATION NOISE LEVEL

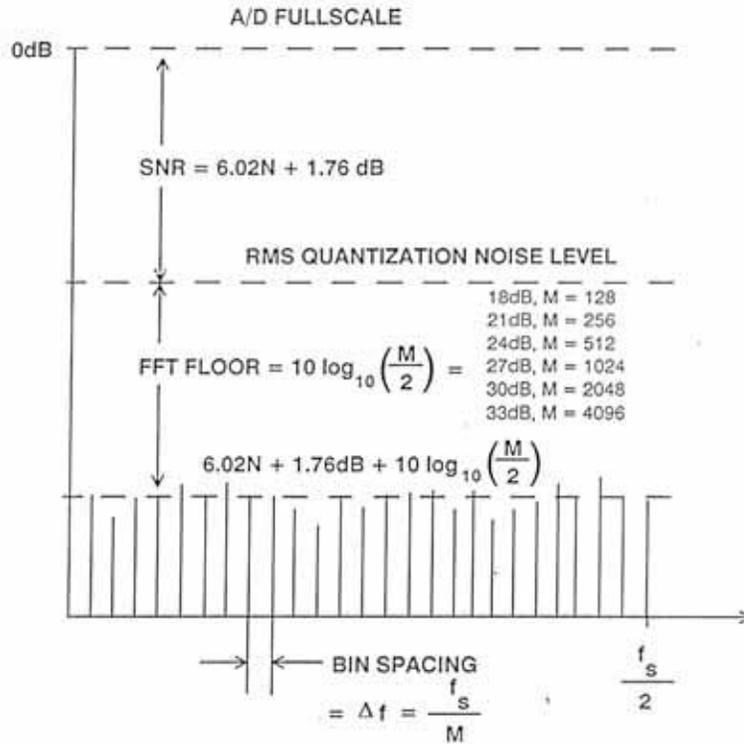


Figure 5.29

NOISE FLOOR FOR AN IDEAL 12-BIT ADC USING 4096-POINT FFT

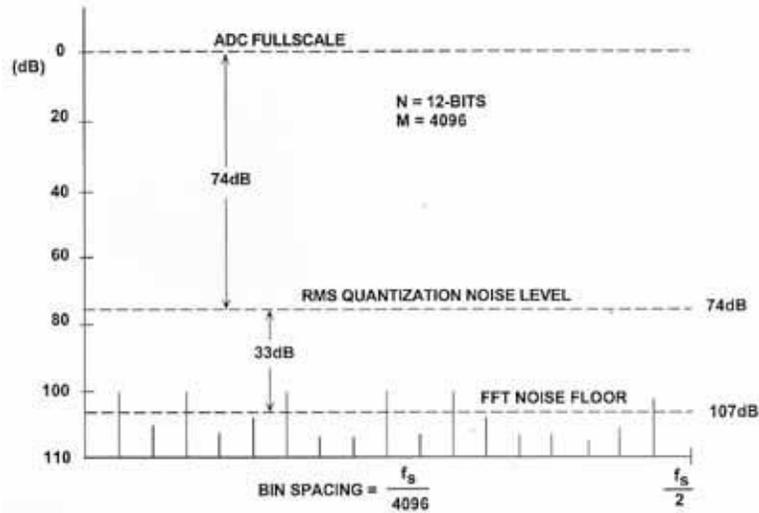


Figure 5.30

Approximately the same dynamic range could be achieved by reducing the resolution of the ADC to 11 bits and using a 16,384 point FFT. There is a tradeoff, however, because lower resolution ADCs tend to have quantization noise which is correlated to the input signal, thereby producing larger frequency spurs. Averaging the results of several FFTs will tend to smooth out the FFT noise floor, but does nothing to reduce the average noise floor.

Using more bits improves the SFDR only if the ADC AC linearity improves with the additional bits. For instance, there would be little advantage in using a 14-bit ADC which has only 12-bit linearity. The extra bits would only serve to slightly reduce the overall noise floor, but the improvement in SFDR would be only marginal.

FUTURE TRENDS IN UNDERSAMPLING ADCS

Future ADCs specifically designed for undersampling applications will incorporate the previously discussed techniques in a single-chip designs. These ADCs will be characterized by their wide SFDR at input frequencies extending well above the Nyquist limit, $f_s/2$. The basic architecture of the digital IF receiver is shown in Figure 5.31. The addition of a low-distortion PGA under DSP control increases the dynamic range of the system. IF frequencies associated with 900MHz digital cellular base stations are typically around 70MHz with bandwidths between 5 and 10MHz. SFDR requirements are between 70 and 80dBc. On the other hand, 1.8GHz digital receivers typically have IF frequencies between 200 and 240MHz with bandwidths of 1MHz. SFDR requirements are typically 50dBc.

**DIRECT IF TO DIGITAL RECEIVER USING PGA
TO INCREASE SYSTEM DYNAMIC RANGE**

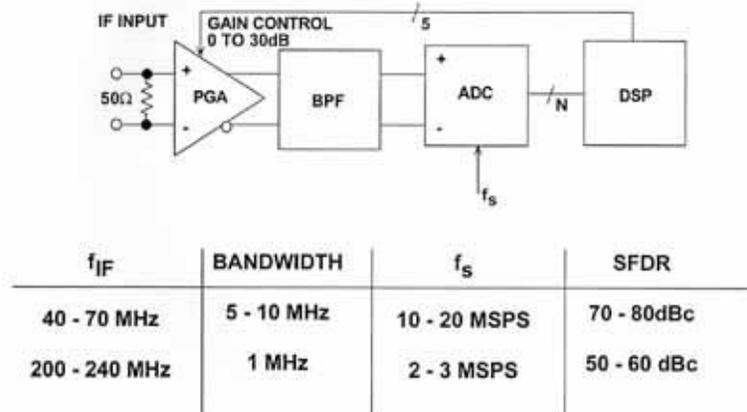


Figure 5.31

The bandpass sigma-delta architecture offers interesting possibilities in this area. Traditional sigma-delta ADCs contain integrators, which are lowpass filters. They have passbands which extend from DC, and the quantization noise is pushed up into the higher frequencies. At present, all commercially available sigma-delta ADCs are of this type (although some which are intended for use in audio or telecommunications contain bandpass filters to eliminate any DC response).

There is no particular reason why the filters of the sigma-delta modulator should be lowpass filters, except that traditionally ADCs have been thought of as being baseband devices, and that integrators are somewhat easier to construct than bandpass filters. If we replace the integrators in a sigma-delta ADC with bandpass filters as shown in Figure 5.32, the quantization noise is moved up and down in frequency to leave a virtually noise-free region in the passband (see Figure 5.33). If the digital filter is then programmed to have its passband in this noise-free region, we have a sigma-delta ADC with a bandpass, rather than a lowpass characteristic.

REPLACING INTEGRATORS WITH BANDPASS FILTERS GIVES A BANDPASS SIGMA-DELTA ADC

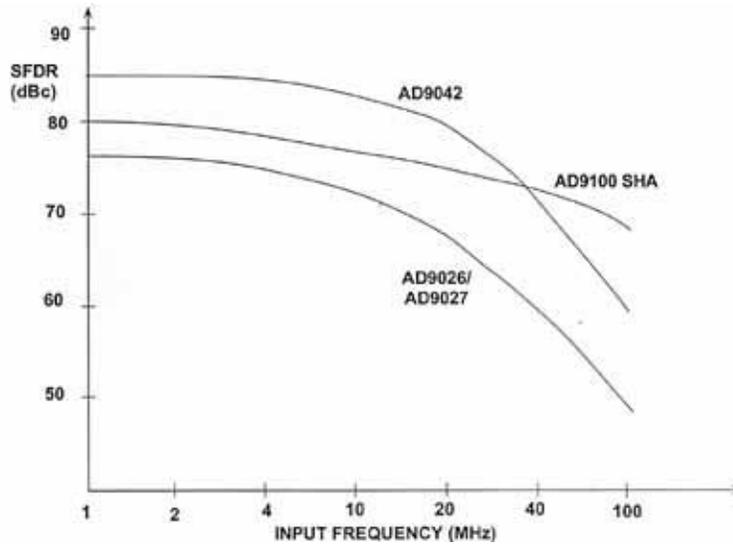


Figure 5.32

NOISE SHAPING FUNCTIONS FOR TRADITIONAL AND BANDPASS SIGMA-DELTA ADCs

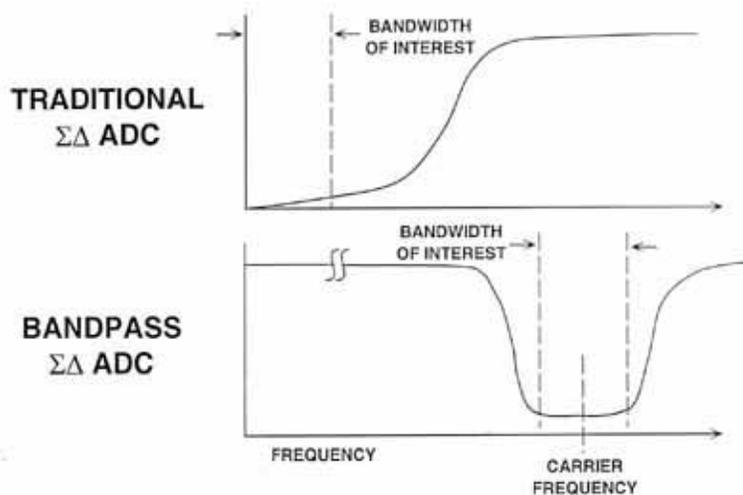


Figure 5.33

The theory is straightforward, but the development of a sigma-delta ADC is expensive, and there is no universal agreement on ideal characteristics for such a bandpass sigma-delta ADC, so developing such a converter from scratch to verify the theory would be unlikely to yield a commercial product. Researchers at Analog Devices and the University of Toronto (See References 16, 17, and 18) have therefore modified a commercial baseband (audio) sigma-delta ADC chip by rewiring its integrators as switched capacitor bandpass filters and reprogramming its digital

filter and decimator. This has provided a fast, and comparatively inexpensive, proof of the concept, but at the expense of relative low Effective Bits (11-bits), the result of less than ideal bandpass filters. Nevertheless the results are extremely encouraging and open the way to the design of purpose-built bandpass sigma-delta ADC chips for specific ASIC applications, especially, but not exclusively, radio receivers.

The overall performance characteristics of the experimental ADC are shown in Figure 5.34. The device was designed to digitize the popular radio IF frequency of 455kHz.

**SUMMARY OF RESULTS FOR EXPERIMENTAL
BANDPASS SIGMA-DELTA ADC**

■ Center Frequency:	455kHz
■ Bandwidth:	10kHz
■ Sampling Rate:	1.852MSPS
■ Oversampling Ratio:	91
■ SNR in Specified Band:	65dB
■ Supply: ±5V,	Power: 750mW
■ Process: 3μm CMOS,	Active Area: 1.8 x 3.4 mm

Figure 5.34

In the future it may be possible to have such bandpass sigma-delta ADCs with user-programmable digital filter coefficients, so that the passband of a receiver could be modified during operation in response to the characteristics of the signal (and the interference!) being received. Such a function is very attractive, but difficult to implement, since it would involve loading, and storing, several hundreds or even thousands of 16-22 bit filter coefficients, and would considerably increase the size, and cost, of the converter.

A feature which could be added comparatively easily to a sigma-delta ADC is a more complex digital filter with separate reference (I) and quadrature (Q) outputs. Such a feature would be most valuable in many types of radio receivers.

Technology exists today which should allow the bandpass sigma-delta architecture to achieve 16-bit resolution, SFDR of 70 to 80dBc, and an effective throughput rate of 10 to 20MSPS (input sampling rate = 100MSPS, corresponding to an oversampling ratio of 5 to 10). This would allow 40MHz IF with a 2MHz bandwidth to be digitized directly.

CHARACTERISTICS OF A BANDPASS SIGMA-DELTA ADC DESIGN FOR IF-SAMPLING

- IF Frequency: 40 to 70MHz
- Signal Bandwidth: 2MHz
- Input Sampling Rate: 100MSPS
- Output Data Rate: 10 to 20MSPS
- Process: BiCMOS

Figure 5.35

EFFECTS OF SAMPLING CLOCK JITTER IN UNDERSAMPLING APPLICATIONS

The effects of sampling clock jitter on Signal-to-Noise Ratio (SNR) and Effective Bit (ENOB) performance discussed in Section 3 are even more dramatic in undersampling applications because of the higher input signal frequencies. Figure 5.36 shows the relationship between sampling clock jitter and SNR previously presented.

Consider the case where the IF frequency is 70MHz, and 12-bit dynamic range is required (70 to 80dB). From Figure 5.36, the rms sampling clock jitter required to maintain this SNR is approximately 1ps rms. This assumes an ideal ADC with no internal aperture jitter. ADC aperture jitter combines with the sampling clock jitter in an rms manner to further degrade the SNR.

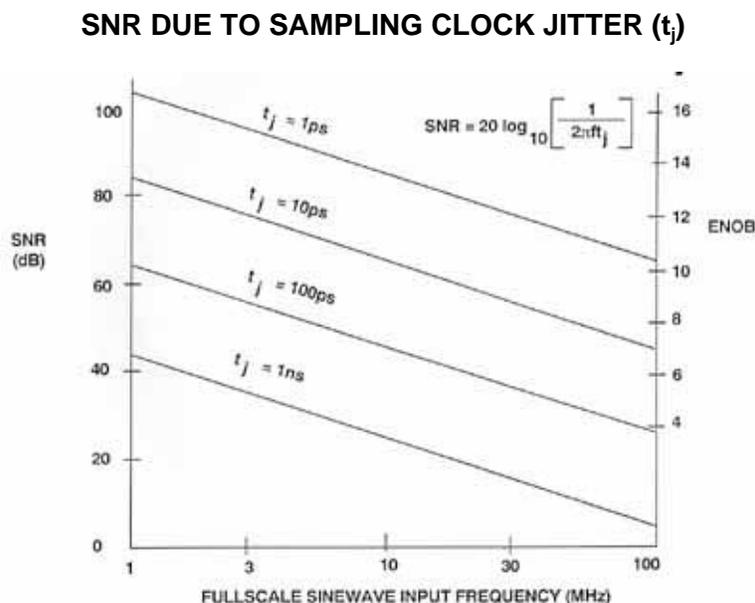


Figure 5.36

The implications of this analysis are extremely important in undersampling applications. The ADC aperture jitter must be minimal, and the sampling clock generated from a low phase-noise quartz crystal oscillator. Furthermore, the oscillator should use discrete bipolar and FET devices in the circuits recommended by the crystal manufacturers. The popular oscillator design which uses a resistor, one or more logic gates, a quartz crystal, and a couple of capacitors should never be used! For very high frequency clocks, a surface acoustic wave (SAW) oscillator is preferable.

SAMPLING CLOCK OSCILLATORS

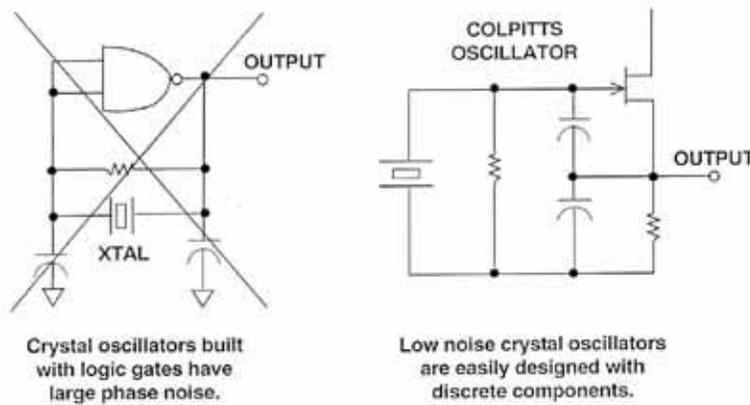


Figure 5.37

The sampling clock should be isolated as much as possible from the noise present in the digital parts of the system. There should be few or no logic gates in the sampling clock path, as a single ECL gate has approximately 4ps rms timing jitter. The sampling clock generation circuitry should be on separate chips, perhaps with separately decoupled power supplies, from the remainder of the digital system, and the sampling clock signal lines should not be located where they can pick up digital noise from the rest of the system. All sampling clock circuitry should be grounded and decoupled to the analog ground plane, as would be the case for a critical analog component.

Of course, the sampling clock is itself a digital signal. It has as much potential for causing noise in the analog part of the system as any other digital signal. We therefore see that a sampling clock is very inconvenient, as it must be isolated from both the analog and digital parts of the system.

Because the sampling clock jitter is wideband and therefore creates wideband random noise, digital filtering can be used to reduce its effects in a system. In the case of an FFT, however, doubling the FFT record length reduces the noise floor by only 3dB.

This discussion illustrates the basic fact that undersampling systems have fundamental limitations with respect to their ability to process wide dynamic range broadband signals, and system tradeoffs between broadband and narrowband approaches must ultimately be made in the design of such systems.

SAMPLING CLOCK NOISE

- Low phase-noise crystal (or SAW) oscillators mandatory in high frequency undersampling applications
- Ground and decouple sampling clock circuitry to the Analog Ground Plane!
- Route sampling clock away from digital and analog signals
- Digital filtering techniques can be used to reduce the effects of sampling clock phase noise
- Sampling clock noise can ultimately dictate the tradeoffs between broadband and narrowband digital receivers

Figure 5.38

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