

## SECTION 8

### SUPPORT CIRCUITRY

- **Voltage References:**  
Types of Voltage References, Voltage Reference Specifications, Low-Noise References for High Resolution Converters
- **Multiplexing Signals with Analog Switches:**  
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**LINEAR DESIGN SEMINAR**

## SECTION 8

### SUPPORT CIRCUITRY

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#### VOLTAGE REFERENCES

(MATERIAL LARGELY EXTRACTED FROM REFERENCES 4 AND 7)

Voltage references have a major impact on the performance and accuracy of analog systems. A  $\pm 5\text{mV}$  tolerance on a 5V reference corresponds to  $\pm 0.1\%$  absolute accuracy—only 10-bits. For a 12-bit system, choosing a reference that has a  $\pm 1\text{mV}$  tolerance may be far more cost effective than performing manual calibration, while both high initial accuracy and calibration will be necessary in a system making absolute 16-bit measurements. (Many systems make *relative* measurements rather than absolute ones, and in such cases the absolute accuracy of the reference is not important, although noise and short-term stability may be.)

Temperature drift or drift due to aging may be an even greater problem than absolute accuracy. The initial error can always be trimmed, but compensating for drift is difficult. Where possible, references should be chosen to have a temperature coefficient and aging characteristics that preserve adequate accuracy over the operating temperature range and expected lifetime of the system.

Noise in voltage references is often overlooked, but it can be very important in system design. It is generally specified on data sheets, but system designers frequently ignore the specification and assume that voltage references do not contribute to system noise.

There are two dynamic issues that must be considered with voltage references: their behavior at start-up and their behavior with transient loads. Voltage references do not power up instantly (this is true of references inside ADCs and DACs as well as discrete designs). Many early designs took tens, or even hundreds, of milliseconds to deliver any output at all, and as long again before reaching full accuracy - modern designs tend to start up more quickly (but read the data sheet), but still need time to reach thermal equilibrium. It is rarely possible to turn on an ADC and reference, whether internal or external, make a reading, and turn off again within a few microseconds, however attractive such a procedure might be in terms of energy saving. (There are also issues, which we shall not consider here, of anomalous ADC logic states on start-up. Irrespective of reference accuracy, the first, and sometimes even the second, result from an ADC after powering up may be in error because of misbehavior arising from the state of its logic immediately after power is applied.)

Many references have low power, and therefore low bandwidth, buffer amplifiers. This makes for poor behavior under fast transient loads, which may degrade the performance of fast ADCs, especially successive approximation and flash ADCs. Suitable decoupling can

ease the problem (but some references oscillate with capacitive loads), or an additional external broadband buffer

amplifier may be used to drive the node where the transients occur.

## **CHOOSING VOLTAGE REFERENCES FOR HIGH RESOLUTION SYSTEMS**

- Tight Tolerance Improves Accuracy, Reduces Costs
- Temperature Drift Affects Accuracy
- Long-Term Stability Assures Repeatability
- Noise Limits System Resolution
- Dynamic Loading Causes Errors

**Figure 8.1**

## **TYPES OF VOLTAGE REFERENCES**

Two simple diode-based references are shown in Figure 8.2. In the first, a current-driven forward biased diode (or diode-connected transistor) produces a voltage,  $V_f$ . While the junction drop is somewhat decoupled from the raw power supply, it has numerous deficiencies as a reference including a  $-0.3\text{%/}^{\circ}\text{C}$  temperature coefficient, sensitivity to loading, and an inflexible output volt-

age (only available in 600mV increments). This simple reference (as well as other shunt-type regulators) does have one basic advantage in that the polarity is easily reversible by flipping connections and reversing the drive current polarity. However, a basic limitation of all shunt regulators is that the load current must always be much less than the driving current  $I_D$ .

## SIMPLE DIODE REFERENCE CIRCUITS

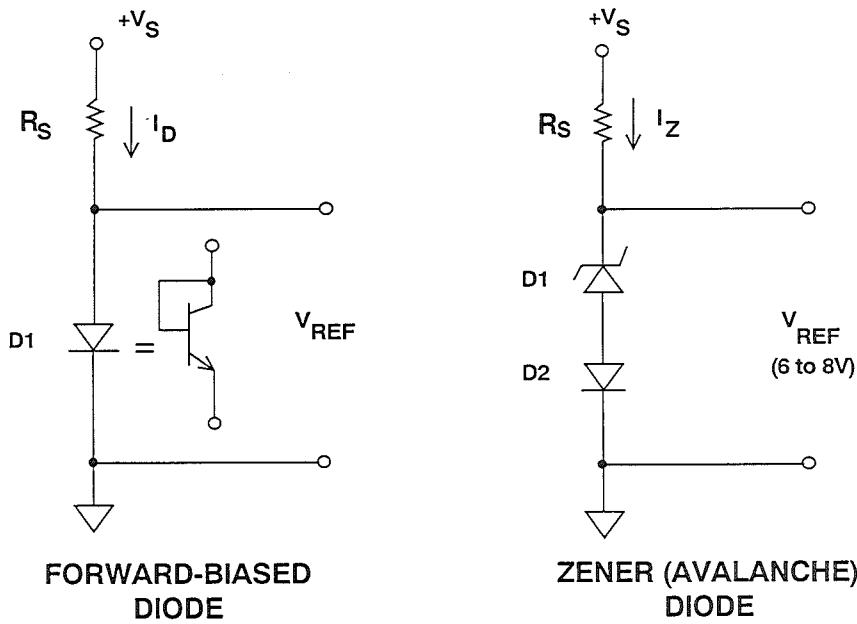


Figure 8.2

In the second circuit of Figure 8.2, a zener or avalanche diode is used, and an appreciably higher output voltage is realized. While true *zener* breakdown occurs below 5V, *avalanche* breakdown occurs at higher voltages and has a positive temperature coefficient. (Diode reverse breakdown is referred to almost universally today as *zener*, even though it is usually avalanche breakdown.) With a D1 breakdown voltage in the 5 to 8V range, the net positive TC is such that it equals the negative TC of a forward-biased diode D2, yielding a net TC of 100ppm/ $^{\circ}\text{C}$  or less with proper bias current. Combinations of such carefully chosen diodes formed the basis of the early single package "temperature-compensated zener" references, such as the 1N821-1N829 series.

The temperature-compensated zener reference is limited in terms of initial

accuracy, as the best TC combinations fall at odd voltages, such as the 1N829's 6.2V. In order to obtain the best TC, the diode current must be carefully controlled, making loading somewhat difficult. Zener references must also be driven from voltage sources higher than 6V levels, precluding their operation in 5V systems. References based on low TC avalanche diodes also tend to be noisy due to the noise of the breakdown mechanism. Monolithic zener references described below provide significant improvements.

The development of low voltage (<5V) references based on the bandgap voltage of silicon led to the introductions of various ICs which could be operated on low voltage supplies with good TC performance. The first was the LM109 (Reference 1), and the basic bandgap reference cell is shown in Figure 8.3.

## BASIC BANDGAP REFERENCE

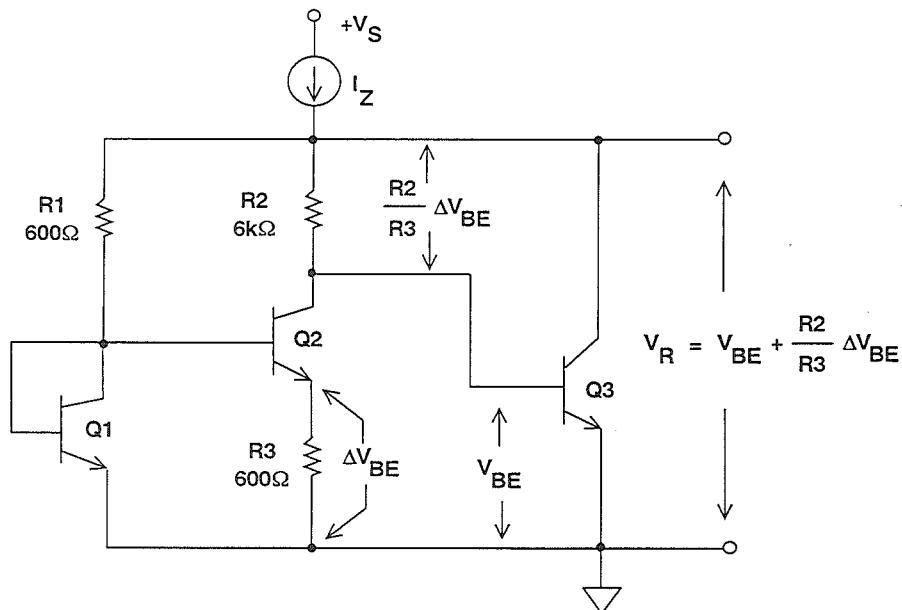


Figure 8.3

This circuit is also called a “ $\Delta V_{BE}$ ” reference because the differing current densities between matched transistors Q1-Q2 produces a  $\Delta V_{BE}$  across R3. It works by summing the  $V_{BE}$  of Q3 with the amplified  $\Delta V_{BE}$  of Q1-Q2, developed across R2. The  $\Delta V_{BE}$  and  $V_{BE}$  components have opposite polarity TCs;  $\Delta V_{BE}$  is proportional-to-absolute-temperature (PTAT), while  $V_{BE}$  is complementary-to-absolute-temperature (CTAT). The summed output is  $V_R$ , and when it is equal to 1.205V (silicon bandgap voltage), the TC is a minimum.

The bandgap reference technique is attractive in IC designs because of its relative simplicity, the avoidance of zeners and their noise, and the fact that

it operates at low voltages. Not only is it used in stand-alone IC references, but it is also used in the design of many other linear ICs such as ADCs, DACs, and op-amps. Buffered forms of 1.2V bandgap references, such as the AD589, remain stable under varying load currents. The AD589 1.235V reference supplies  $50\mu A$  to  $5mA$  with an output impedance of  $0.6\Omega$ , and TCs ranging between 10 and  $100\text{ppm}/^\circ\text{C}$ .

An improved bandgap reference (popularly called the “Brokaw Cell”, see References 2 and 3) shown in Figure 8.4 provides on-chip buffering which allows good drive capability and voltage scaling. The AD580, which uses this circuit, was the first precision bandgap based IC reference.

### AD580 PRECISION BANDGAP REFERENCE USES BROKAW CELL

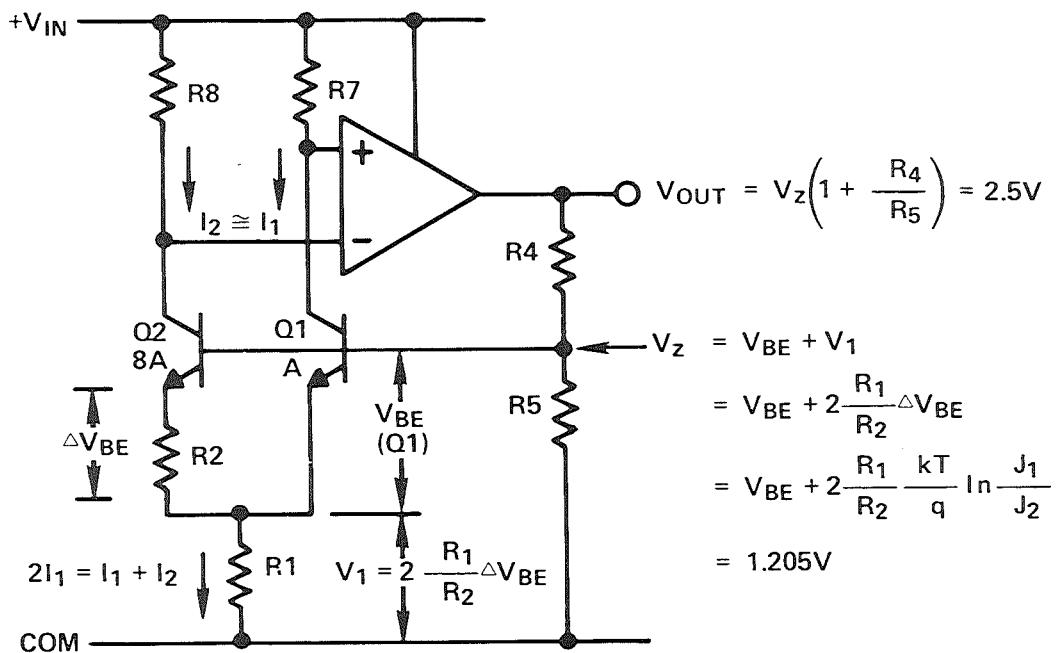


Figure 8.4

The AD580 has two 8:1 emitter-scaled transistors Q1-Q2 operating at identical collector currents (and thus 1/8 current densities), because of equal load resistors and a closed loop around the buffer op-amp. Due to the resultant smaller  $V_{\text{BE}}$  of 8x area Q2, R2 in series with Q2 drops the  $\Delta V_{\text{BE}}$  voltage, while R1 (due to the current relationships) drops a PTAT voltage  $V_1$ , which is:

$$V_1 = 2 \times \frac{R_1}{R_2} \times \Delta V_{\text{BE}}$$

The bandgap cell reference voltage  $V_Z$  appears at the base of Q1, and is the sum of  $V_{\text{BE}}(Q1)$  and  $V_1$ , or 1.205V, the bandgap voltage.

$$V_Z = V_{\text{BE}}(Q1) + V_1$$

$$= V_{\text{BE}}(Q1) + 2 \times \frac{R_1}{R_2} \times \Delta V_{\text{BE}}$$

$$= V_{\text{BE}}(Q1) + 2 \times \frac{R_1}{R_2} \times \frac{kT}{q} \times \ln \frac{J_1}{J_2}$$

$$= V_{\text{BE}}(Q1) + 2 \times \frac{R_1}{R_2} \times \frac{kT}{q} \times \ln 8$$

$$= 1.205V$$

Note that  $J_1$  = current density in Q1,  $J_2$  = current density in Q2, and  $J_1/J_2 = 8$ . However, because of the presence of the  $R_4/R_5$  (laser trimmed) thin film divider

and the op-amp, the actual voltage appearing at  $V_{OUT}$  can be scaled higher, in this case 2.5V. This voltage can be raised to any practical level, and the AD584 reference provides taps for 2.5, 5, 7.5, and 10V operation. The AD580 provides up to 10mA output current while operating from supplies between 4.5 and 30V. It is available in tolerances as low as 10mV, with TCs as low as 10ppm/ $^{\circ}$ C.

Modern IC references come in a variety of styles, but three-terminal, fixed output positive types dominate. They use either bandgap or zeners at the device core, which has an impact on ultimate specifications and performance.

Figure 8.5 shows the standard footprint for an IC positive reference. There are several details which are important. Many references allow optional trimming by connecting an external trim circuit to drive the references' *trim* input pin. Some bandgap references have a PTAT output ( $V_{TEMP}$ ) for Kelvin temperature sensing. All references should use decoupling capacitors on the input, but the amount of decoupling placed on the output depends upon the stability of the reference's output op-amp with capacitive load (more about this important point shortly).

## STANDARD POSITIVE OUTPUT THREE TERMINAL REFERENCE HOOKUP (8-PIN DIP PINOUT)

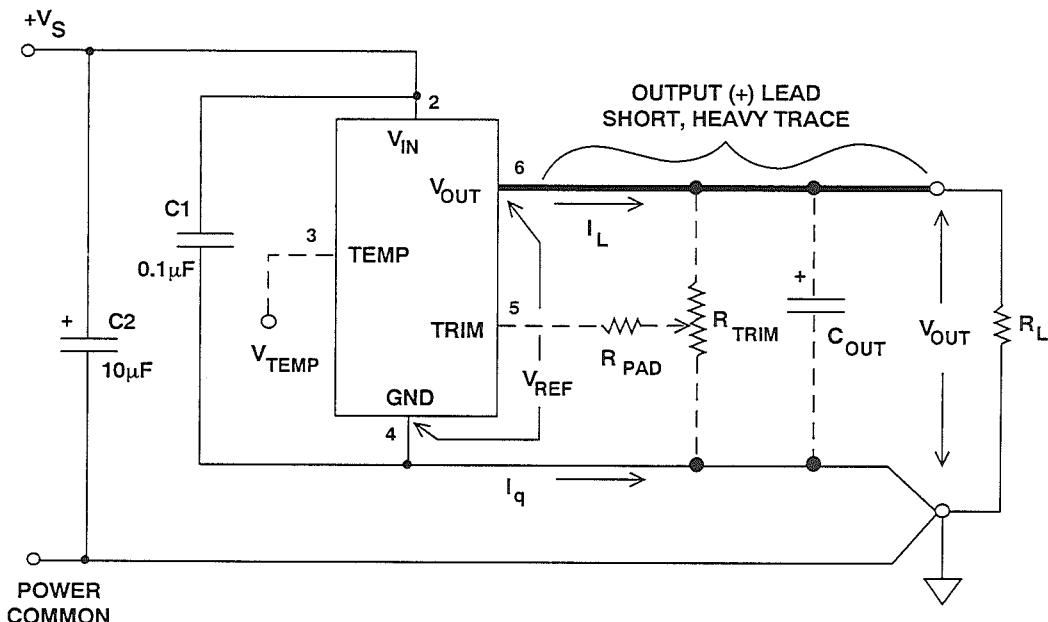


Figure 8.5

There are two basic types of IC references: bandgap and buried zener. Bandgaps have been discussed, but zeners warrant further discussion. The surface of a chip is prone to contamination and lattice dislocations, and zener diodes at the surface are more noisy and less stable than buried ones. All Analog Devices IC references using zeners employ a *buried* (sub-surface) zener technology which improves upon the noise and drift of surface-mode zeners.

Buried zener diodes may be made with a range of voltages, and all have good low noise performance (better than

bandgap references). Ones which have a breakdown voltage just below 7V (in combination with their temperature compensating diodes) have the best temperature performance.

Buried zener references offer the lowest drift, down to the 1-2ppm/°C (AD588 and AD586), and the lowest noise as a percent of fullscale, 100nV/√Hz or less. The best way to compare the noise of references is to compare the ratio of the noise to the output voltage. By this criterion, a 10V reference with 100 $\mu$ V noise is quieter than a 5V reference with 100 $\mu$ V noise.

## ATTRIBUTES OF REFERENCE ARCHITECTURES

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BANDGAP	BURIED ZENER
■ Low Reference Voltage	■ Low Noise
■ Low Quiescent Power	■ Good Long-Term Stability
	■ Lowest Temperature Drift

Figure 8.6

## VOLTAGE REFERENCE SPECIFICATIONS

### TOLERANCE

It is better to select a reference with the required value and accuracy and to avoid external trimming and scaling if possible. This allows the best TCs to be realized, as tight tolerances and low TCs usually go hand-in-hand. Tolerances as low as 0.04% can be achieved with the AD586, AD780, REF-195,

while the AD588 is 0.01%. If trimming must be used, be sure to use the recommended trim network with no more range than is absolutely necessary. If additional external scaling is required, a precision op-amp should be used, along with ratio-accurate, low TC tracking thin film resistors.

### DRIFT

Buried zener references have the best long term drift and TC performance. TCs as low as 1-2ppm/ $^{\circ}$ C are available with the AD586 and AD588. The AD780 bandgap reference is almost as good at 3ppm/ $^{\circ}$ C. The AD588 offers the lowest long term drift of 25ppm/1000 hours. Where a figure is given for long term drift, it is usually drift expressed in ppm/1000 hours. There are 8766 hours in a year, and many engineers multiply the 1000 hour figure by 8.77 to find the annual drift - this is incorrect. Long term drift in precision analog circuits is a "random walk" phenomenon and increases with the *square root* of the elapsed time (this supposes that drift is due to random micro-effects in the chip and not some over-riding cause such as contamination). The 1 year figure will therefore be about  $\sqrt{8.766} \approx 3$

times the 1000 hour figure, and the ten year value will be roughly 9 times the 1000 hour value. In practice, things are a little better even than this, as devices tend to stabilize with age.

The accuracy of an ADC or DAC can be no better than that of its reference. Reference temperature drift affects fullscale accuracy as shown in Figure 8.7. This table shows system resolution and the TC required to maintain 1/2 LSB error over an operating temperature range of 100 $^{\circ}$ C. For example, a TC of about 1ppm/ $^{\circ}$ C is required to maintain 1/2 LSB error at 12-bits. For smaller operating temperature ranges, the drift requirement will be less. The last three columns of the table show the voltage value of 1/2 LSB for popular fullscale ranges.

**REFERENCE TEMPERATURE DRIFT  
REQUIREMENTS FOR VARIOUS SYSTEM ACCURACIES  
(1/2 LSB CRITERIA, 100°C SPAN)**

BITS	REQUIRED DRIFT, (ppm/°C)	1/2 LSB WEIGHT (mV), VARIOUS FULLSCALE RANGES		
		10V	5V	2.5V
8	19.53	19.53	9.77	4.88
9	9.77	9.77	4.88	2.44
10	4.88	4.88	2.44	1.22
11	2.44	2.44	1.22	0.61
12	1.22	1.22	0.61	0.31
13	0.61	0.61	0.31	0.15
14	0.31	0.31	0.15	0.08
15	0.15	0.15	0.08	0.04
16	0.08	0.08	0.04	0.02

Figure 8.7

### SUPPLY RANGE

IC reference supply voltages range from about 3V (or less) above rated output to 30V (or more) above rated output. Exceptions are devices designed for low

dropout, such as the REF-195 and the AD780. At low currents, the REF-195 can deliver 5V with an input as low as 5.1V (100mV dropout).

### LOAD SENSITIVITY

Load sensitivity (or output impedance) is usually specified in  $\mu\text{V}/\text{mA}$  of load current, or  $\text{m}\Omega$ . While figures of  $100\mu\text{V}/\text{mA}$  ( $100\text{m}\Omega$ ) or less are quite good (AD780, REF-43, REF-195), external wiring drops can produce comparable errors at high currents without care in layout. Load current dependent errors are minimized with short, heavy conductors on the (+) output and on the ground return. For the highest precision, buffer amplifiers and Kelvin sensing circuits (AD588 and AD688) are

used to ensure accurate voltages at the load.

The output of a buffered reference is the output of an op amp, and therefore is a function of frequency. Typical reference output impedance rises at 6dB/octave from the DC value, and are nominally about  $10\Omega$  at a few hundred kHz. This impedance can be lowered with an external capacitor, provided the op-amp in the reference remains stable.

## LINE SENSITIVITY

Line sensitivity (or regulation) is usually specified in  $\mu\text{V}/\text{V}$  of input change, and is lower than  $50\mu\text{V}/\text{V}$  ( $-86\text{dB}$ ) in the REF-43, REF-195, AD680, and AD780. For DC and very low frequencies, such errors are easily masked by noise.

As with op-amps, the line sensitivity (or power supply rejection) of references

degrades with increasing frequency, typically 30 to 50dB at a few hundred kHz. For this reason, the reference input should be highly decoupled (LF and HF). Line rejection can also be increased with a pre-regulator, such as the 78Lxx-series.

## VOLTAGE REFERENCE DC SPECIFICATIONS (TYPICAL VALUES AVAILABLE)

■ Tolerance:

AD586, AD780, REF-195:	0.04%
AD588:	0.01%

■ Drift (Temperature Coefficient):

AD586, AD588:	1 - 2 ppm/ $^{\circ}\text{C}$
AD780:	3 ppm/ $^{\circ}\text{C}$

■ Drift (Long Term):

25ppm/1000 hours

■ Supply Range: 3V to 30V above rated voltage output  
REF-195 Low Dropout (100mV)

■ Load Sensitivity:  $100\mu\text{V}/\text{mA}$  ( $100\text{m}\Omega$ )

■ Line Sensitivity:  $50\mu\text{V}/\text{V}$  ( $-86\text{dB}$ )

Figure 8.8

## NOISE

Reference noise is not always specified, and when it is, there is not total uniformity on how. For example, some devices are characterized for peak-to-peak noise in a 0.1 to 10Hz bandwidth, while others are specified in terms of wideband rms or peak-to-peak noise over a specified bandwidth. The most useful way to specify noise (as with op-amps) is a plot of noise voltage spectral density (nV/ $\sqrt{\text{Hz}}$ ) versus frequency.

Low noise references are important in high resolution systems to prevent loss of accuracy. Since white noise is statistical, a given noise density must be related to an equivalent peak-to-peak noise in the relevant bandwidth. Strictly speaking, the peak-to-peak noise in a gaussian system is infinite (but its probability is infinitesimal). Conventionally, the figure of  $6.6 \times \text{rms}$  is used to define a practical peak value - statistically, this occurs less than 0.1% of the time. This peak-to-peak value should be less than 1/2LSB in order to maintain required accuracy. If peak-to-

peak noise is assumed to be 6 times the rms value, then for an  $N$ -bit system, reference voltage fullscale  $V_{\text{REF}}$ , reference noise bandwidth (BW), the required noise voltage spectral density  $E_n$  (V/ $\sqrt{\text{Hz}}$ ) is given by:

$$E_n \leq \frac{V_{\text{REF}}}{12 \cdot 2^N \cdot \sqrt{\text{BW}}}$$

For a 10V, 12-bit, 100kHz system, the noise requirement is a modest 643nV/ $\sqrt{\text{Hz}}$ . Figure 8.9 shows that increasing resolution and/or lower fullscale references make noise requirements more stringent. The 100kHz bandwidth assumption is somewhat arbitrary, but the user may reduce it with external filtering, thereby reducing the noise. Most good IC reference have noise spectral densities around 100nV/ $\sqrt{\text{Hz}}$ , so additional filtering is obviously required in most high resolution systems, especially those with low values of  $V_{\text{REF}}$ .

## REFERENCE NOISE REQUIREMENTS FOR VARIOUS SYSTEM ACCURACIES (1/2 LSB / 100kHz CRITERIA)

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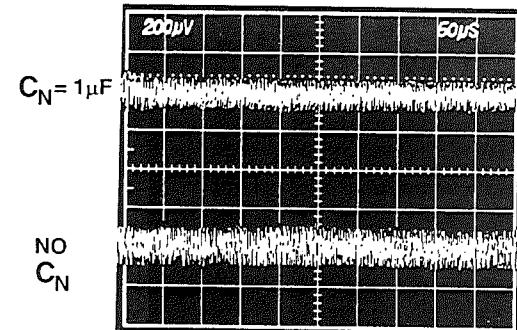
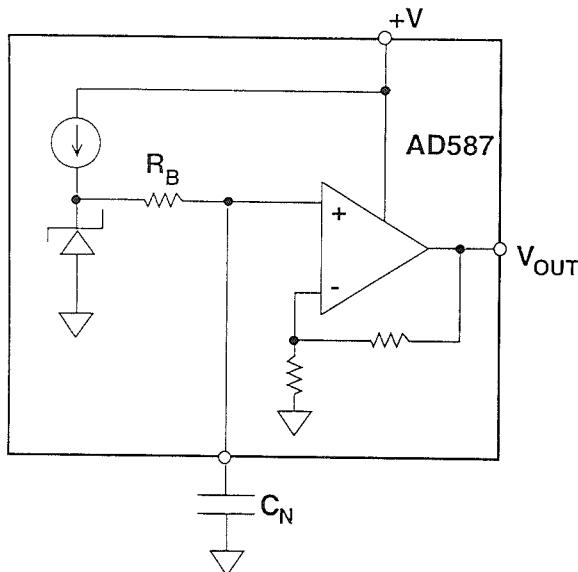
BITS	NOISE DENSITY (nV/ $\sqrt{\text{Hz}}$ )		
	VARIOUS FULLSCALE RANGES		
	10V	5V	2.5V
12	643	322	161
13	322	161	80
14	161	80	40
15	80	40	20
16	40	20	10

Figure 8.9

Some references like the AD587 (see Figure 8.10) have a pin designated as the *noise reduction pin*. The capacitor  $C_N$  forms a low pass filter with the internal resistor  $R_B$  that limits the noise bandwidth at the *output* of the zener diode. A  $1\mu F$  capacitor gives a 3dB bandwidth of 40Hz. The photo shows noise measured in a 1MHz

bandwidth with and without the external filter capacitor, indicating that the filtering provides little value. Although  $C_N$  reduces the zener reference noise, it does not affect the wideband noise generated by the output buffer op-amp. This noise can only be reduced with external filtering.

### REFERENCE NOISE REDUCTION USING THE NOISE REDUCTION PIN



VERTICAL SCALE:  $200\mu V/div.$   
HORIZONTAL SCALE:  $50\mu s/div.$

Figure 8.10

The reference circuit in Figure 8.11 (Reference 4) uses external filtering and a precision low-noise op-amp to provide both low noise and dc accuracy. Reference U1 is a 2.5, 3.0, 5, or 10V reference with a low noise buffered output. The output of U1 is applied to the  $R1-C1/C2$  noise filter to produce a corner frequency of about 1.7Hz. Electrolytic

capacitors usually imply dc leakage errors, but bootstrapping C1 causes its bias voltage to be only the small drop across R2. This lowers the leakage current through R1 to acceptable levels. Since attenuation is modest below 10Hz, the reference noise still affects overall performance at low frequencies.

**COMBINING LOW-NOISE AMPLIFIER WITH EXTENSIVE  
FILTERING YIELDS EXCEPTIONAL NOISE PERFORMANCE  
(1.5 TO 5nV/ $\sqrt{\text{Hz}}$  @ 1kHz)**

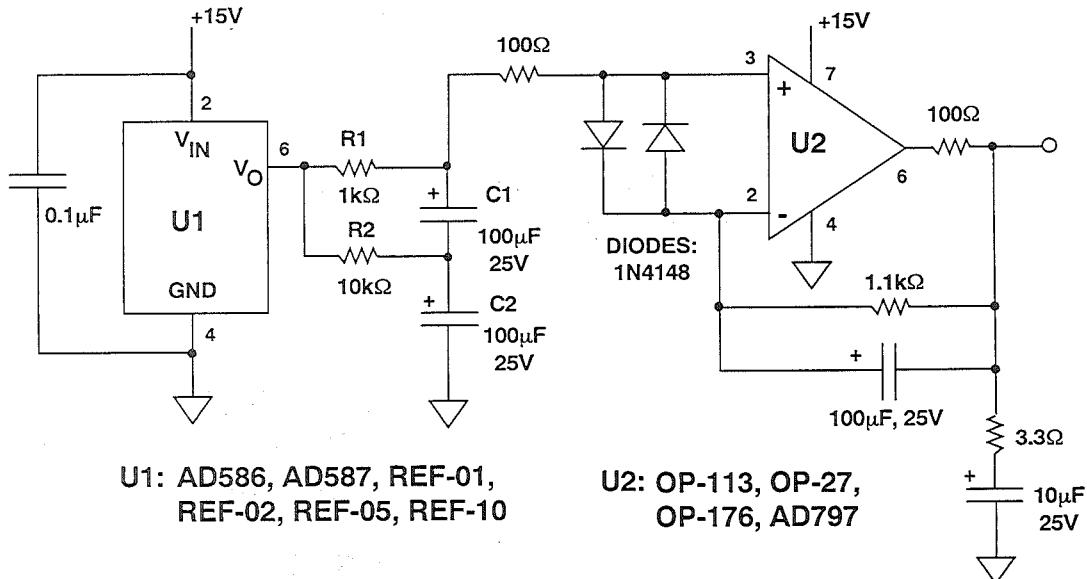


Figure 8.11

The output of the filter is then buffered by a precision low noise unity-gain follower, such as the OP-113EP. With less than  $\pm 150\mu\text{V}$  of offset error and under  $1\mu\text{V}/^\circ\text{C}$  drift, buffer dc performance will not affect the accuracy/drift of most references. The OP-113 has a typical current limit of 40mA, providing output currents higher than a typical IC reference.

While the single-supply OP-113 is useful over the entire 2.5 to 10V range, even lower noise op-amps are available for 5-10V use. The AD797 offers 1kHz noise performance less than 2nV/ $\sqrt{\text{Hz}}$ , compared to about 5nV/ $\sqrt{\text{Hz}}$  for the OP-113. Other op-amps suitable for the 5 to 10V range include the OP-27 and OP-176.

## REFERENCE PULSE CURRENT RESPONSE

The response of references to dynamic loads is often a concern, especially in applications such as driving ADCs and DACs. Fast changes in load current invariably perturb the output, often outside the rated error band. For example, the reference input to a sigma-

delta ADC may be the switched capacitor circuit shown in Figure 8.12. The dynamic load causes current spikes in the reference as the capacitor is charged and discharged. As a result, noise may be induced on the ADC reference circuitry.

**SWITCHED CAPACITOR INPUT OF SIGMA-DELTA ADC PRESENTS A DYNAMIC LOAD TO THE VOLTAGE REFERENCE**

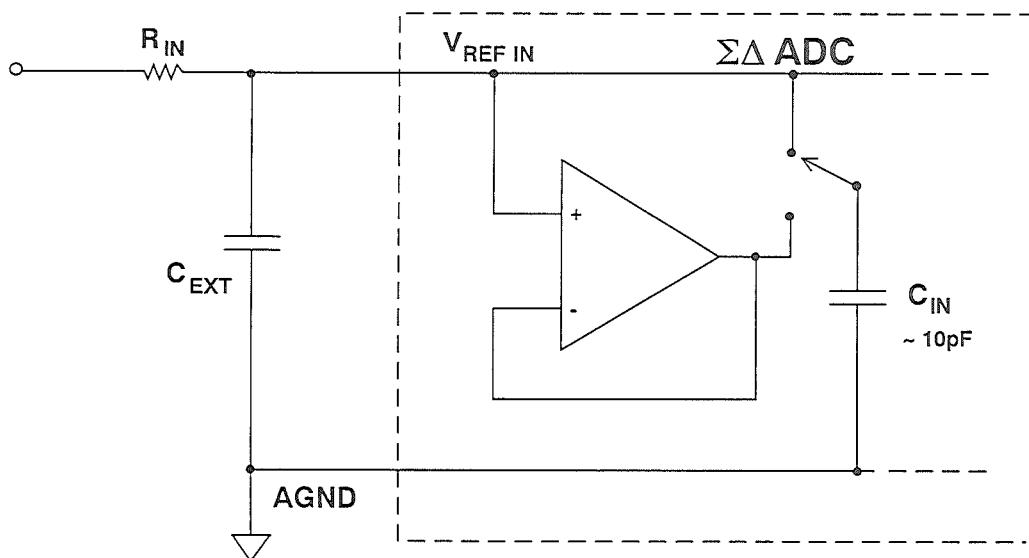
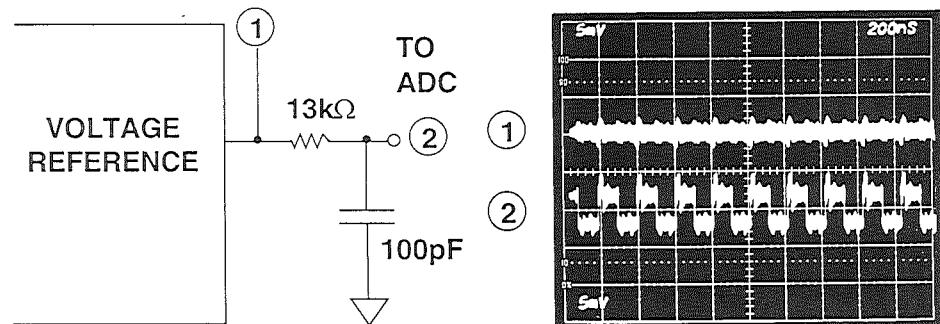


Figure 8.12

Although sigma-delta ADCs have an internal digital filter, transients on the reference input can still cause appreciable conversion errors. An example of sampling noise on a sigma-delta ADC reference is shown in Figure 8.13. The bottom trace shows the noise that is generated if the reference source impedance is too high. The dynamic load causes the reference input to shift by more than 5mV.

A bypass capacitor on the output of a reference may help it to cope with load transients, but many references are unstable with large capacitive loads, and it is important to verify that the one chosen will drive the capacitance required. (The input to references should always be decoupled - with  $0.1\mu\text{F}$  in all cases, and with an additional  $5-50\mu\text{F}$  if there is any LF ripple on its supply.)

**TYPICAL NOISE INDUCED AT THE  
REFERENCE INPUT OF A SIGMA-DELTA ADC**



VERTICAL SCALE: 5mV/div.  
HORIZONTAL SCALE: 200ns/div.

Figure 8.13

**BYPASSING REFERENCE OUTPUT WITH LARGE  
CAPACITOR HELPS MINIMIZE TRANSIENT LOADS  
PROVIDED THE REFERENCE REMAINS STABLE**

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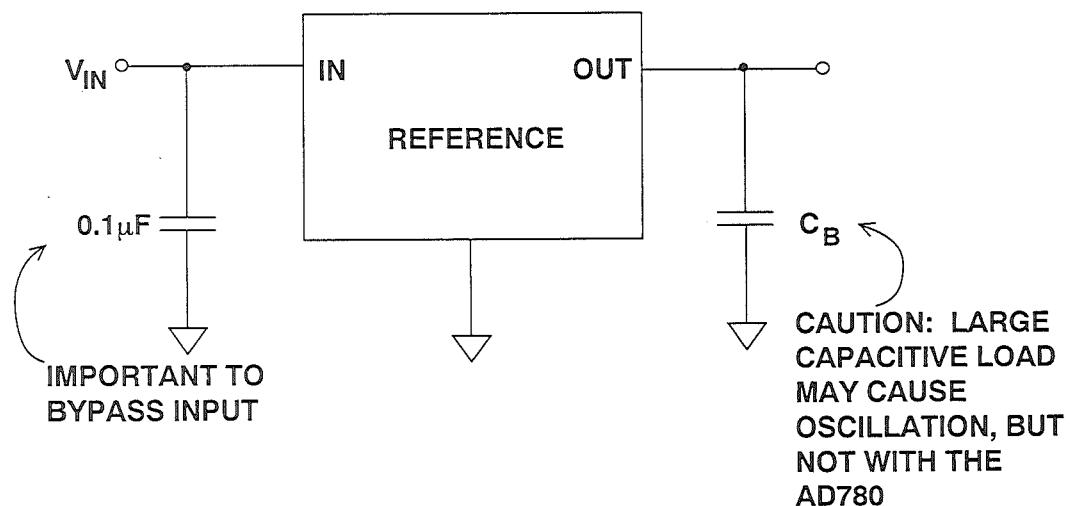


Figure 8.14

Since references do misbehave with transient loads, either by oscillating or by losing accuracy for comparatively long periods, it is advisable to test the pulse response of voltage references which may encounter transient loads. A suitable circuit is shown in Figure 8.15.

In a typical voltage reference, a step change of 1mA produces the transients shown. Both the duration of the transient, and the amplitude of the ringing *increase* when a  $0.01\mu\text{F}$  capacitor is connected to the reference output.

### MAKE SURE REFERENCE IS STABLE WITH LARGE CAPACITIVE LOADS

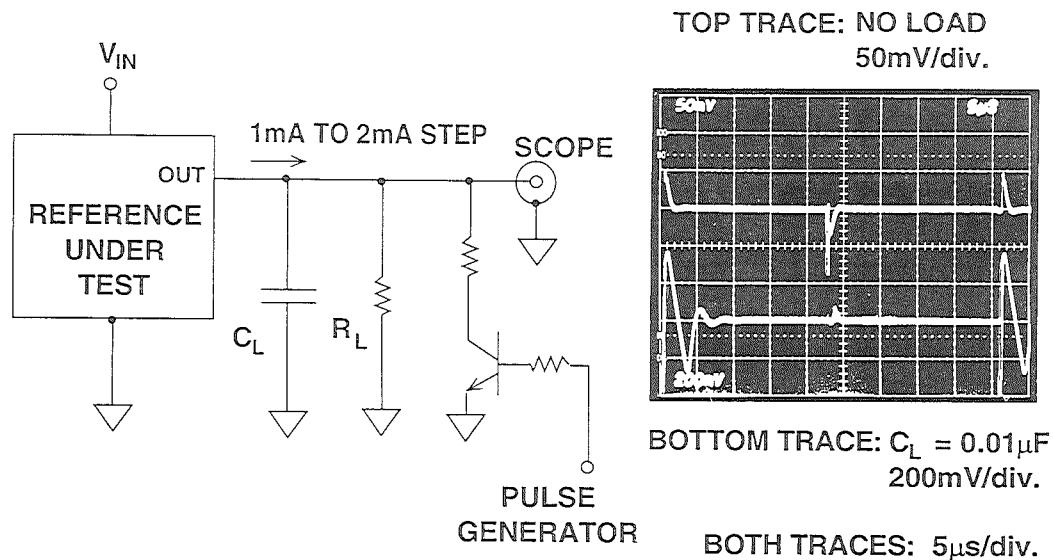


Figure 8.15

Where possible, a reference should be designed to drive large capacitive loads. The AD780 is designed to drive unlimited capacitance without oscillation. It has excellent drift and an accurate output in addition to low power consumption.

Large reference bypass capacitors are useful when driving the reference inputs of successive-approximation

ADCs. Figure 8.16 illustrates reference voltage settling behavior immediately following a "Conversion Start" command. A small capacitor ( $0.01\mu\text{F}$ ) does not provide sufficient charge storage to keep the reference voltage stable during conversion, and errors may result. Decoupling with a  $>1\mu\text{F}$  capacitor maintains the reference stability during conversion.

## SUCCESSIVE APPROXIMATION ADCs CAN PRESENT A DYNAMIC TRANSIENT LOAD TO THE REFERENCE

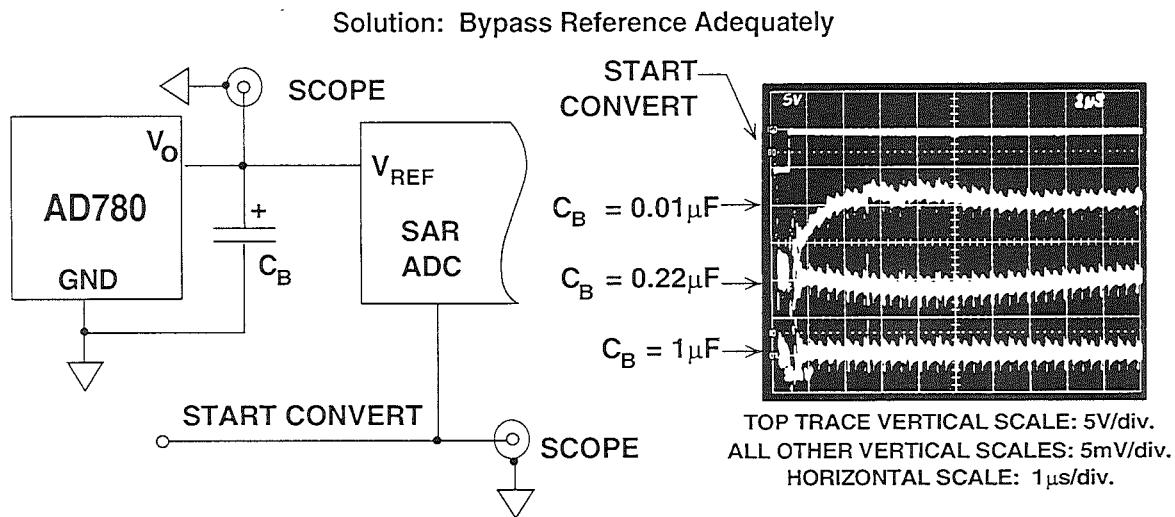


Figure 8.16

Where voltage references drive large capacitances, it is important to realize that their turn-on time will be prolonged. Experiment may be needed to determine the delay before the output of

the reference reaches full accuracy, but it will certainly be much longer than the time specified on the data sheet for the unloaded reference.

## LOW NOISE REFERENCES FOR HIGH RESOLUTION CONVERTERS

High resolution converters (both sigma-delta and high speed ones) can benefit from recent improvements in IC references, such as lower noise and the ability to drive capacitive loads. Even though many data converters have internal references, the performance of these references is often compromised because of the limitations of the converter process. Using an external reference rather than the internal one often yields better overall performance. For example, the AD7710-series of 22-bit ADCs has a 2.5V internal reference with a 0.1 to 10Hz noise of  $8.3\mu\text{V}$  rms (2600nV/Hz), while the AD780 refer-

ence only  $0.67\mu\text{V}$  rms (200nV/Hz). The internal noise of the AD7710-series in this bandwidth is about  $1.7\mu\text{V}$  rms. The use of the AD780 increases the effective resolution of the AD7710 from about 20.5-bits to 21.5 bits.

Figure 8.17 shows the AD780 used as the reference for the AD7710-series ADCs. The 3V scaling enhances the dynamic range of the ADC, while lowering overall system noise as described above. In addition, the AD780 allows a large decoupling capacitor on its output thereby minimizing conversion errors due to transients.

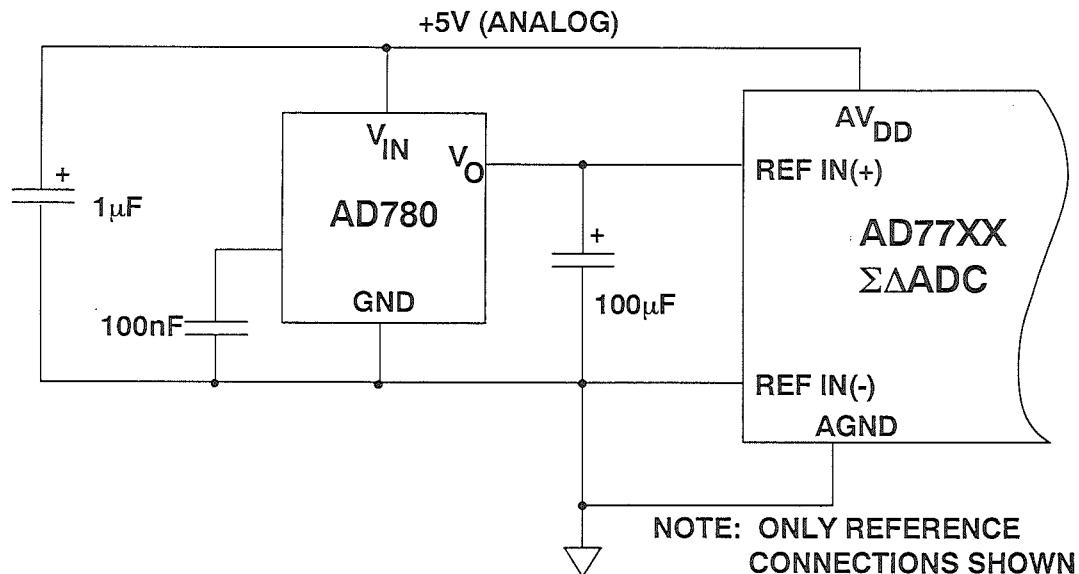
THE AD780 IS IDEAL FOR DRIVING  
PRECISION SIGMA-DELTA ADCs

Figure 8.17

There is one possible problem when replacing the internal reference of a converter with a high precision external one. The converter may have been trimmed, during manufacture, to deliver its specified performance with an inaccurate internal reference. In this case, using an accurate reference may introduce additional gain error. For example, the early AD574 had a guar-

anteed uncalibrated gain accuracy of 0.125% when using an internal 10V reference which itself had a specified accuracy of only  $\pm 1\%$ . It is obvious that if such a device, having an internal reference which is at one end of the specified range, is used with an external reference of exactly 10V, then its gain will be about 1% in error.

# MULTIPLEXING SIGNALS WITH ANALOG SWITCHES

## *Jerry Whitmore, James Bryant*

Analog signals can be switched, multiplexed, and easily connected using analog switches. With sufficient care, there will be little or no degradation of signal quality. This section is devoted to CMOS technology in analog switch

circuitry, their parasitic latchup mechanisms, and effective protection methods. It also discusses AC switch characteristics and how they affect the performance of a system, and some application circuits.

### MULTIPLEXING CONCEPTS

- Advantages of CMOS Technology in Analog Switch Circuitry
- Parasitic Transistors/Latchup and Protection Methods
- Switch Equivalent Circuit dc and ac Analysis
- Applying the Analog Switch

Figure 8.18

The ideal analog switch has no ON-resistance, infinite OFF impedance and zero time delay, and can handle large signal and common-mode voltages. Real

CMOS analog switches meet none of these criteria, but if we understand the limitations of analog switches, most of these limitations can be overcome.

## CHARACTERISTICS OF THE IDEAL ANALOG SWITCH

- On Resistance: Zero
- Off Impedance: Infinite at All Frequencies
- Switching Time: Zero
- Switch Leakage: Zero
- Power Dissipation: Zero
- MTBF: Infinite

Figure 8.19

CMOS switches have an excellent combination of attributes. In its most basic form, the MOSFET transistor is a voltage-controlled resistor. In the ON state, its resistance can be less than  $100\Omega$ , while in the OFF-state, the resistance increases to several hundreds of megohms, with nanoamp leakage currents.

CMOS technology is compatible with logic circuitry and can be densely packed in an IC. Its fast switching characteristics are well controlled with minimum circuit parasitics.

MOSFET transistors are bilateral. That is, they can switch positive and negative voltages and conduct positive and negative currents with equal ease.

A MOSFET transistor has a voltage controlled resistance which varies nonlinearly with signal voltage as shown in Figure 8.21. Figure 8.22 shows a basic CMOS switch using complementary P-channel and N-channel MOS devices connected in parallel. This reduces the ON-resistance and also produces a resistance which varies less with signal voltage.

## ADVANTAGES OF MIXED SIGNAL CMOS TECHNOLOGY

- A Great Logic Technology
  - ◆ High Density
  - ◆ Moderate to High Speed
  - ◆ Low Power Dissipation
  
- An Excellent Switch Technology
  - ◆ MOSFETs are Voltage Controlled Resistors
  - ◆ MOSFETs Lose No Current to the Control Input (Gate)
  - ◆ MOSFETs are Electrically Bilateral -- Can Switch Positive or Negative Voltages or Steer Positive or Negative Current with Equal Ease
  - ◆ No Offset Voltage in Series With ON MOSFET (Unlike Bipolar Transistor)

Figure 8.20

### MOSFET SWITCH ON-RESISTANCE VERSUS SIGNAL VOLTAGE

8

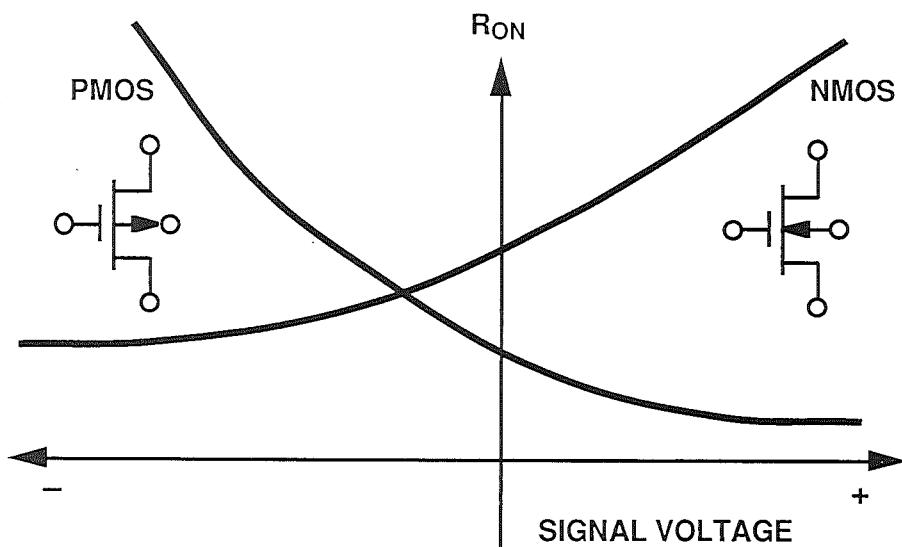


Figure 8.21

## BASIC CMOS SWITCH USES COMPLEMENTARY PAIR TO MINIMIZE $R_{on}$ VARIATION DUE TO INPUT SIGNAL SWING

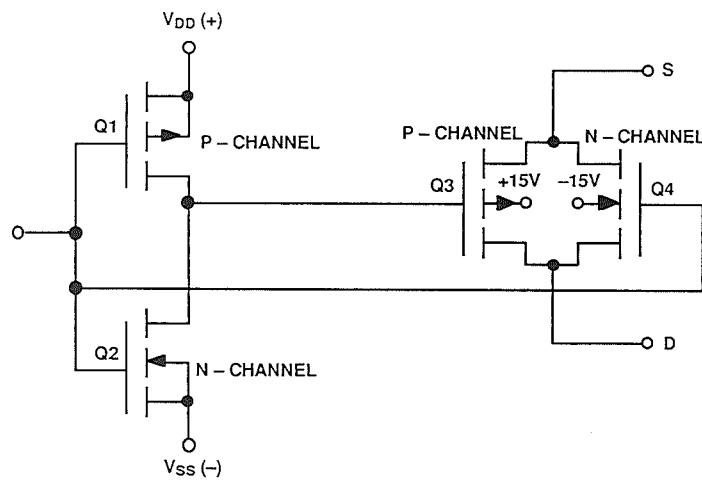


Figure 8.22

Figure 8.23 shows the ON-resistance changing with channel voltage for both N-type and P-type devices. This nonlinear resistance can cause errors in DC accuracy as well as AC distortion. The bilateral CMOS switch solves this

problem. ON-resistance is minimized and its linearity is also improved. The bottom curve of Figure 8.23 shows the improved flatness of the ON-resistance characteristic of the switch.

## CMOS SWITCH ON-RESISTANCE VERSUS SIGNAL VOLTAGE

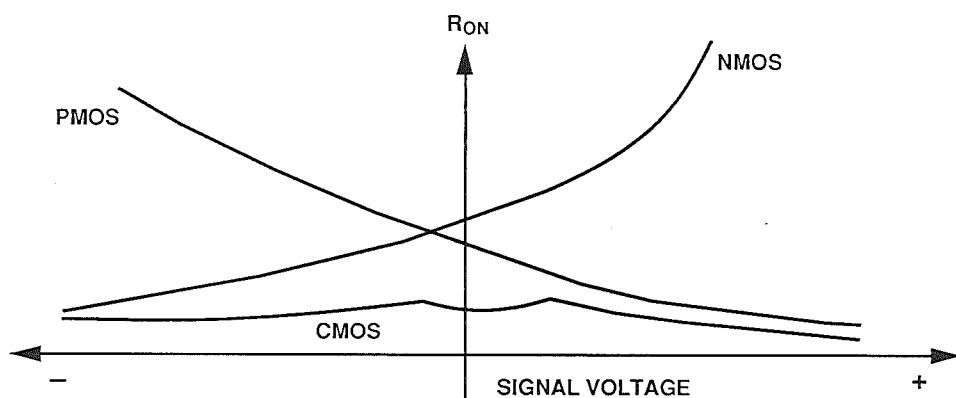


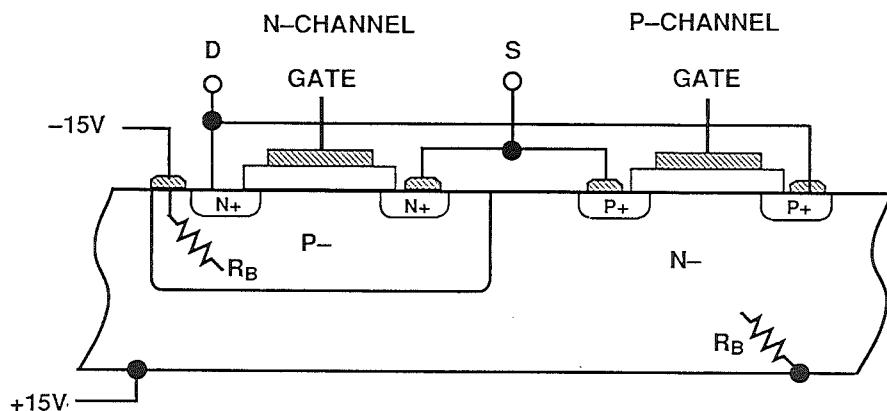
Figure 8.23

## PARASITIC LATCHUP

Most CMOS analog switches are built using junction-isolated CMOS processes. A cross-sectional view of a single switch cell is shown in Figure 8.24. Parasitic SCR (silicon controlled rectifier) latchup can occur if the analog switch terminal has voltages more positive than  $V_{DD}$  (+15V) or more

negative than  $V_{SS}$  (-15V). Even a transient situation, such as power-on with an input voltage present, can trigger a parasitic latchup. If the conduction current is too great (several hundred milliamperes or more), it can damage the switch.

## CROSS SECTION OF JUNCTION-ISOLATED CMOS SWITCH



- Problems Occur if Voltages More Positive Than  $V_{DD}$  or More Negative than  $V_{SS}$  are Applied to an Analog Switch Terminal

Figure 8.24

The parasitic SCR mechanism is shown in Figure 8.25. SCR action takes place when either terminal of the switch (source or the drain) is either one diode drop more positive than  $V_{DD}$  or one diode drop more negative than  $V_{SS}$ . In the former case, the  $V_{DD}$  terminal becomes the SCR gate input and provides the current to trigger SCR action.

In the case where the voltage is more negative than  $V_{SS}$ , the  $V_{SS}$  terminal becomes the SCR gate input and provides the gate current. In either case, high current will flow between the supplies. The amount of current depends on the collector resistances of the two transistors, which can be fairly small.

## BIPOLAR TRANSISTOR EQUIVALENT CIRCUIT OF CMOS SWITCH SHOWS PARASITIC ACTION (A CLASSIC SCR LATCH)

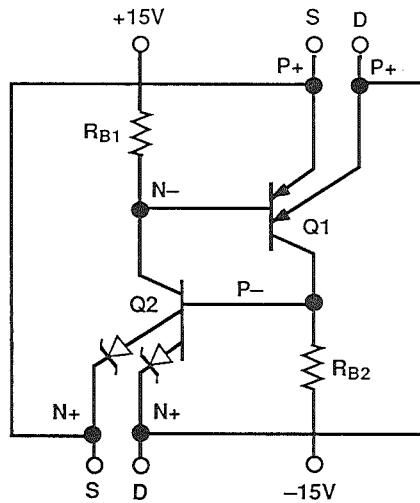


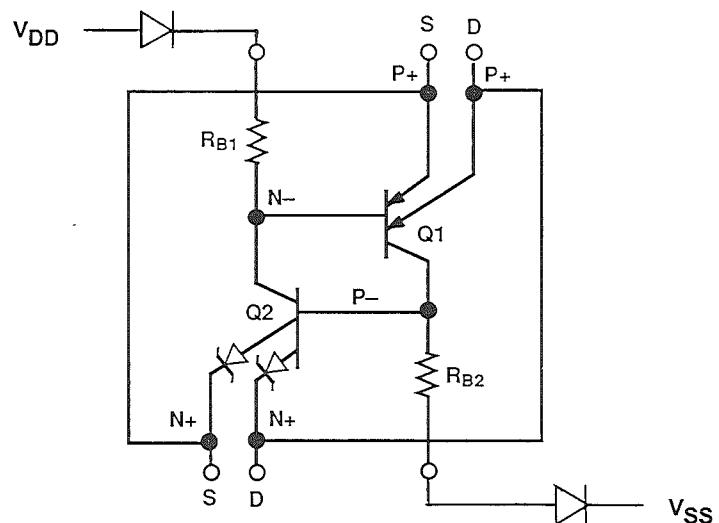
Figure 8.25

In order to prevent this type of SCR latchup, a series diode can be inserted into the  $V_{DD}$  and  $V_{SS}$  terminals as shown in Figure 8.26. The diodes block the SCR gate current. Normally the parasitic transistors Q1 and Q2 have low beta (usually less than 10) and require a comparatively large gate current to fire the SCR. The diodes limit the reverse gate current so that the SCR is not triggered.

If diode protection is used, the analog voltage range of the switch will be reduced by one  $V_{be}$  drop at each rail.

Analog switches must also be protected from possible overcurrent by inserting a series resistor to limit the current to a safe level, generally less than 25mA. This method works only if the switch drives a high impedance load (Figure 8.28).

## DIODE PROTECTION SCHEME FOR CMOS SWITCH



- Protection Diodes CR1 and CR2 Block Base Current Drive to Q1 and Q2 in Event of Overvoltage at S or D

Figure 8.26

8

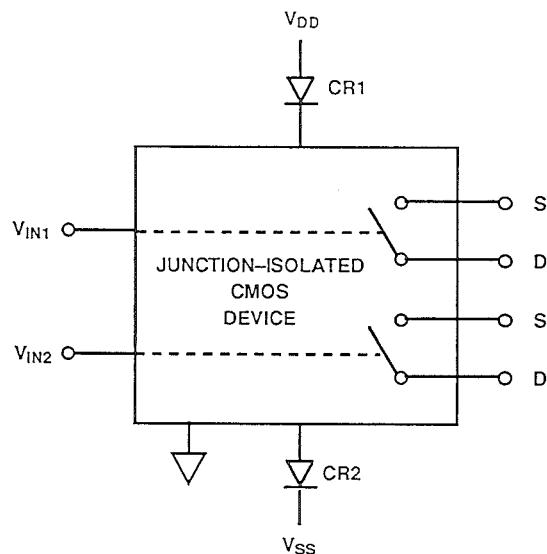
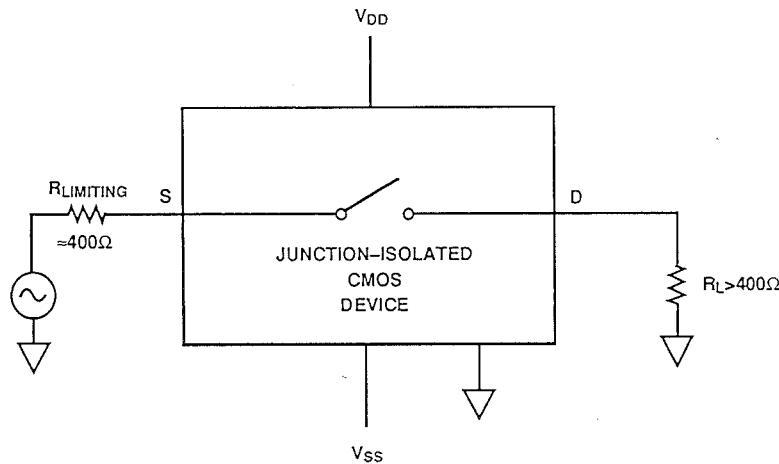
PROTECTING CMOS SWITCH / MUX  
FROM LATCHUP USING DIODES

Figure 8.27

## PROTECTING CMOS SWITCH / MUX FROM OVERCURRENT



- External Resistor Limits Current to Safe Value

Figure 8.28

Latchup protection does not provide overcurrent protection and vice versa. If both fault conditions can exist in a

system, then both protection protective diodes and resistors should be used.

## "LATCHPROOF" VERSUS "OVERVOLTAGE PROTECTED"

- *Latchproof* only means the device won't go into an SCR mode.
- It does not guarantee *Overvoltage Protection*.

Figure 8.29

## THE ANATOMY OF THE ANALOG SWITCH

It is important to understand the error sources in an analog switch. Many affect AC and DC performance, while others only affect AC. Figure 8.30

shows the equivalent circuit of two adjacent switches. It includes leakage currents and junction capacitances.

### EQUIVALENT CIRCUIT OF TWO ADJACENT SWITCHES

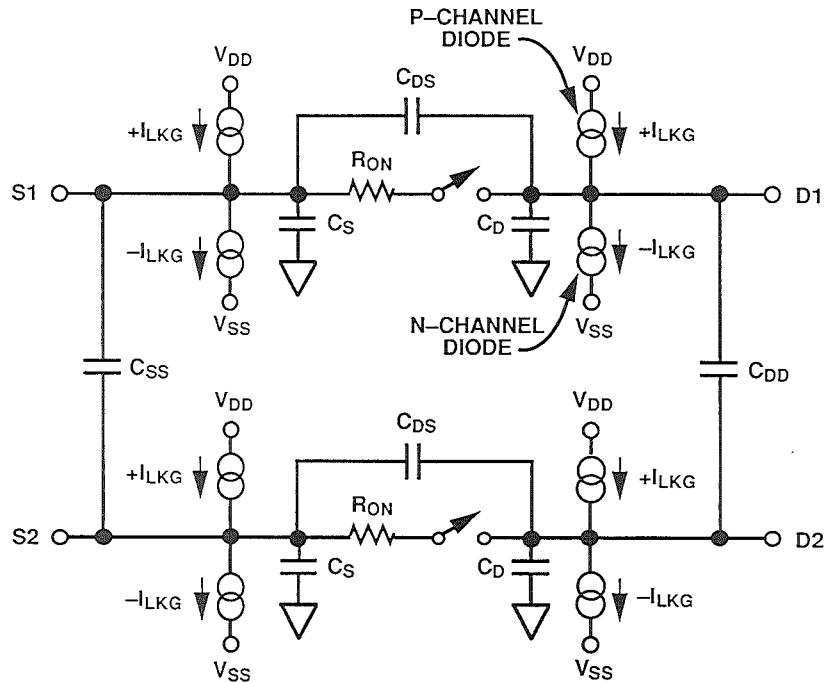
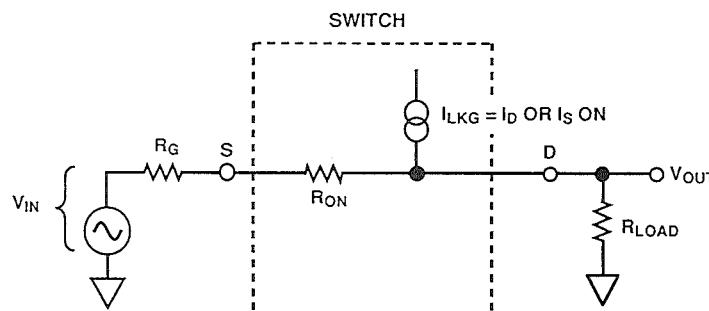


Figure 8.30

DC performance is affected mainly by the switch ON-resistance ( $R_{ON}$ ) and leakage. Low resistance circuits are more subject to errors due to  $R_{ON}$ ,

while high resistance circuits are affected by leakage currents. Figure 8.31 shows how these parameters affect DC performance.

## FACTORS AFFECTING DC PERFORMANCE FOR ON SWITCH CONDITION: $R_{ON}$ , $R_{LOAD}$ , AND $I_{LKG}$



$$V_{OUT} = V_{IN} \left[ \frac{R_{LOAD}}{R_G + R_{ON} + R_{LOAD}} \right] + I_{LKG} \left[ \frac{R_{LOAD}(R_{ON} + R_G)}{R_G + R_{ON} + R_{LOAD}} \right]$$

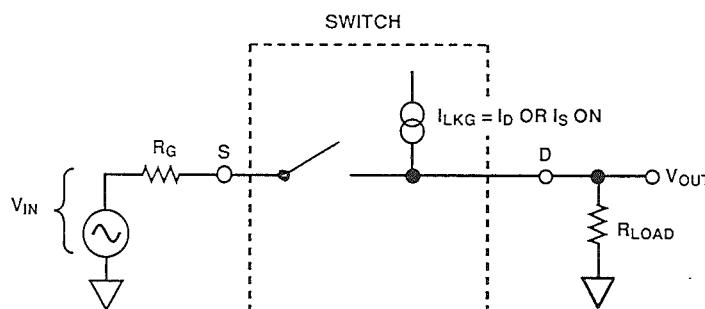
IF  $R_G \rightarrow 0$ ,

$$V_{OUT} = V_{IN} \left[ \frac{R_{LOAD}}{R_{ON} + R_{LOAD}} \right] + I_{LKG} \left[ \frac{R_{LOAD}R_{ON}}{R_{ON} + R_{LOAD}} \right]$$

Figure 8.31

When the switch is OFF, leakage current can introduce errors. (Figure 8.32)

## FACTORS AFFECTING DC PERFORMANCE FOR OFF SWITCH CONDITION: $I_{LKG}$ , AND $R_{LOAD}$



- Leakage Current Creates Error Voltage at  $V_{OUT}$  Equal to:

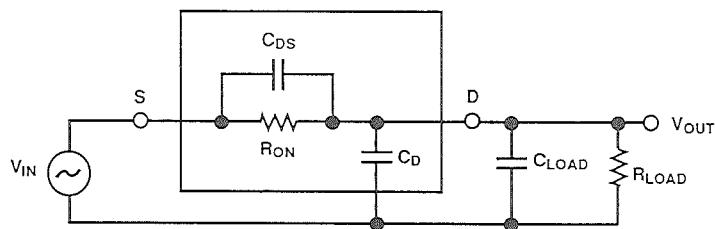
$$V_{OUT} = I_{LKG} \times R_{LOAD}$$

Figure 8.32

Figure 8.33 illustrates the parasitic components that affect the AC performance of CMOS switches. Additional external capacitances will further

degrade performance. These capacitances affect feedthrough, crosstalk and system bandwidth.

## DYNAMIC PERFORMANCE CONSIDERATIONS: TRANSFER ACCURACY VERSUS FREQUENCY



$$A(s) = \left[ \frac{R_{LOAD}}{R_{LOAD} + R_{ON}} \right] \left[ \frac{s R_{ON} C_{DS} + 1}{s \left( \frac{R_{LOAD} R_{ON}}{R_{LOAD} + R_{ON}} \right) (C_{LOAD} + C_D + C_{DS}) + 1} \right]$$

$$A(\text{dB}) = 20 \log \left[ \frac{R_{LOAD}}{R_{LOAD} + R_{ON}} \right] + 10 \log \left[ \omega^2 (R_{ON} C_{DS})^2 + 1 \right] - 10 \log \omega^2 \left[ \left( \frac{R_{LOAD} R_{ON}}{R_{LOAD} + R_{ON}} \right)^2 (C_{LOAD} + C_D + C_{DS})^2 + 1 \right]$$

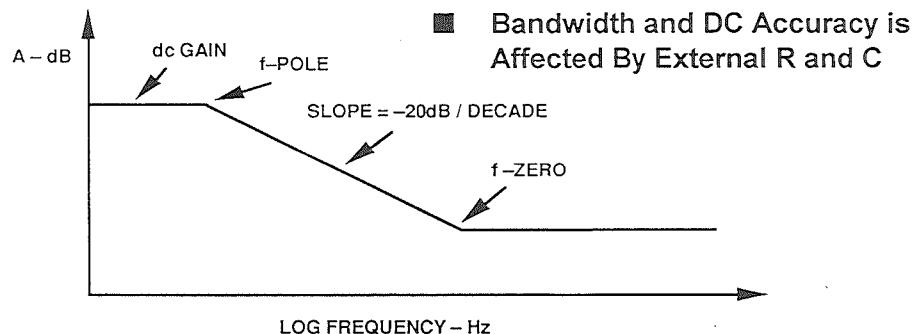
Figure 8.33

8

The signal transfer characteristic is dependent on the switch channel capacitance,  $C_{DS}$ . This capacitance creates a frequency zero in the numerator of the transfer function  $A(s)$ . This zero usually occurs at high frequencies because the switch ON resistance is small. The bandwidth is also a function of the switch output capacitance in combination with  $C_{DS}$  and the load capacitance. This frequency pole appears in the denominator of the equation.

The composite frequency domain transfer function may be re-written as shown in Figure 8.34. In most cases, the pole breakpoint frequency occurs first because of the dominant effect of the output capacitance  $C_D$ . Thus, to maximize bandwidth, a switch must have low input and output capacitance and low ON resistance.

## DYNAMIC PERFORMANCE CONSIDERATIONS: TRANSFER ACCURACY VERSUS FREQUENCY



$$A(s) = \left[ \frac{R_{LOAD}}{R_{LOAD} + R_{ON}} \right] [sR_{ON}C_{DS} + 1] \left[ \frac{1}{s \left( \frac{R_{LOAD}R_{ON}}{R_{LOAD} + R_{ON}} \right) (C_{LOAD} + C_D + C_{DS}) + 1} \right]$$

$$DC\ GAIN = \frac{R_{LOAD}R_{ON}}{R_{LOAD} + R_{ON}}, \quad f_{ZERO} = \frac{0.159}{R_{ON}C_{DS}}, \quad f_{POLE} = \frac{0.159}{\left( \frac{R_{LOAD}R_{ON}}{R_{LOAD} + R_{ON}} \right) (C_{LOAD} + C_D + C_{DS})}$$

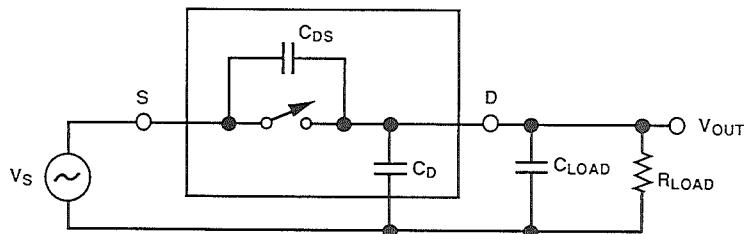
Figure 8.34

The series-pass capacitance,  $C_{DS}$ , not only creates a zero in the response in the ON-state, it degrades the feedthrough performance of the switch

during its OFF state. When the switch is off,  $C_{DS}$  couples the input signal to the output load. (Figure 8.35)

## DYNAMIC PERFORMANCE CONSIDERATIONS: OFF ISOLATION

- OFF Isolation is Affected by External R and C Load



$$A(s) = \frac{s(R_{LOAD})(C_{DS})}{s(R_{LOAD})(C_{LOAD} + C_D + C_{DS}) + 1}$$

Figure 8.35

Large values of  $C_{DS}$  will produce large values of feedthrough, proportional to the input frequency. Figure 8.36 illustrates the drop in OFF-isolation as a

function of frequency. The simplest way to maximize the OFF-isolation is to choose a switch that has as small a  $C_{DS}$  as possible.

## DYNAMIC PERFORMANCE CONSIDERATIONS: OFF ISOLATION VERSUS FREQUENCY

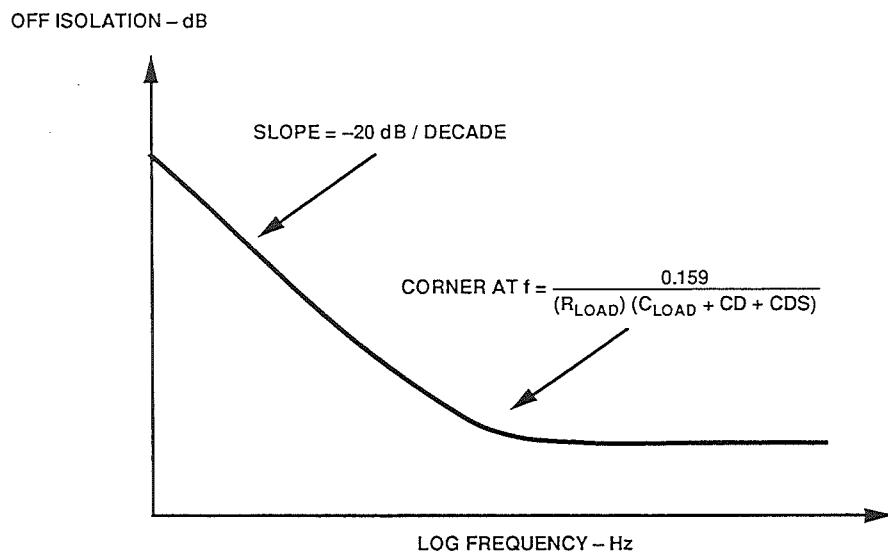


Figure 8.36

Figure 8.37 shows typical CMOS analog switch OFF-isolation as a function of frequency. From DC to several kilohertz, the switch has over 100dB isol-

ation. As the frequency increases, an increasing amount of signal reaches the output. However, even at 1MHz, the switch still has nearly 70dB of isolation.

## TYPICAL CMOS SWITCH OFF ISOLATION PERFORMANCE (ADG511/ADG512)

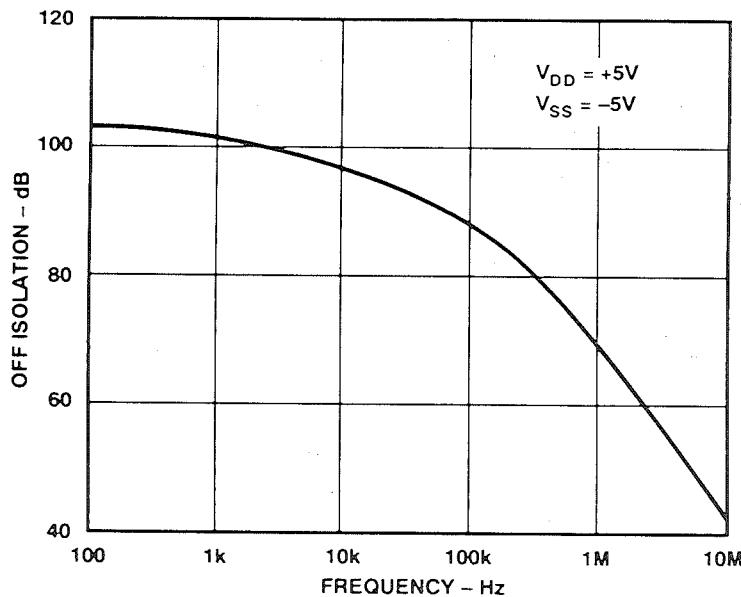


Figure 8.37

Another AC parameter that affects system performance is the charge injection that takes place during switch-

ing. Figure 8.38 shows the equivalent circuit of the charge injection mechanism.

### DYNAMIC PERFORMANCE CONSIDERATIONS: CHARGE INJECTION MODEL

- Step Waveforms of  $\pm (V_{dd} - V_{ss})$  are Applied to  $C_Q$ , the Gate Capacitance of the Output Switches

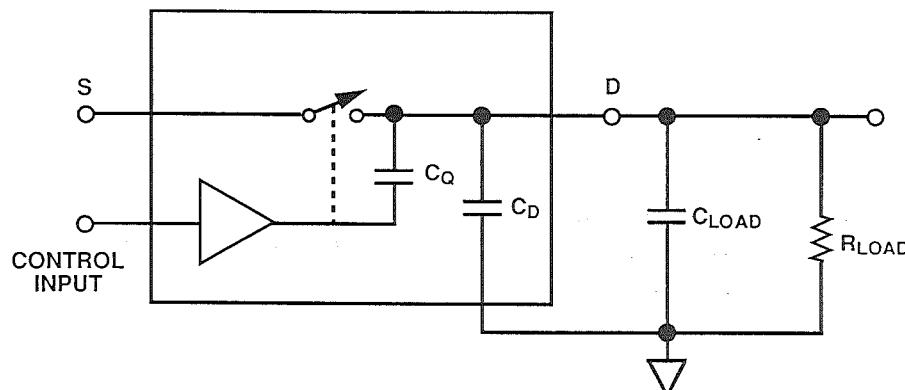


Figure 8.38

When the switch control input is asserted, it causes the control circuit to apply a large voltage change (from  $V_{DD}$  to  $V_{SS}$ , or vice versa) at the gate of the MOSFET switch. This fast change in voltage injects a charge into the switch output through the gate-drain capacitance  $C_Q$ . The amount of charge coupled depends on the gate-drain capacitance.

The charge injection introduces a step change in output voltage when switching (refer to Figure 8.39). The change in voltage is a function of the amount of charge injected, which is in turn a function of the gate-drain capacitance.

## EFFECTS OF CHARGE INJECTION

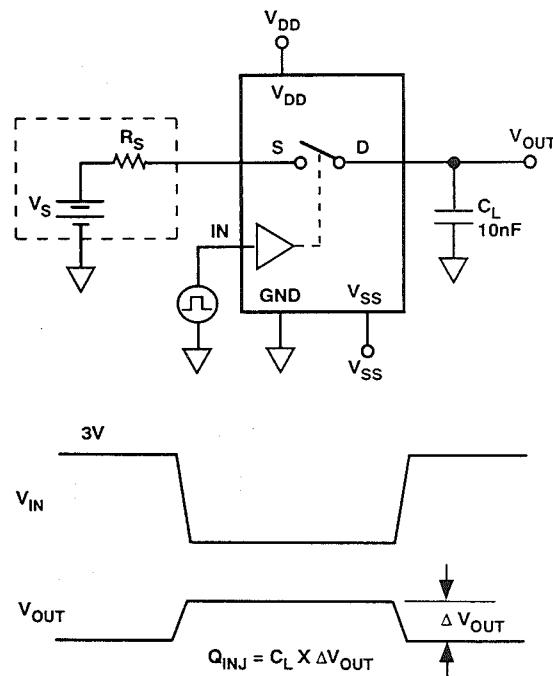


Figure 8.39

Another problem caused by switch capacitance is the retained charge, when channel switching which can

cause transients in the switch output. Figure 8.40 illustrates the phenomenon.

## CHARGE COUPLING CAUSES DYNAMIC SETTLING NOISE WHEN MULTIPLEXING SIGNALS

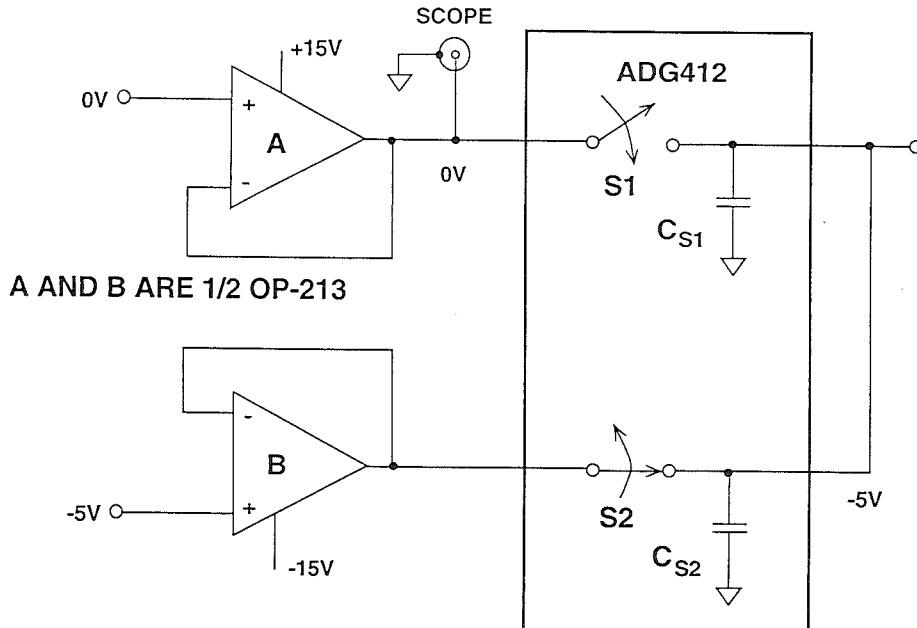


Figure 8.40

Assume that initially S2 is closed and S1 open.  $C_{S1}$  and  $C_{S2}$  are charged to -5V. As S2 opens, the -5V remains on  $C_{S1}$  and  $C_{S2}$ , as S1 closes. Thus, the output of Amplifier A sees a -5V transient. The output will not stabilize until Amplifier A's output fully discharges  $C_{S1}$  and  $C_{S2}$  and settles to 0V. The scope photo in Figure 8.41 depicts this

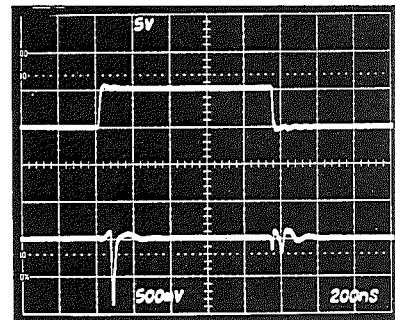
transient. The amplifier's transient load settling characteristics will be an important consideration when choosing the right device.

Crosstalk is related to the capacitances between two switches. This is the  $C_{SS}$  shown in Figure 8.42.

## OUTPUT OF OP AMP SHOWS DYNAMIC SETTLING DUE TO CHARGE COUPLING

SWITCH CONTROL  
5V/div.

AMPLIFIER A OUTPUT  
500mV/div.



HORIZONTAL SCALE: 200ns/div.

Figure 8.41

## CHANNEL-TO-CHANNEL CROSSTALK CONSIDERATION: EQUIVALENT CIRCUIT FOR ADJACENT SWITCHES

8

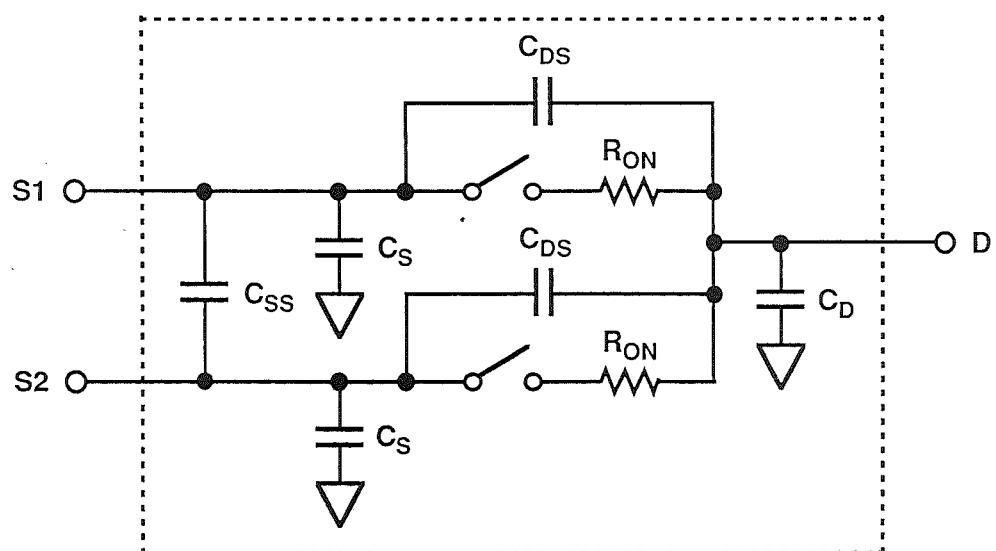


Figure 8.42

Figure 8.43 shows typical crosstalk performance of a CMOS analog switch.

Finally, the switch itself has a settling time that must be considered. Figure

8.44 shows the dynamic transfer function.

## CROSSTALK PERFORMANCE OF ADG511 SWITCH

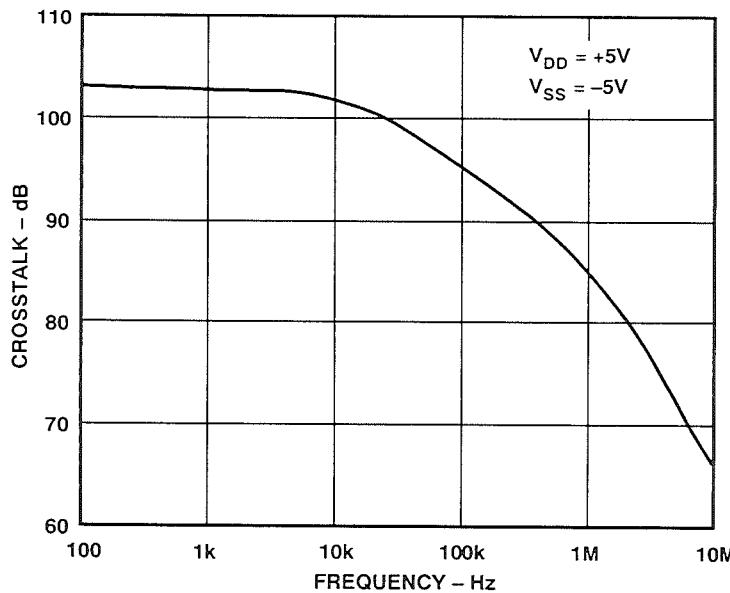
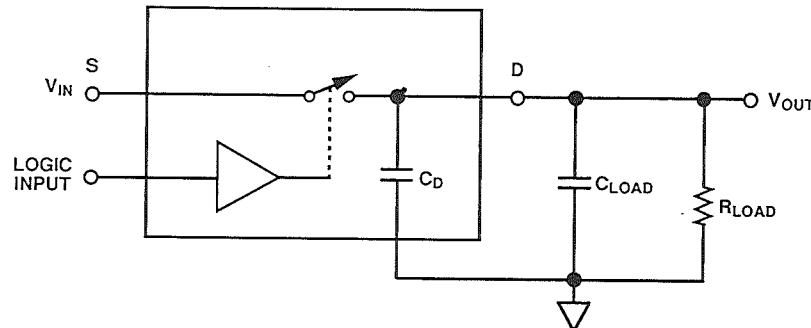


Figure 8.43

## DYNAMIC PERFORMANCE CONSIDERATIONS: SETTLING TIME

- Settling Time is the Time Required for the Switch Output Voltage to Settle to Within a Given Accuracy Band of the Final Value.



$$\text{OFF-TO-ON: } t_{\text{SETT}} = t_{\text{ON}} + \left( \frac{R_{\text{ON}} R_{\text{LOAD}}}{R_{\text{ON}} + R_{\text{LOAD}}} \right) (C_{\text{LOAD}} + C_{\text{D}}) \left( -\ln \frac{\% \text{ERROR}}{100} \right)$$

$$\text{ON-TO-OFF: } t_{\text{SETT}} = t_{\text{OFF}} + (R_{\text{LOAD}})(C_{\text{LOAD}} + C_{\text{D}}) \left( -\ln \frac{\% \text{ERROR}}{100} \right)$$

Figure 8.44

The settling time can be calculated because the response is a function of the switch and circuit resistances and capacitances. One can assume that this

is a single-pole system and calculate the number of time constants required to settle to the desired system accuracy (Figure 8.45).

### NUMBER OF TIME CONSTANTS REQUIRED TO SETTLE TO GIVEN ACCURACY BAND

RESOLUTION	% REQUIRED FOR 1/2 LSB	# OF TIME CONSTANTS
8 Bits	0.1953	6.24
10 Bits	0.0488	7.63
12 Bits	0.0122	9.01
14 Bits	0.0031	10.38
16 Bits	0.0008	11.74
18 Bits	0.0002	13.12

Figure 8.45

## TRENCH-ISOLATED LC2MOS ANALOG SWITCH FAMILY OFFERS MANY BENEFITS

Analog Devices uses trench-isolation technology to produce its LC<sup>2</sup>MOS analog switches. The process reduces the latchup susceptibility of the device,

the junction capacitances, increases switching time and leakage current, and extends the analog voltage range to the supply rails.

## ADG411/ADG511 FAMILY OF TRENCH-ISOLATED LC<sup>2</sup>MOS ANALOG SWITCHES

- Latch-Up Proof
- Analog Signal Range to Supply Rails
- Fast Switching Times
- Break Before Make Switching
- Low ON-Resistance
- Low Leakage

Figure 8.46

Figure 8.47 shows the cross-sectional view of the complementary CMOS structure. The buried oxide layer and the side walls completely isolate the substrate from each transistor junction.

Therefore, no reverse-biased PN junction is formed. Consequently the bandwidth-reducing capacitances and the possibility of SCR latchup are greatly reduced.

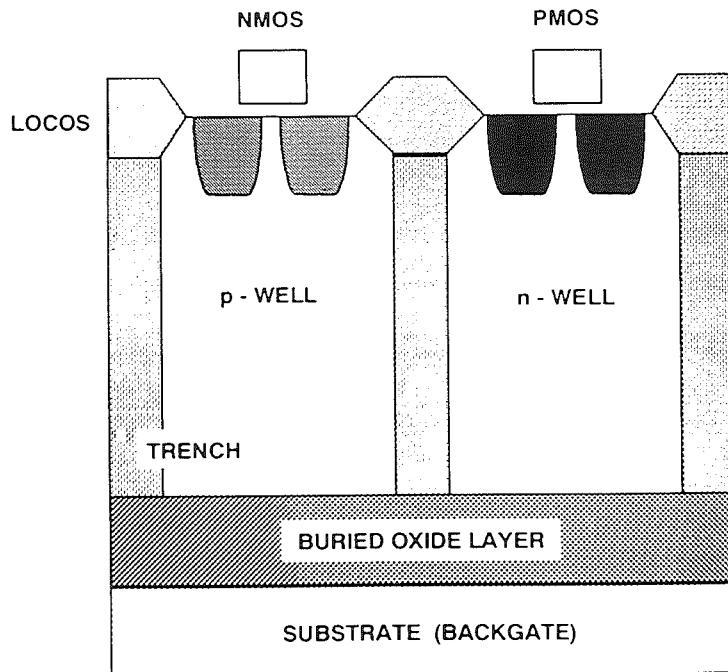
TRENCH-ISOLATION LC<sup>2</sup>MOS STRUCTURE

Figure 8.47

## APPLYING THE ANALOG SWITCH

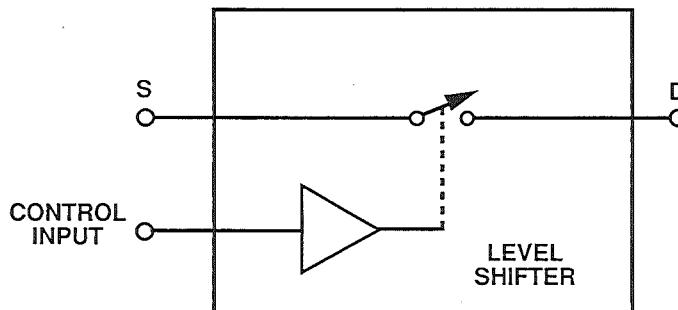
Switching time is an important consideration in applying analog switches, but switching time should not be confused with settling time. ON and OFF times are simply a measure of the propaga-

tion delay from the control input to the toggling of the switch, and are largely caused by time delays in the drive and level-shift circuits.

8

APPLYING THE ANALOG SWITCH:  
DYNAMIC PERFORMANCE CONSIDERATIONS

- ton and toff should not be confused with settling time.



- ton and toff are simply a measure of the propagation delay from control input to operation of the analog switch. It is caused by time delays in the drive / level-shifter logic circuitry.

Figure 8.48

When a CMOS multiplexer switches inputs to an inverting summing amplifier, it should be noted that the ON-resistance, and its nonlinear change as a function of input voltage, will cause errors (refer to Figure 8.49). If the

resistors are large, the switch leakage current may introduce error. Small resistors minimize leakage current error but increase the error due to the finite value of  $R_{ON}$ .

## APPLYING THE ANALOG SWITCH: UNITY GAIN INVERTER WITH SWITCHED INPUT

- Problem: Effect of  $\Delta R_{ON}$  versus  $\Delta V_S$  on Circuit Linearity.
- $R_{ON}$  variation due to  $\Delta V_{IN}$  degrades linearity of  $V_{OUT}$  relative to  $V_{IN}$

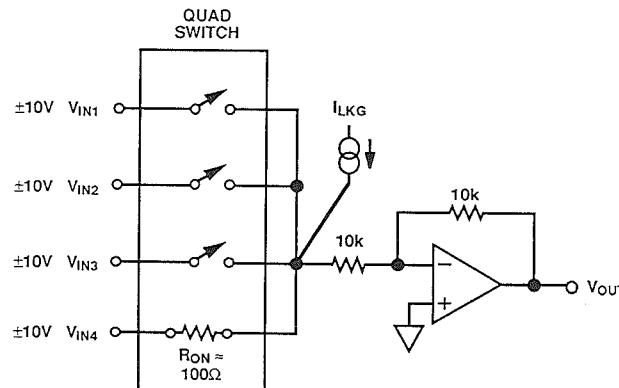


Figure 8.49

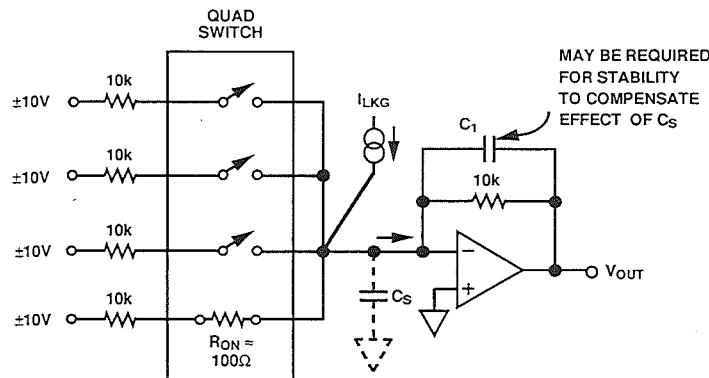
To minimize the effect of  $R_{ON}$  change due to the change in input voltage, it is advisable to put the multiplexing switches at the op amp summing junction as shown in Figure 8.50. This ensures the switches are only modulated with about  $\pm 100mV$  rather than the full  $\pm 10V$  - but a resistor is required for each input leg.

It is important to know how much parasitic capacitance has been added to the summing junction as a result of adding a multiplexer, because any capacitance added to that node intro-

duces phase shift to the amplifier closed loop response. If the capacitance is too large, the amplifier may become unstable and oscillate. A small capacitance,  $C_1$ , across the feedback resistor may be required to stabilize the circuit.

The finite value of  $R_{ON}$  is a significant error source. The gain-set resistors should be at least 1,000 times larger than the switch ON-resistance to guarantee 0.1% gain accuracy. Higher values yield greater accuracy, but the proper selection of  $C_1$  is critical to maintain stability.

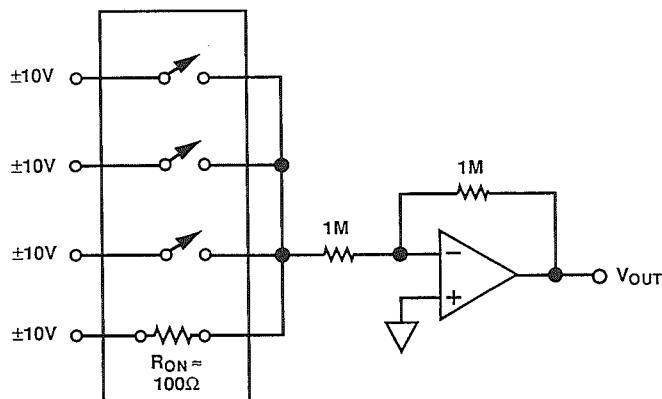
## APPLYING THE ANALOG SWITCH: MINIMIZING THE INFLUENCE OF $\Delta V_S$ (AND THUS $\Delta R_{ON}$ )



- Connecting the Switch at the Summing Point
- The switch only sees  $\pm 100mV$ , not  $\pm 10V$ .  $R_{ON}$  variation is minimized, and  $V_{OUT}$  accuracy is improved.

Figure 8.50

## APPLYING THE ANALOG SWITCH: MINIMIZING THE INFLUENCE OF $\Delta V_S$ (AND THUS $\Delta R_{ON}$ )



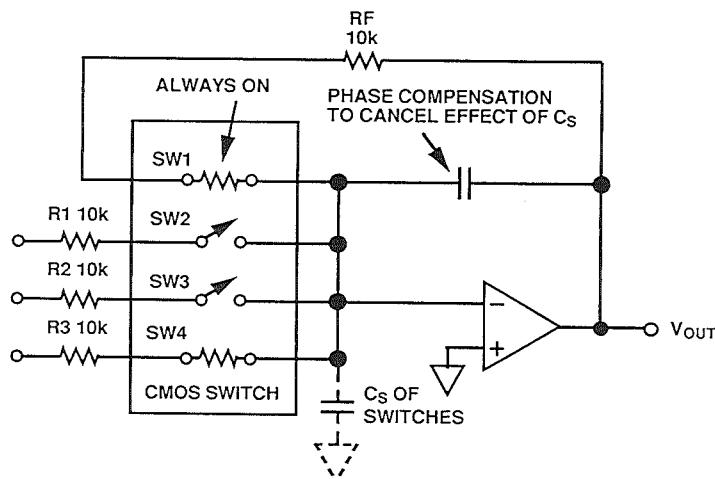
- Using Larger Values of Resistance
- $R_{ON}$  Variation due to Input Signal is Small Compared to the  $1M\Omega$  Switch Load. Effect on Transfer Accuracy is Minimized.
- Bias Current and Leakage are now very important

Figure 8.51

A better method of compensating for  $R_{ON}$  is to place one of the switches in series with the feedback resistor of the inverting amplifier as shown in Figure 8.52. It is a safe assumption that the multiple switches, fabricated on a single

chip, are well-matched in absolute characteristics and tracking over temperature. Therefore, the amplifier is closed-loop gain stable at unity gain, since the total feedforward and feedback resistors are matched.

### APPLYING THE ANALOG SWITCH: MINIMIZING THE INFLUENCE OF $R_{ON}$ AND $\Delta R_{ON}$ VERSUS TEMPERATURE ON CIRCUIT ACCURACY



- Switch in Series With Feedback Resistor Compensates for Gain Error.

Figure 8.52

The best multiplexer drives the non-inverting input of the amplifier. The high input impedance of the non-inverting input eliminates the errors due to  $R_{ON}$ . (Figure 8.53)

When multiplexing signals into an ADC, particularly the successive-approximation (SAR) type, it is advisable to place a buffer between the switch

output and the input of the converter. The transient currents at the ADC input produced by the conversion process (DAC switching) are absorbed by a drive amplifier of sufficiently low output impedance and high bandwidth. Driving the ADC directly with the switches will produce significant conversion errors due to the finite  $R_{ON}$  resistance.

**APPLYING THE ANALOG SWITCH:  
MINIMIZING THE INFLUENCE OF  $\Delta V_S$  (AND THUS  $\Delta R_{ON}$ )  
NON-INVERTING SOLUTION**

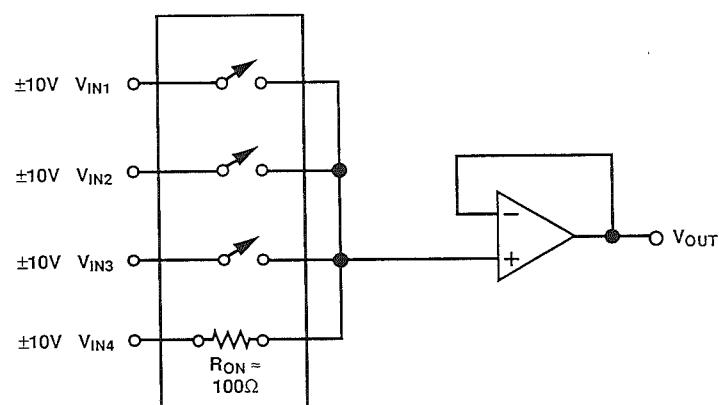


Figure 8.53

**APPLYING THE ANALOG SWITCH:  
BUFFER THE MUX OUTPUT INTO SAR-TYPE  
ADC TO MINIMIZE GAIN ERROR**

8

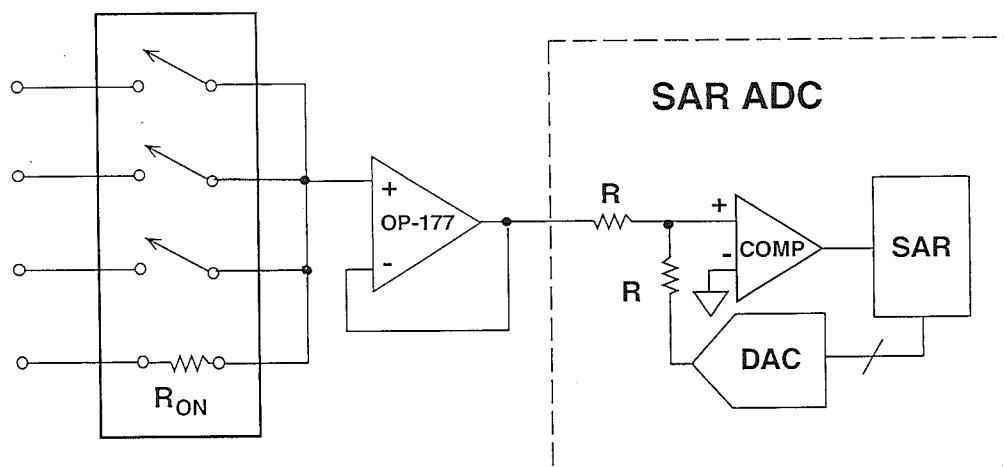


Figure 8.54

## SAMPLE AND HOLD CIRCUITS

*Walt Kester, James Bryant*

The *sample and hold amplifier*, or SHA, is a critical part of many data acquisition systems. It captures an analog signal and holds it during some operation (most commonly analog-digital conversion). The circuitry involved is demanding, and unexpected properties of commonplace components such as capacitors and printed circuit boards may degrade SHA performance.

When the sample-and-hold is in the sample mode, the output follows the input with only a small voltage offset. There do exist SHAs where the output during the *sample* mode does not follow the input accurately, and the output is only accurate during the *hold* period. An example is the AD871. These will not be considered here. Strictly speaking, a sample and hold with good tracking performance should be referred to as a *track and hold* circuit, but in practice the terms are used interchangeably.

In the past, the commonest application of a SHA was to maintain the input to an ADC at a constant value during conversion (with many, but not all,

types of ADC the input may not change by more than 1 LSB during conversion lest the process be corrupted - this either sets very low input frequency limits on such ADCs, or requires that they be used with a SHA to hold the input during each conversion). Today, high density IC processes allow the manufacture of ADCs containing an integral SHA. Wherever possible ADCs with integral SHA (often known as *sampling* ADCs) should be used in preference to separate ADCs and SHAs. The advantage of such a sampling ADC, apart from the obvious ones of smaller size, lower cost, and fewer external components, is that the overall performance is specified, and the designer need not spend time ensuring that there are no specification, interface, or timing issues involved in combining a discrete ADC and a discrete SHA.

Although the largest application of SHAs is driving ADCs, they are also used in DAC deglitchers, peak detectors, analog delay circuits, simultaneous sampling systems, and data distribution systems.

## SAMPLE-AND-HOLD AMPLIFIERS (SHAs)

- Two States of Operation:
  - ◆ *Sample* (or *Track*) the input signal
  - ◆ *Hold* the input signal at the value it has at the instant the Hold Command is asserted
- The terms *Sample-and-Hold* and *Track-and-Hold* are used interchangeably, but some SHAs have degraded track mode performance
- Applications:
  - ◆ Driving ADCs (Holding the signal constant during the conversion process)
  - ◆ Sampling ADCs (on-chip SHA)
  - ◆ DAC Deglitchers
  - ◆ Peak Detectors
  - ◆ Data Acquisition and Distribution Systems

Figure 8.55

## BASIC SHA OPERATION

Regardless of the circuit details or type of SHA in question, all such devices have four major components. The input amplifier, energy storage device (capacitor), output buffer, and switching circuits are common to all SHAs as shown in the typical configuration of Figure 8.56.

The energy-storage device, the heart of the SHA, is almost always a capacitor. The input amplifier buffers the input by presenting a high impedance to the signal source and providing current gain to charge the hold capacitor. In the

**8**  
*track* mode, the voltage on the hold capacitor follows (or tracks) the input signal (with some delay and bandwidth limiting). In the *hold* mode, the switch is opened, and the capacitor retains the voltage present before it was disconnected from the input buffer. The output buffer offers a high impedance to the hold capacitor to keep the held voltage from discharging prematurely. The switching circuit and its driver form the mechanism by which the SHA is alternately switched between track and hold.

## BASIC SAMPLE-AND-HOLD CIRCUIT

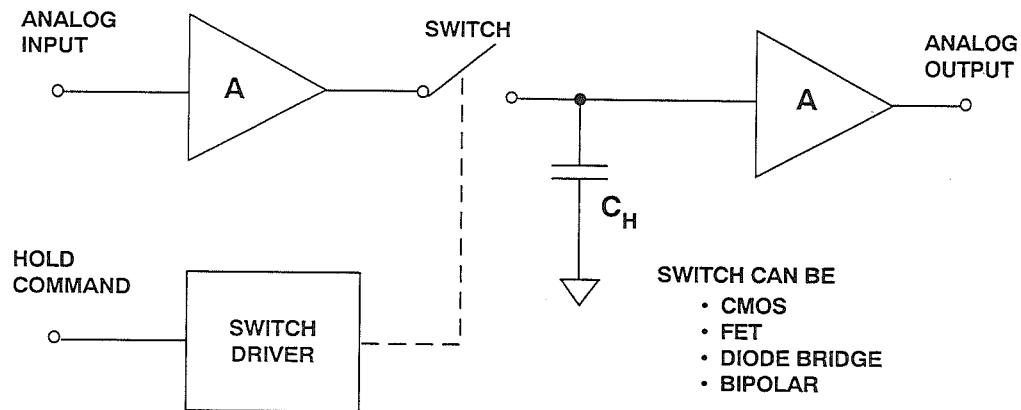


Figure 8.56

There are four groups of specifications that describe basic SHA operation: track mode, track-to-hold transition, hold mode, hold-to-track transition. These specifications are summarized in Figure 8.57, and some of the SHA error

sources are shown in Figure 8.58. Because there are both DC and AC performance implications for each of the four modes, properly specifying a SHA and understanding its operation in a system is a complex matter.

## SAMPLE-AND-HOLD SPECIFICATIONS

SAMPLE MODE	SAMPLE-TO-HOLD TRANSITION	HOLD MODE	HOLD-TO-SAMPLE TRANSITION
STATIC:	STATIC: ◆ Offset ◆ Gain Error ◆ Nonlinearity	STATIC: ◆ Pedestal ◆ Dielectric Absorption	
DYNAMIC:	DYNAMIC: ◆ Settling Time ◆ Bandwidth ◆ Slew Rate ◆ Distortion ◆ Noise	DYNAMIC: ◆ Aperture Delay Time ◆ Aperture Jitter ◆ Switching Transient ◆ Settling Time	DYNAMIC: ◆ Feedthrough ◆ Distortion ◆ Noise ◆ Acquisition Time ◆ Switching Transient

Figure 8.57

## SOME SOURCES OF ERROR IN A SAMPLE-AND-HOLD

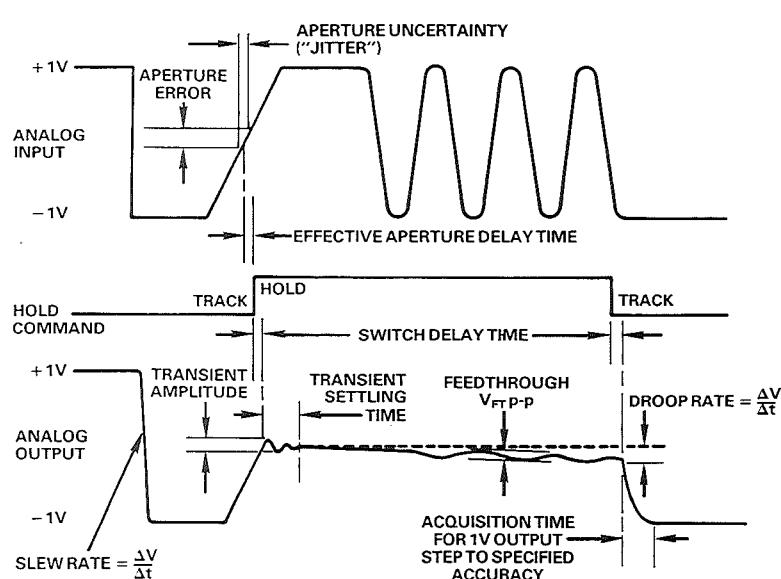


Figure 8.58

## TRACK MODE SPECIFICATIONS

Since a SHA in the sample (or track) mode is simply an amplifier, both the static and dynamic specifications in this mode are similar to those of any amplifier. (SHAs which have degraded performance in the track mode are generally only specified in the hold mode.) The principle track mode specifications are

*offset, gain, nonlinearity, bandwidth, slew rate, settling time, distortion, and noise*, however distortion and noise in the track mode are often of less interest than in the hold mode. Fundamental amplifier specifications are discussed in detail in Section 1 and will not be repeated here.

## TRACK-TO-HOLD MODE SPECIFICATIONS

When the SHA switches from track to hold, there is generally a small amount of charge dumped on the hold capacitor because of non-ideal switches. This results in a hold mode DC offset voltage which is called *pedestal* error. If the SHA is driving an ADC, the pedestal

error appears as a DC offset voltage which may be removed by performing a system calibration. If the pedestal error is a function of input signal level, the resulting nonlinearity contributes to hold mode distortion.

### TRACK-TO-HOLD MODE PEDESTAL, TRANSIENT, AND SETTLING TIME ERRORS

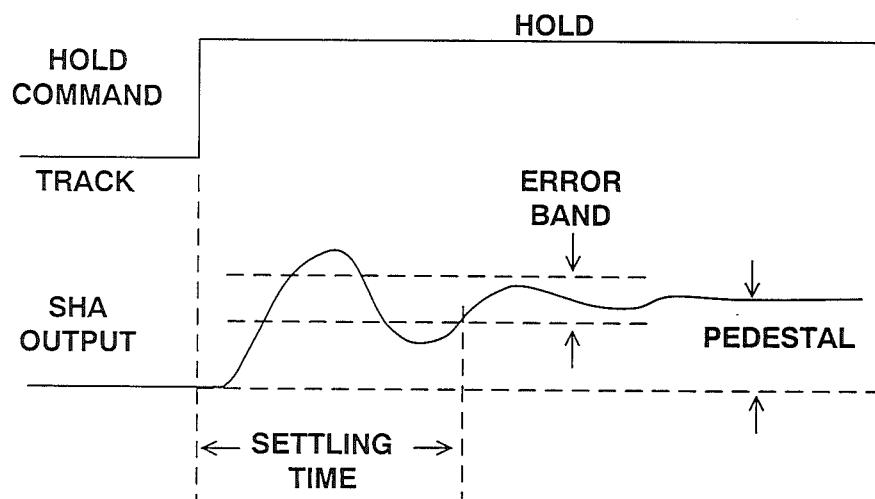


Figure 8.59

Pedestal errors may be reduced by increasing the value of the hold capacitor with a corresponding increase in acquisition time and a reduction in bandwidth and slew rate.

Switching from track to hold produces a transient, and the time required for the SHA output to settle to within a specified error band is called *hold mode settling time*. Occasionally, the peak amplitude of the switching transient is also specified.

Perhaps the most misunderstood and misused SHA specifications are those that include the word *aperture*. The most essential dynamic property of a SHA is its ability to disconnect quickly the hold capacitor from the input buffer amplifier. The short (but non-zero) interval required for this action is called

*aperture time*. The actual value of the voltage that gets held at the end of this interval is a function of both the input signal and the errors introduced by the switching operation itself. Figure 8.61 shows what happens when the hold command is applied with an input signal of arbitrary slope (for clarity, the sample to hold pedestal and switching transients are ignored). The value that finally gets held is a delayed version of the input signal, averaged over the aperture time of the switch as shown in Figure 8.61. The first-order model assumes that the final value of the voltage on the hold capacitor is approximately equal to the average value of the signal applied to the switch over the interval during which the switch changes from a low to high impedance ( $t_a$ ).

## SHA CIRCUIT SHOWING INTERNAL TIMING

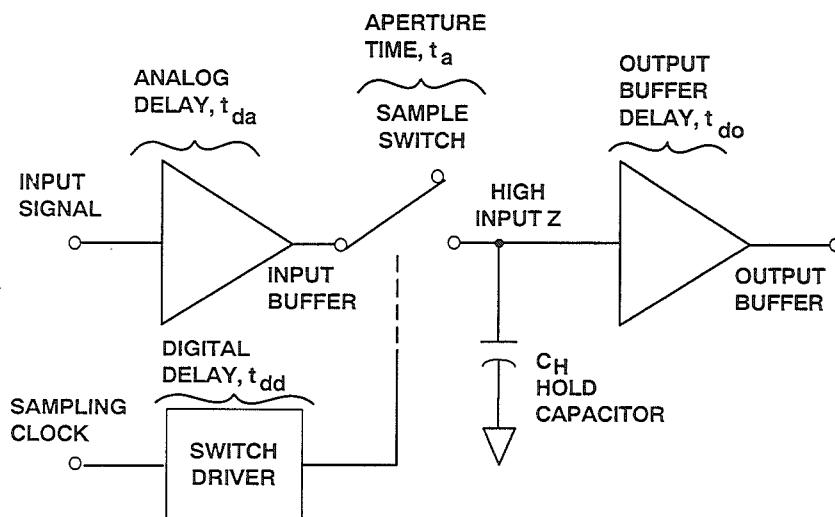


Figure 8.60

## SHA WAVEFORMS

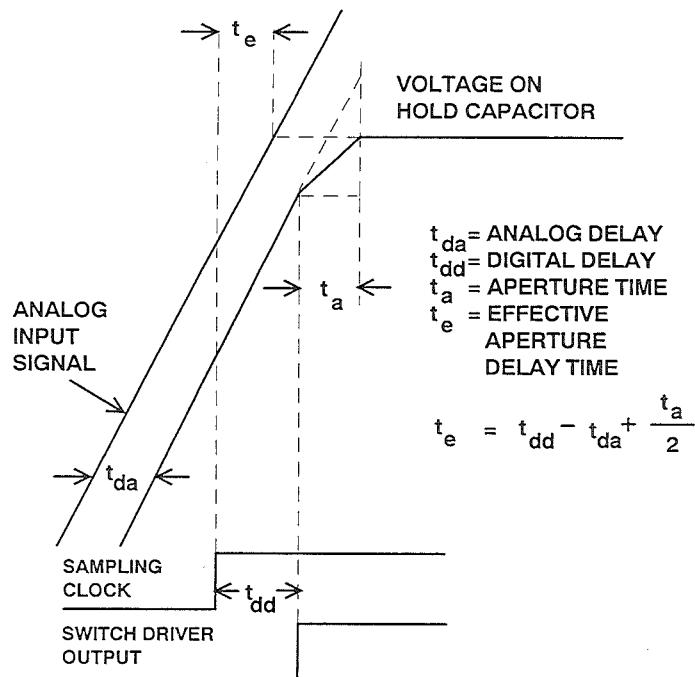


Figure 8.61

The model shows that the finite time required for the switch to open ( $t_a$ ) is equivalent to introducing a small delay in the sampling clock driving the SHA. This delay is constant and may either be positive or negative. It is called *effective aperture delay time*, *aperture delay time*, or simply *aperture delay*, ( $t_e$ ) and is defined as the time difference between the analog propagation delay of the front-end buffer ( $t_{da}$ ) and the switch digital delay ( $t_{dd}$ ) plus one-half the aperture time ( $t_a/2$ ). The effective aperture delay time is usually positive, but may be negative if the sum of one-half the aperture time ( $t_a/2$ ) and the switch digital delay ( $t_{dd}$ ) is less than

the propagation delay through the input buffer ( $t_{da}$ ). The aperture delay specification thus establishes when the input signal is actually sampled with respect to the sampling clock edge.

Aperture delay time can be measured by applying a bipolar sinewave signal to the SHA and adjusting the synchronous sampling clock delay such that the output of the SHA is zero during the hold time. The relative delay between the input sampling clock edge and the actual zero-crossing of the input sinewave is the aperture delay time (see Figure 8.62).

## MEASURING EFFECTIVE APERTURE DELAY TIME

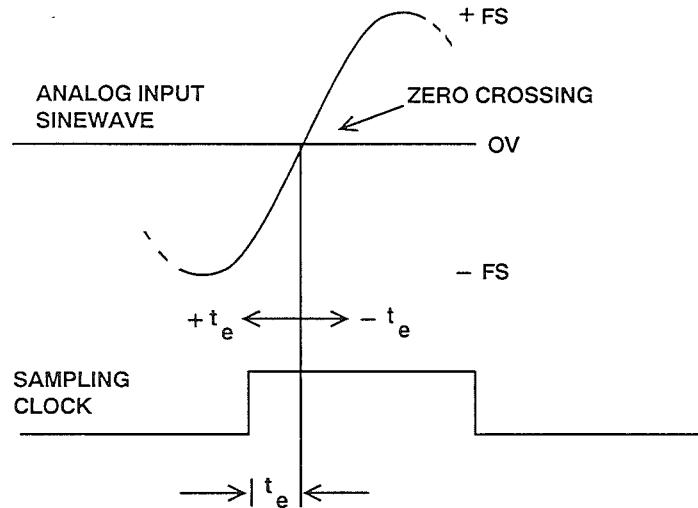


Figure 8.62

Aperture delay produces no errors, but acts as a fixed delay in either the sampling clock input or the analog input (depending on its sign). If there is sample-to-sample variation in aperture delay (*aperture jitter*), then a corresponding voltage error is produced as shown in Figure 8.63. This sample-to-sample variation in the instant the

switch opens is called *aperture uncertainty*, or *aperture jitter* and is usually measured in rms picoseconds. The amplitude of the associated output error is related to the rate-of-change of the analog input. For any given value of aperture jitter, the aperture jitter error increases as the input  $dv/dt$  increases.

## EFFECTS OF APERTURE JITTER ON SHA OUTPUT

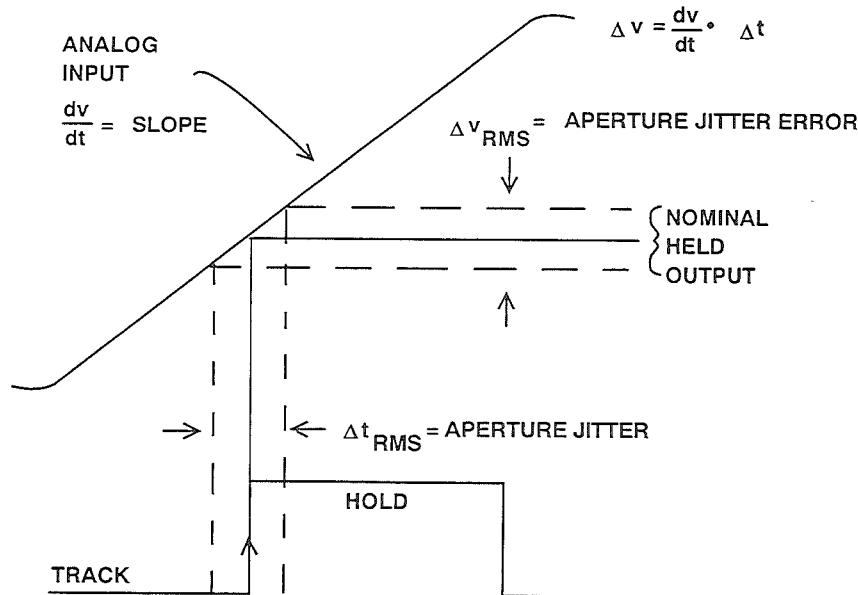


Figure 8.63

Measuring aperture jitter error in a SHA requires a jitter-free sampling clock and analog input signal source, because jitter (or phase noise) on either signal cannot be distinguished from the SHA aperture jitter itself - the effects are the same. In fact, the largest source of timing jitter errors in a system is most often external to the SHA (or the ADC if it is a sampling one) and is caused by noisy or unstable clocks, improper signal routing, and lack of attention to good grounding and

decoupling techniques. SHA aperture jitter is generally less than 50ps rms, and less than 5ps rms in high speed devices.

Figure 8.64 shows the effects of total sampling clock jitter on the signal-to-noise ratio (SNR) of a sampled data system. The total rms jitter will be composed of a number of components, the actual SHA aperture jitter often being the least of them.

## EFFECTS OF SAMPLING CLOCK JITTER ON SNR

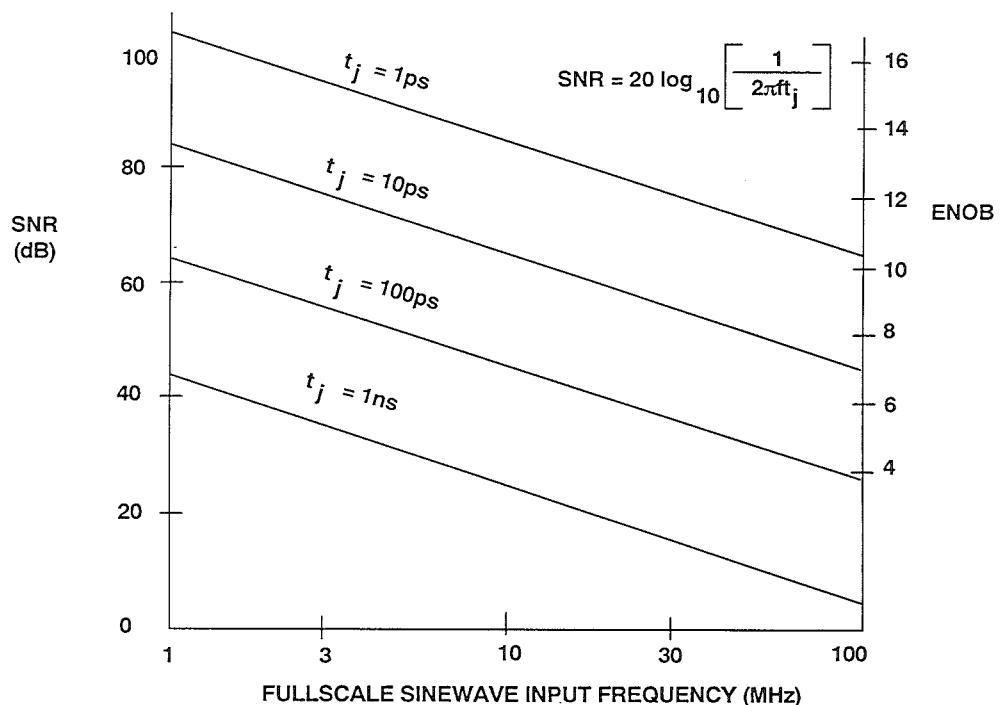


Figure 8.64

## HOLD MODE SPECIFICATIONS

During the hold mode there are errors due to imperfections in the hold capacitor, switch, and output amplifier. If a leakage current flows in or out of the hold capacitor, it will slowly charge or discharge, and its voltage will change. This effect is known as *droop* in the SHA output and is expressed in  $\text{V}/\mu\text{s}$ . Droop can be caused by leakage across a dirty PCB if an external capacitor is used, or by a leaky capacitor, but is most usually due to leakage current in semiconductor switches and the bias current of the output buffer amplifier. An acceptable value of droop is where

the output of a SHA does not change by more than 1/2 LSB during the conversion time of the ADC it is driving. Where droop is due to leakage current in reversed biased junctions (switches or FET amplifier gates), it will double for every  $10^\circ\text{C}$  increase in chip temperature - which means that it will increase a thousand fold between  $+25^\circ\text{C}$  and  $+125^\circ\text{C}$ . Droop can be reduced by increasing the value of the hold capacitor, but this will also increase acquisition time and reduce bandwidth in the track mode.

## HOLD MODE DROOP

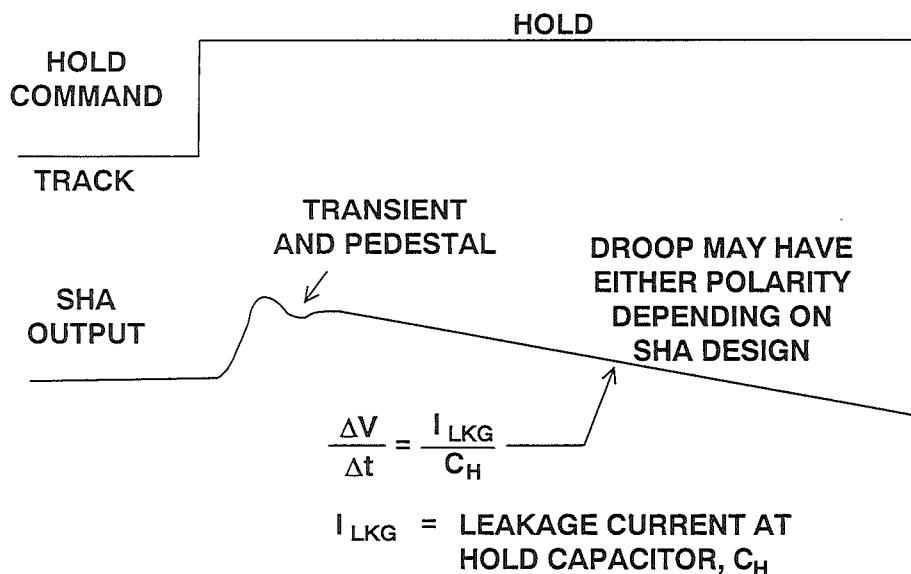
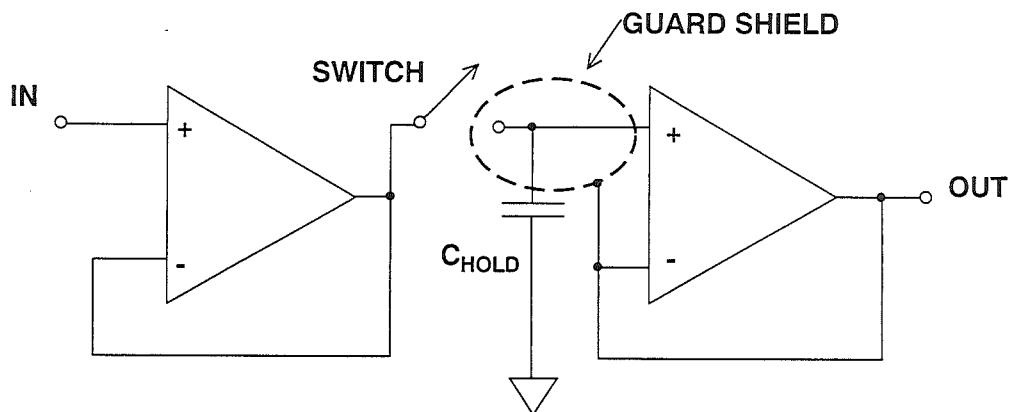


Figure 8.65

Even quite small leakage currents can cause troublesome droop when SHAs use small hold capacitors. Leakage currents in PCBs may be minimized by the intelligent use of guard rings. A guard ring is a ring of conductor which surrounds a sensitive node and is at the same potential. Since there is no voltage between them, there can be no leakage current flow. In a non-inverting application, such as is shown in Figure

8.66, the guard ring must be driven to the correct potential, whereas the guard ring on a virtual ground can be at actual ground potential (Figure 8.67). The surface resistance of PCB material is much lower than its bulk resistance, so guard rings must always be placed on both sides of a PCB - and on multi-layer boards, guard rings should be present in all layers.

**DRIVE THE GUARD SHIELD WITH THE SAME VOLTAGE AS THE HOLD CAPACITOR TO REDUCE BOARD LEAKAGE**



Note: Be Sure a Guard Shield is in Each Layer of the PCB

Figure 8.66

**USING A GUARD SHIELD ON A VIRTUAL GROUND SHA DESIGN**

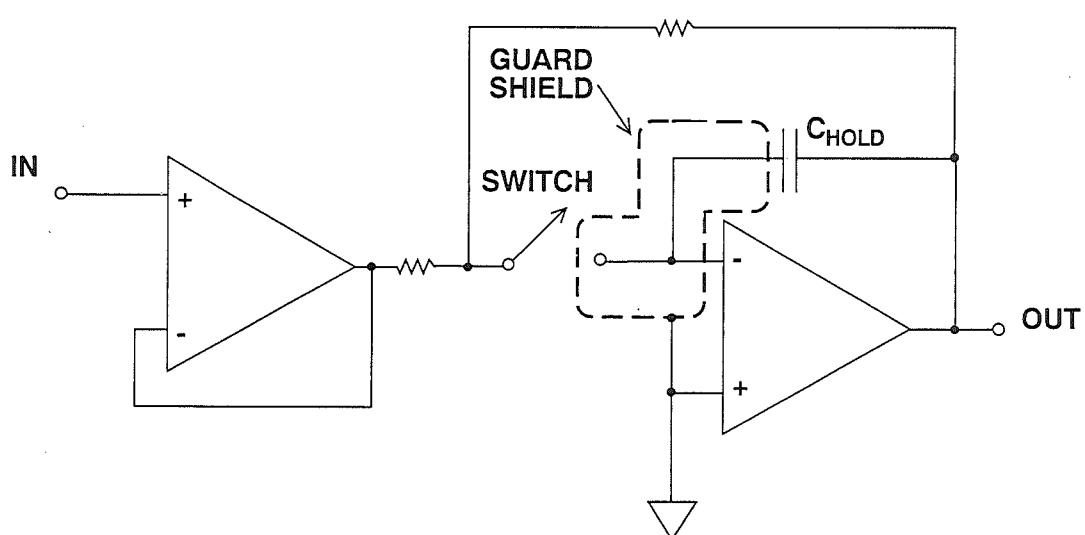


Figure 8.67

Hold capacitors for SHAs must have low leakage, but there is another characteristic which is equally important: low *dielectric absorption*. If a capacitor is charged, then discharged, and then left open circuit, it will recover some of its charge. The phenomenon is known as

*dielectric absorption*, and it can seriously degrade the performance of a SHA, since it causes the remains of a previous sample to contaminate a new one, and may introduce random errors of tens or even hundreds of mV.

### DIELECTRIC ABSORPTION

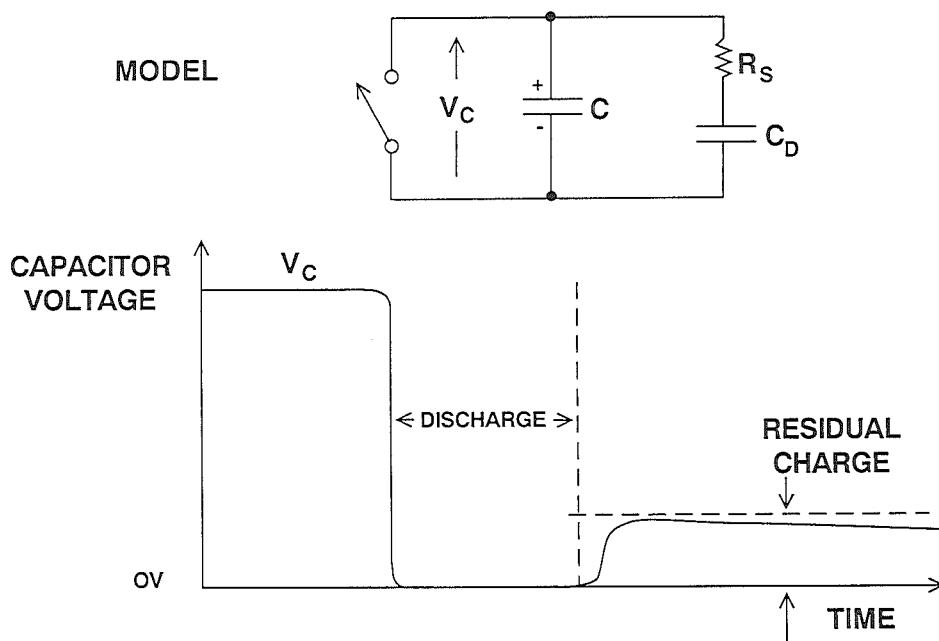


Figure 8.68

Different capacitor materials have differing amounts of dielectric absorption - electrolytic capacitors are dreadful (their leakage is also high), and some high-K ceramic types are bad, while mica, polystyrene and polypropylene are generally good. Unfortunately, dielectric absorption varies from batch to batch, and even occasional batches of

polystyrene and polypropylene capacitors may be affected. It is therefore wise to pay 30-50% extra when buying capacitors for SHA applications and buy devices which are guaranteed by their manufacturers to have low dielectric absorption, rather than types which might generally be expected to have it.

## THE CHOICE OF HOLD CAPACITOR AFFECTS ACCURACY

- Must Have: Low Leakage and Low Dielectric Absorption
- Best:                           ↑ Polystyrene
- ↑ Polypropylene
- ↑ Teflon
- ↑ Polycarbonate
- Worst:                        ↓ Mylar
- ↓ Glass
- ↓ Electrolytic

Figure 8.69

Stray capacity in a SHA may allow a small amount of the AC input to be coupled to the output during hold. This effect is known as *feedthrough* and is dependent on input frequency and amplitude. If the amplitude of the feedthrough to the output of the SHA is more than 1/2 LSB, then the ADC is subject to conversion errors.

In many SHAs, distortion is specified only in the track mode. The *track mode distortion* is often much better than *hold mode distortion*. Track mode distortion does not include nonlinearities due to the switch net-

work, and may not be indicative of the SHA performance when driving an ADC. Modern SHAs, especially high speed ones, specify distortion in both modes. While track mode distortion can be measured using an analog spectrum analyzer, hold mode distortion measurements must be performed using digital techniques as shown in Figure 8.70. A spectrally pure sinewave is applied to the SHA, and a low distortion high speed ADC digitizes the SHA output near the end of the hold time. An FFT analysis is performed on the ADC output, and the distortion components computed.

## MEASURING HOLD MODE DISTORTION

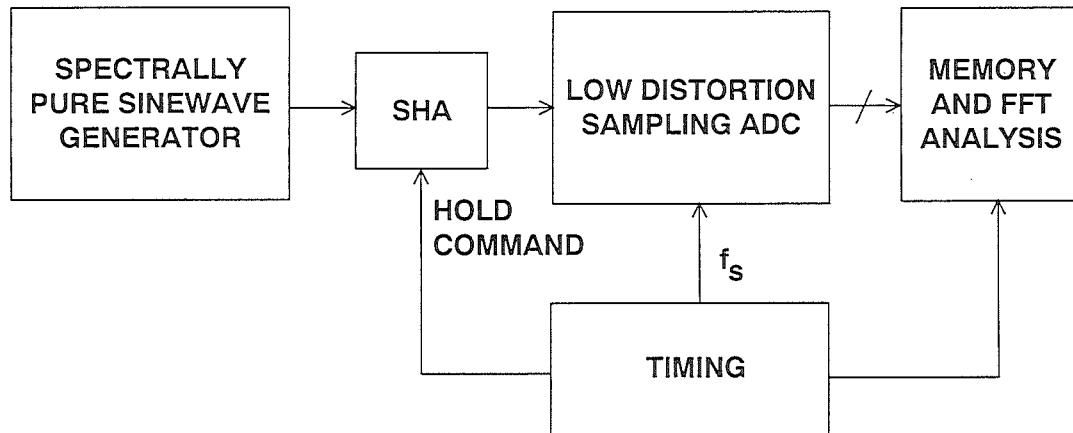


Figure 8.70

SHA *noise* in the track mode is specified and measured like that of an amplifier. Peak-to-peak *hold mode noise* is measured with an oscilloscope and converted to an rms value by dividing by 6. Hold mode noise may be given as a spectral density in  $\text{nV}/\sqrt{\text{Hz}}$ , or as an rms

value over a specified bandwidth. Unless otherwise indicated, the hold mode noise must be combined with the track mode noise to yield the total output noise. Some SHAs specify the total output hold mode noise, in which case the track mode noise is included.

## HOLD TO TRACK TRANSITION SPECIFICATIONS

When the SHA switches from hold to track, it must reacquire the input signal (which may have made a full scale transition during the hold mode). *Acquisition time* is the interval of time required for the SHA to reacquire the signal to the desired accuracy when switching from hold to track. The interval starts at the 50% point of the sampling clock edge, and ends when the SHA output voltage falls within the specified error band (usually 0.1% and 0.01% times are given). Some SHAs also specify acquisition time with respect to the voltage on the hold capacitor, neglecting the delay and settling time of the output buffer. The hold capacitor acquisition time specification

is applicable in high speed applications, where the maximum possible time must be allocated for the hold mode. The output buffer settling time must of course be significantly smaller than the hold time.

Acquisition time can be measured directly using certain sampling scope plug-ins which are insensitive to large overdrives. Figure 8.71 shows the hold capacitor acquisition time and the output acquisition time for the AD9100 30MSPS low distortion SHA. Typical acquisition time (measured at the hold capacitor) is 13ns to 0.1% and 16ns to 0.01% for a 2V step.

## ACQUISITION TIME MEASUREMENTS ON THE AD9100 30MSPS SHA

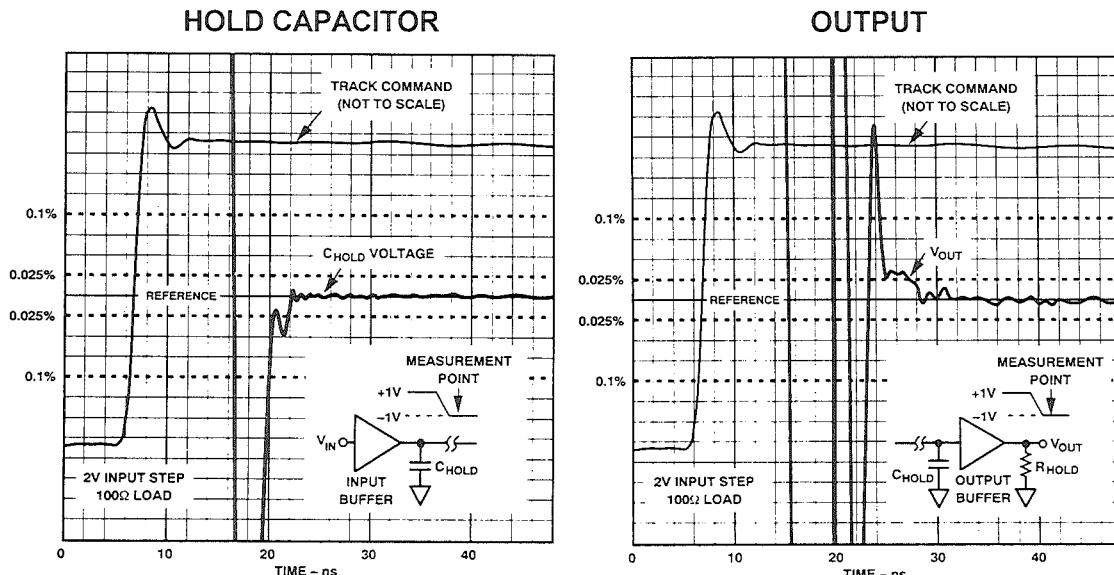


Figure 8.71

## SHA ARCHITECTURES

As with op-amps, there are numerous SHA architectures, and we will examine a few of the most popular ones. The simplest SHA structure is shown in Figure 8.72. The input signal is buffered by an amplifier and applied to the switch. The input buffer may either be open- or closed-loop and may or may not provide gain. The switch can be CMOS, FET, or bipolar (using diodes or transis-

tors) and is controlled by the switch driver circuit. The signal on the hold capacitor is buffered by an output amplifier. This architecture is sometimes referred to as *open-loop* because the switch is not inside a feedback loop. Notice that the entire signal voltage is applied to the switch, therefore it must have excellent common-mode characteristics.

### OPEN-LOOP SHA ARCHITECTURE

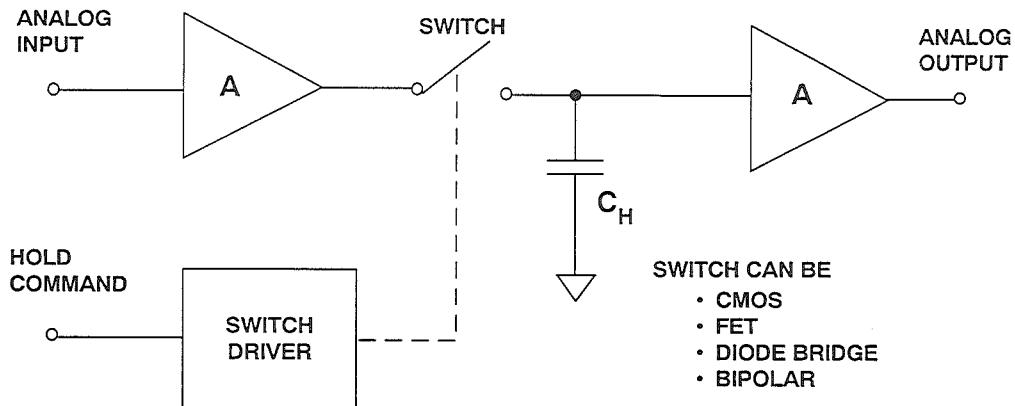


Figure 8.72

An implementation of this architecture is shown in Figure 8.73, where a diode bridge is used for the switch. Reversing the bridge drive currents reverse biases the bridge, and feedback from the

output to the bridge minimizes common-mode errors. This circuit is extremely fast, especially if the input and output buffers are open-loop followers and the diodes are Schottky ones.

## OPEN-LOOP DIODE BRIDGE SHA

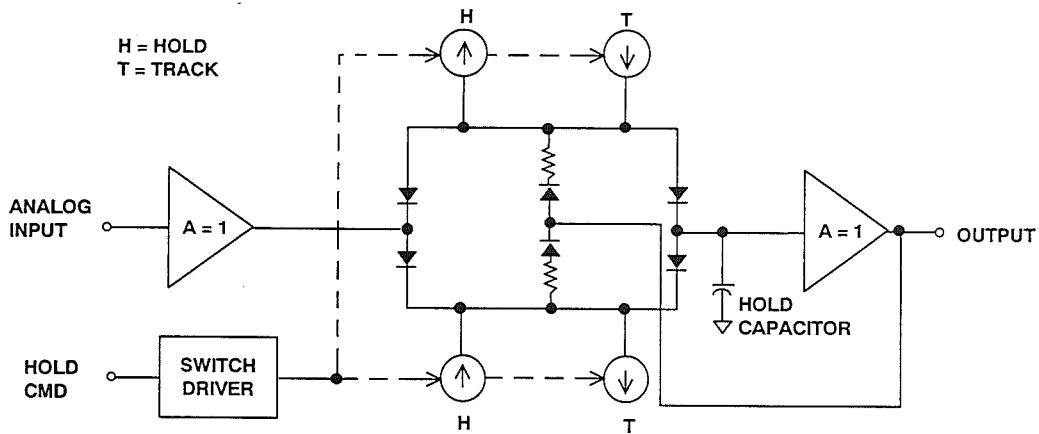


Figure 8.73

The SHA circuit shown in Figure 8.74 represents a classical *closed-loop* design and is used in many CMOS sampling ADCs. Since the switches always operate at virtual ground, there is no common-mode signal across them. Switch S2 is required in order to maintain a constant input impedance and prevent the input signal from coupling to the

output during the hold time. In the track mode, the transfer characteristic of the SHA is determined by the op-amp, and the switches do not introduce DC errors because they are within the feedback loop. The effects of charge injection can be minimized by using the differential switching techniques shown in Figure 8.75.

**CLOSED-LOOP SHA BASED ON INVERTING INTEGRATOR SWITCHED AT THE SUMMING POINT**

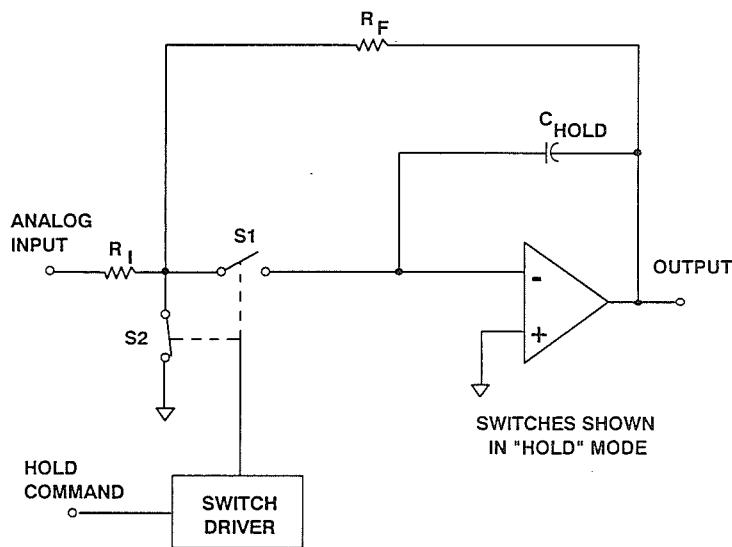


Figure 8.74

**DIFFERENTIAL SWITCHING REDUCES CHARGE INJECTION**

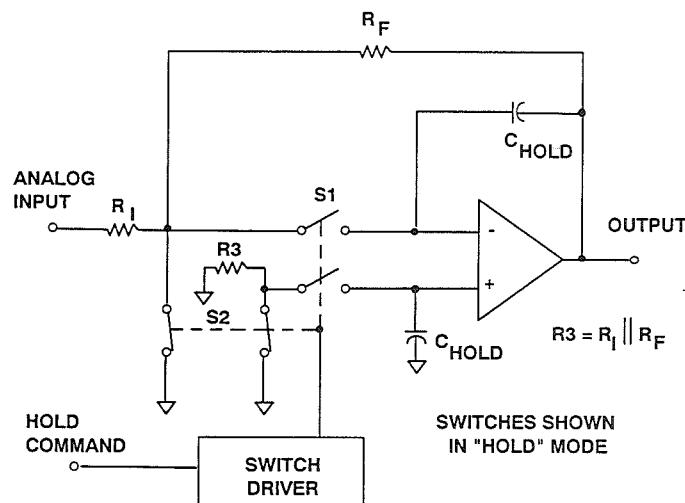


Figure 8.75

High speed sampling ADCs require fast SHAs that have low distortion and good DC characteristics. The architecture shown in Figure 8.76 utilizes closed-loop techniques on a high speed complementary-bipolar process to achieve better than 12-bit AC and DC performance. In the track mode, S1 applies the buffered input signal to the hold capacitor, and S2 provides negative feedback to the input buffer. In the hold mode, both switches are disconnected

from the hold capacitor, and negative feedback to the input buffer is supplied by S1. This architecture is implemented in SHAs such as the AD9100 and AD9101 and provides extremely low hold mode distortion by maintaining high loop gains at high frequency. The output buffer may be configured to provide voltage gain, which allows the switches to operate on lower common-mode voltage, thereby giving lower overall distortion.

### CLOSED-LOOP SHA ARCHITECTURE PROVIDES LOW DISTORTION AND HIGH SPEED (AD9100, AD9101)

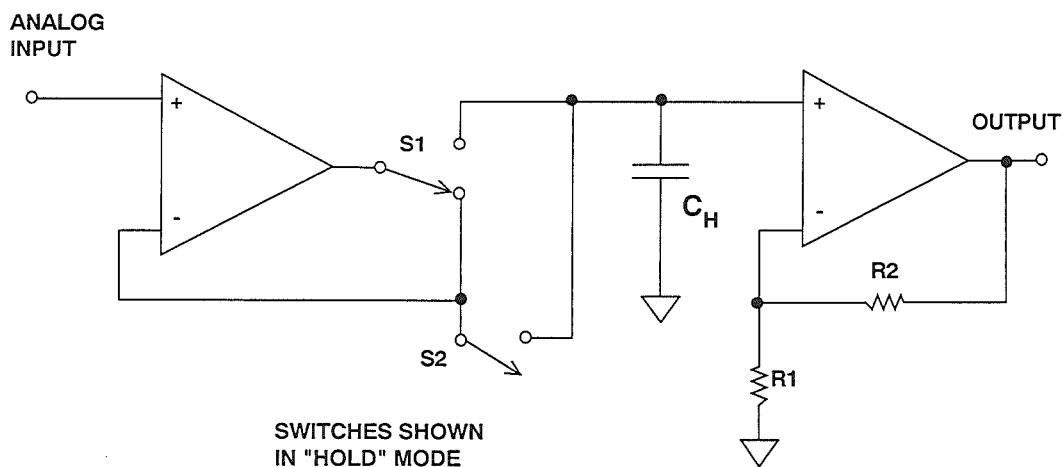


Figure 8.76

## SHA APPLICATIONS

By far the largest application of SHAs is driving ADCs. Most modern ADCs designed for signal processing are sampling ones and contain an internal SHA optimized for the converter design. Sampling ADCs are completely specified for both DC and AC performance and should be used in lieu of discrete SHA/

ADC combinations wherever possible. In a few cases, especially those requiring wide dynamic range and low distortion, there are advantages to using a discrete combination. This complex subject is discussed in more detail in Section 4 and involves many tradeoffs.

### THE ADDITION OF AN EXTERNAL WIDEBAND LOW DISTORTION SHA EXTENDS THE LOW FREQUENCY PERFORMANCE OF AN ADC TO HIGHER FREQUENCIES

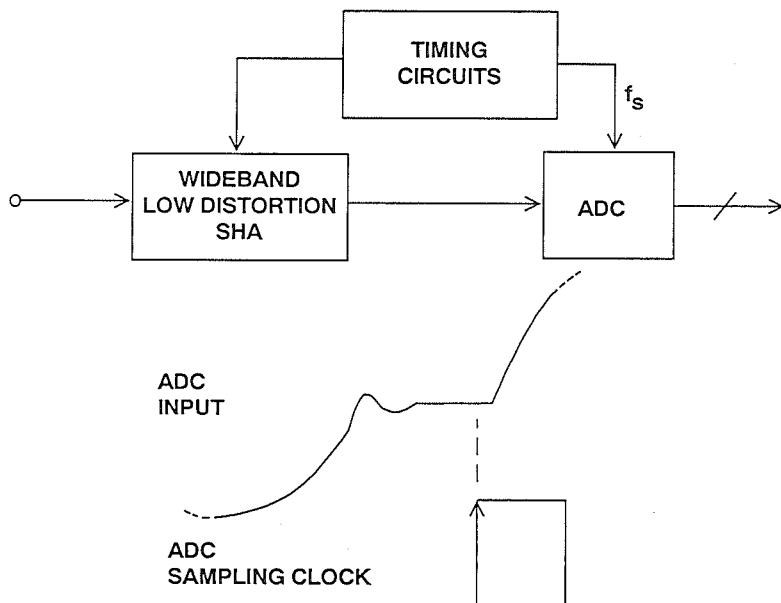


Figure 8.77

A similar application uses a low distortion SHA to minimize the effects of code-dependent DAC glitches as shown in Figure 8.78. Just prior to latching new data into the DAC, the SHA is put into the hold mode so that the DAC switching glitches are isolated from the output. The switching transients produced by the SHA are not code-depen-

dent, occur at the update frequency, and are easily filterable. This technique may be useful at low frequencies to improve the distortion performance of DACs, but has little value when using high speed low-glitch low distortion DACs designed especially for DDS applications.

## DEGLITCHING A DAC OUTPUT USING A SHA REDUCES DISTORTION CAUSED BY CODE-DEPENDENT GLITCHES

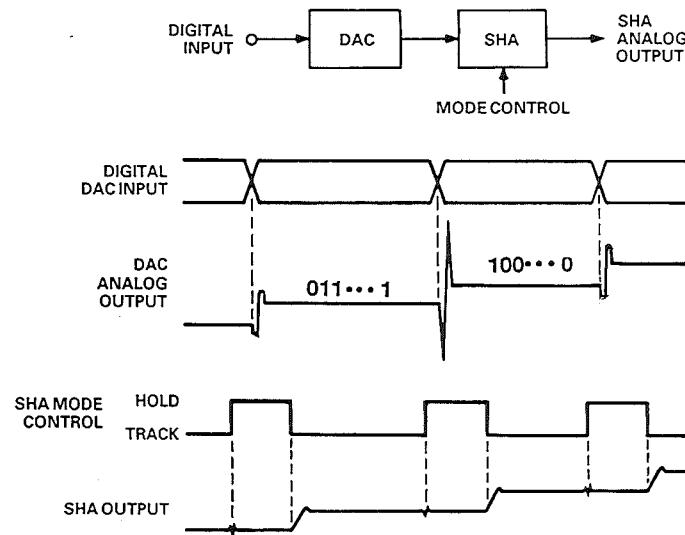


Figure 8.78

Rather than use a single ADC per channel in a simultaneous sampled system, it is often more economical to use multiple SHAs followed by an analog multiplexer and a single ADC

(Figure 8.79). Similarly, in data distribution systems multiple SHAs can be used to route the sequential outputs of a single DAC to multiple channels (Figure 8.80).

## SIMULTANEOUS SAMPLING USING MULTIPLE SHAs AND SINGLE ADC

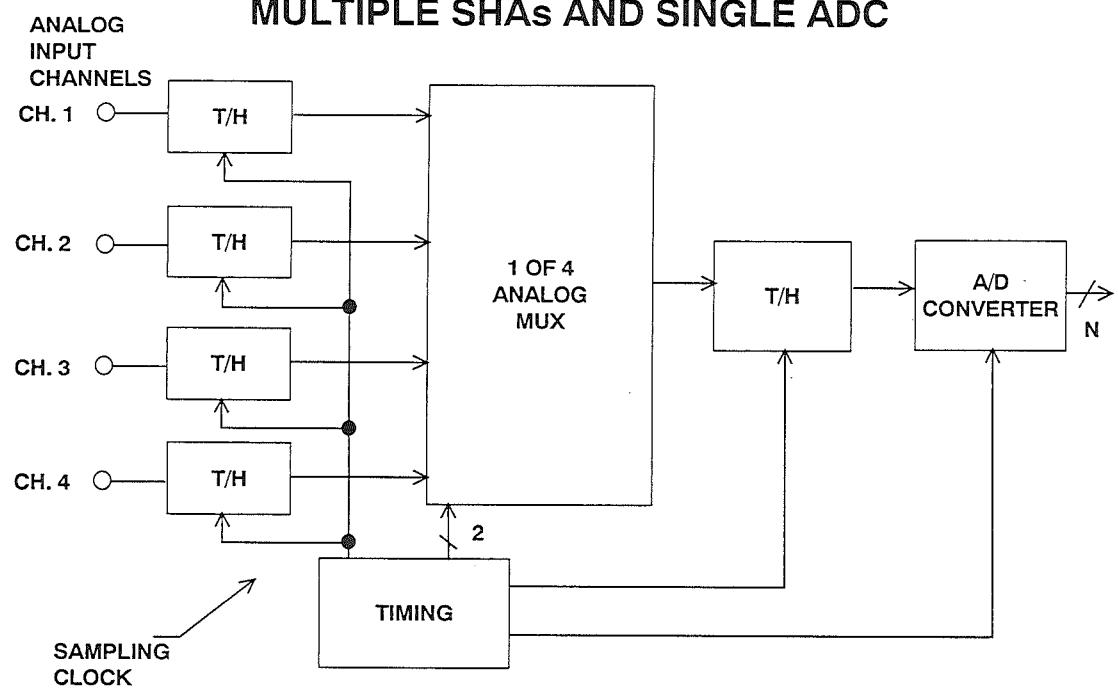


Figure 8.79

## DATA DISTRIBUTION SYSTEM USING MULTIPLE SHAs AND SINGLE DAC

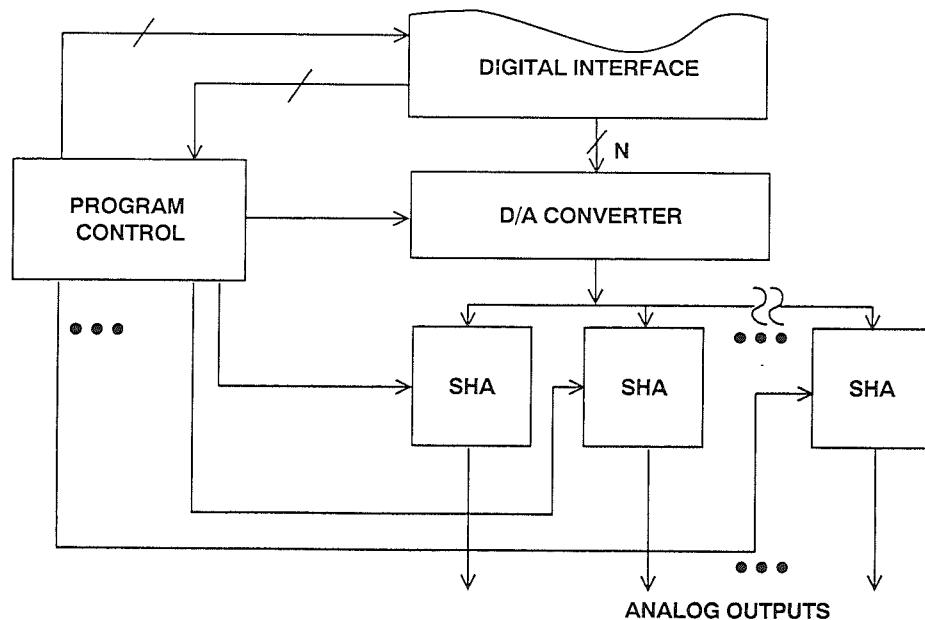


Figure 8.80

A final application for SHAs is shown in Figure 8.81, where SHAs are cascaded to produce analog delay in a sampled data system. SHA 2 is placed in hold just prior to the end of the hold interval for SHA 1. This results in a total pipe-

line delay greater than the sampling period  $T$ . This technique is often used in multi-stage subranging ADCs to allow for the conversion delays of successive stages.

### SHAs USED FOR ANALOG DELAY

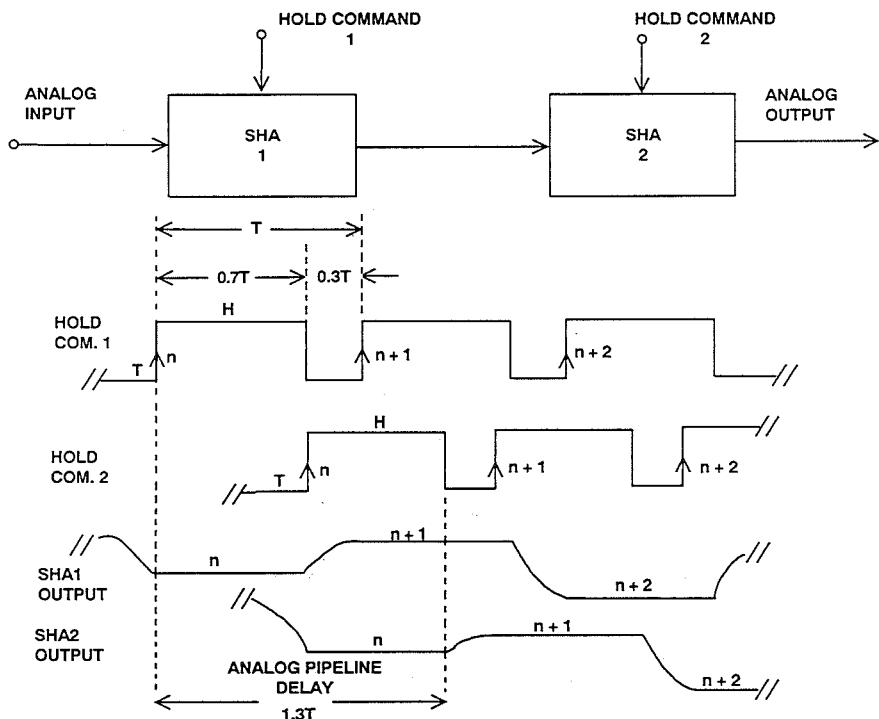


Figure 8.81

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