SECTION 7

DATA ACQUISITION SYSTEM FUNDAMENTALS

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SECTION 7

DATA ACQUISITION SYSTEM FUNDAMENTALS

Walt Kester

DATA ACQUISITION SYSTEM CONFIGURATIONS

There are many applications for data acquisition systems in measurement and process control. All data acquisition applications involve digitizing analog signals for analysis using ADCs. In a measurement application, the ADC is followed by a digital processor which performs the required data analysis. In a process control application, the process controller generates feedback signals which typically must be converted back into analog form using a DAC.

Although a single ADC digitizing a single channel of analog data constitutes a data acquisition system, the term *data acquisition* generally refers to multi-channel systems. If there is feedback from the digital processor, DACs may be required to convert the digital responses into analog. This process is often referred to as *data distribution*.

Figure 7.1 shows a data acquisition/distribution process control system where each channel has its own dedicated ADC and DAC. An alternative configuration is shown in Figure 7.2, where analog multiplexers and demultiplexers are used with a single ADC and DAC. In most cases, especially where there are many channels, this configuration provides an economical alternative.

DATA ACQUISITION SYSTEM USING ADC/DAC PER CHANNEL

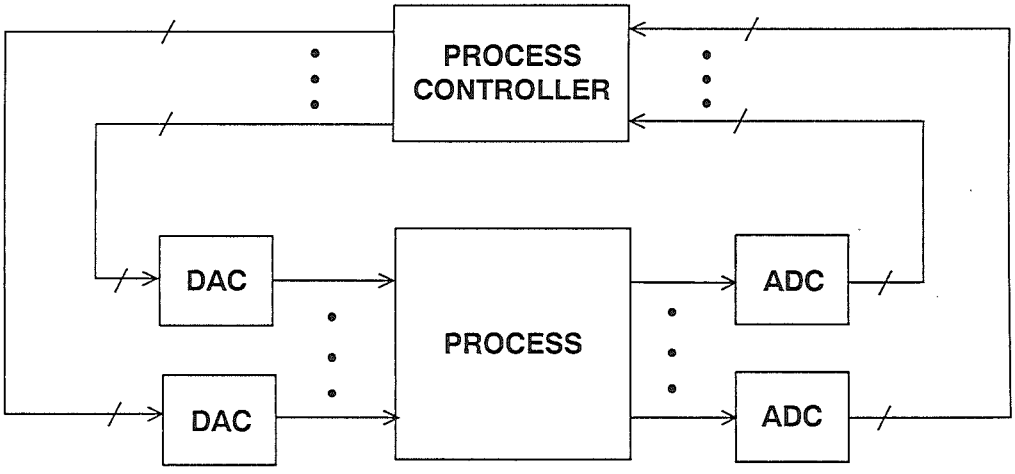


Figure 7.1

DATA ACQUISITION SYSTEM USING ANALOG MULTIPLEXING/DEMULTIPLEXING AND SINGLE ADC/DAC

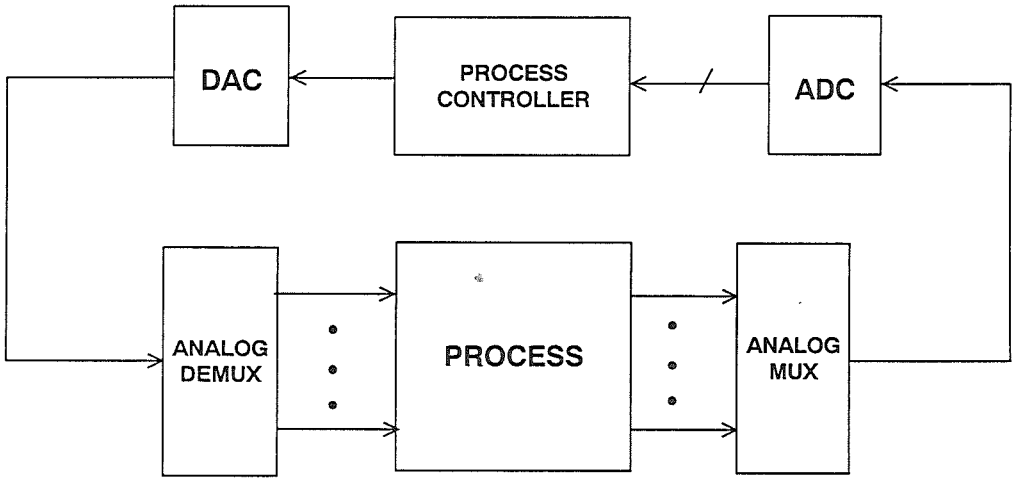


Figure 7.2

There are many tradeoffs involved in designing a data acquisition system. Issues such as filtering, amplification, multiplexing, demultiplexing, sampling frequency, and partitioning must be resolved.

MULTIPLEXING

Multiplexing is a fundamental part of a data acquisition system. Multiplexers and switches are examined in more detail in Section 8, but a fundamental understanding is required to design a data acquisition system. A simplified diagram of an analog multiplexer is shown in Figure 7.3. The number of input channels typically ranges from 4 to 16, and the devices are generally fabricated on CMOS processes. The key specifications are *switching time*, *on-resistance*, *on-resistance modulation*, and *off-channel isolation (crosstalk)*. Multiplexer switching time ranges from about 50ns to over 1μs, on-resistance from 25 to several hundred ohms, and off-channel isolation from 50 to 90dB. Some multiplexers have internal channel-address decoding logic and registers, while with others, these functions must be performed externally. Unused multiplexer inputs *must* be grounded or severe loss of system accuracy may result.

SIMPLIFIED DIAGRAM OF A TYPICAL ANALOG MULTIPLEXER

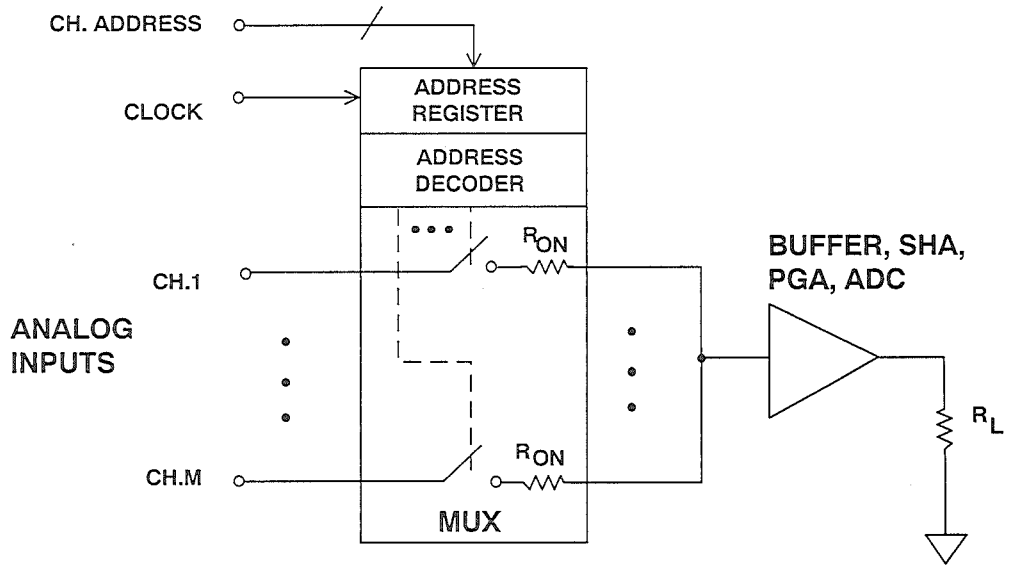
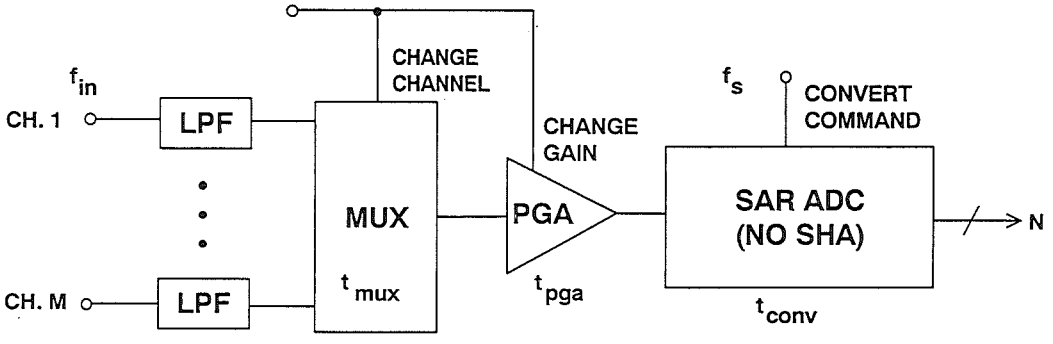


Figure 7.3

Multiplexer on-resistance is generally slightly dependent on the signal level (often called R_{on} modulation). This will cause signal distortion if the multiplexer must drive a load resistance, therefore the multiplexer output should therefore be isolated from the load with a suitable buffer amplifier. A separate buffer is not required if the multiplexer drives a high input impedance, such as a PGA, SHA or ADC - but beware! Some SHAs and ADCs draw high frequency pulse current at their sampling rate and cannot tolerate being driven by an unbuffered multiplexer.

An M-channel multiplexed data acquisition system is shown in Figure 7.4. The multiplexer output drives a PGA whose gain can be adjusted on a per-channel basis depending on the channel signal level. This ensures that all channels utilize the full dynamic range of the ADC. The PGA gain is changed at the same time as the multiplexer is switched to a new channel. The ADC *Convert Command* is applied after the multiplexer and the PGA have settled to the required accuracy (1LSB). The maximum sampling frequency (when switching between channels) is limited by the multiplexer switching time t_{mux}, the PGA settling time t_{pga}, and the ADC conversion time t_{conv} as shown in the formula.

MULTIPLEXED DATA ACQUISITION SYSTEM WITH PGA AND SAR ADC



- $f_s \leq \dfrac{1}{t_{conv} + \sqrt{t_{mux}^2 + t_{pga}^2}}$
- $f_{in} \leq \dfrac{1}{\pi 2^N \cdot t_{conv}}$
- Example: If N = 12 and t_{conv} = 20μsec,

  Then f_{in} ≤ 4Hz!!!!

Figure 7.4

In a multiplexed system it is possible to have a positive fullscale signal on one channel and a negative fullscale signal on the other. When the multiplexer switches between these channels its output is a fullscale step voltage. All elements in the signal path must settle to the required accuracy (1LSB) before the conversion is made. The effect of inadequate settling is dc crosstalk between channels.

The SAR ADC chosen in this application has no internal SHA (similar to the industry-standard AD574-series), and therefore the input signal must be held constant (within 1LSB) during the conversion time in order to prevent encoding errors. This defines the maximum rate-of-change of the input signal:

$$\left.\frac{dv}{dt}\right|_{max} \leq \frac{1\ LSB}{t_{conv}}$$

The amplitude of a fullscale sinewave input signal is equal to $2^N/2$, or $2^{(N-1)}$, and its maximum rate-of change is

$$\left.\frac{dv}{dt}\right|_{max} = 2\pi f_{max} \cdot 2^{N-1} = \pi f_{max} \cdot 2^N$$

Setting the two equations equal, and solving for f_{max},

$$f_{max} \leq \frac{1}{\pi \cdot 2^N t_{conv}}$$

For example, if the ADC conversion time is 20μsec (corresponding to a maximum sampling rate of slightly less than 50kSPS), and the resolution is 12-bits, then the maximum channel input signal frequency is limited to 4Hz. This may be adequate if the signals are DC, but the lack of a SHA function severely limits the ability to process dynamic signals.

Adding a SHA function to the ADC as shown in Figure 7.5 allows processing of much faster signals with almost no increase in system complexity, since sampling ADCs such as the AD1674 have the SHA function on-chip.

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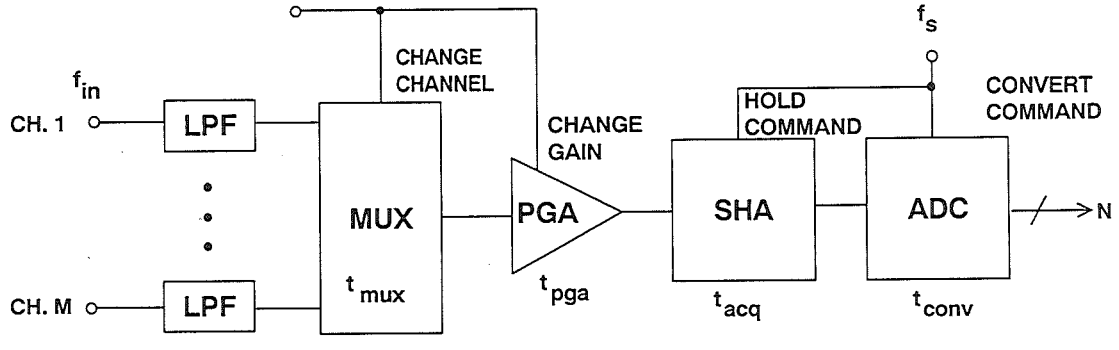
THE ADDITION OF A SHA FUNCTION TO THE ADC ALLOWS PROCESSING OF DYNAMIC INPUT SIGNALS



- In General, $\sqrt{t_{mux}^2 + t_{pga}^2} \ll t_{acq} + t_{conv}$
- Therefore, $f_S \leq \frac{1}{t_{acq} + t_{conv}}$
- Example: If $t_{acq} = 1\mu sec$, $t_{conv} = 9\mu s$, then $f_S \leq 100kSPS$

  Then $f_{in} \leq f_S/2M$

Figure 7.5

TYPICAL TIMING DIAGRAM FOR MULTIPLEXED DATA ACQUISITION SYSTEM USING SHA

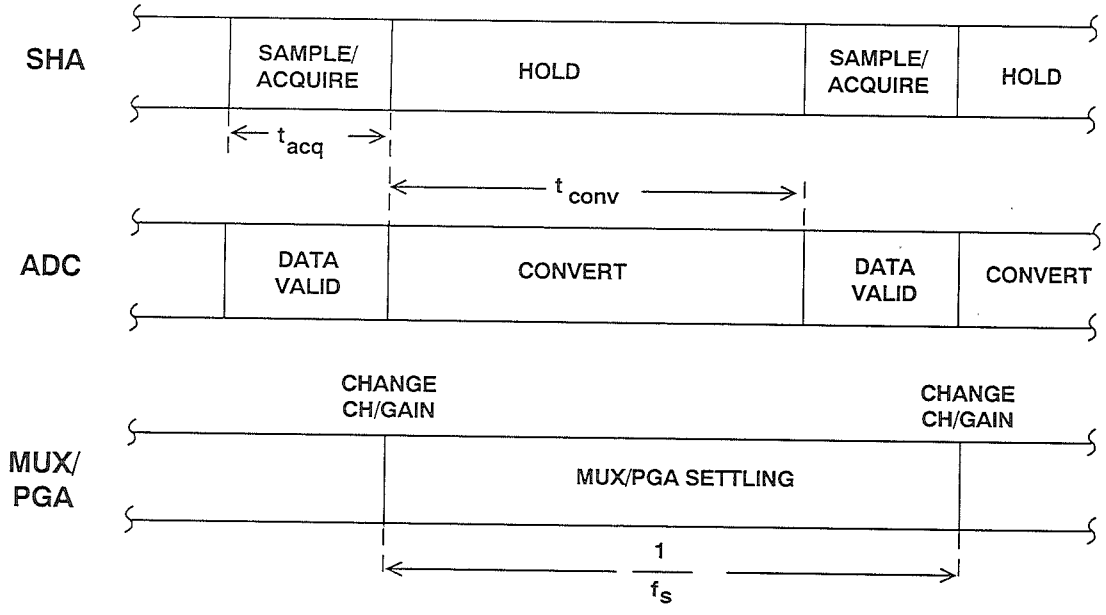


Figure 7.6

The timing is adjusted such that the multiplexer and the PGA are switched immediately following the acquisition time of the SHA. If the combined multiplexer and PGA settling time is less than the ADC conversion time (see Figure 7.6), then the maximum sampling frequency of the system is given by:

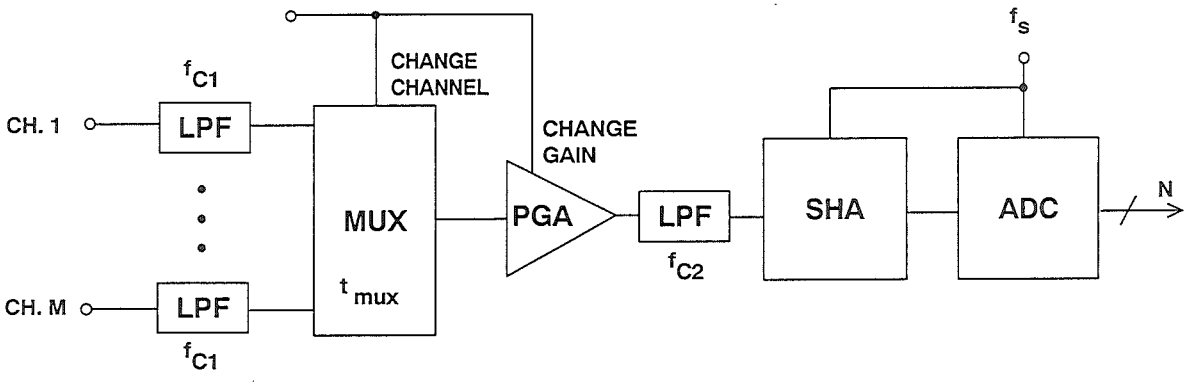
$$f_S \leq \frac{1}{t_{acq} + t_{conv}}$$

The AD1674 has a conversion time of 9μs, an acquisition time of 1μs to 12-bits, and a sampling rate of 100kSPS is possible. If all the channels are addressed. The per-channel sampling rate is obtained by dividing the ADC sampling rate by M.

FILTERING CONSIDERATIONS IN DATA ACQUISITION SYSTEMS

Filtering in data acquisition systems not only prevents aliasing of unwanted signals but also reduces noise by limiting bandwidth. In a multiplexed system, there are basically two places to put filters: in each channel, and at the multiplexer output.

FILTERING IN A DATA ACQUISITION SYSTEM



For Sequential Sampling, $f_{C1} < \frac{f_S}{M}$

Figure 7.7

The filter at the input of each channel is used to prevent aliasing of signals which fall outside the Nyquist bandwidth. The per-channel sampling rate (assuming each channel is sampled at the same rate) is f_S/M, and the corresponding Nyquist frequency is $f_S/2M$. The filter should provide sufficient attenuation at $f_S/2M$ to prevent dynamic range limitations due to aliasing. Specifying this filter is discussed in detail in Section 4.

A second filter can be placed in the signal path between the multiplexer output and the ADC, usually between the PGA and the SHA. The cutoff frequency of this filter must be carefully chosen because of its impact on settling time. In a multiplexed system such as shown in Figure 7.7, there can be a fullscale step voltage change at the multiplexer output when it is switched between channels. This occurs if the signal on one channel is positive

fullscale, and the signal on the adjacent channel is negative fullscale. From the timing diagram shown in Figure 7.6, the signal from the filter has essentially the entire conversion period ($1/f_S$) to settle from the step voltage. The signal should settle to within 1LSB of the final value in order not to introduce a significant error. The settling time requirement therefore places a lower limit on the filter's cutoff frequency. The single-pole filter settling time required to maintain a given accuracy is shown in Figure 7.8. The settling time requirement is expressed in terms of the filter time constant and also the ratio of the filter cutoff frequency, f_{c2},to the ADC sampling frequency, f_S.

SINGLE-POLE FILTER SETTLING TIME TO REQUIRED ACCURACY

RESOLUTION, # OF BITS	LSB (%FS)	# OF TIME CONSTANTS	f_{c2}/f_S
6	1.563	4.16	0.67
8	0.391	5.55	0.89
10	0.0977	6.93	1.11
12	0.0244	8.32	1.32
14	0.0061	9.70	1.55
16	0.00153	11.09	1.77
18	0.00038	12.48	2.00
20	0.000095	13.86	2.22
22	0.000024	15.25	2.44

Figure 7.8

As an example, assume that the ADC is a 12-bit one sampling at 100kSPS. From the table in Figure 7.8, 8.32 time constants are required for the filter to settle to 12-bit accuracy, and

$$\frac{f_{c2}}{f_S} \geq 1.32, \text{ or}$$

$$f_{c2} \geq 132\text{kSPS}.$$

While this filter will help prevent wideband noise from entering the SHA, it does not provide the same function as the antialiasing filters at the input of each channel.

The above analysis assumes that the multiplexer/PGA combined settling time is significantly less than the filter settling time. If this is not the case, then the filter cutoff frequency must be larger, and in most cases it should be left out entirely in favor of per-channel filters.

SHA AND ADC SETTLING TIME REQUIREMENTS IN MULTIPLEXED APPLICATIONS

We have discussed the importance of the fullscale settling time of the multiplexer/PGA/filter combination, but what is equally important is the ability of the ADC to acquire the final value of the step voltage input signal to the required accuracy. Failure of any link in the signal chain to settle will result in dc crosstalk between adjacent channels and loss of accuracy. If the data acquisition system uses a separate SHA and ADC, then the key specification to examine is the SHA acquisition time, which is usually specified as a the amount of time required to acquire a fullscale input signal to 0.1% accuracy (10-bits) or 0.01% accuracy (13-bits). In most cases, both 0.1% and 0.01% times are specified. If the SHA acquisition time is not specified for 0.01% accuracy or better, it should not be used in a 12-bit multiplexed application.

If the ADC is a sampling one (with internal SHA), the SHA acquisition time required to achieve a level of accuracy may still be specified, as in the case of the AD1674 (1μs to 12-bit accuracy). SHA acquisition time and accuracy are not directly specified for some sampling ADCs, so the transient response specification should be examined. The transient response of the ADC (settling time to within 1 LSB for a fullscale step input) must be less than $1/f_S$, where fs is the ADC sampling rate. This often ignored specification may become the weakest link in the signal chain. In some cases neither the SHA acquisition time to specified accuracy nor the transient response specification may appear on the data sheet for the particular ADC, in which case it is probably not acceptable for multiplexed applications. Because of the difficulty in measuring and achieving better than 12-bit settling times using discrete components, the accuracy of most multiplexed data acquisition systems is limited to 12-bits. Designing multiplexed systems with greater accuracy is extremely difficult, and using a single ADC per channel should be strongly considered at higher resolutions.

SHA AND ADC CONSIDERATIONS IN MULTIPLEXED DATA ACQUISITION SYSTEMS

- Examine SHA Acquisition Time Specification to Required Accuracy :

  0.1% = 10-bits

  0.01% = 13-bits

- If Sampling ADC, SHA Acquisition Time may not be given, so examine Transient Response Specification
- Inadequate Settling Results in Loss of Accuracy and Causes DC Crosstalk Between Channels
- Multiplexing at greater than 12-bits Accuracy, or at Video Speeds is Extremely Difficult!

Figure 7.9

COMPLETE DATA ACQUISITION SYSTEMS ON A CHIP

VLSI mixed-signal processing allows the integration of large and complex data acquisition circuits on a single chip. Most signal conditioning circuits including multiplexers, PGAs, and SHAs, may now be manufactured on the same chip as the ADC. This high level of integration permits data acquisition systems to be specified and tested as a single complex function.

Such functionality relieves the designer of most of the burden of testing and calculating error budgets. The DC and AC characteristics of a complete data acquisition system are specified as a complete function, which removes the necessity of calculating performance from a collection of individual worst case device specifications. A complete monolithic system should achieve a higher performance at much lower cost than would be possible with a system built up from discrete functions. Furthermore, system calibration is easier and in fact many monolithic DASs are self calibrating.

With these high levels of integration, it is both easy and inexpensive to make many of the parameters of the device programmable. Parameters which can be programmed include gain, filter cutoff frequency, and even ADC resolution and conversion time, as well as the obvious digital/MUX functions of input channel selection, output data format, and unipolar/bipolar range.

The AD7890 is an example of a highly integrated monolithic data acquisition system. It has 8 multiplexed input channels, a SHA amplifier, an internal voltage reference, and a fast 12-bit

ADC. Input scaling allows up to ±10V inputs when operating on a single +5V supply. Its block diagram is shown in Figure 7.10, and key specifications are summarized in Figure 7.11. Both AC and DC parameters are fully specified, simplifying the preparation of an error budget, and three types are available with three different standard input ranges:-

AD7890-10	±10 V
AD7890-5	0 to 5V
AD7890-2	0 to +2.5V

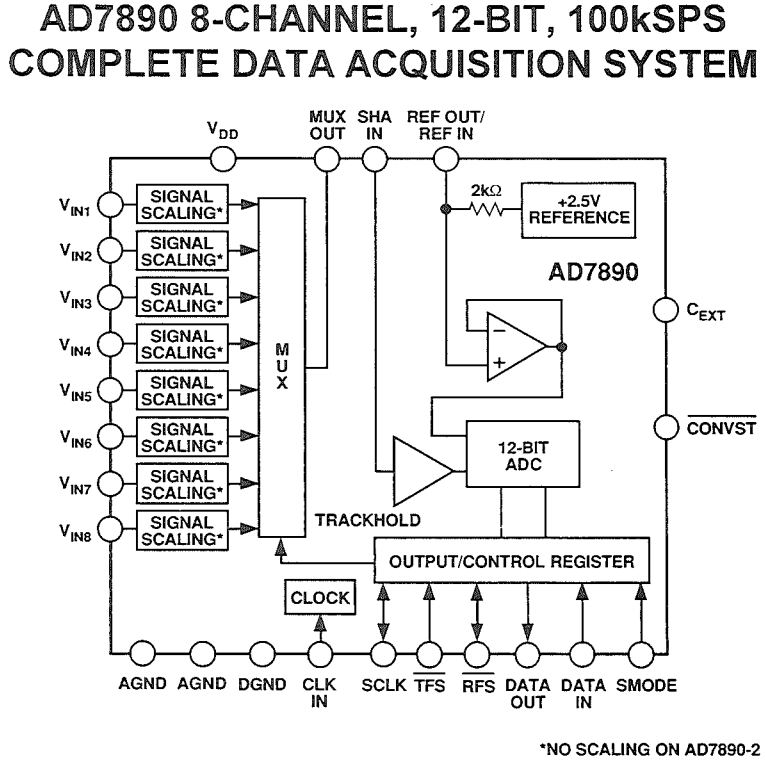


Figure 7.10

AD7890 SPECIFICATIONS

- ADC Conversion Time: 5.9µs
- SHA Acquisition Time: 2µs
- 117kSPS Throughput Rate (Includes 0.6µs Overhead)
- AC and DC Specifications
- Single +5V Operation
- Low Power Drain:
  - Operational: 30mW
  - Power Down Mode: 1mW
- Standard Input Ranges:
  - AD7890 - 10: ± 10V
  - AD7890 - 5: 0 to +5V
  - AD7890 - 2: 0 to +2.5V

Figure 7.11

The input channel selection is via a serial input port. A total of 5 bits of data control the AD7890 via a serial port:- 3 address bits select the input channel, a CONV bit starts the A-D conversion, and 1 in the STBY register places the device in a power-down mode where its power consumption is under 1mW. All timing takes place on the chip and a single external capacitor controls the acquisition time of the internal track-and-hold. A-D conversion may also be initiated externally using the $\overline{\text{CONVST}}$ pin.

With the serial clock rate at its maximum of 10MHz, the achievable throughput rate for the AD7890 is 5.9μs (conversion time) plus 0.6μs (six serial clocks of internal overhead) plus 2μs (acquisition time). This results in a minimum throughput time of 8.5μs (equivalent to a throughput rate of 117kSPS). The AD7890 draws 30mW from a +5V supply.

MULTIPLEXING INPUTS TO SIGMA-DELTA ADCS

As was discussed in Section 5, the digital filter is an integral part of a sigma-delta ADC. If the inputs to a sigma-delta ADC are switched using a multiplexer, the digital filter must be allowed to settle before valid data is available. As an example, the AD7710-family of ADCs contains an on-chip multiplexer (see Figure 7.12 and Figure 7.13), and the digital filter (frequency response shown in Figure 7.13) requires three conversion cycles (300ms at a 10Hz throughput rate) to settle. It is thus possible to multiplex sigma-delta converters, provided adequate time is allowed for the internal digital filter to settle.

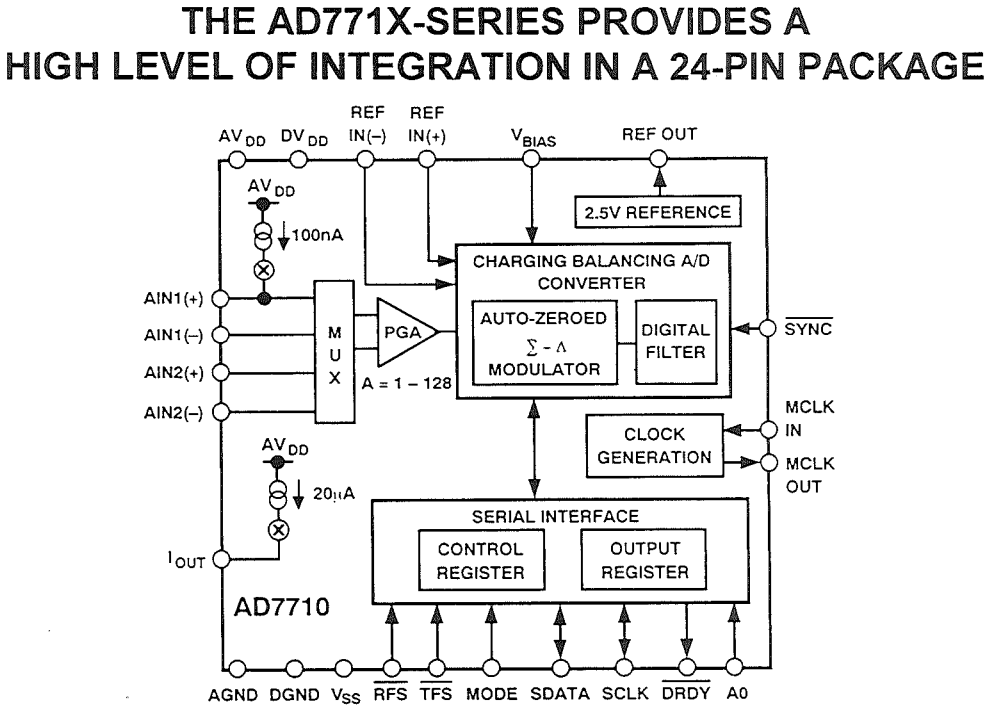


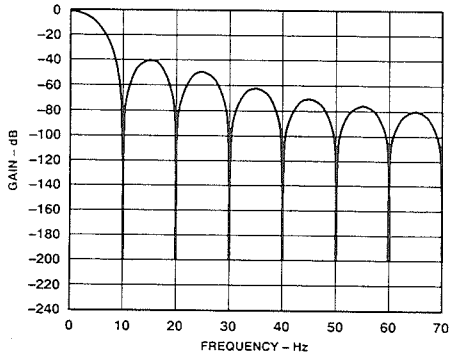
Figure 7.12

KEY FEATURES OF THE AD7710

- ±0.0015% Nonlinearity
- Two Channels with Differential Inputs
- Programmable Gain Amplifier (G = 1 to 128)
- Programmable Low Pass Filter
- System or Self-Calibration Option
- Single or Dual 5V Supply Operation
- Microcontroller Serial Interface

Figure 7.13

AD7710 DIGITAL FILTER FREQUENCY RESPONSE



- Response Follows a $\text{sinc}^3 = \left(\frac{\sin x}{x}\right)^3$
- First Notch Frequency is Programmable and given by:

$$f_{notch} = \left(\frac{f_{clkin}}{512}\right)\left(\frac{1}{\text{Decimal Value of Digital Code}}\right)$$

- For f_{clkin} = 10MHz, 9.76Hz ≤ f_{notch} ≤ 1.028kHz

Figure 7.14

If sigma-delta ADCs are used in multi-channel applications, consider using one sigma-delta ADC per channel. Products such as the AD7716 (see Figure 7.15) make this approach attractive. The AD7716 is a quad sigma-delta ADC with up to 22-bit resolution and an over-sampling rate of 570kSPS. A functional diagram of the AD7716 is shown in Figure 7.15 and some of its key features in Figure 7.16. The device does not have a "start conversion" control input, but samples continuously. The cutoff frequency of the digital filters (which may be changed during operation, but only at the cost of a loss of valid data for a short time while the filters clear) is programmed by data written to the DAS. The output register is updated at a rate which depends on the cutoff frequency chosen. The AD7716 contains an auto-zeroing system to minimize input offset drift.

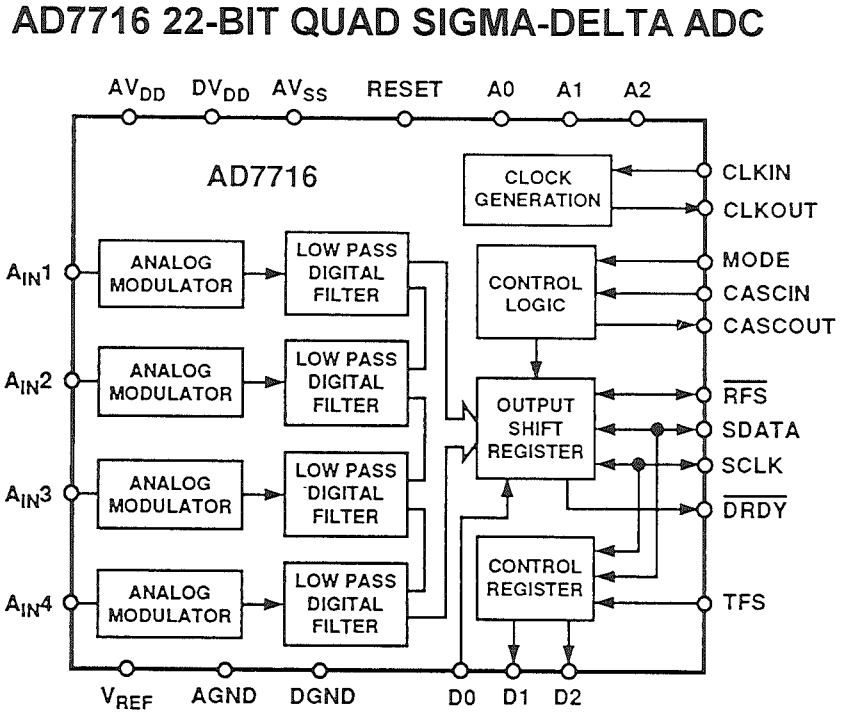


Figure 7.15

AD7716 QUAD SIGMA-DELTA ADC KEY FEATURES

- Up to 22-Bit Resolution, 4 Input Channels
- ΣΔ Architecture, 570kSPS Oversampling Rate
- On-Chip Lowpass Filter, Programmable from 36.5Hz to 584Hz
- Serial Input / Output Interface
- ±5V Power Supply Operation
- Low Power: 50mW

Figure 7.16

SIMULTANEOUS SAMPLING SYSTEMS

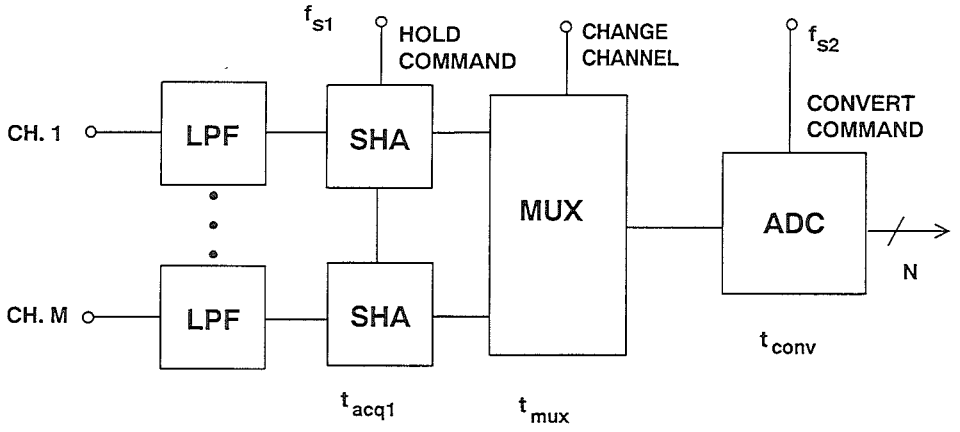
There are certain applications where it is desirable to sample a number of channels simultaneously such as in-phase and quadrature (I and Q) signal processing. A typical configuration is shown in Figure 7.17. Each channel requires its own filter and SHA. Each SHA is simultaneously placed in the hold mode by a common command signal. During the input SHAs' hold time the multiplexer is sequentially switched from channel to channel, and the single non-sampling ADC is used to digitize the signal on each channel. The maximum ADC sampling rate is the reciprocal of the sum of the multiplexer settling time, t_{mux}, and the ADC conversion time, t_{conv}.

$$f_{s2} \leq \frac{1}{t_{mux} + t_{conv}}$$

The maximum per-channel sampling frequency is determined by M, t_{mux}, t_{conv}, and the acquisition time of the simultaneous SHAs, t_{acq1}.

$$f_{s1} \leq \frac{1}{t_{acq1} + M(t_{mux} + t_{conv})}$$

SIMULTANEOUSLY SAMPLED DATA ACQUISITION SYSTEM USING NON-SAMPLING ADC



$$f_{S2} \leq \frac{1}{t_{mux} + t_{conv}}$$

$$f_{S1} \leq \frac{1}{t_{acq1} + M(t_{mux} + t_{conv})}$$

Figure 7.17

7

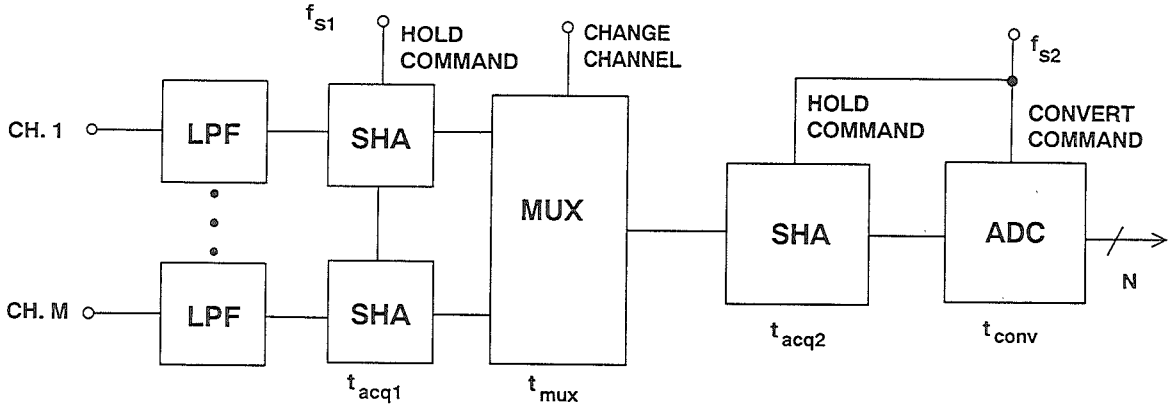
If a sampling ADC is used to perform the conversion (see Figure 7.18), the acquisition time of the second SHA, t_{acq2}, must be considered in determining the maximum ADC sampling rate, f_{s2}. The multiplexer should be switched to the next channel after the single SHA goes into the hold mode. If the multiplexer settling time is less than the ADC conversion time, then the maximum ADC sampling rate f_{s2} is the reciprocal of the sum of the SHA acquisition time and the ADC conversion time.

$$f_{s2} \leq \frac{1}{t_{acq2} + t_{conv}}$$

The maximum input sampling frequency is less than this value divided by M, where M is the number of channels. Additional timing overhead (t_{acq1}) is required for the simultaneous SHAs to acquire the signals.

$$f_{s1} < \frac{1}{t_{acq1} + M(t_{conv} + t_{acq2})}$$

SIMULTANEOUSLY SAMPLED DATA ACQUISITION SYSTEM USING SAMPLING ADC



$$f_{S2} \leq \frac{1}{t_{acq2} + t_{conv}}$$

$$f_{S1} \leq \frac{1}{t_{acq1} + M(t_{acq2} + t_{conv})} = \frac{1}{t_{acq1} + \frac{M}{f_{S2}}}$$

Assuming $t_{mux} < t_{acq2} + t_{conv}$

Figure 7.18

DATA DISTRIBUTION SYSTEMS USING DACS

The simplest method to distribute data in a multi-channel data acquisition system is to use a single DAC per channel as shown in Figure 7.19. The process controller digitally demultiplexes the data for each channel and presents it in parallel format to each DAC. Each DAC is followed by a lowpass antialiasing filter.

An alternate approach is shown in Figure 7.20 where a single DAC output is applied to the input of multiple SHAs. The timing circuits provide the hold commands sequentially to the individual SHAs as the DAC output is updated. Timing is adjusted so that each SHA enters the hold-mode near just prior to the DAC update.

If this approach is used with a large number of channels, the SHA hold time may become large enough so that SHA droop introduces errors in the outputs. In this case, the multiple DAC approach shown in Figure 7.19 should be used.

DATA DISTRIBUTION SYSTEM USING MULTIPLE DACs

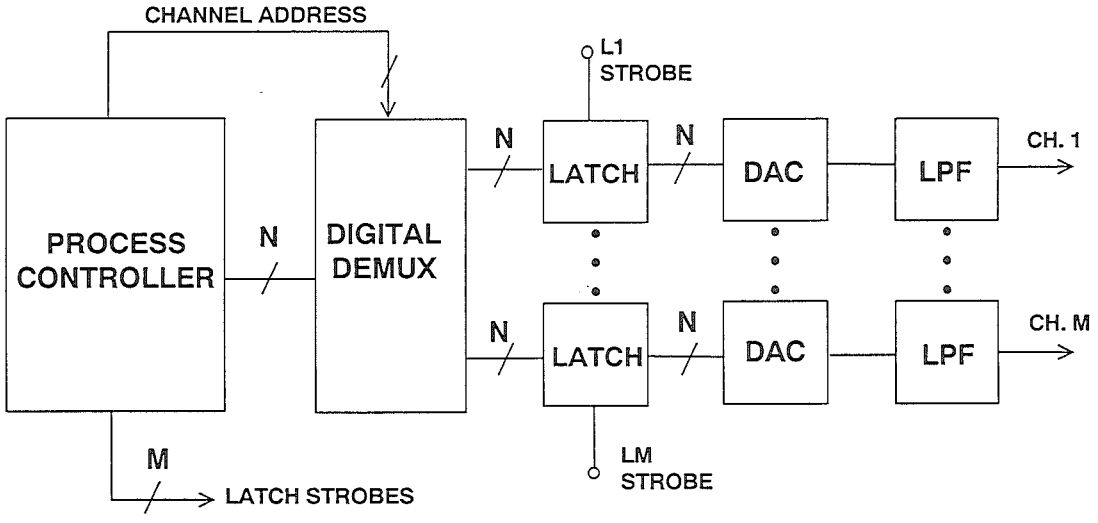


Figure 7.19

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DATA DISTRIBUTION SYSTEM USING SINGLE DAC WITH MULTIPLE SHAs

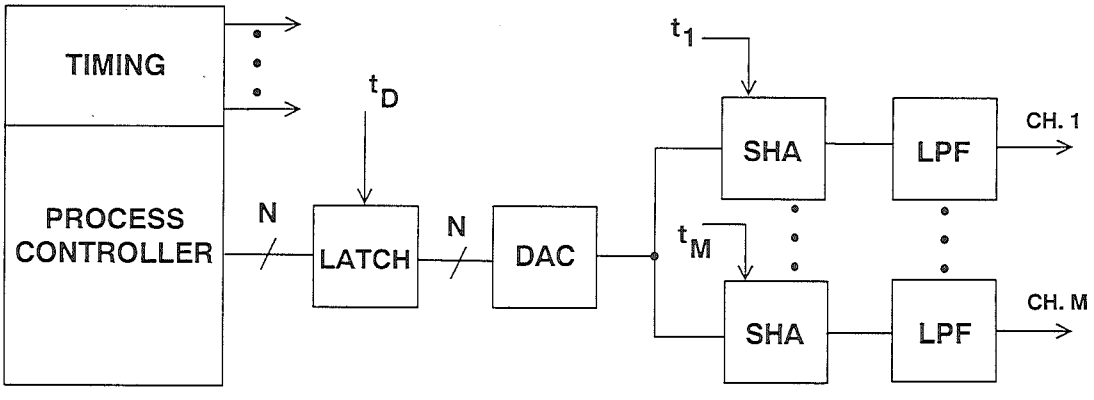

Figure 7.20

REFERENCE

Dan Sheingold, **Analog-Digital Conversion Handbook, Third Edition,** Prentice-Hall, 1986.