

SECTION 4

SAMPLED DATA SYSTEMS

- Discrete Time Sampling of Analog Signals
- Specifying the ADC Sampling Rate and the Antialiasing Filter
- ADC Resolution and Dynamic Range Requirements
- Undersampling (Super-Nyquist)

SECTION 4

SAMPLED DATA SYSTEMS

Walt Kester

Designing a signal processing system is a challenge which involves many tradeoffs. We have discussed signal amplification in detail and explored many of the various options available. When selecting the ADC, you must continue to keep the goal of preserving signal fidelity and dynamic range in mind, while resisting the temptation to overspecify. Overspecifying the ADC, its antialiasing filter, and other peripheral circuitry is especially dangerous, because it may result in high cost and even unrealizable component requirements. In order to specify intelligently the ADC portion of the system, one

must first understand the fundamental concepts of sampling and quantization and their effects on the signal.

We will first consider the traditional problem of sampling and quantizing a *baseband* signal whose bandwidth lies between dc and an upper frequency of interest, f_s . This is often referred to as *Nyquist, or Sub-Nyquist Sampling*. The topic of *Super-Nyquist* sampling (sometimes called *undersampling*) where the signal of interest falls outside of the Nyquist bandwidth (dc to $f_s/2$) is treated later in this section.

4

KEY ELEMENTS OF A BASEBAND SAMPLED DATA SYSTEM

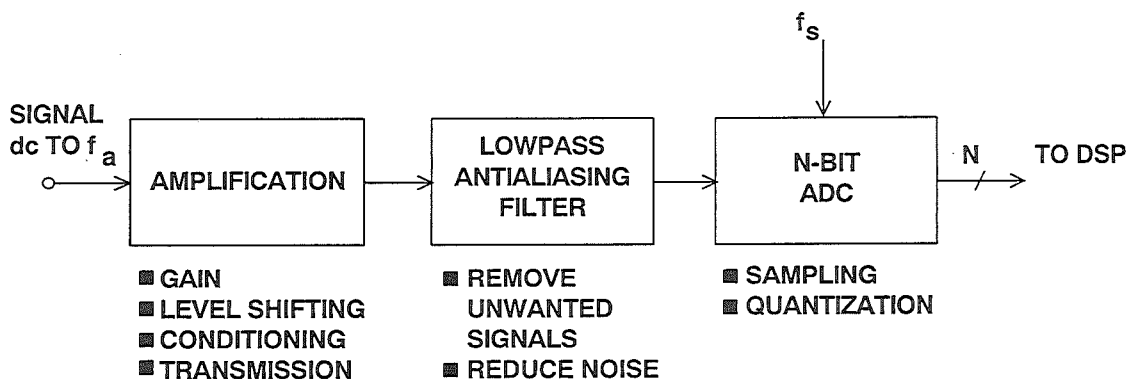


Figure 4.1

DISCRETE TIME SAMPLING OF ANALOG SIGNALS

The concept of discrete time and amplitude sampling of an analog signal is shown in Figure 4.2. The continuous analog data must be sampled at discrete intervals, t_s , which must be carefully chosen to insure an accurate representation of the original analog signal. It is clear that the more samples taken (faster sampling rates),

the more accurate the digital representation, but if fewer samples are taken (lower sampling rates), a point is reached where critical information about the signal is actually lost. This leads us to the statement of Shannon's Information Theorem and Nyquist's Criteria given in Figure 4.3.

SAMPLING AND QUANTIZING AN ANALOG SIGNAL

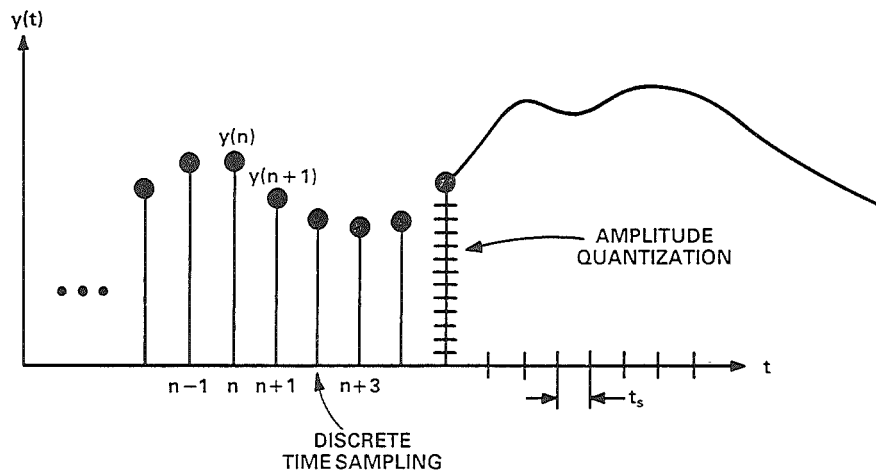


Figure 4.2

SHANNON'S INFORMATION THEOREM AND NYQUIST'S CRITERIA

■ Shannon:

- ◆ An Analog Signal with a *Bandwidth* of f_a Must be Sampled at a Rate $f_s > 2f_a$ in Order to Avoid the Loss of Information.
- ◆ The signal bandwidth may extend from DC to f_a (*Baseband Sampling*) or from f_1 to f_2 , where $f_a = f_2 - f_1$ (*Undersampling, or Super-Nyquist*)

■ Nyquist:

- ◆ If $f_s < 2f_a$, then a Phenomena Called *Aliasing* Will Occur.
- ◆ *Aliasing* is used to advantage in undersampling applications.

Figure 4.3

In order to understand the implications of *aliasing* in both the time and frequency domain, first consider the four cases of a time domain representation of a sampled sinewave signal shown in Figure 4.4. In the Case 1, it is clear that an adequate number of samples have been taken to preserve the information about the sinewave. In Case 2 of the figure, only four samples per cycle are taken; still an adequate number to preserve the information. Case 3 represents the ambiguous limiting condition where $f_s = 2f_a$. If the relationship between the sampling points and the sinewave were such that the sinewave

was being sampled at precisely the zero crossings (rather than at the peaks, as shown in the illustration), then all information regarding the sinewave would be lost. Case 4 of Figure 4.4 represents the situation where $f_s < 2f_a$, and the information obtained from the samples indicates a sinewave having a frequency which is lower than $f_s/2$, i.e. the out-of-band signal is *aliased* into the Nyquist bandwidth between dc and $f_s/2$. As the sampling rate is further decreased, and the analog input frequency f_a approaches the sampling frequency f_s , the aliased signal approaches dc in the frequency spectrum.

TIME DOMAIN EFFECTS OF ALIASING

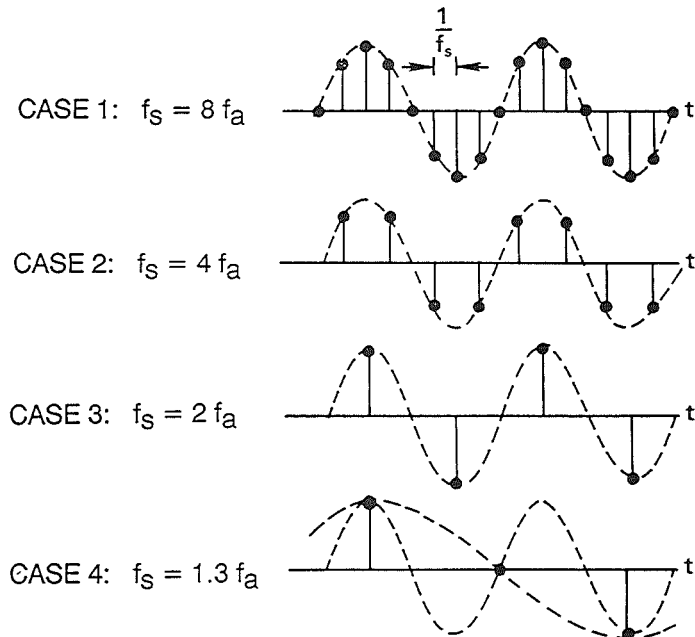


Figure 4.4

The corresponding frequency domain representation of the above scenario is shown in Figure 4.5. Note that sampling the analog signal f_a at a sampling rate f_s actually produces two alias frequency components, one at $f_s + f_a$, and the other at $f_s - f_a$. The upper alias, $f_s + f_a$, seldom presents a problem, since it lies outside the Nyquist bandwidth. It is the lower alias component, $f_s - f_a$, which causes problems when the input signal exceeds the Nyquist bandwidth, $f_s/2$.

From Figure 4.5, we make the important observation that *regardless of*

where the analog signal being sampled happens to lie in the frequency spectrum, the effects of sampling will cause either the actual signal or an aliased component to fall within the Nyquist bandwidth between dc and $f_s/2$. Therefore, any signals which fall outside the bandwidth of interest, whether they be spurious tones or random noise, must be adequately filtered *before* sampling. If unfiltered, the sampling process will alias them back within the Nyquist bandwidth where they will corrupt the wanted signals.

FREQUENCY DOMAIN EFFECTS OF ALIASING

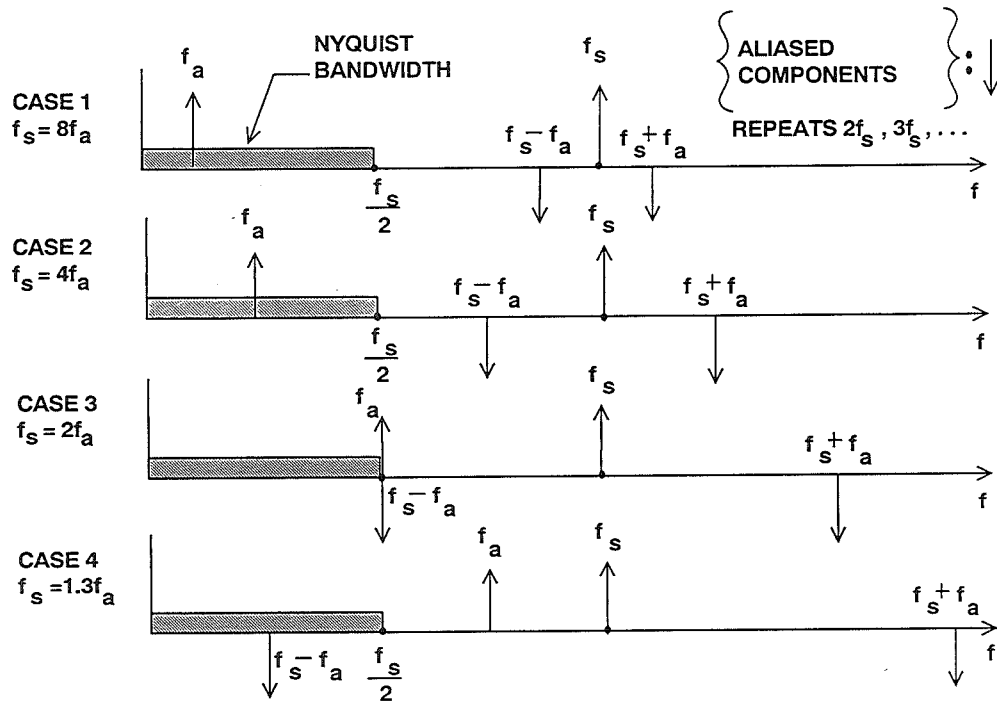


Figure 4.5

SPECIFYING THE ADC SAMPLING RATE AND THE ANTIALIASING FILTER

Properly specifying the ADC sampling rate basically involves trading off higher ADC sampling rates against increased antialiasing filter complexity. The first step is to know the characteristics of the signal being processed. Assume that the highest frequency of interest is f_a . The antialiasing filter passes signals from dc to f_a while attenuating signals above f_a . We have

now reached the first decision point, since there is no such thing as a perfect analog lowpass filter.

Assume that the corner frequency of the filter is chosen to be equal to f_a . The effect of the finite transition from minimum to maximum attenuation on system dynamic range is illustrated in Figure 4.6.

EFFECTS OF ANTIALIASING FILTER ON SYSTEM DYNAMIC RANGE

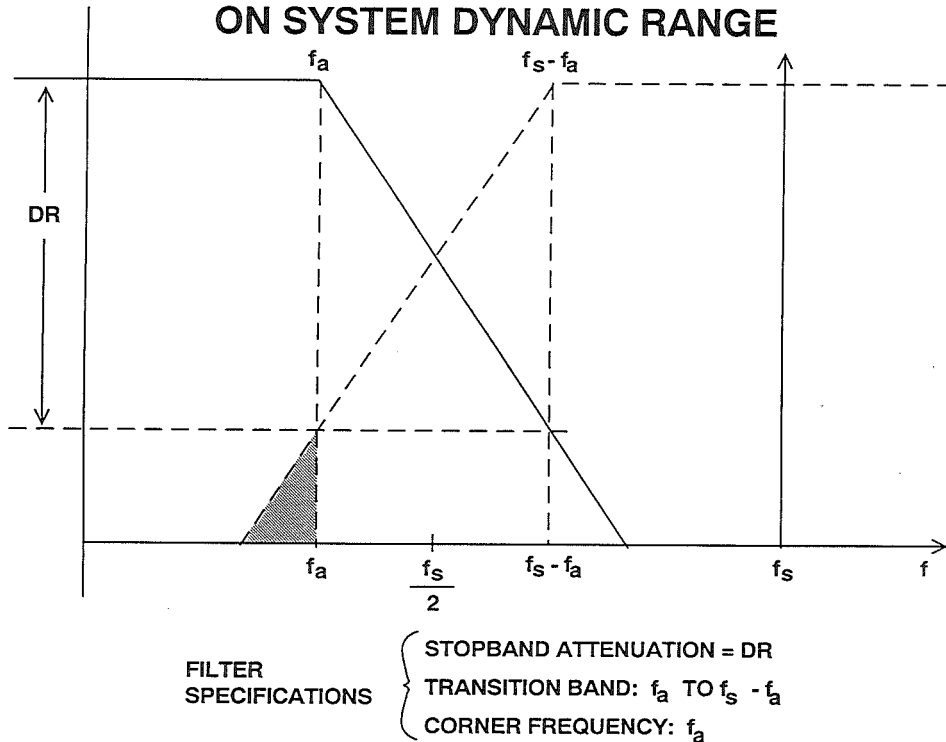


Figure 4.6

Assume that the input signal has fullscale components well above the maximum frequency of interest, f_a . The diagram shows how fullscale frequency components above $f_s - f_a$ are aliased back into the bandwidth dc to f_a . These aliased components are indistinguishable from actual signals and therefore limit the dynamic range to the value on the diagram which is shown as *DR*.

Some texts recommend specifying the antialiasing filter with respect to the Nyquist frequency, $f_s/2$, but this assumes that the signal bandwidth of interest extends from dc to $f_s/2$ which is rarely the case. In the example shown in Figure 4.6, the aliased components between f_a and $f_s/2$ are not of interest and do not limit the dynamic range.

The antialiasing filter transition band is therefore determined by the corner frequency f_a , the stopband frequency

$f_s - f_a$, and the stopband attenuation, *DR*. We choose the required system dynamic range based on our requirement for signal fidelity.

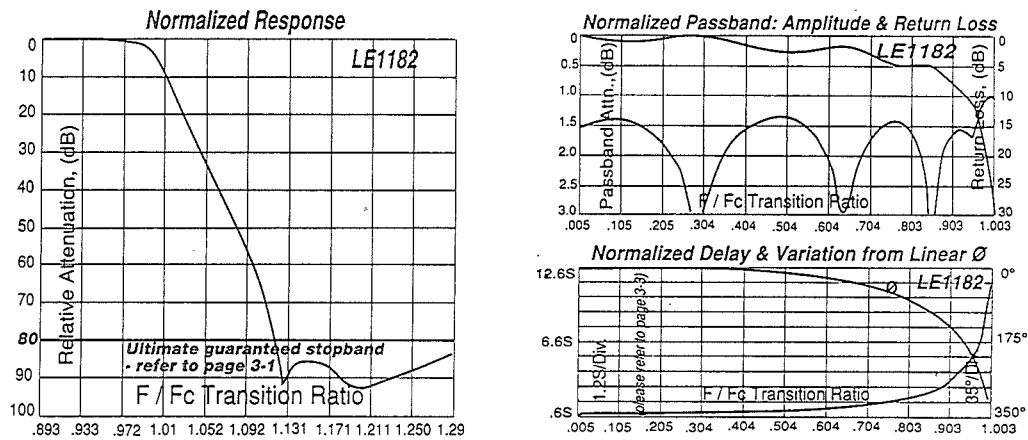
Filters become more complex as the transition band becomes sharper, all other things being equal. For instance, a Butterworth filter design gives 6dB attenuation per octave for each filter pole. Achieving 60dB attenuation in a transition region between 1MHz and 2MHz (1 octave) requires a minimum of 10 poles.

Other filter designs are generally more suited to high speed applications where the requirement for a sharp transition band is combined with requirements on in-band flatness and linear phase response. Elliptic filters are popular choices for high speed antialiasing filters.

There are a number of companies which specialize in designing custom analog filters. As an example, the normalized response of the TTE, Inc., LE1182 11-pole elliptical antialiasing filter is shown in Figure 4.7. Notice that this filter is specified to achieve at least 80dB attenuation between f_c and $1.2f_c$ (Refer-

ence 1). The corresponding passband ripple, return loss, delay, and phase response are also shown in Figure 4.7. This custom filter is available in corner frequencies up to 100MHz and in a choice of PC board, BNC, or SMA compatible packages.

CHARACTERISTICS OF TTE, INC., L31182-SERIES 11-POLE ELLIPTICAL FILTER



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Figure 4.7

From this discussion, we can see how the sharpness of the antialiasing transition band can be traded off against the ADC sampling frequency. Choosing a higher sampling rate (oversampling) reduces the requirement on transition band sharpness (hence, the filter complexity) at the expense of using a faster ADC and processing data at a faster rate. Remember that high speed ADCs are not oversampling as in the case of Sigma-Delta converters.

The above design process is started by choosing an initial sampling rate of 2 to 4 times f_a . Determine the filter specifications based on the required dynamic range and see if such a filter is realizable within the constraints of the system cost and performance. If not, consider a higher sampling rate and a faster ADC.

The antialiasing filter requirements may be relaxed somewhat if it is certain

that there will never be a fullscale signal at the stopband frequency $f_s - f_a$. In many applications it is improbable that fullscale signals will occur at this frequency. If the maximum signal at the frequency $f_s - f_a$ will never exceed XdB below fullscale, then the filter stopband attenuation requirement is reduced by that same amount. The new

requirement for stopband attenuation at $f_s - f_a$ based on this knowledge of the signal is now only $DR - XdB$. When making this type of assumption, be careful to treat any noise signals which may occur above the maximum signal frequency f_a as unwanted signals which will also alias back into the signal bandwidth.

ADC RESOLUTION AND DYNAMIC RANGE REQUIREMENTS

So far, we have discussed only the effects of ADC sampling and aliasing on the system dynamic range. The effects of dividing the signal amplitude into a finite number of discrete quantization levels must also be considered.

fullscale input range is chosen to be approximately 2V which is popular for higher speed ADCs. The bit size (or LSB weight, q) is determined by dividing the fullscale range of the converter by the number of possible quantization levels. Hence, a 10bit ADC having 1024 discrete levels has an LSB weight of $2.048V/1024$, or 2mV.

Figure 4.8 shows a table of relative bit sizes for various resolution ADCs. The

BIT SIZES, THEORETICAL QUANTIZATION NOISE, AND SNR FOR 2.048V FULLSCALE CONVERTERS

Resolution (N Bits)	1 LSB = q	% FS	ppm FS	dB FS (6N)	RMS Quantization Noise, $q/\sqrt{12}$	Theoretical Fullscale SNR (dB)
6	32mV	1.56	15625	36	9.2mV	37.9
8	8mV	0.39	3906	48	2.3mV	50.0
10	2mV	0.098	977	60	580 μ V	62.0
12	500 μ V	0.024	244	72	144 μ V	74.0
14	125 μ V	0.0061	61	84	36 μ V	86.0
16	31 μ V	0.0015	15	96	13 μ V	98.1

Figure 4.8

The selection process for determining the ADC resolution should begin by determining the ratio between the largest signal (fullscale) and the smallest signal you wish the ADC to detect. Convert this ratio to dB, and divide by 6. This is your *minimum* ADC resolution requirement for dc signals. You will actually need more resolution to account for extra signal headroom, since ADCs act as hard limiters at both ends of their range. Remember that this computation is for dc or low frequency signals and that the ADC performance will degrade as the input signal slewrate increases. What will actually occur is that the final ADC resolution will be dictated by dynamic performance at high frequencies. This may lead to the selection of an ADC which has more resolution at dc than is actually required.

Also shown in the table of Figure 4.8 is the theoretical rms quantization noise produced by a perfect N-bit ADC. In the development of classical ADC quantization noise theory, the assumption is usually made that the quantization error signal is uncorrelated with the ADC input signal. If this is true, then the quantization noise appears as random noise spread uniformly over the Nyquist bandwidth, dc to $f_s/2$, and it has an rms value equal to $q/\sqrt{12}$.

If, however, the input signal is locked to a non-prime integer sub-multiple of f_s , the quantization noise will no longer appear as uniformly distributed random noise, but instead will appear as harmonics of the fundamental input sinewave. This is especially true if the

input is an exact even submultiple of f_s . Figure 4.9 illustrates the point using FFT simulation for an ideal 12 bit ADC. The FFT record length was chosen to be 4096. The spectrum on the left shows the FFT output when the input signal is an exact even submultiple (1/32) of the sampling frequency (the frequency was chosen so that there were exactly 128 cycles per record). The ratio of the worst harmonic to the signal (Spurious Free Dynamic Range, SFDR) is approximately 78dBc. The spectrum on the right shows the output when the input signal is such that there are exactly 127 cycles per record. The SFDR is now about 92dBc which is an improvement of 14dB. Signal-correlated quantization noise is highly undesirable in spectral analysis applications, where it becomes difficult to differentiate between real signals and system-induced spurious components, especially when searching the spectrum for the presence of low-level signals in the presence of large signals.

There are a number of ways to reduce this problem, but the easiest way is to add a small amount of broadband rms noise to the ADC input signal as shown in Figure 4.10. The rms value of this noise should be equal to about 1/2 LSB. The effect of this is to randomize the quantization noise and eliminate its possible signal-dependence. In many systems, there is usually enough random noise on the input signal and the sampling clock so that this happens automatically. This is especially likely when using high speed ADCs which have 12 or more bits of resolution and a relatively small input range of 2V p-p.

**EFFECTS OF SAMPLING A SIGNAL WHICH IS AN EXACT EVEN SUB-MULTIPLE OF THE ADC SAMPLING FREQUENCY
(M = 4096, IDEAL 12-BIT ADC SIMULATION)**

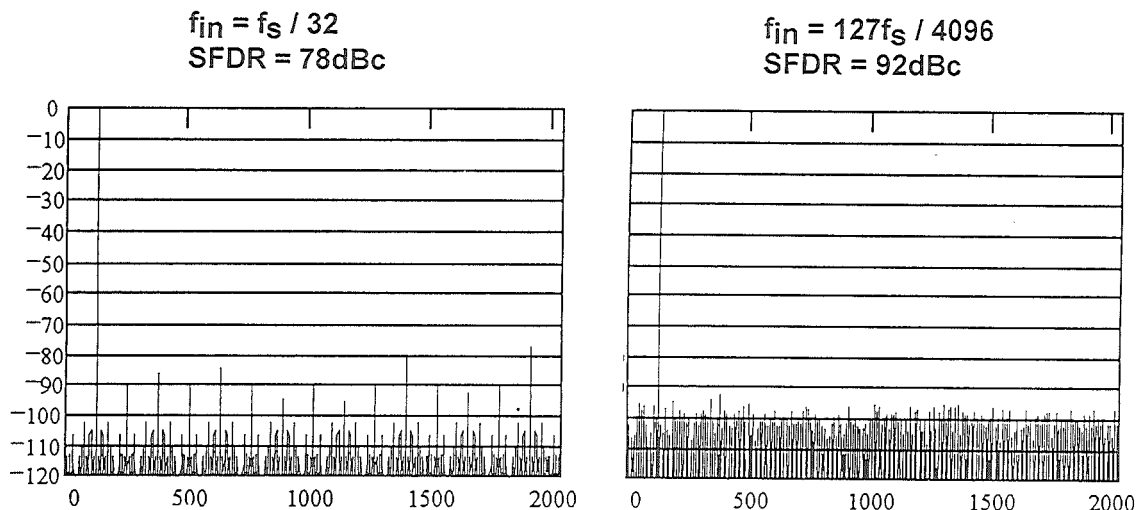


Figure 4.9

THE ADDITION OF GAUSSIAN WIDEBAND NOISE TO THE ADC INPUT RANDOMIZES QUANTIZATION NOISE AND REMOVES INPUT SIGNAL DEPENDENCE

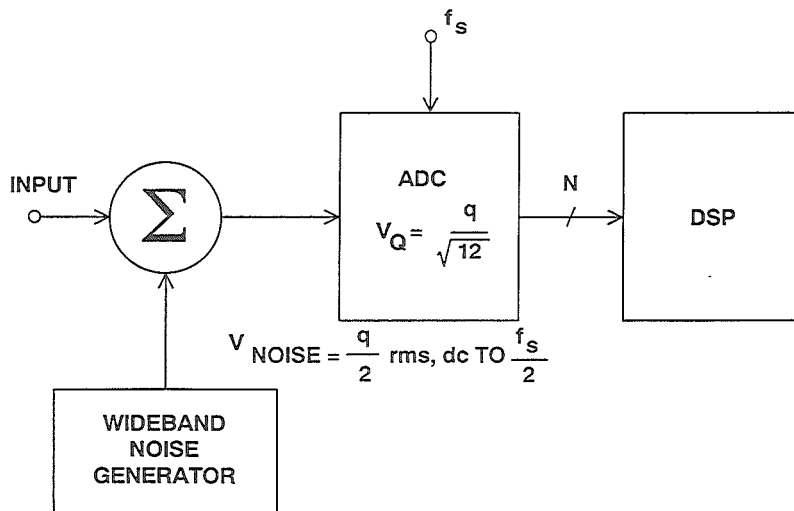


Figure 4.10

Quantization noise is therefore spread over the entire Nyquist bandwidth dc to $f_s/2$. The theoretical fullscale rms sinewave signal-to-noise ratio (SNR) may then be calculated using the well known formula, $SNR = 6.02N + 1.76dB$.

In actual practice, sampling ADCs are evaluated for their dynamic performance by first applying a spectrally pure sinewave input and then perform-

ing an FFT on the ADC output data as shown in Figures 4.11 and 4.12. The FFT output can be used to calculate harmonic distortion, THD, and SNR. The actual SNR is then compared to the theoretical SNR. The measured SNR may be substituted in the SNR formula, and the equation solved for N. The resulting value for N is called the *effective number of bits, or ENOBs*.

ADC DYNAMIC TESTING

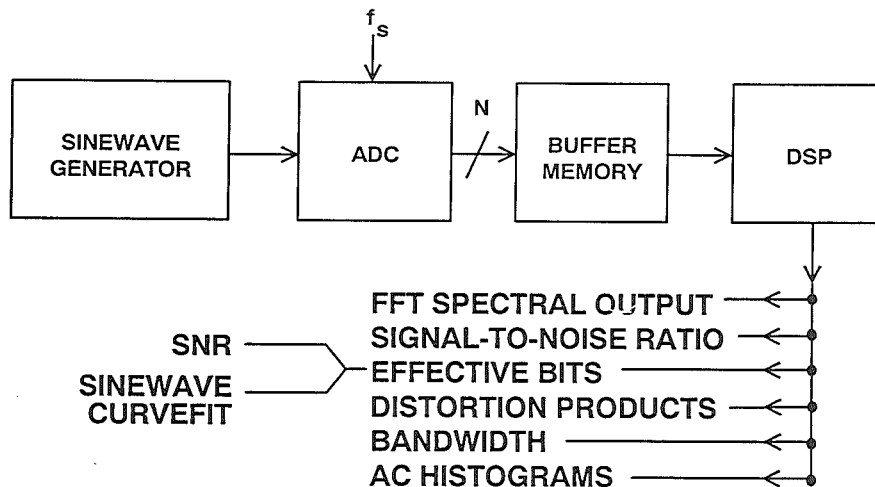


Figure 4.11

4096 POINT FFT OUTPUTS FOR AD9022 12-BIT, 20MSPS ADC

$F_S = 20 \text{ MSPS}$

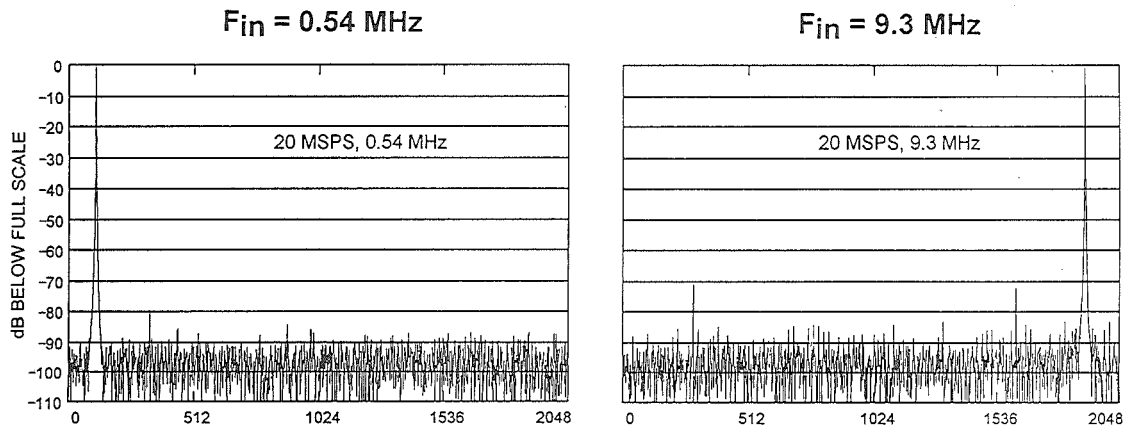


Figure 4.12

QUANTIZATION THEORY BASICS

- RMS Quantization Noise in Nyquist Bandwidth, DC to $f_S/2$:
 $q/\sqrt{12}$, q = LSB Weight

- Fullscale Sinewave RMS Signal to RMS Noise Ratio in Nyquist Bandwidth:

$$\text{SNR} = 6.02N + 1.76\text{dB}$$

- Effective Number of Bits (ENOB):

$$\text{ENOB} = \frac{\text{SNR}_{\text{ACTUAL}} - 1.76\text{dB}}{6.02}$$

Figure 4.13

The SNR and effective bits measurement is made for both low, intermediate, and high frequency input signals. All ADCs exhibit some degradation in SNR and ENOBs at higher input signal

frequencies due to various sources of nonlinearities. Figure 4.12 shows the $S/(N + D)$ for the AD9022 12 bit, 20MSPS monolithic sampling ADC.

S/(N+D) AND EFFECTIVE BIT PERFORMANCE OF AD9022 12-BIT, 20MSPS SAMPLING ADC

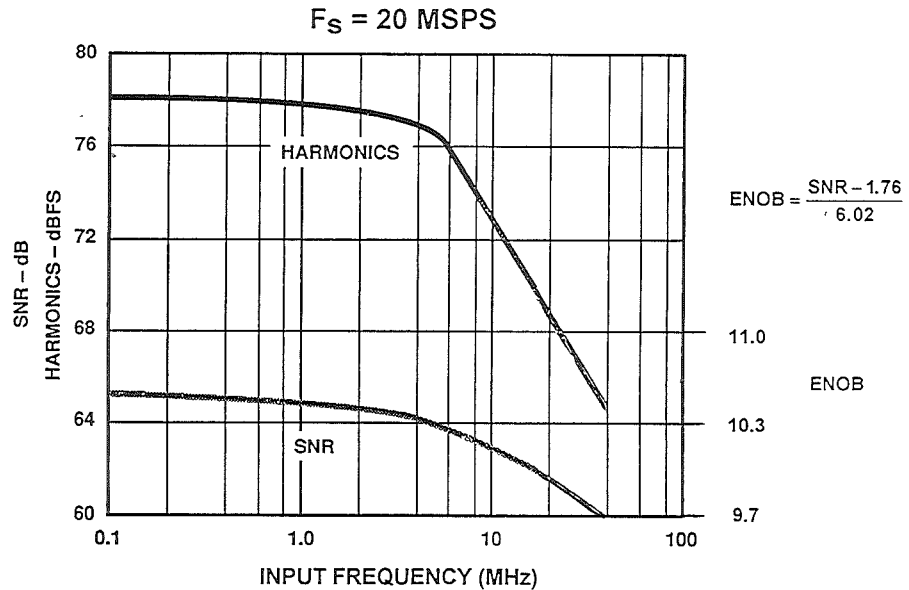


Figure 4.14

The AD9022 is representative of a class of high-performance *sampling* ADCs. Sampling ADCs have the sample-and-

hold function on-chip and are characterized in terms of both dc and ac specifications.

MODERN SIGNAL-PROCESSING ADCs

- Most are *Sampling* ADCs Containing on-chip SHA Function as Opposed to *Encoders*, which have no SHA
- Interface Between SHA and ADC Handled on-chip
- Complete DC and AC Specifications Usually Provided: SNR, THD, SFDR, ENOB, Bandwidth, etc.
- Input Full-Power Bandwidth is Usually Much Greater than $f_s/2$

Figure 4.15

The input bandwidth of the ADC should be considerably greater than the highest-frequency baseband signal of interest. The full-power bandwidth (FPBW) of an ADC is that input frequency at which the amplitude of the reconstructed FFT *fundamental* is reduced by 3dB for a fullscale input. Generally, though, there is considerable loss of

resolution at frequencies well below this. Full-power bandwidth must be examined in conjunction with SNR, ENOB, and THD in order to determine the actual dynamic performance of the ADC at the FPBW frequency. The small signal ADC bandwidth is approximately equal to the FPBW if there is no slewrate limiting.

ADC FULL-POWER BANDWIDTH

- The Frequency at Which the Amplitude of the *Fundamental* Component in the FFT Output is Down 3dB
- FPBW Usually $> f_s$ (Except for $\Sigma\Delta$ ADCs)
- Must Examine ENOB and THD at FPBW Frequency - Usually Much Reduced
- Example: AD9022 FPBW = 100MHz, 9.7 ENOB @ 40MHz INPUT
- Use FPBW or Small Signal BW (if Greater Than FPBW) for Noise Calculations

Figure 4.16

The next step in the process of determining the ADC resolution is to determine the effective bit (ENOB) requirement or SNR at the highest input frequency of interest, f_a . Most modern sampling ADCs have these specifications and also curves similar to that of Figure 4.14. Remember that the S/(N+D) calculation includes all distortion products as well as those due to quantization.

The *peak spurious* or peak harmonic component is the largest spectral com-

ponent excluding the input signal and dc (measured with FFT techniques). This value is expressed in dB relative to the rms value of the input signal. This specification is also referred to as *spurious free dynamic range*, or SFDR. In applications such as digital spectral analysis using FFT techniques, harmonic distortion, THD, or spurious free dynamic range (SFDR) may be of greater concern than the actual broadband rms noise level.

The FFT takes a discrete number of time samples, M , and converts them into $M/2$ discrete spectral components. The spacing between the spectral lines is $\Delta f = f_s/M$. If an FFT is performed on broadband quantization noise which has a bandwidth of $f_s/2$, the average value of the noise contained in each FFT frequency cell is $10\log_{10}(M/2)$ dB less than the rms value of the quantization noise. This is illustrated in Figure

4.17. This is equivalent to sweeping an analog spectrum analyzer from dc to $f_s/2$ with the bandwidth set to Δf . The average value of the noise components in each frequency bin can be reduced 3dB by doubling the record length M . Using deeper FFTs, averaging the results of a number of FFTs, or other filtering techniques may also be used to reduce the rms noise floor and allow greater dynamic range.

**THE EFFECTIVE NOISE FLOOR OF AN M-POINT FFT
(MEASUREMENT BANDWIDTH = f_s/M) IS MUCH LESS THAN
THE RMS VALUE OF THE QUANTIZATION NOISE
(MEASUREMENT BANDWIDTH = $f_s/2$)**

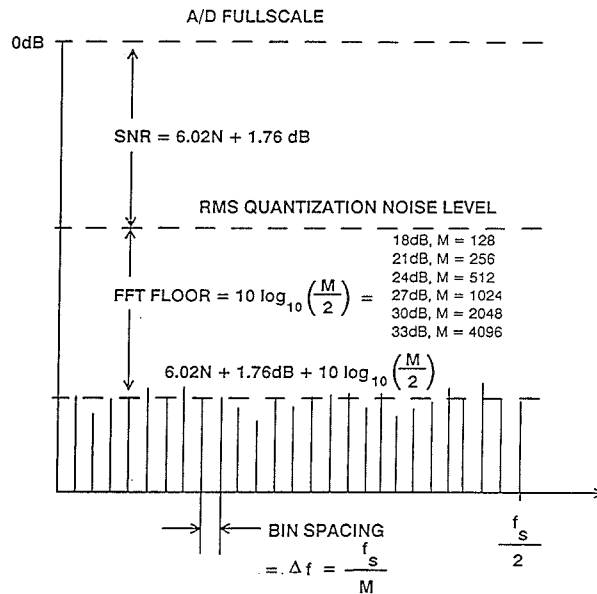


Figure 4.17

The SFDR of an ADC is generally a function of both input frequency and amplitude. Figure 4.18 shows the SFDR versus the input signal level for the AD9014 14 bit 10MSPS ADC. The data is given for two input frequencies:

4.3MHz and 9.9MHz. Notice that the SFDR at 4.3MHz reaches its maximum value at fullscale. For the 9.9MHz input, however, the point of maximum SFDR occurs several dB below fullscale.

SPURIOUS FREE DYNAMIC RANGE AS A FUNCTION OF INPUT SIGNAL LEVEL FOR THE AD9014 14-BIT, 10MSPS ADC

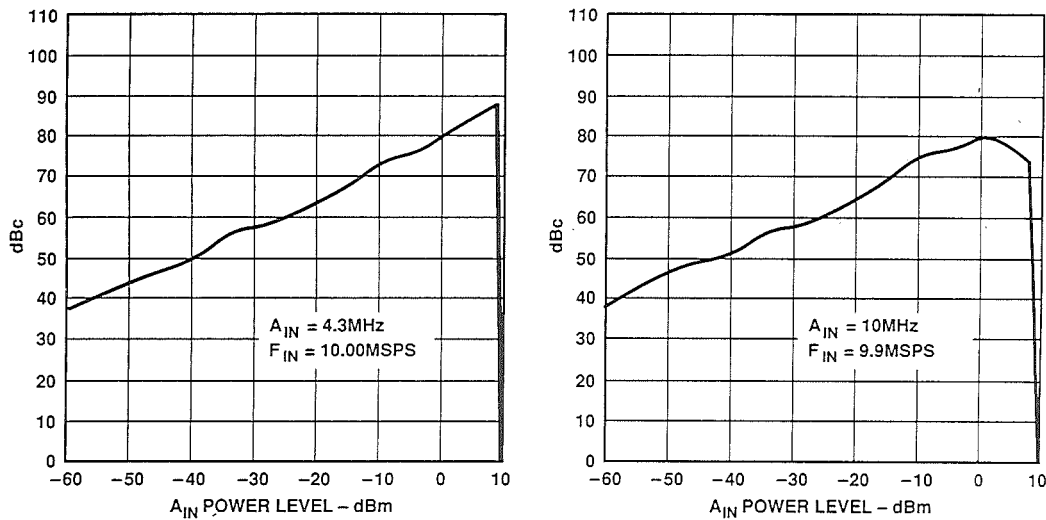


Figure 4.18

As discussed above, SFDR should not be confused with SNR. SNR depends more on the rms value of the quantization noise and is therefore a function of the number of ADC bits. SFDR, on the other hand, depends more on the linearity of the ADC and is relatively independent of the number of actual bits. This is dramatically illustrated in Figure 4.19, where SNR and SFDR is

shown for the AD9014 ADC. The top curve in the figure shows the SFDR of the AD9014 utilizing 14, 12, and 10 bits of the ADC. The bottom three curves show the SNR of the AD9014 operating with 14, 12, and 10 bits. The level of the internally generated spurs will not rise as bits are omitted, but the broadband rms noise floor rises for each bit that is dropped.

AD9014 SFDR AND SNR VERSUS FREQUENCY FOR 14, 12, AND 10 ACTIVE BITS

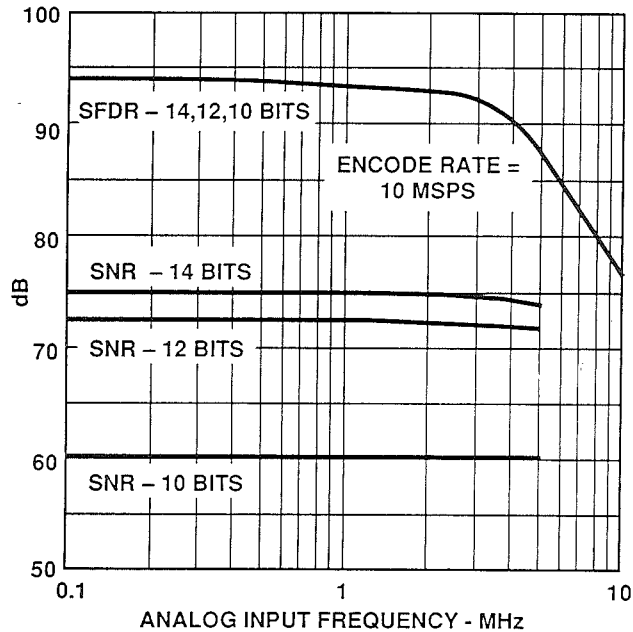


Figure 4.19

The distortion produced by an ADC cannot be analyzed in terms of second and third-order intercepts as in the case of an amplifier. This is because there are two components of distortion in a high performance ADC. One component is due to the non-linearity associated with the analog front end amplifier and the sample-and-hold. This non-linearity has the familiar “bow” or “s”-shaped curve shown in Figure 4.20. The distortion associated with this type of non-linearity is sometimes referred to as *soft*

distortion and produces low-order distortion products. This component of distortion behaves in the traditional manner and is a function of signal level. In a practical ADC, however, the soft distortion is usually much less than the other component of distortion which is due to the nonlinearity of the encoder transfer function itself. This function is more likely to have discrete points of discontinuity across the signal range as shown in Figure 4.20.

TRANSFER CHARACTERISTICS FOR "SOFT" AND "HARD" DISTORTION

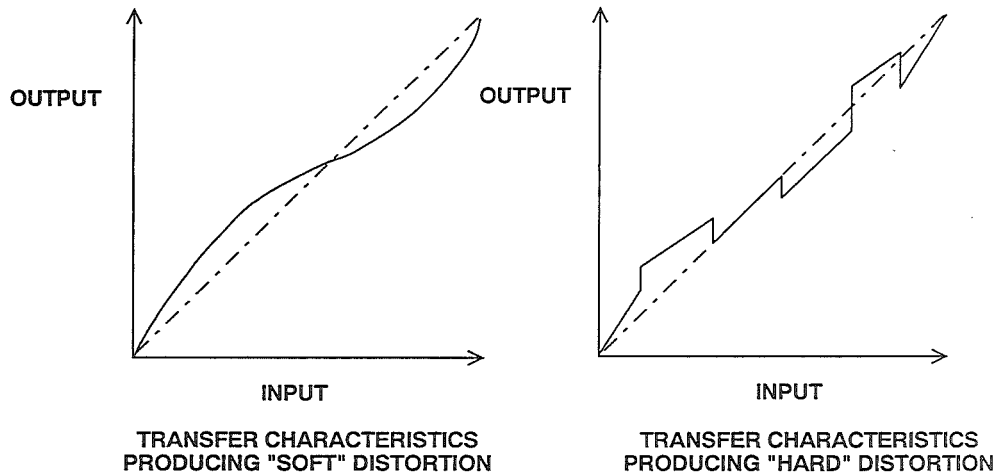


Figure 4.20

The actual location of the points of discontinuity depends on the particular ADC architecture, but nevertheless such discontinuities occur in practically all high speed ADCs. Non-linearity of this type produces high-order distortion products which are relatively unpredictable with respect to input signal level. For lower-amplitude signals, this constant level *hard* distortion causes the SFDR of the ADC to decrease as input amplitude decreases. The soft distortion

in a well-designed ADC generally only comes into play for high frequency large-amplitude input signals where it may rise above the hard distortion floor. This can be observed in Figure 4.18, where the 4.3MHz input data indicates a relatively constant hard distortion floor as the signal amplitude is increased to fullscale. The 9.9MHz data, however, indicates an increase in soft distortion as the input signal approaches fullscale.

UNDERSAMPLING (SUPER-NYQUIST)

Many modern signal processing applications require ADCs with extremely wide dynamic range. The ADC is often the limiting factor in the performance of digital spectrum analyzers. In direct IF-to-digital receivers, the ADC must accurately digitize narrowband signals with a center frequency much greater than the Nyquist frequency of one-half the sampling rate. This is called *undersampling*, and often requires that a high-performance sample-and-hold be placed in front of the ADC to increase the dynamic range. The traditional sigma-delta architecture can be modified to yield a bandpass rather than a lowpass transfer function, thereby allowing it to be used to process IF signals well above 1MHz. Finally, variable gain, high speed, low distortion amplifiers may extend system dynamic range as in the case of ultrasound systems.

Digital techniques are common in modern signal intelligence (SIGINT) and other high performance radios. The information is extracted from the signals using fast FFTs, digital filtering, and other powerful DSP techniques. One of the important and often limiting characteristics of such receivers is the inherent spectral purity and noise of the ADC. Digital spectral analysis is an-

other application where the spectral purity and noise of the ADC may be the performance-limiting factor. In this section, we will examine the tradeoffs and illustrate some techniques which may be used to improve ADC performance.

Digital techniques have become widespread in radar receivers, broadband communications receivers, and mobile radio. A simplified block diagram of a traditional digital receiver using baseband sampling is shown in Figure 4.21. The mixer in the RF section of the receiver mixes the signal from the antenna with the RF frequency of the first local oscillator, LO1. The desired information is contained in relatively small bandwidth of frequencies Δf . In actual receivers, Δf may be as high as a few megahertz. The LO1 frequency is chosen such that the Δf band is centered about the IF frequency at the bandpass filter output. Popular IF frequencies are generally between 30 and 100MHz. The IF mixer then translates the Δf frequency band down to baseband where it is filtered and processed by a baseband ADC. Actual receivers generally have several stages of RF and IF processing, but the simple diagram serves to illustrate the concepts.

SIMPLIFIED DIGITAL RECEIVER USING BASEBAND SAMPLING

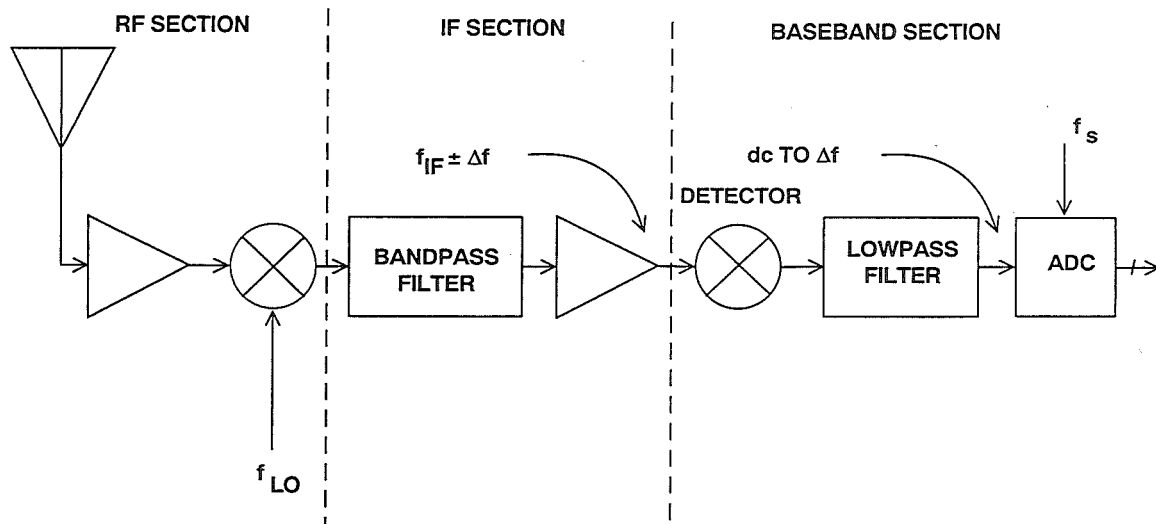


Figure 4.21

In a receiver which uses direct IF-to-digital techniques (IF sampling), the IF signal is applied directly to a wide bandwidth ADC as shown in Figure 4.22. The ADC sampling rate is chosen to be at least $2\Delta f$. The process of sampling the IF frequency at the proper rate causes one of the aliased components of Δf to appear in the dc to $f_s/2$ Nyquist bandwidth of the ADC output. DSP techniques can now be used to process the digital baseband signal. This approach may yield an improvement in overall signal-to-noise ratio by eliminating the detector stage. There is

also more flexibility in the DSP because the ADC sampling rate can be shifted to tune the exact position of the Δf signal within the baseband. The obvious problem with this approach is that the ADC must now be able to accurately digitize signals which are well outside the dc to $f_s/2$ Nyquist bandwidth which most ADCs were designed to handle. Special techniques are available, however, which can extend the dynamic range of ADCs to include IF frequencies. Before examining the ADC problem, we will first look at the basic theory behind undersampling.

SIMPLIFIED DIGITAL RECEIVER USING IF SAMPLING

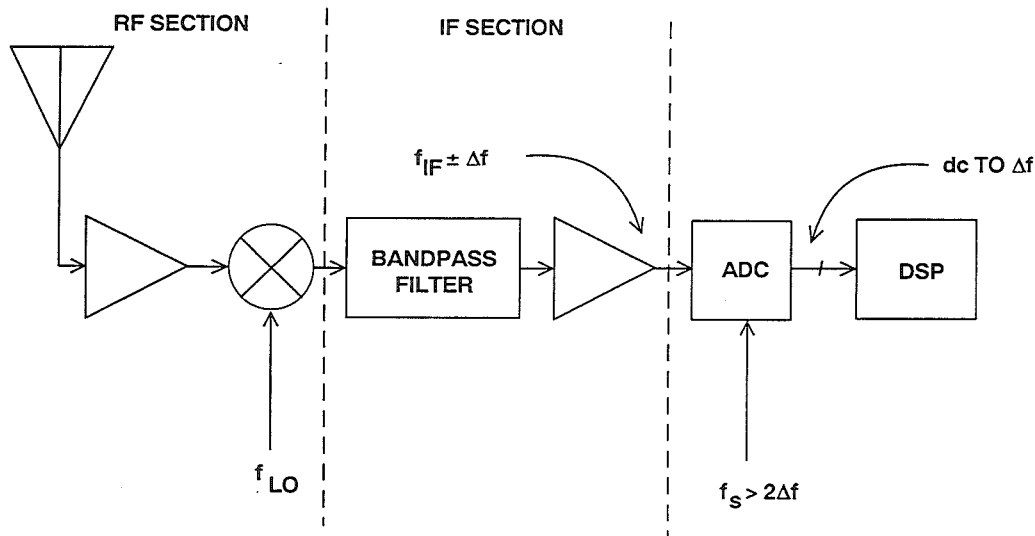


Figure 4.22

Figure 4.23 shows four cases where a signal having about a 1MHz bandwidth is located at different portions of the frequency spectrum. The minimum sampling rate required for no aliasing is also shown. In general, the sampling frequency must be at least twice the signal bandwidth, and the sampled signal must not cross an integer multiple of $f_s/2$.

In the first case, the signal occupies the band from dc to 1MHz, and therefore must be sampled at greater than

2MSPS. The second case shows a 1MHz signal which occupies the band from 0.5 to 1.5MHz. Notice that this signal must be sampled at a minimum of 3MHz to avoid aliasing. In the third case, the signal occupies the band from 1 to 2MHz, and the minimum required sampling rate for no aliasing drops back to 2MHz. The last case shows a signal which occupies the band from of 1.5 to 2.5MHz. This signal must be sampled at a minimum of 2.5MHz to avoid aliasing.

MINIMUM SAMPLING RATE REQUIRED FOR NO ALIASING OF A 1MHz BANDWIDTH SIGNAL

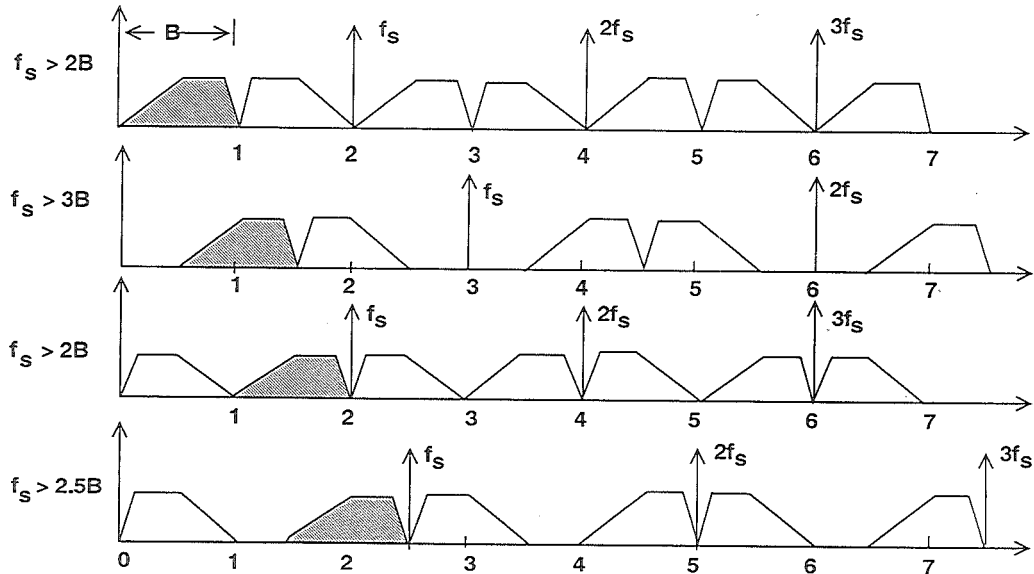


Figure 4.23

This analysis can be generalized as shown in Figure 4.24. The actual minimum required sampling rate is a func-

tion of the ratio of the highest frequency component to the total signal bandwidth.

MINIMUM REQUIRED SAMPLING RATE AS A FUNCTION OF THE RATIO OF THE HIGHEST FREQUENCY COMPONENT TO THE TOTAL SIGNAL BANDWIDTH

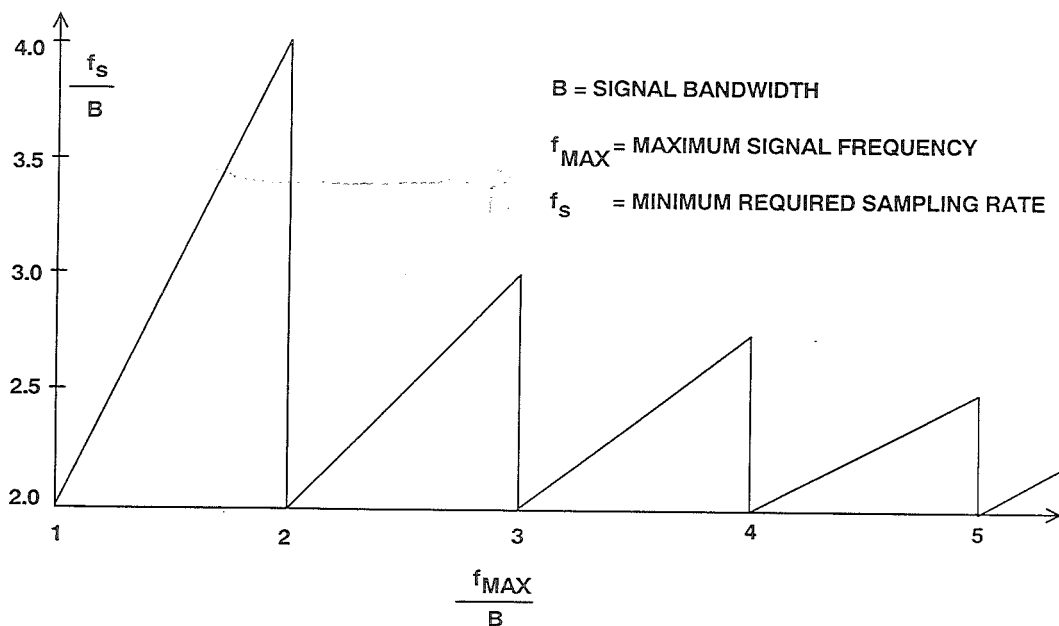


Figure 4.24

Let us now examine a signal which occupies a band between 6 and 7MHz as shown in Figure 4.25. Assume the ADC sampling rate is 2MHz. Notice that the sampling process generates aliases of this signal around multiples

of f_s . In the frequency spectrum, the alias component falling between 0 and 1MHz is an accurate representation of the original signal, assuming no ADC errors.

INTERMEDIATE FREQUENCY (IF) SIGNAL BETWEEN 6 AND 7 MHz IS ALIASED BETWEEN DC AND 1 MHz BY SAMPLING AT 2MSPS

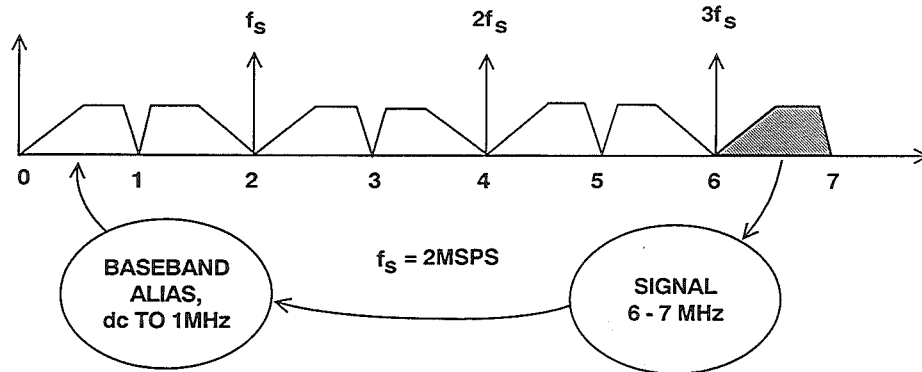


Figure 4.25

The above discussions show that although the concept of direct IF sampling is relatively straightforward, the implications for the ADC dynamic performance characteristics are significant.

Let us consider a typical example, where the IF frequency is 72.5MHz, and the desired signal occupies a bandwidth of 4MHz ($B=4\text{MHz}$), centered on the IF frequency (see Figure 4.26). We know from the previous discussion that the minimum sampling rate must be greater than 8MHz, probably on the order of 10MHz in order to prevent

dynamic range limitations due to aliasing. If we place the sampling frequency at the lower band-edge of 70MHz ($72.5-2.5$), we will definitely recover the aliased component of the signal in the dc to 5MHz baseband. There is, however, no need to sample at this high rate, so we may choose any sampling frequency 10MHz or greater which is an integer sub-multiple of 70MHz, i.e., $70 \div 2 = 35.000\text{MHz}$, $70 \div 3 = 23.333\text{MHz}$, $70 \div 4 = 17.500\text{MHz}$, $70 \div 5 = 14.000\text{MHz}$, $70 \div 6 = 11.667\text{MHz}$, or $70 \div 7 = 10.000\text{MHz}$. We will therefore choose the lowest possible sampling rate of 10.000MHz ($70 \div 7$).

INTERMEDIATE FREQUENCY (IF) SIGNAL AT 72.5MHz (± 2 MHz) IS ALIASED BETWEEN DC AND 5MHz BY SAMPLING AT 10MSPS

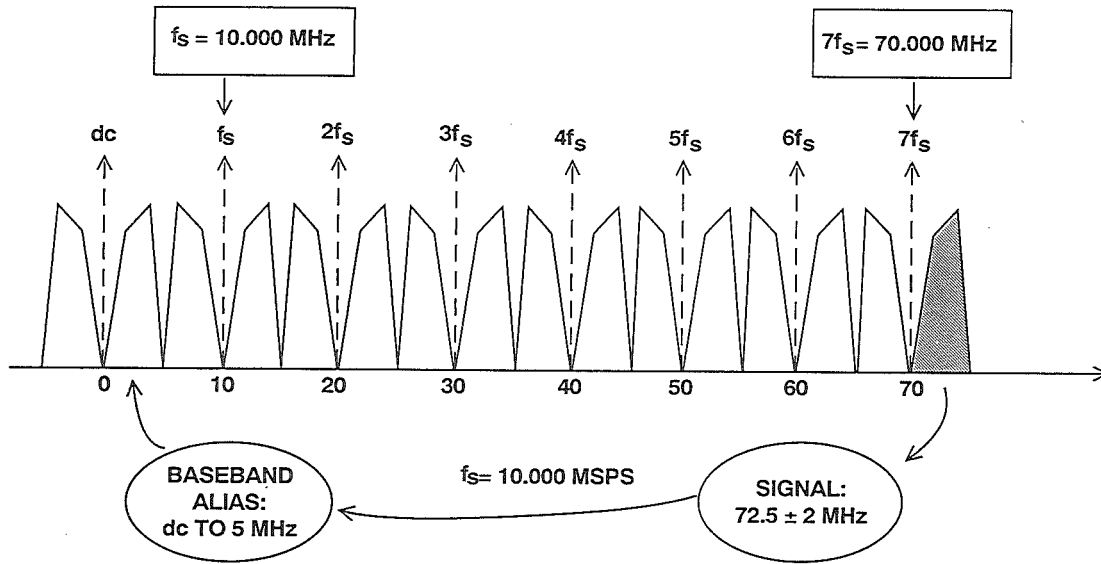


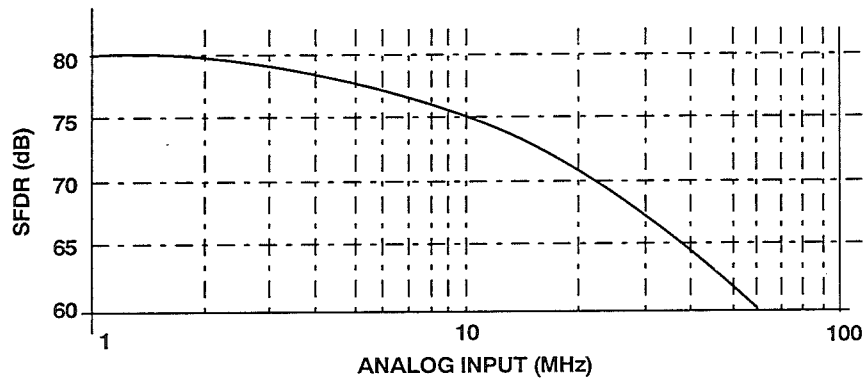
Figure 4.26

There is an advantage in choosing a sampling frequency which is a sub-multiple of the lower band-edge in that there is no frequency inversion in the baseband alias as would be the case for a sampling frequency equal to a sub-multiple of the lower band-edge. (Frequency inversion can be easily dealt with in the DSP software should it occur, so the issue is not very important).

The next step is to select an ADC which has sufficient dynamic range with a 70

to 75MHz input to meet our system requirement. In most radar receivers, a SFDR of 60 to 80dB is desirable. Unfortunately, this requirement will not be met with standard Nyquist-sampling ADCs due to degradations which occur at high input frequencies. Figure 4.27 shows the SFDR of the AD9022 12 bit, 20MSPS ADC, which represents one of the best monolithic designs available. Note that at 1MHz the SFDR is 80dB, but at the IF frequency of 70MHz, the SFDR of the device is less than 60dB.

SPURIOUS FREE DYNAMIC RANGE OF THE AD9022 12-BIT, 20MSPS ADC FOR $f_s = 10\text{MSPS}$



4

Figure 4.27

Meeting this performance requirement of 80dB SFDR requires the addition of an external wide-bandwidth, low distortion sample-and-hold, such as the AD9100 as shown in Figure 4.28. The external SHA serves to hold the signal

constant during the ADC conversion cycle. The ADC sees a dc value during the hold-time of the external SHA. The process of optimizing the design for the best SFDR is not simple, and involves many tradeoffs.

THE ADDITION OF AN EXTERNAL WIDEBAND LOW DISTORTION SHA EXTENDS THE LOW FREQUENCY PERFORMANCE OF THE ADC TO HIGHER FREQUENCIES

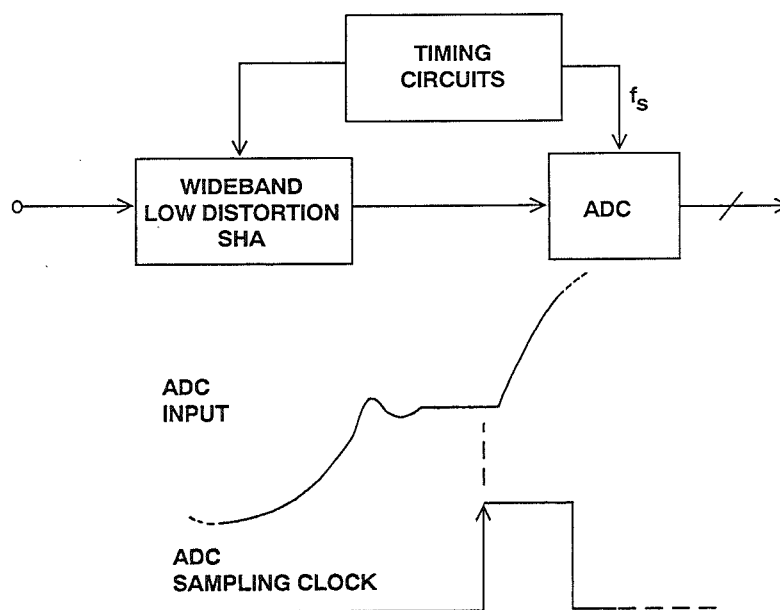


Figure 4.28

The first step in the process is to select an ADC which has sufficient SFDR at low frequencies. The low frequency distortion of an ADC is an indicator of the inherent non-linearity in the dc transfer function. The addition of an ideal external SHA will do nothing to improve on this basic performance. The best you can expect the SHA to do is to extend the low frequency performance of the ADC to higher frequencies. Because of its excellent low frequency distortion (-80dBc @ 1MHz), the AD9022 is good choice.

The next step is to select a low distortion SHA which will maintain sufficient dynamic performance at the IF frequency. Most SHAs are specified for distortion when operating in the track mode. What is of real interest, however, is the signal distortion in the hold mode when the SHA is operating dynamically. The AD9100 and AD9101 are ultra-fast SHAs and are specified in terms of hold-mode distortion. The measurement is done using a high performance low distortion ADC (such as the AD9014 14-bit, 10MSPS) to digitize the held value of the SHA output. An FFT is performed on the ADC output, and the distortion is measured digitally. For sampling rates greater than 10MSPS, the ADC is clocked at an integer sub-multiple of the SHA sampling frequency. This causes a frequency translation in the FFT output because of undersampling, but the distortion measurement still represents that of the SHA operating at the higher sampling rate.

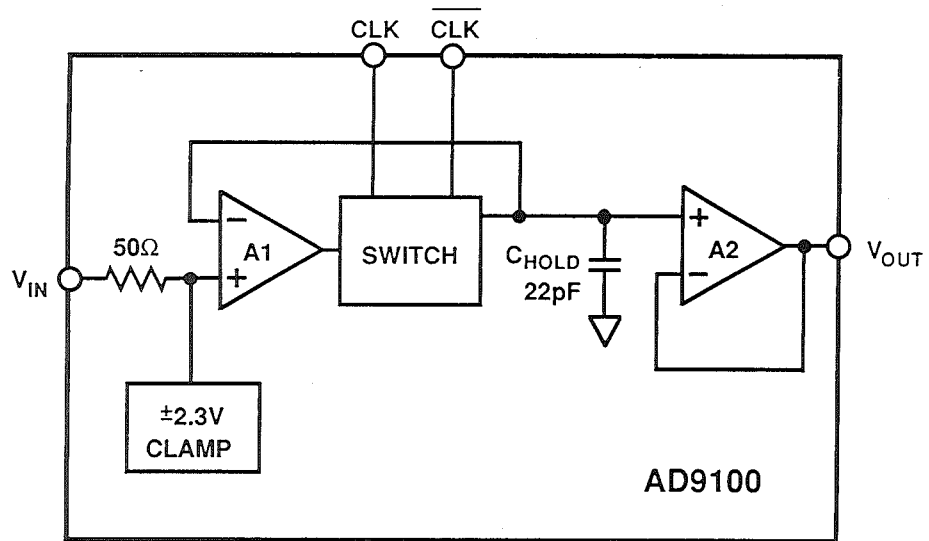
The AD9100 is optimized for low distortion operation up to 30MSPS, while the AD9101 will provide low distortion performance up to a sampling rate of 125MSPS.

A block diagram of the AD9100 track-and-hold is shown in Figure 4.29. The switching bridge is integrated into the first stage closed-loop input amplifier. This innovation provides error (distortion) correction for both the switch and amplifier, while still achieving slewrates representative of a more traditional open-loop design. The device has a 250MHz input bandwidth and a 16ns acquisition time to 0.01%.

However, the distortion performance of the AD9100 can be optimized by reducing the input signal level. This will decrease the signal-to-noise ratio, but will also reduce the distortion produced by the switching bridge nonlinearity.

The test configuration shown in Figure 4.30 was used to collect the AD9100 performance data for low amplitude input signals. The data shown in Figure 4.31 was taken at a 10MSPS sampling rate for three input amplitudes. For each amplitude, the gain of the AD9618 op amp was adjusted so that its output exactly filled the 2V p-p input range of the AD9014 ADC. Notice that the SFDR is optimum (70dBc) for a 200mV p-p input signal to the AD9100, and a corresponding post-amplifier gain of 10.

AD9100 MONOLITHIC 30MSPS TRACK-AND-HOLD



4

Figure 4.29

TEST CONFIGURATION AND TIMING FOR MEASURING AD9100 HOLD-MODE SFDR AT 10MSPS

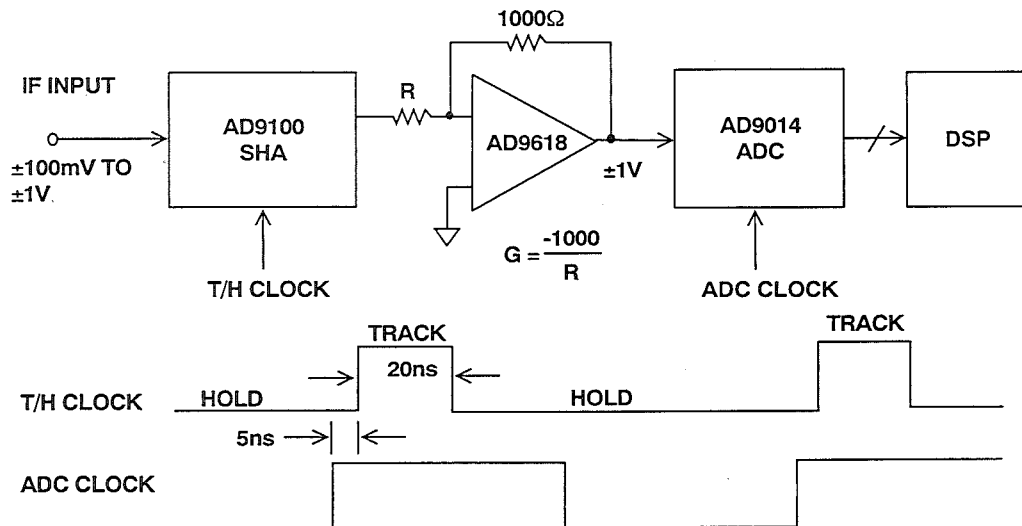


Figure 4.30

AD9100 HOLD-MODE SFDR MEASURED WITH AD9014 ADC SAMPLING AT 10MSPS

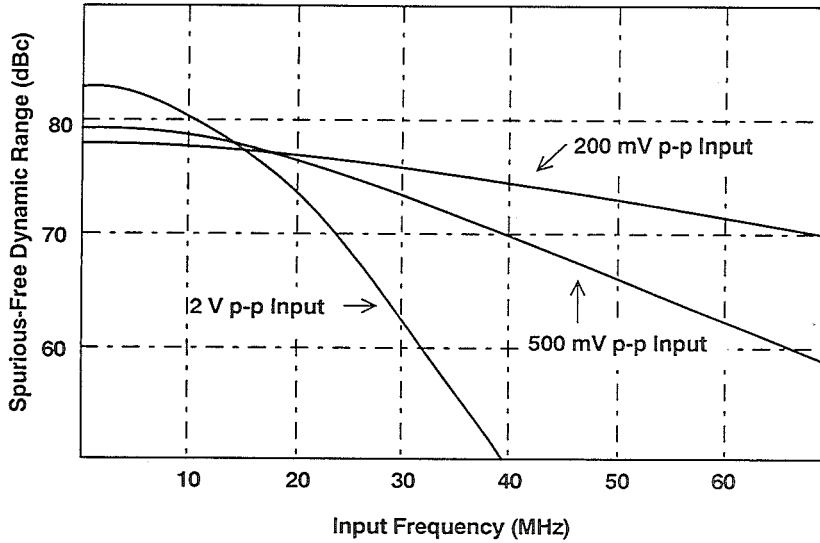


Figure 4.31

The performance of the AD9100 driving the AD9022 under identical conditions yielded the FFT spectrum shown in

Figure 4.32. The 72MHz SFDR is greater than 70dBc, and the measured SNR is 62dB.

FFT OUTPUT FOR AD9100 DRIVING AD9022 ADC, INPUT = 200mV p-p, G = 10, $f_s = 10\text{MSPS}$, $f_{in} = 71.4\text{MHz}$

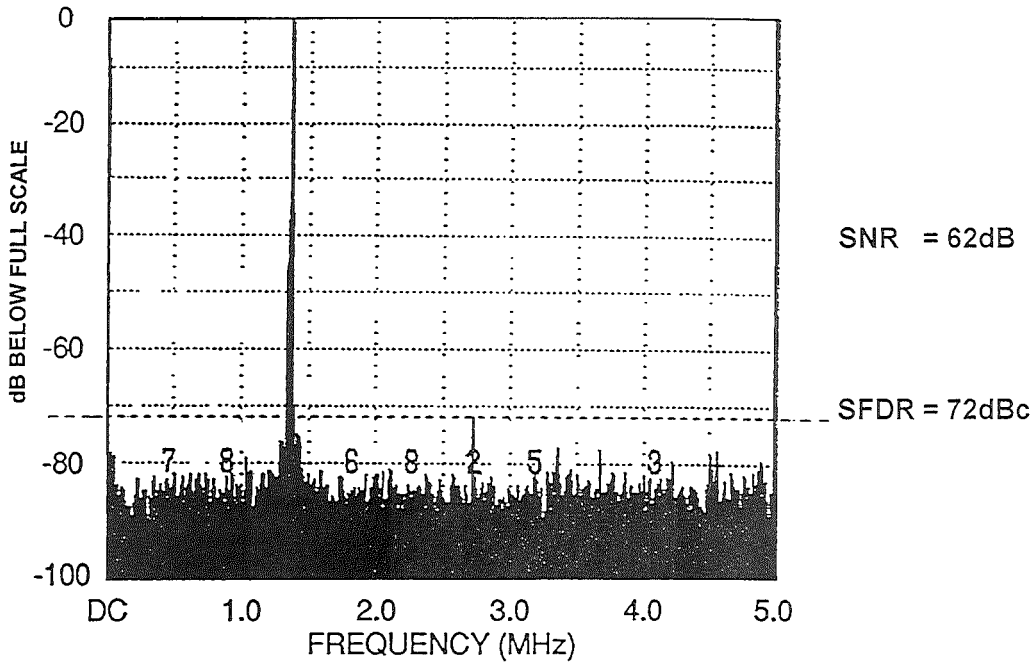


Figure 4.32

The tradeoff in optimizing the circuit for the best SFDR is the increase in overall noise resulting from the high-gain post-amplifier amplifying the hold-mode noise of the AD9100.

The other part of a successful wide-dynamic range design involves the optimization of the timing between the SHA and the ADC. This involves even more tradeoffs. The SHA acquisition time should be long enough to achieve the desired accuracy, but short enough to allow sufficient hold-time for the ADC front-end to settle and yield a low-distortion conversion. For the example above, the optimum performance was achieved using an acquisition time of 20ns and a track time of 80ns. As shown in Figure 4.30, the ADC is clocked close to the end of the SHA's

hold time. Best performance in designs such as these is always achieved by optimizing the timing in the actual circuit.

Similar dynamic range improvements can be achieved with high speed flash converters at higher sampling rates using the AD9101 SHA whose block diagram is shown in Figure 4.33. The AD9101 is a track-and-hold with an internal post-amplifier. This configuration allows the front end sampler to operate at relatively low signal amplitudes, resulting in dramatic improvement in hold-mode distortion at high input frequencies and sampling rates up to 125MSPS. The AD9101 has an input bandwidth of 350MHz and an acquisition time of 7ns to 0.1% and 11ns to 0.01%.

4

AD9101 125MSPS SAMPLING AMPLIFIER

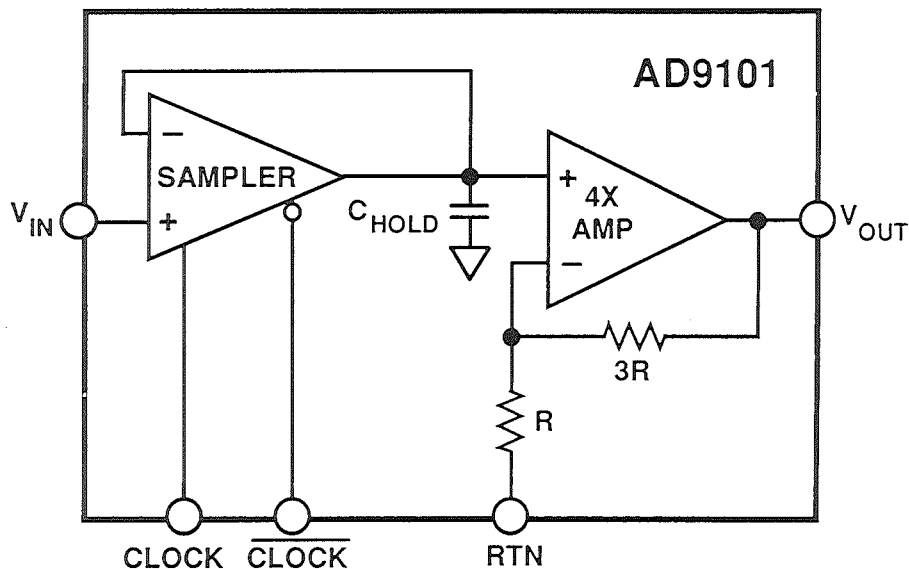


Figure 4.33

A block diagram and a timing diagram is shown for the AD9101 driving the AD9002 8 bit flash converter at 125MSPS (see Figure 4.34). The corre-

sponding dynamic range with and without the AD9101 is shown in Figure 4.35.

AD9101 SHA DRIVING AD9002 8-BIT, 125MSPS FLASH CONVERTER FOR IMPROVED DYNAMIC RANGE

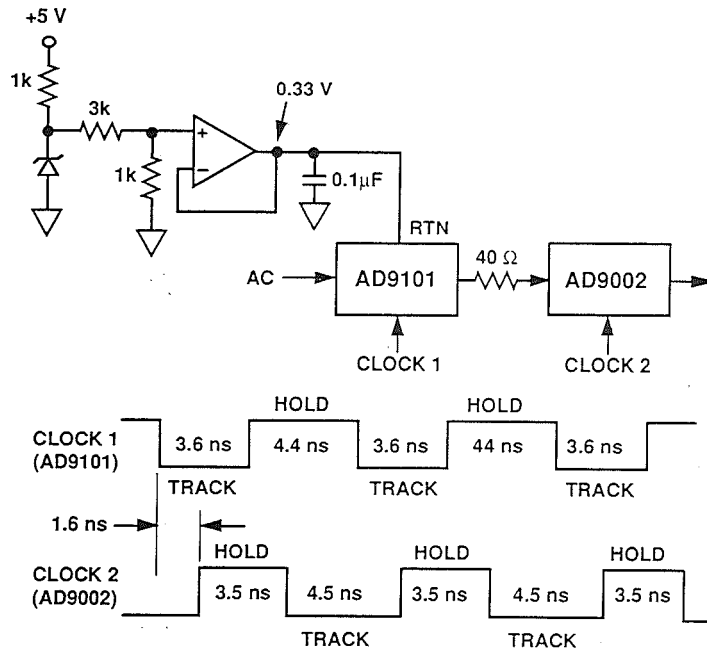


Figure 4.34

AD9002 DYNAMIC PERFORMANCE WITH AND WITHOUT AD9101 SHA

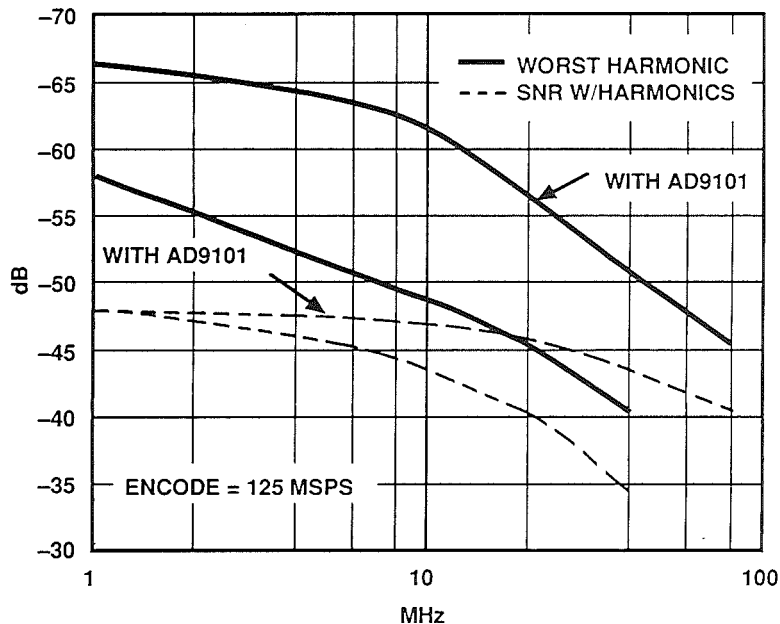


Figure 4.35

The sigma-delta ADC architecture may also be used in undersampling applica-

tions as will be described in the next section.

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