SECTION 2

SPECIAL PURPOSE AMPLIFIERS

- Instrumentation Amplifiers (In-Amps):
  Instrumentation Amplifier Configurations,
  Instrumentation Amplifier DC Error Sources,
  Instrumentation Amplifier Noise Sources
- Active Feedback Amplifiers
- Programmable Gain Amplifiers
- Isolation Amplifiers
- Comparators

SECTION 2

SPECIAL PURPOSE AMPLIFIERS

Walt Kester, Joe Buxton

INSTRUMENTATION AMPLIFIERS (IN-AMPS)

An instrumentation amplifier is a closed-loop gain block which has a differential input and an output which is single-ended with respect to a reference terminal. The input impedances are balanced and have high values, typically $10^9\Omega$ or higher. Unlike an op amp, which has its closed-loop gain determined by external resistors connected between its inverting input and its output, an in-amp employs an internal feedback resistor network which is isolated from its signal input terminals. With the input signal applied across the two differential inputs, gain is either preset internally or is user-set by an internal (via pins) or external gain resistor, which is also isolated from the signal inputs. Typical in-amp gain settings range from 1 to 10,000.

INSTRUMENTATION AMPLIFIER

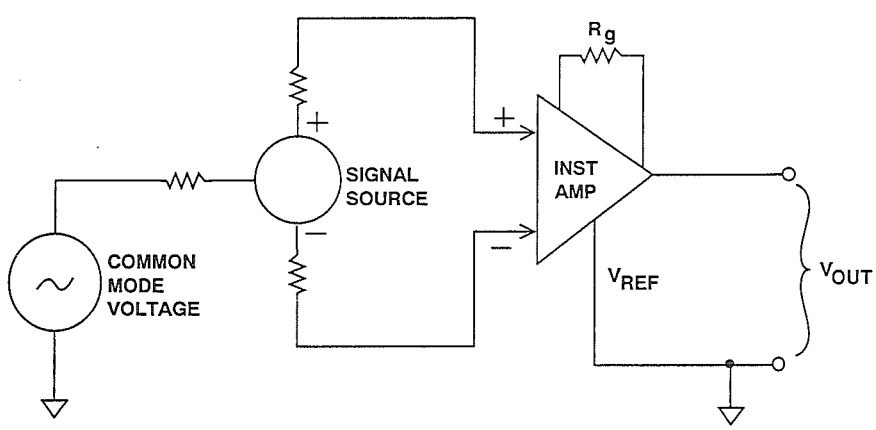
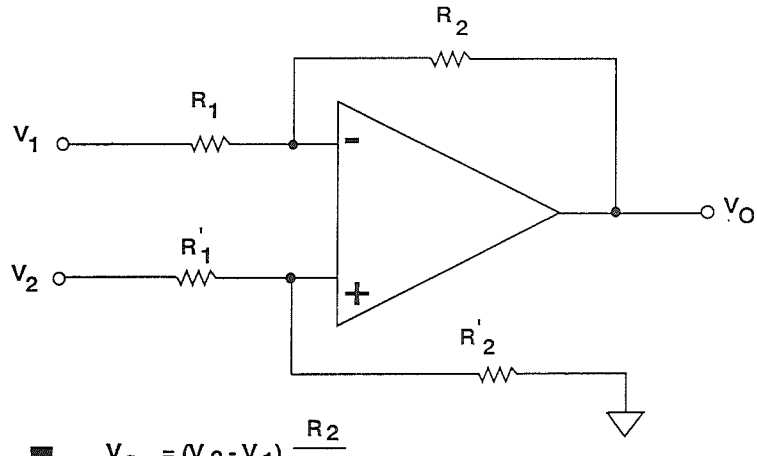


Figure 2.1

In order to be effective, an in-amp needs to be able to amplify microvolt-level signals, while simultaneously rejecting volts of common-mode signal at its inputs. This requires that in-amps have very high common-mode rejection (CMR): typical values of CMR are 70dB to over 100dB, with CMR usually improving at higher gains. Op amps, connected as subtractors as shown in Figure 2.2, provide common-mode rejection, but require closely matched external resistors. A mismatch of only 0.1% in the resistor ratios will reduce the CMR to approximately 66dB. Another problem with the simple op amp subtractor is that the input impedances are relatively low and are unbalanced between the two sides. (The input impedance seen by V_1 is R_1, and the input impedance seen by V_1' is $R_1' + R_2'$.)

OP-AMP SUBTRACTOR



- $V_O = (V_2 - V_1)\frac{R_2}{R_1}$
- $\frac{R_2}{R_1} = \frac{R_2'}{R_1'}$ CRITICAL FOR HIGH CMR
- ≥ 0.1% MISMATCH YIELDS ≤ 66dB CMR

Figure 2.2

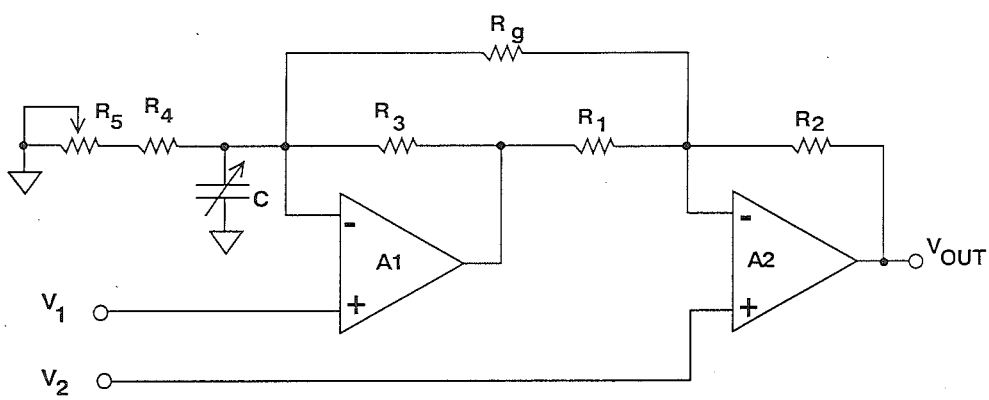
Instrumentation Amplifier Configurations

Instrumentation amplifier configurations are based on op amps, but the simple subtractor circuit described above lacks the performance required for precision applications. An in-amp architecture which overcomes some of the weaknesses of the subtractor circuit uses two op amps as shown in Figure 2.3. The circuit gain may be trimmed with an external resistor, R_g. The input impedance is high, permitting the signal sources to have high and unbalanced output impedance. One major disadvantage of this design is that common-mode voltage input range must be traded off against gain. The amplifier A1 must amplify a common-mode signal by

$$\frac{R3 + R4 + R5}{R4 + R5}.$$

If R3 >(R4+R5), saturation of A1 will occur if the common-mode signal is too high, leaving no headroom to amplify the wanted differential signal. If R3<(R4+R5), low gains cannot be realized, and since the two amplifiers are operating at different closed-loop gains (and thus at different bandwidths), there will be generally poor AC common-mode rejection without the use of the AC CMR trim capacitor shown in the diagram. Resistor R5 allows DC CMR to be optimized. Best gain TC results when the resistors are ratio-matched. If R_g is external to a thin film array, this goal is compromised.

TWO OP-AMP INSTRUMENTATION AMPLIFIER



- $V_{OUT} = (V_2 - V_1)\left(1 + \frac{R_2}{R_1} + \frac{2R_2}{R_g}\right)$
- FOR $R_1 = R_3$ AND $R_2 = R_4 + R_5$
- R_5 = DC CMR TRIM
- C = AC CMR TRIM

Figure 2.3

For true balanced high impedance inputs, three op amps may be connected to form the in-amp shown in Figure 2.4. The gain of the amplifier is set by the resistor, Rg, which may be internal, external, or pin-programmable. In this configuration, gain accuracy and CMR depend upon the ratio matching of R3/R2 to R3'/R2'. CMR does not depend on the matching of R1 to R2', and gain may be adjusted by R_g without affecting the common-mode error signal. Thus, CMR will theoretically increase in direct proportion to gain. Furthermore, common-mode signals are only amplified by a factor of 1 regardless of gain (no common-mode voltage will appear across R_g, hence, no common-mode current will flow in it because the input terminals of an op amp will have no significant potential difference between them). This means the large common-mode signals (within the op amp limits) may be handled at all gains. Finally, because of the symmetry of this configuration, common-mode errors in the input amplifiers, if they track, tend to be canceled out by the output stage subtractor. These features explain the popularity of this type of instrumentation amplifier.

"CLASSIC" THREE OP-AMP INSTRUMENTATION AMPLIFIER

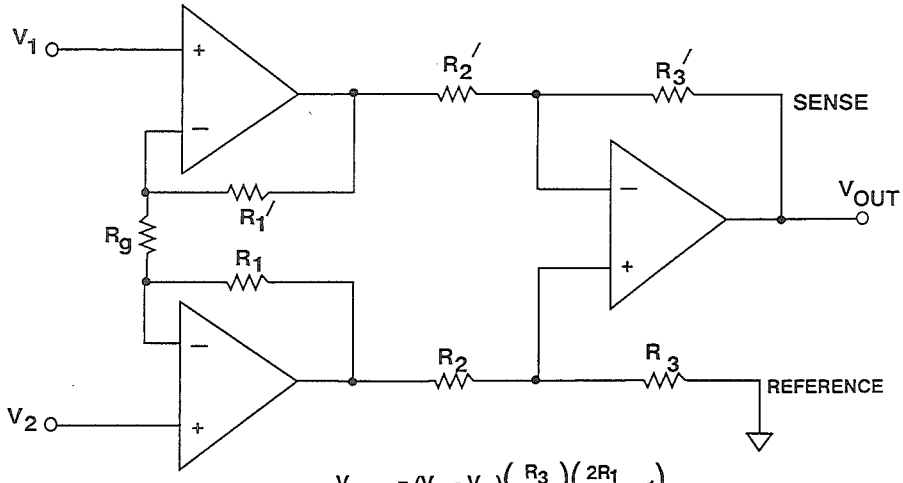


Figure 2.4

The classic three op amp configuration has been used in a number of monolithic IC instrumentation amplifiers. Besides offering excellent matching between the three internal op amps, thin-film laser trimmed resistors provide excellent ratio matching and gain accuracy at much lower cost than using discrete op amps and resistor networks. The AD524 is an excellent example of monolithic in-amp technology, and a simplified schematic is shown in Figure 2.5.

SIMPLIFIED SCHEMATIC OF THE AD524 IN-AMP

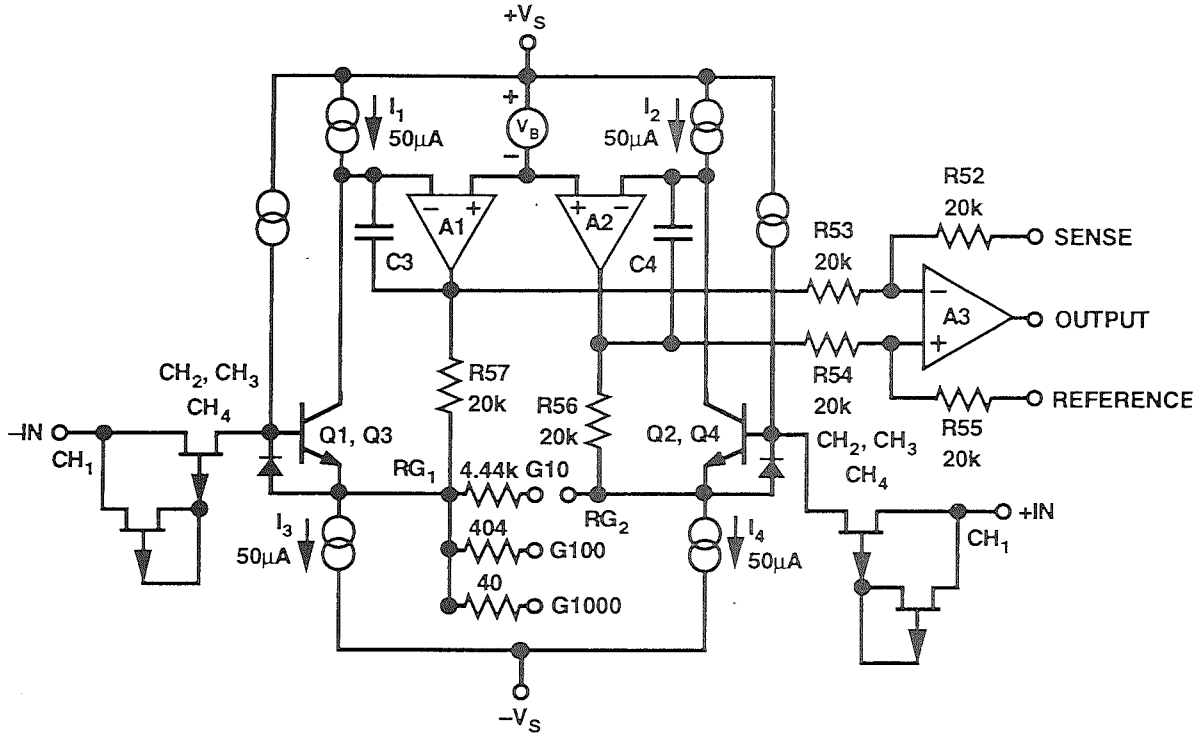


Figure 2.5

As interface amplifiers for data acquisition systems, instrumentation amplifiers are often subjected to input overloads, i.e., voltage levels in excess of the full scale for the selected gain range. The same considerations discussed in Section 1 for op amps apply to in-amps. The manufacturer's "absolute maximum" input ratings for the device should be closely observed. As with op amps, many in-amps have absolute maximum input voltage specifications equal to $\pm V_S$. Series resistors (for current limiting) and Schottky diode clamps may be used to prevent overload, if necessary. Some instrumentation amplifiers have built-in overload protection circuits in the form of series resistors (thin film) or series-protection FETs. In-amps such as the AMP-02 and the AD524 (see Figure 2.5) utilize series-protection FETs to minimize noise.

INSTRUMENTATION AMPLIFIER INPUT OVERVOLTAGE CONSIDERATIONS

- Always observe absolute maximum data sheet specs!
- Schottky diode clamps to the supply rails will limit input to $\pm V_S$ ±0.3V (This is not quite true, but near enough for safety)
- External resistors (or internal thin-film resistors) on inputs can limit input current.
- Some in-amps have series-protection input FETs for lower noise and higher input over voltages (up to ±60V, depending on device)

Figure 2.6

Instrumentation Amplifier DC Error Sources

The DC and noise specifications for instrumentation amplifiers differ slightly from conventional op amps, so some discussion is required in order to fully understand the error sources.

The gain of an in-amp is set by a resistor. If the resistor is external to the in-amp (as for the AD620 shown in Figure 2.7), its value is either calculated from a formula or chosen from a table on the data sheet, depending on the desired gain. In the case of the AD620, the internal resistors R1 and R2 are trimmed to an absolute value of 24.7kΩ. The gain formula is

$$G = \frac{49.4\text{k}\Omega}{Rg} + 1 \text{ , and therefore}$$

$$Rg = \frac{49.4\text{k}\Omega}{G - 1}$$

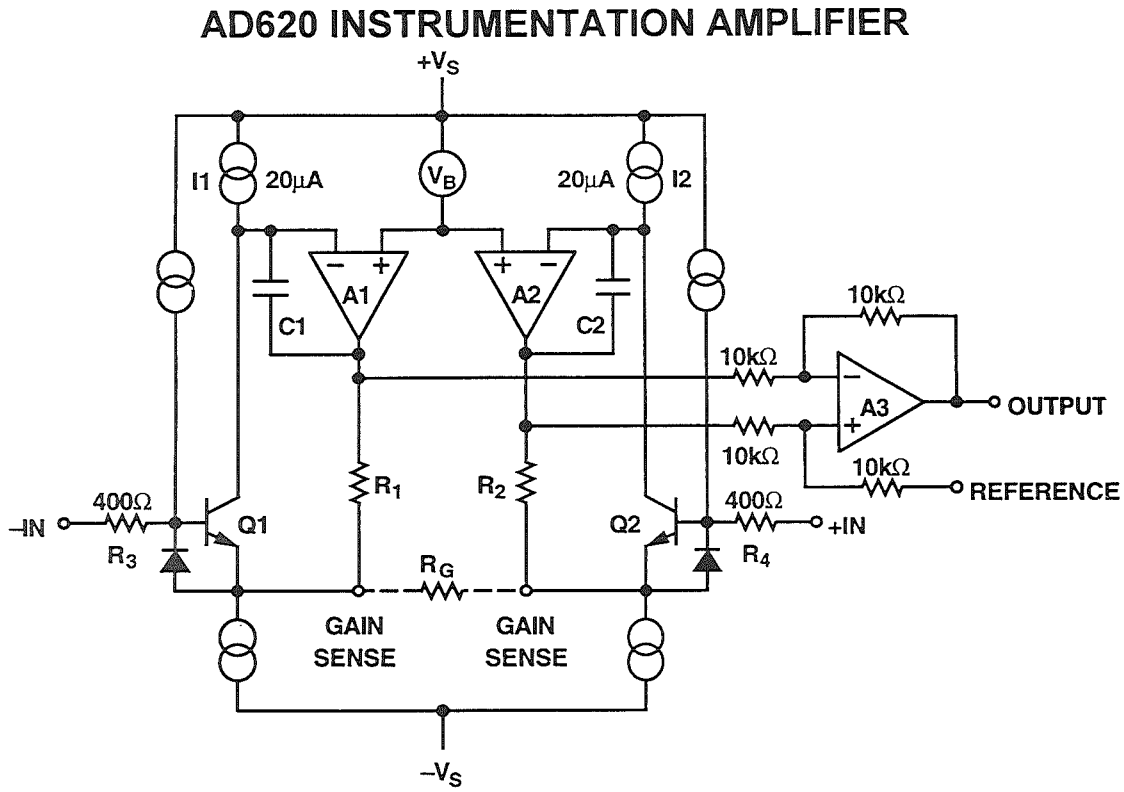


Figure 2.7

Absolute value laser wafer trimming allows the user to program gain accurately (to 0.15% at G=100) with this single resistor. The absolute accuracy and temperature coefficient of this resistor directly affects the in-amp gain accuracy and drift. Gain accuracy and drift specifications for this type of in-amp assume a perfect external gain-setting resistor. Therefore, a low TC (<25ppm/°C) metal film resistor should be chosen, preferably with a 0.1% or better accuracy.

Often specified as having a gain range of 1 to 1000, or 1 to 10,000, many in-amps will work at higher gains, but the manufacturer will not guarantee a specific level of performance at these high gains. In practice, as the gain-setting resistor becomes smaller, any errors due to the resistance of the metal runs and bond wires become significant. These errors, along with an increase in noise and drift, may make higher single-stage gains impractical.

In a pin-programmable in-amp such as the AD621, the gain setting resistors are internal, well matched, and the gain accuracy and gain drift specifications include their effects.

The *gain error* specification is the maximum deviation from the gain equation. Monolithic in-amps such as the AD624 have very low factory trimmed gain errors, with its maximum error of 0.05% at G = 1 and 1% at G = 1000 being typical for a high quality in-amp. Notice that the gain error increases with increasing gain. Although externally connected gain networks allow the user to set the gain exactly, the temperature coefficients of the external resistors and the temperature differences between individual resistors within the network all

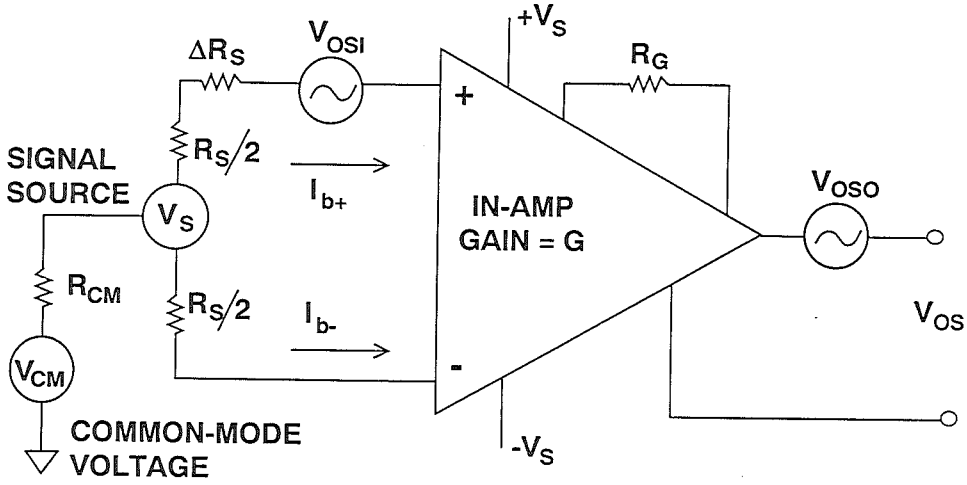
contribute to the overall gain error. If the data is eventually digitized and presented to a digital processor, it may be possible to correct for gain errors by measuring a known reference voltage and then multiplying by a constant.

Nonlinearity is defined as the maximum deviation from a straight line on the plot of output versus input. The straight line is drawn between the end-points of the actual transfer function. Gain nonlinearity in a high quality in-amp is usually 0.01% or less, and is relatively insensitive to gain over the recommended gain range.

The total input offset voltage of an in-amp consists of two components (see Figure 2.8). Input offset voltage, V_{OSI}, is that component of input offset which is reflected to the output of the in-amp by the gain G. Output offset voltage, V_{OSO}, is independent of gain. At low gains, output offset voltage is dominant, while at high gains input offset dominates. The output offset voltage drift is normally specified as drift at G=1 (where input effects are insignificant), while input offset voltage drift is given by a drift specification at a high gain (where output offset effects are negligible). The total output offset error, referred to the input (RTI), is equal to $V_{OSI} + V_{OSO}/G$. In-amp data sheets may specify V_{OSI} and V_{OSO} separately or give the total RTI input offset voltage for different values of gain.

Input bias currents also produce errors in in-amp circuits (see Figure 2.8). If the source resistance, R_S, is unbalanced by an amount, ΔR_S, (often the case in bridge circuits), then there is an input offset voltage error due to the bias current equal to $I_b \Delta R_S$ (assuming that $I_{b+} \approx I_{b-} = I_b$). This error is reflected to the output, scaled by the gain G. The input offset current, I_{OS}, creates an input offset voltage error across the source resistance, $R_S + \Delta R_S$, equal to $I_{OS}(R_S + \Delta R_S)$, which is also reflected to the output by the gain, G.

IN-AMP OFFSET VOLTAGE AND BIAS CURRENT MODEL



$$I_{OS} = \left| I_{b+} - I_{b-} \right|, \quad V_{OS} = V_{OSO} + G\left[V_{OSI} + I_b \Delta R_S + I_{OS}(R_S + \Delta R_S)\right]$$

Figure 2.8

In-amp common-mode error is a function of both gain and frequency as shown in Figure 2.9. It is customary to specify in-amp CMR for a 1kΩ source impedance unbalance. The RTI error is obtained by dividing the common mode voltage, V_{cm}, by the common-mode rejection ratio, CMRR.

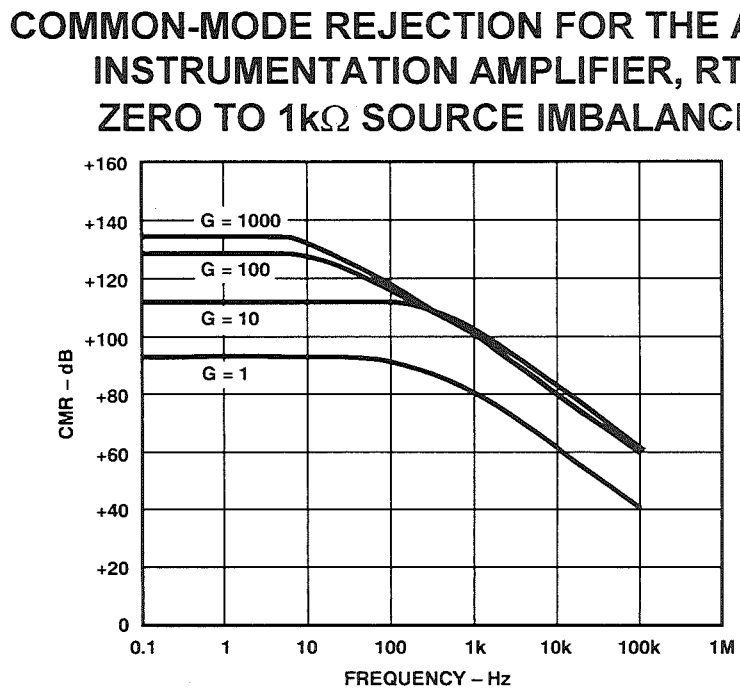


Figure 2.9

Power supply rejection (PSR) is also a function of gain and frequency (Figure 2.10). For in-amps, it is customary to specify the sensitivity to each power supply separately.

Now that all DC error sources have been accounted for, a worst case error budget can be calculated by reflecting all the sources to the in-amp input (Figure 2.11).

POSITIVE AND NEGATIVE POWER SUPPLY REJECTION (PSR) FOR THE AD620 REFERRED TO INPUT

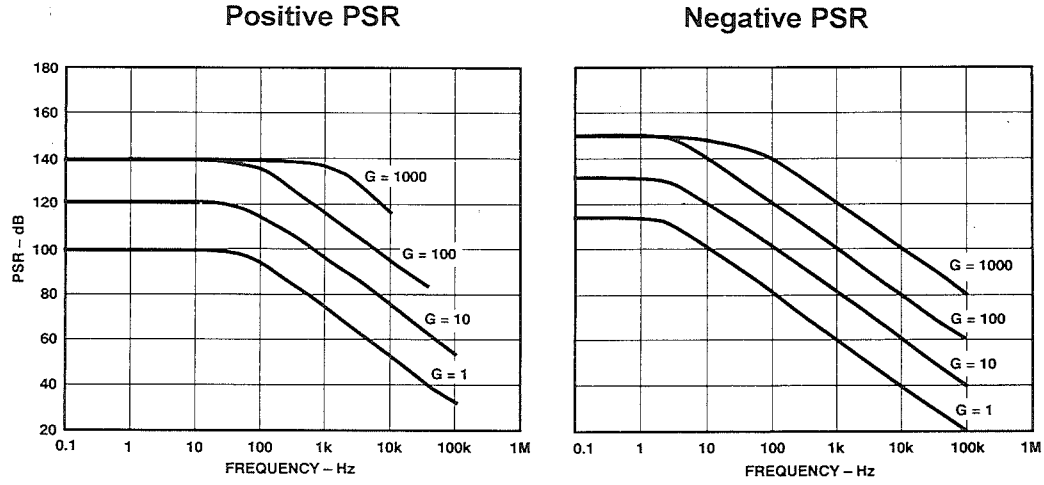


Figure 2.10

INSTRUMENTATION AMPLIFIER DC ERRORS REFERRED TO THE INPUT

ERROR SOURCE	REFERRED TO INPUT (RTI) VALUE
Gain Accuracy (%)	Gain Accuracy × FS Input
Gain Nonlinearity (%)	Gain Nonlinearity × FS Input
Input Offset Voltage, V_{osi}	V_{osi}
Output Offset Voltage, V_{oso}	V_{oso} / G
Input Bias Current, I_b Flowing in ΔR_S	$I_b \Delta R_S$
Input Offset Current, I_{os} Flowing in R_S	I_{os} ($R_S + \Delta R_S$)
Common Mode Input Voltage, V_{cm}	V_{cm} / CMRR
Power Supply Variation, ΔV_S	ΔV_S / PSRR

Figure 2.11

Instrumentation Amplifier Noise Sources

Since in-amps are primarily used to amplify small precision signals, it is important to understand the effects of the associated noise sources. The in-amp noise model is shown in Figure 2.12. There are two sources of input voltage noise. The first is represented as a noise source, V_{ni}, in series with the input, as in a conventional op amp circuit. This noise is reflected to the output by the in-amp gain, G. The second noise source is the output noise, V_{no},represented as a noise voltage in series with the in-amp output. The output noise is referred to the input by dividing by the gain, G.

There are four noise sources associated with the input noise currents I_{n+} and I_{n-}. Even though I_{n+} and I_{n-} are usually equal ($I_{n+} \approx I_{n-} = I_n$), they are uncorrelated, and therefore, the noise they each create must summed in a root-sum-squares (RSS) fashion. I_{n+} flows through one half of R_S, and I_{n-} the other half. This generates two noise voltages, each having an amplitude, $I_nR_S/2$. The third and fourth noise voltage is due to I_{n+} and I_{n-} flowing through the common-mode resistance, R_{cm}. There are two corresponding noise voltages generated, each having an amplitude of I_nR_{cm}. Each of these four noise sources is reflected to the output by the in-amp gain, G.

The total output noise, V_{on}, is calculated by combining all six noise sources in an RSS manner:

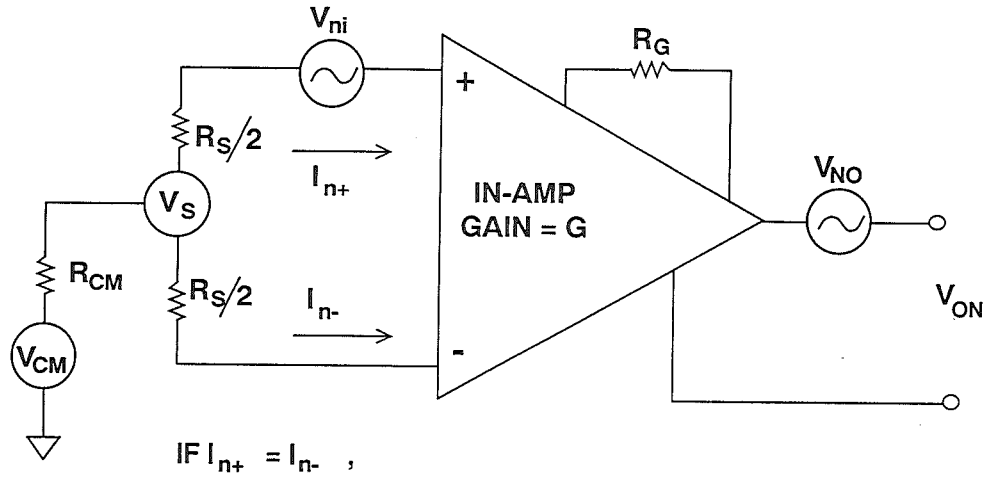
$$V_{on} = \sqrt{V_{no}^2 + G^2\left(V_{ni}^2 + \frac{I_{n+}^2R_S^2}{4} + \frac{I_{n-}^2R_S^2}{4} + I_{n+}^2R_{cm}^2 + I_{n-}^2R_{cm}^2\right)}$$

Let $I_{n+} = I_{n-} = I_n$,

$$V_{on} = \sqrt{V_{no}^2 + G^2\left(V_{ni}^2 + \frac{I_n^2R_S^2}{2} + 2I_n^2R_{cm}^2\right)}$$

The total noise, referred to the input (RTI) is simply the above expression divided by the in-amp gain, G.

INSTRUMENTATION AMPLIFIER NOISE MODEL



$$\text{IF } I_{n+} = I_{n-},$$

$$V_{ON} = \sqrt{V_{NO}^2 + G^2\left(V_{ni}^2 + \frac{I_n^2 R_S^2}{2} + 2I_n^2 R_{CM}^2\right)}$$

Figure 2.12

In-amp data sheets often present the total voltage noise RTI as a function of gain (Figure 2.13). This noise spectral density includes both the input (V_{ni}) and output (V_{no}) noise contributions. Figure 2.13 also shows the input current noise spectral density for the AD620. As in the case of op amps, the total noise RTI must be integrated over the in-amp closed-loop bandwidth to compute the RMS value. The bandwidth may be determined from data sheet curves which show frequency response as a function of gain. Figure 2.14 shows such a curve for the AD620.

AD620 IN-AMP INPUT VOLTAGE AND CURRENT NOISE

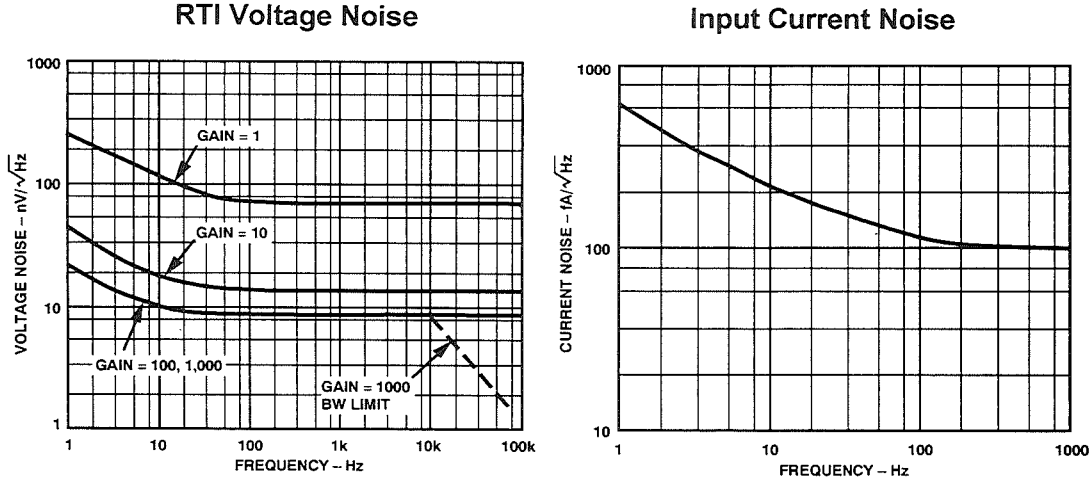


Figure 2.13

AD620 IN-AMP FREQUENCY RESPONSE

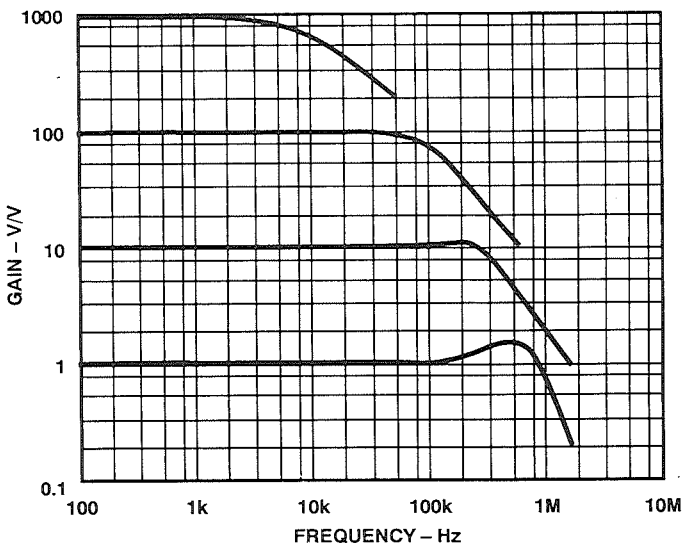


Figure 2.14

SUMMARY OF INSTRUMENTATION AMPLIFIER TYPICAL CHARACTERISTICS

- Balanced, High Impedance Inputs (>$10^9\Omega$)
- High Common Mode Rejection (CMR) : 70dB to >100dB @ 60Hz
- One Resistor Sets Gain (typically, G = 1 to 10,000, 0.2% Accuracy)

  External Resistor, User Selectable or

  Pin-Programmable Internal Resistors
- Low Noise (<10nV/√Hz and 100fA/√Hz @ 1kHz)
- Low Nonlinearity (< 0.01%)
- Bandwidth: 500kHz to 1MHz
- Low Input Offset Voltage (100μV) and Input Bias Current (1nA for Bipolar Input, 50pA for FET Input)

Figure 2.15

ACTIVE FEEDBACK AMPLIFIERS

The AD830 represents Analog Devices' first amplifier product to embody a powerful new amplifier topology. Referred to as *active feedback*, the topology used in the AD830 provides inherent advantages in the handling of high-speed differential signals, differing system grounds, level shifting, and low distortion high frequency amplification. In addition, it makes possible the implementation of many functions not realizable with single op amp circuits, and is often superior to op amp based equivalent circuits. The AD830 is a versatile high-speed amplifier with excellent video performance, but it is not a general purpose in-amp with extremely low DC errors.

The AD830 topology, reduced to its elemental form, is shown in Figure 2.16. Nonideal effects such as nonlinearity, bias currents and limited input range are omitted from this model for simplicity. The key feature of this topology is the use of two, identical voltage-to-current converters, G_M, that make up input and feedback signal interfaces. They are labeled with inputs V_X and V_Y, respectively. These voltage-to-current converters' inputs are fully differential, highly linear, are high impedance, and have wide common-mode, small signal voltage ranges. The device can handle ±1V differential input signals in the linear mode. The inputs provide common-mode rejection, low distortion, and negligible loading on the source. The label, G_M, is meant to convey that the transconductance is a large signal quantity, unlike in the front end of most op amps which are not linear, except with minimal differential input. The two G_M stage current outputs, I_X and I_Y, sum together at the high impedance node, which is characterized by an equivalent resistance and capacitance connected to an "AC" ground. A unity voltage gain output stage follows the high impedance node to provide buffering. Relative to either input, the open loop gain, A_{OL}, is set by the transconductance, G_M, working into the resistance, R_P: $A_{OL} = G_M \times R_P$. The unity gain frequency, ω_{odB}, for the open loop gain is established by the transconductance, G_M, working into the capacitance, C_C: $\omega_{odB} = G_M/C_C$.

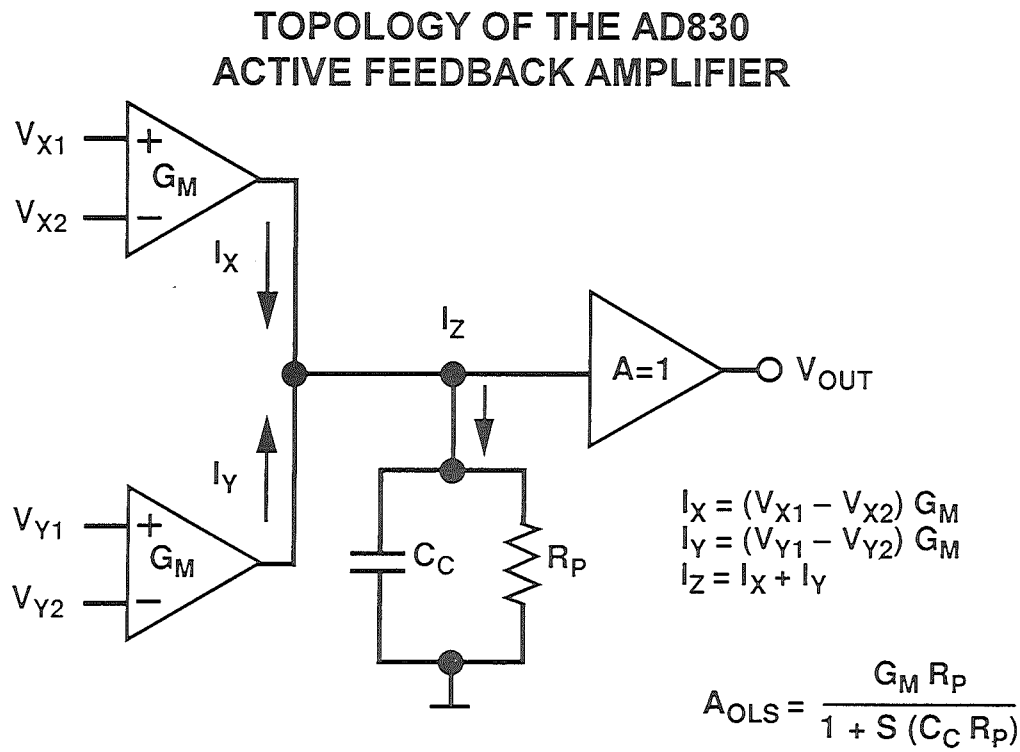
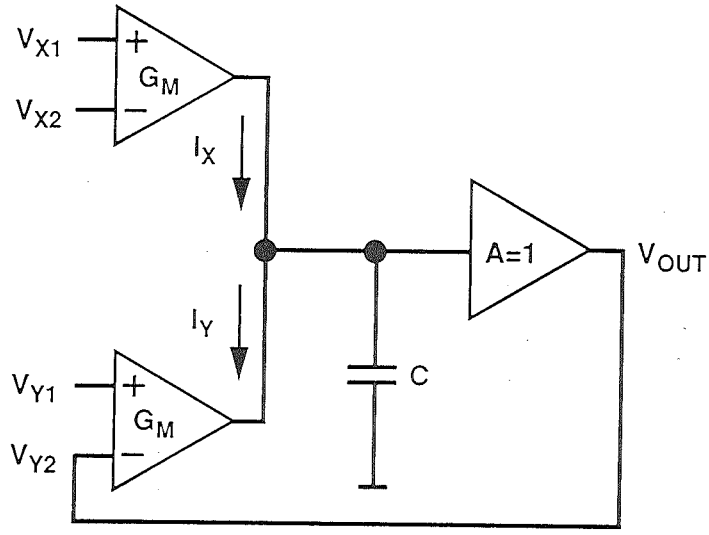


Figure 2.16

Precise amplification is accomplished through closed loop operation as shown in Figure 2.17. Voltage feedback is implemented via the Y G_M stage, where the output is connected to the –Y input for negative feedback. An input signal is applied across the X G_M stage, either fully differentially, or single-ended referred to common. It produces a current signal which is summed at the high impedance node with the output current from the Y G_M stage. Negative feedback nulls this sum to a small error current necessary to develop the output voltage at the high impedance node. The error current is usually negligible, so the null condition essentially forces the Y G_M output stage current to exactly equal the X G_M output current. Since the two transconductances are identical, the differential voltage across the Y inputs equals the negative of the differential voltage across the X input: $V_Y = -V_X$,or more precisely, $V_{Y2} - V_{Y1} = V_{X1} - V_{X2}$. This simple relationship provides the basis to analyze any function possible with the AD830, including any feedback situation.

CLOSED LOOP CONNECTION FOR THE AD830 ACTIVE FEEDBACK TOPOLOGY



$$V_{X1} - V_{X2} = V_{Y2} - V_{Y1}$$

FOR $V_{Y2} = V_{OUT}$

$$V_{OUT} = (V_{X1} - V_{X2} + V_{Y1}) \frac{1}{1 + S(C_C/G_M)}$$

Figure 2.17

The bandwidth of the circuit is defined by the G_M and the capacitor, C_C. The highly linear G_M stages give the amplifier a single-pole response, excluding the output amplifier and loading effects. The bandwidth and general dynamic behavior is symmetrical (identical) for the noninverting and the inverting connections of the AD830. In addition, the input impedance and CMRR are the same for either connection. This is very advantageous, and unlike the situation with a voltage or current feedback amplifier, where there is a distinct difference in performance between the inverting and noninverting gain stages. The practical importance of this cannot be overemphasized and is a key feature offered by the AD830 active feedback topology.

The AD830 is a flexible device which may be used in a number of configurations with excellent video performance. Figure 2.18 shows how the AD830 may be configured as an instrumentation amplifier. The input signal is connected differentially to the internal V-to-I converter #1. The gain is set via the feedback resistors, R2 and R1, in the same manner as a noninverting op amp circuit. The polarity of the gain is established by the relative connections at input pins 1 and 2. Inverting gain is set by reversing the connections. As in a conventional voltage feedback op amp, the bandwidth decreases with increasing gain.

GAIN-OF-N INSTRUMENTATION AMPLIFIER USING THE AD830

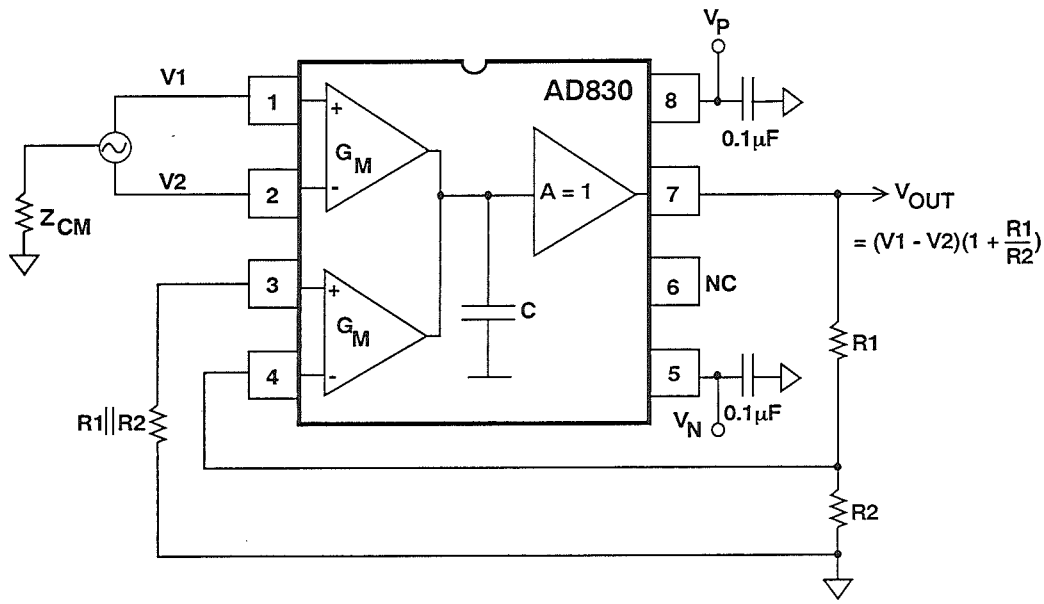


Figure 2.18

The video cable receiver/driver circuit shown in Figure 2.19 not only provides ground noise rejection, but also supplies a gain-of-two so that the AD830 output can drive a source and load terminated 75Ω cable without signal attenuation. The 499Ω resistors set the gain at 2, and the 249Ω resistor between pin 3 and ground cancels the offset due to the input bias currents. The signal from system "A" is received differentially by the AD830 and is reproduced relative to the ground in system "B". Common mode noise is rejected by the excellent CMRR of the AD830 (50dB at 10MHz).

VIDEO CABLE RECEIVER/DRIVER USING THE AD830

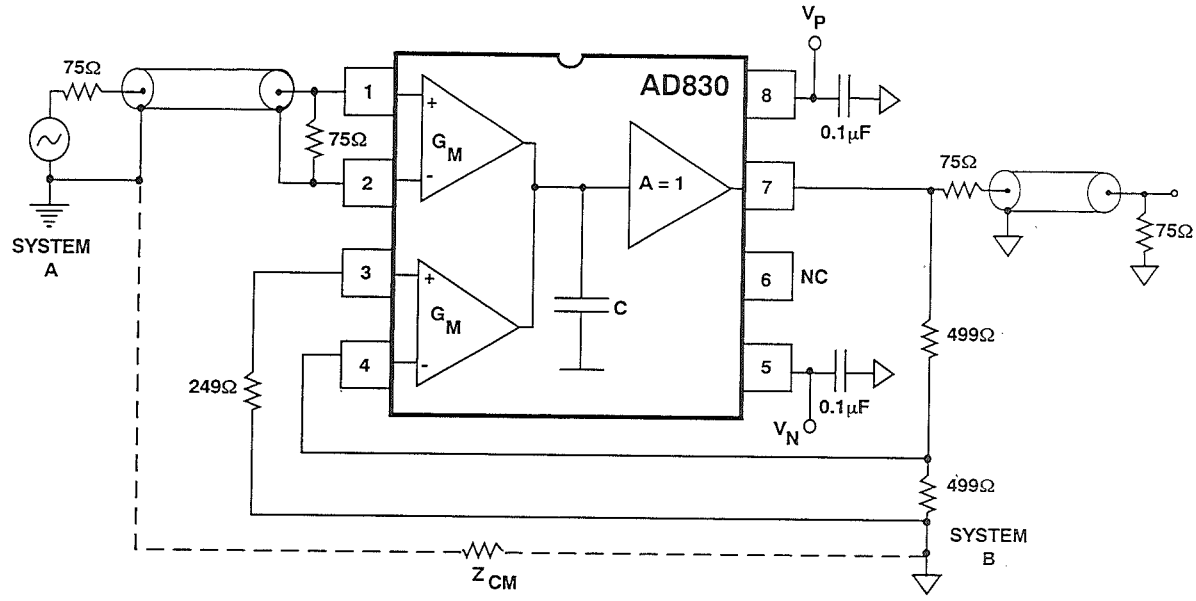


Figure 2.19

The video loop-through connection is a popular method of connecting several different pieces of equipment. High input impedance differential amplifiers connect to taps along the distribution cable. The cable is terminated in its characteristic impedance at the source and at the far end. The AD830 makes an ideal choice for this loop-through amplifier because of its high input impedance and good common mode rejection at high frequencies. The high input impedance provides negligible loading on the cable. More significantly, the benign loading is maintained while the AD830 is powered down. Figure 2.20 shows a typical loop-through connection using the AD830.

VIDEO LOOP-THROUGH CONNECTION USING THE AD830

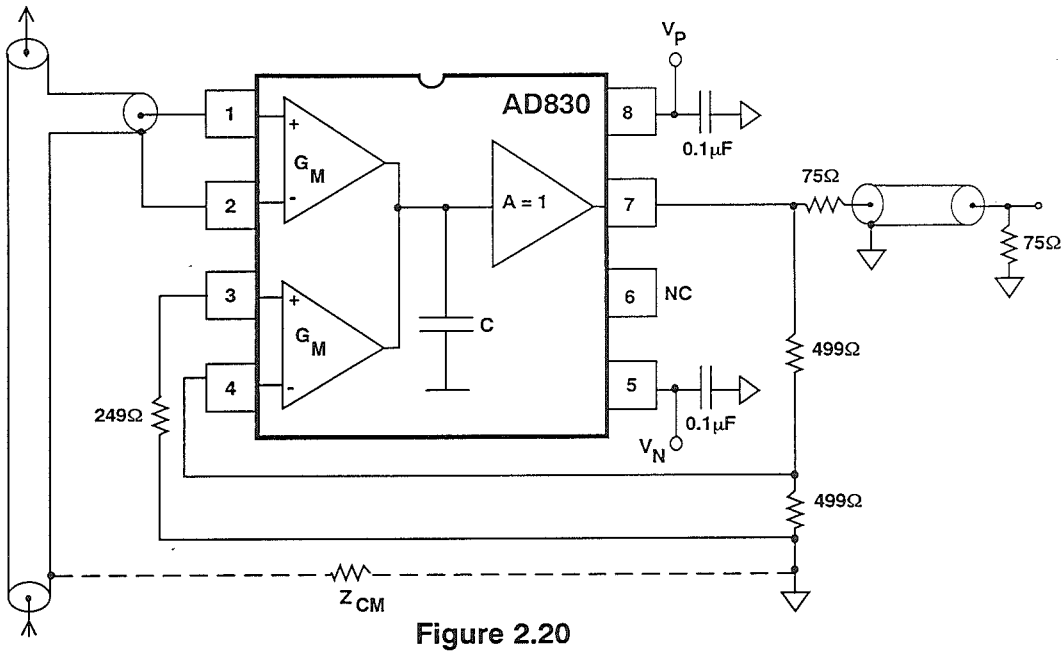


Figure 2.20

Key specifications for the AD830 are shown in Figure 2.21. CMRR and frequency response are shown in Figure 2.22.

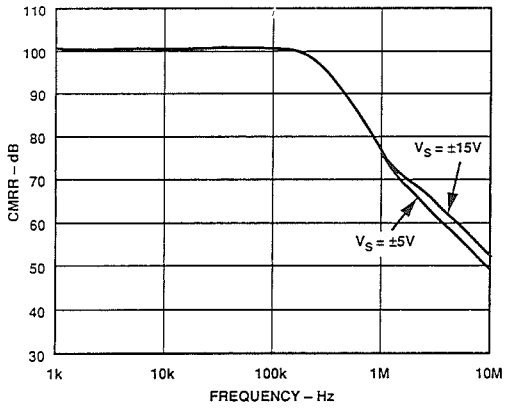
AD830 ACTIVE FEEDBACK VIDEO DIFFERENCE AMPLIFIER KEY SPECIFICATIONS

- Common Mode Voltage Range: ±11.5V (for V_{SY} = ±15V)
- Differential Voltage Range: ±2V
- CMRR: 60dB @ 4.43MHz, 50dB @ 10MHz
- Bandwidth: 50MHz
- Distortion: -60dBc @ 4.43Mhz
- Differential Gain: 0.1%, Differential Phase: 0.1°

Figure 2.21

AD830 CMR AND FREQUENCY RESPONSE (G = 1) FOR ±5V AND ±15V SUPPLIES

CMRR



FREQUENCY RESPONSE

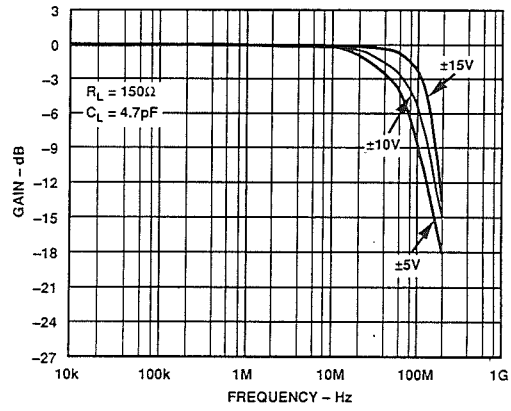


Figure 2.22

PROGRAMMABLE GAIN AMPLIFIERS

Most systems with wide dynamic range need some method of adjusting the input signal level to the analog-to-digital-converter (ADC). The ADC compares the input signal to a fixed voltage reference (+5V or +10V are typical values). To achieve the rated precision of the converter, the maximum input should be fairly near its full scale voltage. However, transducers have a wide range of output voltages. High gain is needed for a small sensor voltage, but with a large transducer output, a high gain will cause the amplifier or ADC to saturate. So some type of controllable gain device is needed. Such a device has a gain that is controlled by a DC voltage or, more commonly, a digital input. This device is known as a *programmable gain amplifier*, or PGA. Programmable gain amplifiers have a variety of applications, and Figure 2.23 lists some of them.

PGA APPLICATIONS

- Instrumentation
- Photodiode Circuits
- Ultrasound Preamplifiers
- Sonar
- Wide Dynamic Range Sensors
- Driving ADCs
- Automatic Gain Control (AGC) Loops

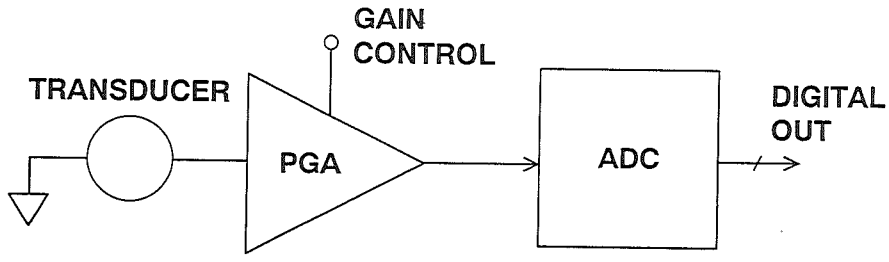
Figure 2.23

A PGA is usually located between a sensor and its ADC. Additional signal conditioning may take place before or after the PGA, depending on the application. For example, a photodiode needs a current to voltage converter between it and the PGA. In most other systems, it is better to place the gain first, and condition a larger signal. This reduces errors introduced by the signal conditioning circuitry.

To understand the benefits of variable gain, assume an ideal PGA with two settings, gains of one and two. The dynamic range of the system is increased by 6dB. Increasing the gain to four results in a 12dB increase in dynamic range.

If the LSB of an ADC is equivalent to 10mV of input voltage, the ADC cannot resolve smaller signals, but when the gain of the PGA is increased to two, input signals of 5mV may be resolved. Thus, the processor can combine PGA gain information with the digital output of the ADC to increase its resolution by one bit. Essentially, this is the same as adding additional resolution to the ADC.

PROGRAMMABLE GAIN AMPLIFIERS (PGAs)



- Used to Increase Dynamic Range of Circuit
- A PGA With a Gain From 1 To 2 Theoretically Increases the Dynamic Range by 6dB, A Gain of 1 To 4 Gives 12dB Increase, etc.

Figure 2.24

In practice, PGAs are not ideal, and their error sources must be studied. The most fundamental problem with PGA design is accurate gain programming. Electromechanical relays have minimal R_{ON}, but are otherwise unsuitable for gain switching. They are slow, large, and expensive. Silicon switches, as discussed in the section on switches and multiplexers (Section 8 of this book), have quite large R_{ON}, which is both voltage- and temperature-variable, and stray capacities, which may affect the AC parameters of a PGA using them.

PGA DESIGN ISSUES

- How to Switch the Gain
- Effects of Switch On-Resistance
- Gain Accuracy
- Gain Linearity
- Bandwidth versus Frequency versus Gain
- Offset
- Temperature Effects on Gain and Offset
- Settling Time After Switching

Figure 2.25

To understand how R_{ON} can affect the performance of a PGA, let us consider a poor PGA design (Figure 2.26). An op amp is configured in the standard non-inverting gain circuit with 4 different gain setting resistors, each grounded by a switch. Most silicon switches have ON resistance in the range of 100Ω-500Ω. Even if the ON resistance were as low as 25Ω, the error for a gain of 16 would be 2.4%, much worse than 8-bits. Furthermore, R_{ON} drifts over temperature, and varies from switch to switch. If the value of the feedback and gain setting resistors were increased, noise and offset would become a problem. The only way to achieve accuracy with this circuit is to replace silicon switches with relays which have virtually no ON resistance.

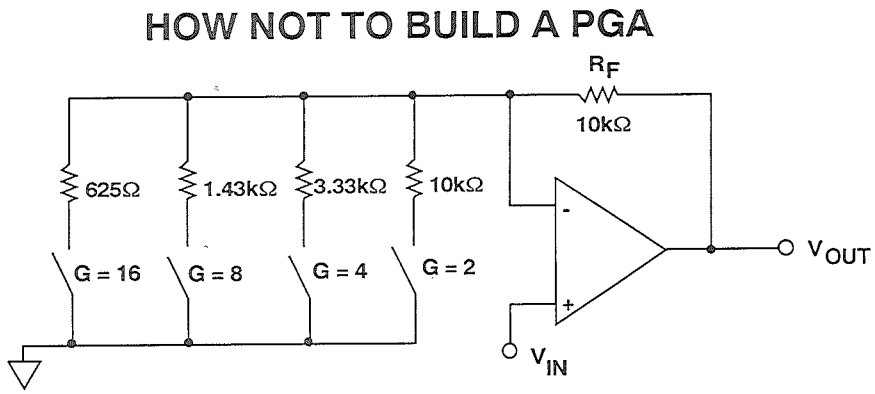
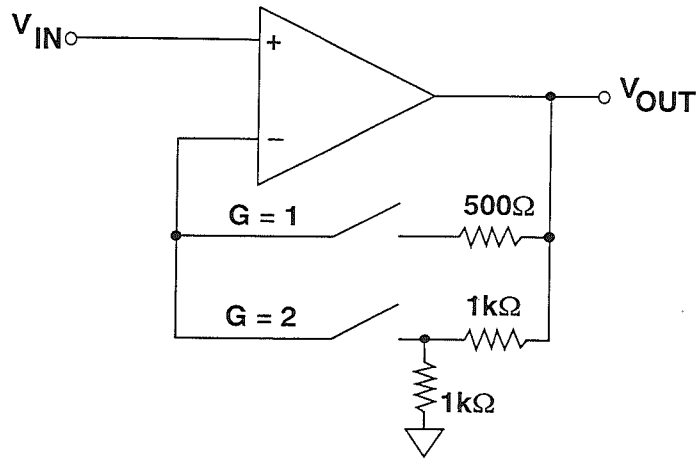


Figure 2.26

It is better to use a circuit where R_{ON} is unimportant. In Figure 2.27, the switch is placed in series with the inverting input of an op amp. Since the input impedance of an op amp is very large, the R_{ON} of the switch is irrelevant. The gain is now determined by the external resistors. The R_{ON} may add a small offset error if the op amp bias current is significant.

ALTERNATE CONFIGURATION MAKES THE EFFECTS OF R_{on} NEGLIGIBLE



- R_{on} is Not in Series With Gain Setting Resistors
- R_{on} is Very Small Compared to Input Impedance
- Only a Slight Offset Error Occurs Due to the Bias Current Flowing Through the Switch

Figure 2.27

The AD526 amplifier uses this method of building a PGA and integrates it onto a single chip. The AD526 has 5 binary gain settings from 1 to 16, and its internal JFET switches are connected to the inverting input of the amplifier.

The gain resistors are laser trimmed. The maximum gain error is only 0.02%, far better than the 2.4% error in Figure 2.26. The linearity is also very good at 0.001%. The AD526 is controlled by a latched digital interface.

AD526 MONOLITHIC SOFTWARE PROGRAMMABLE PGA

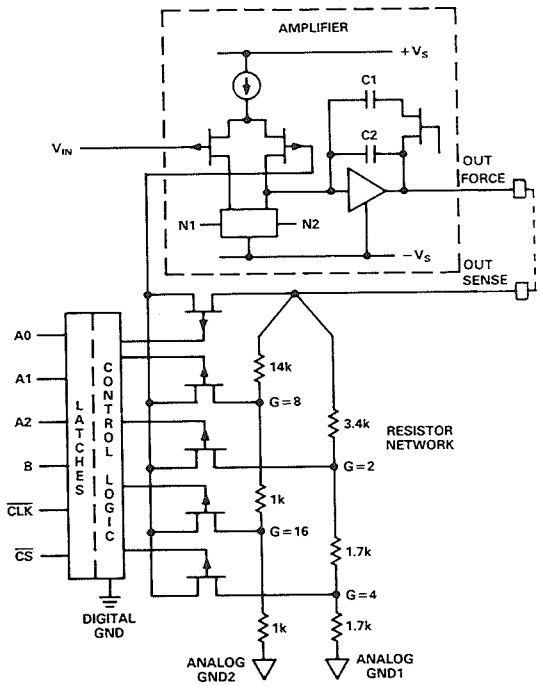


Figure 2.28

AD526 SOFTWARE PROGRAMMABLE PGA KEY FEATURES

- Software Programmable Binary Gains From 1 to 16
- Low Bias Current JFET Input Stage
- Worst Case Gain Error is 0.02% (12 Bit Performance)
- Gain Nonlinearity is 0.001% Maximum
- Latched TTL Compatible Control Inputs

Figure 2.29

This same design can be used to build the discrete PGA shown in Figure 2.30. It uses a single op amp, a quad switch, and precision resistors. The low-noise AD797 replaces the JFET input op amp of the AD526, but almost any voltage feedback op amp could be used in this circuit. The ADG412 was picked for its low ON resistance of 35Ω.

The resistors were chosen to give gains of 1, 10, 100 and 1000, but if other gains are required, the resistor values may easily be altered. Ideally, a trimmed resistor network should be used both for initial gain accuracy and for low drift over temperature. The 20pF capacitor ensures stability and holds the output voltage when the gain is switched. The control signal to the switches turns one switch off a few nanoseconds before the second switch turns on. During this break, the op amp is open-loop. If the capacitor was not used, the output would start slewing. Instead, the capacitor holds the output voltage during the switching. Since the time that both switches are open is very short, only 20pF is needed. For slower switches, a larger capacitor may be necessary.

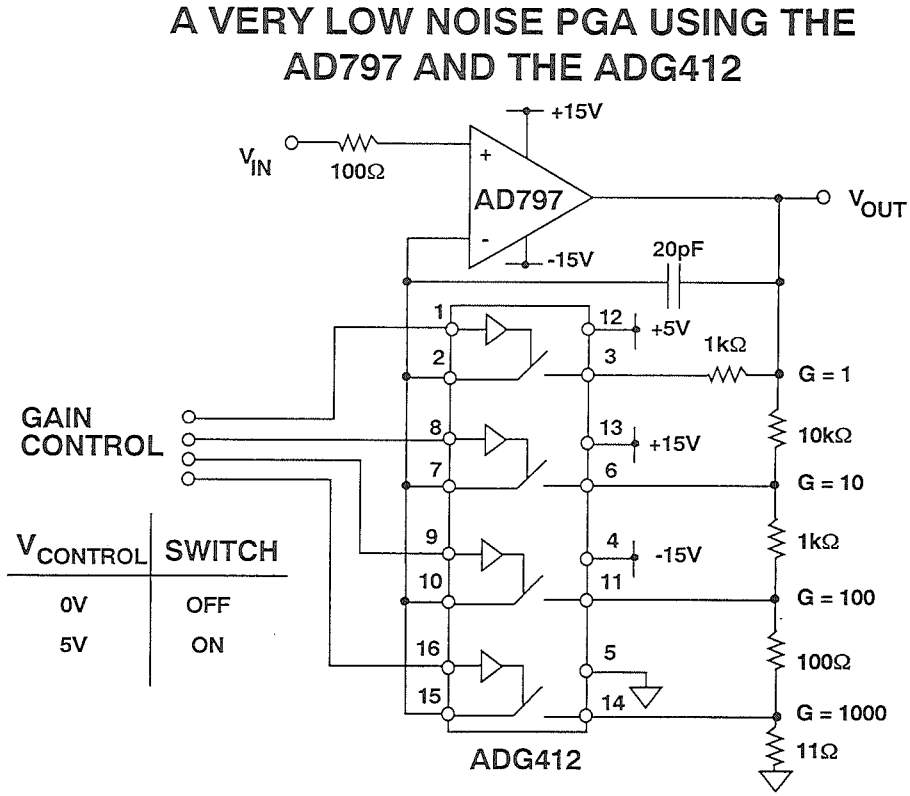


Figure 2.30

The PGA's input voltage noise spectral density is only 1.65nV/√Hz at 1kHz, only slightly higher than the noise performance of the AD797 alone. The increase is due to the noise of the ADG412, and the current noise of the AD797 flowing through the ON resistance. The noise was measured at a gain of 1000.

The accuracy of the PGA is important in determining the overall accuracy of a system. The AD797 has a bias current of 0.9μA, which, flowing in 35Ω R_{ON}, results in an additional offset error of 31.5μV (Figure 2.31). Combined with the AD797 offset, the total V_{OS} becomes 71.5μV (max). Offset temperature drift is affected by the change in bias current and ON resistance. Calculations show that the total temperature coefficient increases from 0.6μV/°C to 1.6μV/°C. These errors are small, and may not matter, but it is important to be aware of them. In practice, circuit accuracy and TC will be determined by the external resistors. Input characteristics such as common mode range and input bias current are determined solely by the AD797. The circuit could be converted to single supply simply by changing the op amp. The switches do not need to be changed.

AD797 PGA ACCURACY

- R_{on} Adds Additional Input Offset And Drift:

  $\Delta V_{OS} = I_b R_{on} = (0.9\mu A)(35\Omega) = 31.5\mu V$ (max)

  Total V_{OS} = 40μV + 31.5μV = 71.5μV (max)
  (Note: 40μV is Due To The AD797B)

- Temperature Drift Due To R_{on} :

  At +85°C, $\Delta V_{OS} = (2\mu A)(45\Omega) = 90\mu V$ (max), TC = 1μV/°C

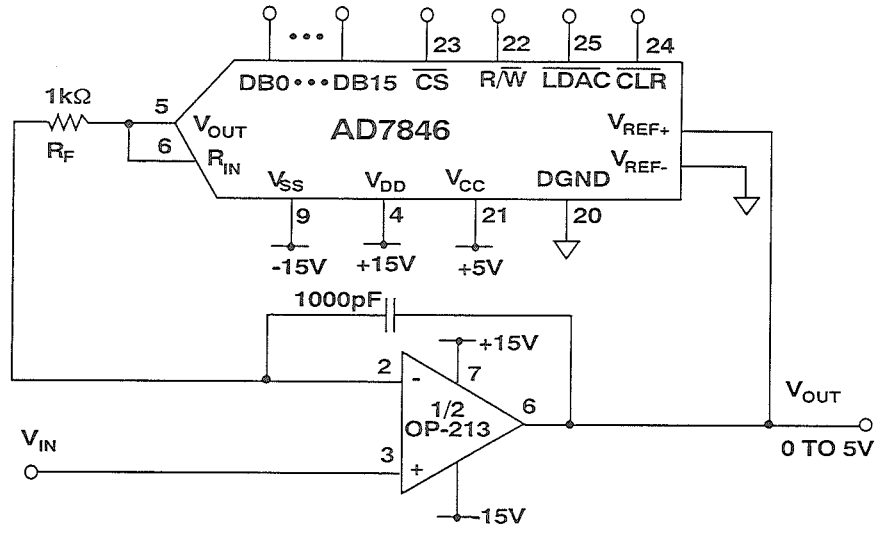
- Temperature Coefficient Total:

  $\Delta V_{OS} / \Delta T$ = 0.6μV/°C + 1.0μV/°C = 1.6μV/°C (max)
  (Note: 0.6μV/°C is due to the AD797B)

Figure 2.31

Another PGA configuration uses a DAC in the feedback loop of an op amp to adjust the gain under digital control (Figure 2.32). The digital code of the DAC controls its attenuation. Attenuating the feedback signal increases the closed-loop gain. A non-inverting PGA of this type requires a multiplying DAC with a voltage output (a multiplying DAC is a DAC with a wide reference voltage range *which includes zero*). For most applications of the PGA, the reference input must be capable of handling bipolar signals. The AD7846 is a 16-bit converter that meets these requirements. In this application, it is used in standard 2-quadrant multiplying mode. The OP-213 is a low drift, low noise amplifier, but the choice of amplifier is flexible, and depends on the application. The input voltage range depends on the output swing of the AD7846, which is 3V less than the positive supply, and 4V above the negative supply. A 1000pF capacitor is used in the feedback loop for stability.

ACCURATE BINARY GAIN PGA
USES DAC IN OP-AMP FEEDBACK LOOP



- Multiplying DAC in Feedback Loop Adjusts Gain
- $G = \frac{2^{16}}{\text{Decimal Value of Digital Code}}$

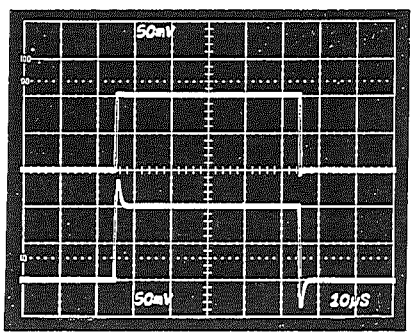
Figure 2.32

The gain of the circuit is set by adjusting the digital inputs of the DAC, according to the equation given in Figure 2.32. D0-15 represents the decimal value of the digital code. For example, if all the bits were set high, the gain would be 65,536/65,535 = 1.000015. If the 8 least significant bits are set high and the rest low, the gain would be 65,536/255 = 257.

Figure 2.33 shows the small signal response at a gain of 1 with a 100mV square wave input. The bandwidth is a fairly high 4MHz. However, this does reduce with gain, and for a gain of 256, the bandwidth is only 600Hz. If the gain-bandwidth product were constant, the bandwidth in a gain of 256 should be 15.6kHz; but the internal capacitance of the DAC reduces the bandwidth to 600Hz.

BINARY GAIN PGA PERFORMANCE

SMALL SIGNAL RESPONSE



Top Trace: Input, 50mV/div.
Bottom Trace: Output, 50mV/div.
Horizontal Scale: 10µs/div.

Bandwidth (G=+1) = 4MHz
Bandwidth (G=+256) = 600Hz

Nonlinearity (G=+1) = 0.001%

Offset = 100µV

Noise = 50nV/√Hz

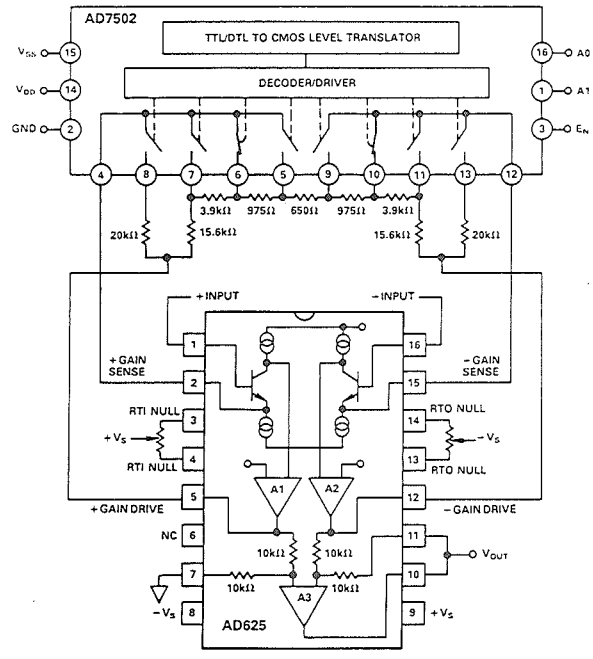
Gain Accuracy (G=+1) = 0.003%
Gain Accuracy (G=+256) = 0.1%

Figure 2.33

The gain accuracy of the circuit is determined by the resolution of the DAC and the gain setting. At a gain of 1, all bits are on, and the accuracy is determined by the DNL specification of the DAC, which is ±1 LSB maximum. Thus, the gain accuracy is equivalent to 1LSB in a 16-bit system, or 0.003%. However, as the gain is increased, fewer of the bits are on. For a gain of 256, only bit 8 is turned on. The gain accuracy is still dependent on the ±1 LSB of DNL, but now that is compared to only the lowest 8 bits. Thus, the gain accuracy is reduced to 1 LSB in a 8-bit system, or 0.4%. If the gain is increased above 256, the gain accuracy is reduced further. The designer must determine an acceptable level of accuracy. In this particular circuit, the gain was limited to 256.

There are often applications where a PGA with differential inputs is needed, instead of the single ended types discussed so far. The AD625 combines an instrumentation amplifier topology with gain switching capabilities to accomplish 12-bit gain accuracy (Figure 2.34). An external switch is needed to switch between different gain settings. In the example shown, resistors were chosen for gains of 1, 4, 16, and 64. Other features of the AD625 are 0.001% nonlinearity, wide bandwidth, and very low input noise.

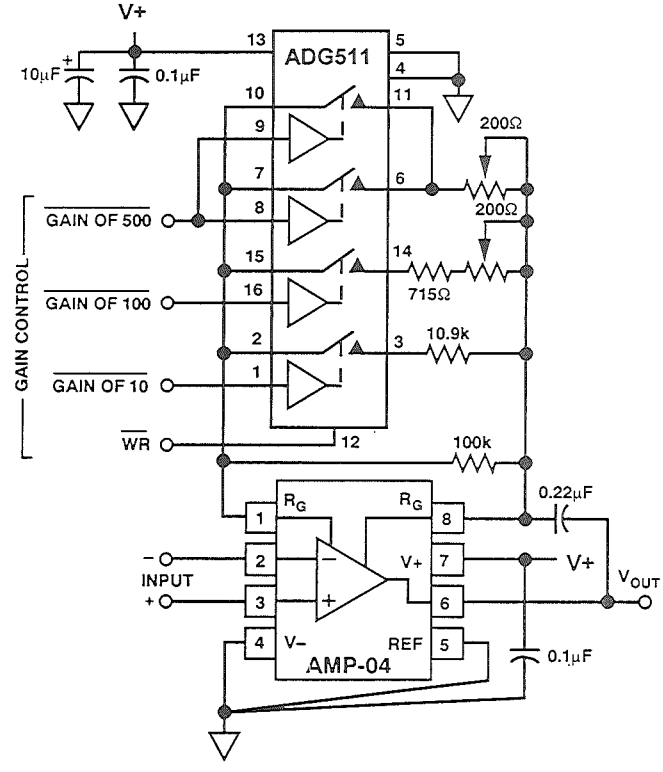
A SOFTWARE PROGRAMMABLE GAIN AMPLIFIER



- G = 1, 4, 16, 64
- Differential Input Stage
- 12 Bit Gain Accuracy
- Nonlinearity = ± 0.001% (G = 1 to 256)
- Low Noise: 4nV/√Hz
- 25MHz Gain-Bandwidth Product

Figure 2.34

SINGLE SUPPLY (+5V TO +10V) INSTRUMENTATION PGA



- $G = 100k\Omega/R_G$
- R_G Is a Combination of Switch R_{on} and the External Resistor
- Trim Required at High G Due to Uncertainty Of R_{on}
- Relays Can Be Used to Avoid Trim

Figure 2.35

Non-inverting PGA circuits using an op amp are easily adaptable to single supply operation, but the instrumentation amplifier topology does not lend itself to single supply applications. However, the AMP-04 can be used with an external switch to produce the single supply instrumentation PGA shown in Figure 2.35. This circuit has selectable gains of 1, 10, 100, and 500, which are controlled by an ADG511. The ADG511 was chosen as a single supply switch with a low R_{ON} of 45Ω. The gain of this circuit is dependent on the R_{ON} of the switches. Trimming is required at the higher gains to achieve accuracy. At a gain of 500, two switches are used in parallel, but their resistance causes a 10% gain error in the absence of adjustment.

Certain ADCs (AD7710, AD7711, AD7712, AD7713) have built in PGAs. Circuit design is much easier because an external PGA and its control logic are not needed. Furthermore, all the errors of the PGA are included in the specifications of the ADC, making error calculations simple. The PGA gain is controlled over the same serial interface as the ADC, and the gain setting is factored into the conversion, saving additional calculations to determine input voltage. This combination of ADC and PGA is very powerful and enables the realization of a highly accurate system, with a minimum of circuit design.

THE AD7710 ADC HAS A BUILT-IN PGA WITH GAIN CONTROLLED BY A SERIAL INTERFACE

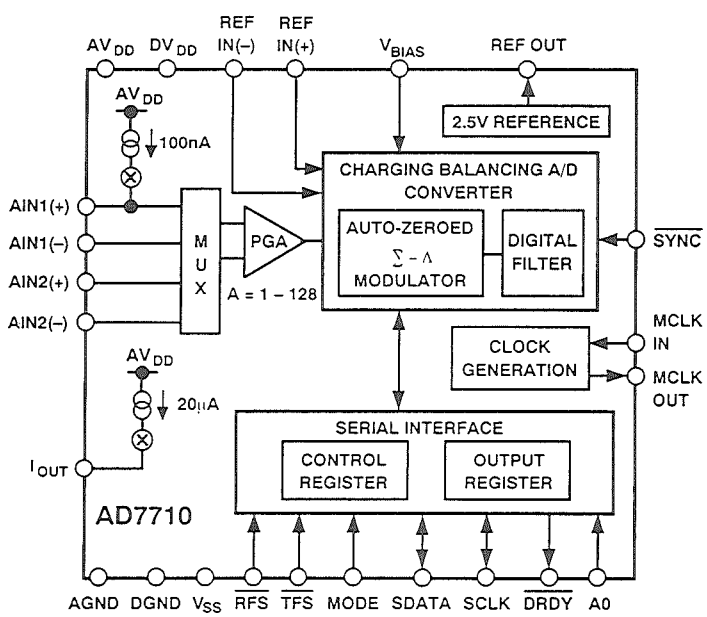


Figure 2.36

ISOLATION AMPLIFIERS

There are many applications where it is desirable, or even essential, for a transducer to have no direct ("galvanic") electrical connection with the system to which it is supplying data, either in order to avoid the possibility of dangerous voltages or currents from one half of the system doing damage in the other, or to break an intractable ground loop. Such a system is said to be "isolated", and the arrangement which passes a signal without galvanic connections is known as an "isolation barrier".

The protection of an isolation barrier works in both directions, and may be needed in either, or even in both. The obvious application is where a sensor may accidentally encounter high voltages, and the system it is driving must be protected. It is equally possible that a sensor may need to be isolated from accidental high voltages arising downstream, in order to protect its environment: examples include the need to prevent the ignition of explosive gases by sparks at sensors and the protection from electric shock of patients whose ECG, EEG or EMG is being monitored. The ECG case is interesting, as protection may be required in *both* directions: the patient must be protected from accidental electric shock, but if the patient's heart should stop, the ECG machine must be protected from the very high voltages (>7.5 kV) applied to the patient by the defibrillator which will be used to attempt to restart it.

WHERE IS ISOLATION USED?

- **Transducer is at a High Potential Relative to other Circuitry (or may become so under fault conditions)**
- **Transducer may not Carry Dangerous Voltages, Irrespective of Faults in other Circuitry (e.g. Patient Monitoring and Intrinsically Safe Equipment for use with Explosive Gases)**
- **To Break Ground Loops**

Figure 2.37

Just as interference, or *unwanted* information, may be coupled by electric or magnetic fields, or by electro-magnetic radiation, these phenomena may be used for the transmission of *wanted* information in the design of isolated systems. The most common isolation amplifiers use transformers, which exploit magnetic fields, and another common type uses small high voltage capacitors, exploiting electric fields.

Opto-isolators, which consist of an LED and a photocell, provide isolation by using light, a form of electro-magnetic radiation. Different isolators have differing performance: some are sufficiently linear to pass high accuracy analog signals across an isolation barrier, with others the signal may need to be converted to digital form before transmission, if accuracy is to be maintained.

TECHNIQUES FOR ISOLATION

- Electric Field → Capacitive Signal Coupling
- Magnetic Field → Transformer Coupling
- Electromagnetic → Optical Coupling
- Sometimes a Technique will not have Adequate Linearity-- In Such Cases There are two Possibilities:
  - Voltage-Frequency Conversion / Transmission / Frequency-Voltage Conversion
  - Analog-Digital Conversion Before Transmission Across the Isolation Barrier

Figure 2.38

Transformers are capable of analog accuracy of 12-16 bits and bandwidths up to several hundred kHz, but their maximum voltage rating rarely exceeds 10kV, and is often much lower. Capacitively coupled isolation amplifiers have lower accuracy, perhaps 12-bits maximum, lower bandwidth, and lower voltage ratings - but they are cheap. Optical isolators are fast and cheap, and can be made with very high voltage ratings (although 4 - 7kV is one of the more common ratings), but they have poor linearity, and are not usually suitable for direct coupling of precision analog signals

Linearity and isolation voltage are not the only issues to be considered in the choice of isolation systems. Power is

essential. Both the input and the output circuitry must be powered, and unless there is a battery on the isolated side of the isolation barrier (which is possible, but rarely convenient), some form of isolated power must be provided. Systems using transformer isolation can easily use a transformer (either the signal transformer or another one) to provide isolated power, but it is impractical to transmit useful amounts of power by capacitive or optical means. Systems using these forms of isolation must make other arrangements to obtain isolated power supplies - this is a powerful consideration in favor of choosing transformer isolated isolation amplifiers: they almost invariably include an isolated power supply.

The isolation amplifier has an input circuit that is galvanically isolated from the power supply and the output circuit. In addition, there is minimal capacitance between the input and the rest of the device. Therefore, there is no possibility for DC current flow, and minimum AC coupling. Isolation amplifiers are intended for applications requiring safe, accurate measurement of low frequency voltage or current (up to about 100kHz) in the presence of high common-mode voltage (to thousands of volts) with high common mode rejection. They are also useful for line-receiving of signals transmitted at high impedance in noisy environments, and for safety in general-purpose measurements, where DC and line-frequency leakage must be maintained at levels well below certain mandated minima. Principle applications are in electrical environments of the kind associated with medical equipment, conventional and nuclear power plants, automatic test equipment, and industrial process control systems.

In the basic two-port form, the output and power circuits are not isolated from one another. In the three-port isolator shown in Figure 2.39, the input circuits, output circuits, and power source are all isolated from one another. The figure shows the circuit architecture of a self-contained isolator, the AD210. An isolator of this type requires power from a two-terminal DC power supply. An internal oscillator (50kHz) converts the DC power to AC, which is transformer-coupled to the shielded input section, then converted to DC for the input stage and the auxiliary power output. The AC carrier is also modulated by the amplifier output, transformer-coupled to the output stage, demodulated by a phase-sensitive demodulator (using the carrier as the reference), filtered, and buffered using isolated DC power derived from the carrier. The AD210 allows the user to select gains from 1 to 100 using an external resistor. Bandwidth is 20kHz, and voltage isolation is 2500V RMS (continuous) and ± 3500V peak (continuous).

AD210 3-PORT ISOLATION AMPLIFIER

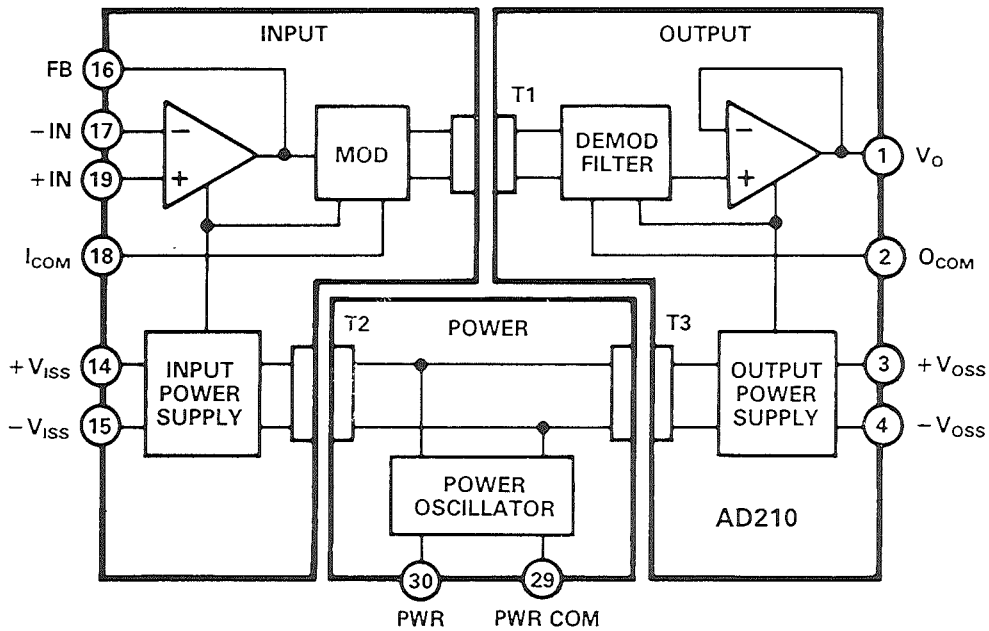


Figure 2.39

The AD210 is a 3-port isolation amplifier: the power circuitry is isolated from both the input and the output stages and may therefore be connected to either - or to neither. It uses transformer isolation to achieve 3500V isolation with 12-bit accuracy. Key specifications for the AD210 are summarized in Figure 2.40.

AD210 ISOLATION AMPLIFIER KEY FEATURES

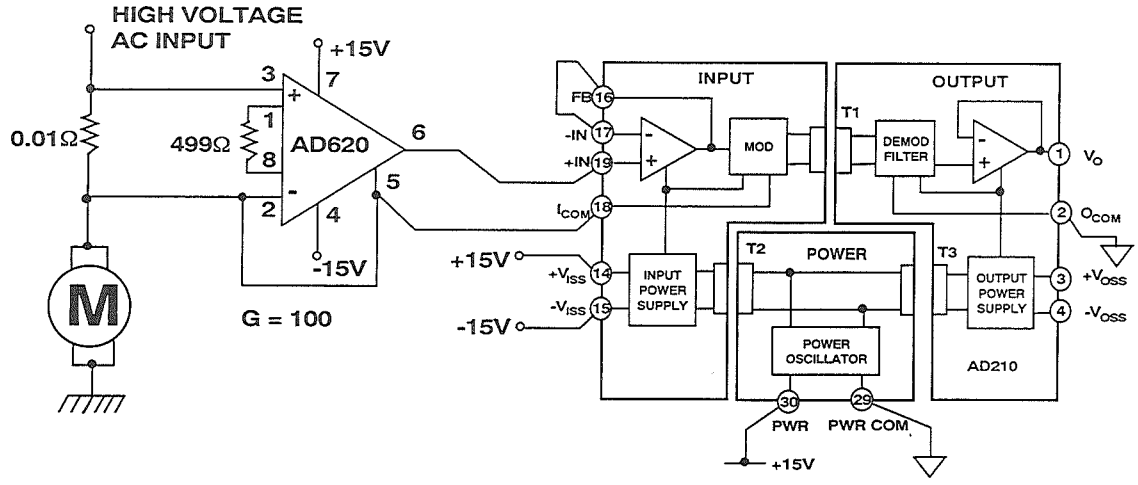
- Transformer Coupled
- High Common-Mode Voltage Isolation:

  2500V RMS Continuous
  ± 3500V Peak Continuous
- Wide Bandwidth: 20kHz (Full-Power)
- ± 0.012% Maximum Non-Linearity
- Input Amplifier: Gain 1 to 100
- Isolated Input and Output Power Supplies, ± 15V @ ± 5mA

Figure 2.40

A typical isolation amplifier application using the AD210 is shown in Figure 2.41. The AD210 is used with an AD620 instrumentation amplifier in a current-sensing system for motor control. The input of the AD210, being isolated, can be connected to a 110 or 230 V power line without any protection, and the isolated ±15 V powers the AD620, which senses the voltage drop in a small current sensing resistor. The 110 or 230V RMS common-mode voltage is ignored by the isolated system. The AD620 is used to improve system accuracy: the V_{OS} of the AD210 is 15mV, while the AD620 has V_{OS} of 30μV and correspondingly lower drift. If higher DC offset and drift are acceptable, the AD620 may be omitted, and the AD210 used directly at a closed loop gain of 100.

MOTOR CONTROL CURRENT SENSING



- High Accuracy/Low-Drift of AD620
- AD620 Powered By AD210
- Floating, Isolated, Senses Up To 2000V

Figure 2.41

Optical isolators using optical fibers may be made with isolation voltages of tens of MV. More general purpose devices consist of an LED and a photo-cell, electrically isolated, but in a single package, and having a breakdown voltage in the range 3.5 - 10kV. The coupling between the two elements is not linear, so they cannot be used in simple analog isolation amplifiers, although they will carry digital signals, and hence the results of A/D or V/F conversion very efficiently.

FOR HIGHER VOLTAGE BARRIERS USE OPTO-ISOLATORS

- Uses Light for Transmission Over a High Voltage Barrier
- An LED is the Transmitter, and a Photodiode or Phototransistor is the Receiver
- High Voltage Isolation is in the Range of 5000V to 7000V
- Usually Not Linear -- Best for Digital or Frequency Information

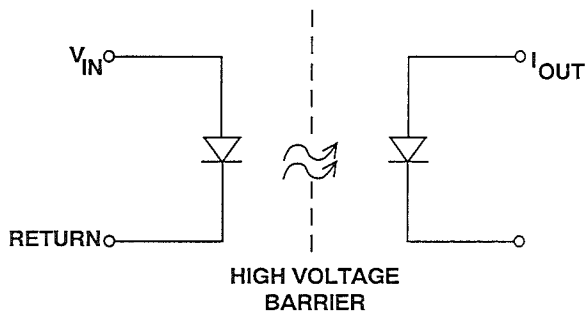


Figure 2.42

Voltage-Frequency Converters (VFCs) are valuable in systems requiring isolation. The analog signal is converted to a frequency in a VFC and may then be transmitted across an isolation barrier by very simple means, with no risk of non-linearity, and greatly reduced susceptibility to noise. At the receiver, there are two options: the signal may be applied to a counter for a fixed period and the count read by a digital processor, the combination of VFC and counter acting as an ADC, or the frequency may be converted back to a voltage in a Frequency-Voltage Converter (FVC). FVC and VFCs are discussed in detail in Section 5 of this book (Data Converters).

ISOLATION USING VOLTAGE-TO-FREQUENCY (V/F) CONVERTERS

- Converts a DC Voltage to a Frequency
- Frequency Information is Immune to Offsets and Noise
- V/F Output Can Be Transmitted Over Non-Linear Transmission Media
- Long Distance Transmission Over Twisted Pair or Fiber Optic Links
- A Frequency-to-Voltage (F/V) Converteris Used as the Receiver
- Accuracy is Determined by the V/F and F/V Conversion Process

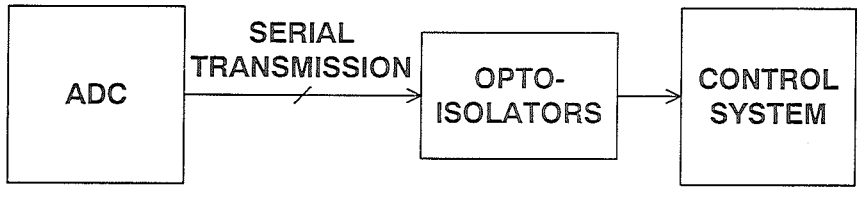
Figure 2.43

Despite the preceding discussion of analog isolation techniques, there is no doubt that the most accurate technique is analog-to-digital conversion *before* transmission across the isolation barrier (VFC-FVC is, after all, one version of this technique). If the signal will eventually be required in digital form, the technique is particularly attractive, especially as there is no serious limit on the distance the data may be transmitted (Figure 2.44).

In the past, the limitations of ADCs may have discouraged this approach, but inexpensive, modern, high-resolution, low-power ADCs with serial data output, and inexpensive digital opto-isolators may make the technique attractive, even when the output signal required is analog, and a digital-to-analog conversion is necessary after transmission.

Despite evolution in the techniques available, the need for galvanic isolation will remain for the foreseeable future. Each technique has its advantages and disadvantages, and engineers must choose the most appropriate technique for the particular application.

FOR HIGH ACCURACY ISOLATION, DIGITIZE FIRST



- Accuracy Limited Only By ADC
- Digital Transmission Relatively Immune To Noise

Figure 2.44

ISOLATING TRANSDUCERS SUMMARY

TECHNOLOGY	ADVANTAGES	DISADVANTAGES
AD20x-Family Transformer Coupled	Fully Self-Contained 3-Port Isolation High Linearity Wide Bandwidth (20kHz)	Lower Breakdown Voltage
Capacitive Couping	Cheap	Lower Breakdown Voltage Low Resolution Separate Power Needed
Opto-Isolators	High Voltage Immunity	Separate Power Needed External Amplifiers Required Poor Linearity
V/F and F/V Isolation	High Linearity Long Distance Transmission High Noise Immunity	Separate Power Needed DC Inputs Only
Digitize First	Highest Accuracy Best Linearity High Noise Immunity Long Distance Transmission	Separate Power Needed

Figure 2.45

COMPARATORS

A comparator is similar to an op amp and is specifically designed to compare the voltages between its two inputs. The comparator operates open-loop, providing a two-state logic output voltage. These two states represent the sign of the net difference between the two inputs (including the effects of the comparator input offset voltage). Therefore, the comparator's output will be a logic "1" if the differential input signal exceeds the offset voltage, V_{OS}, and a logic "0" for the opposite case. A comparator is normally used in applications where some varying signal level is compared to a fixed level (usually a voltage reference). Since it is, in effect, a 1-bit analog-to-digital converter (ADC), the comparator is a basic element in all ADCs.

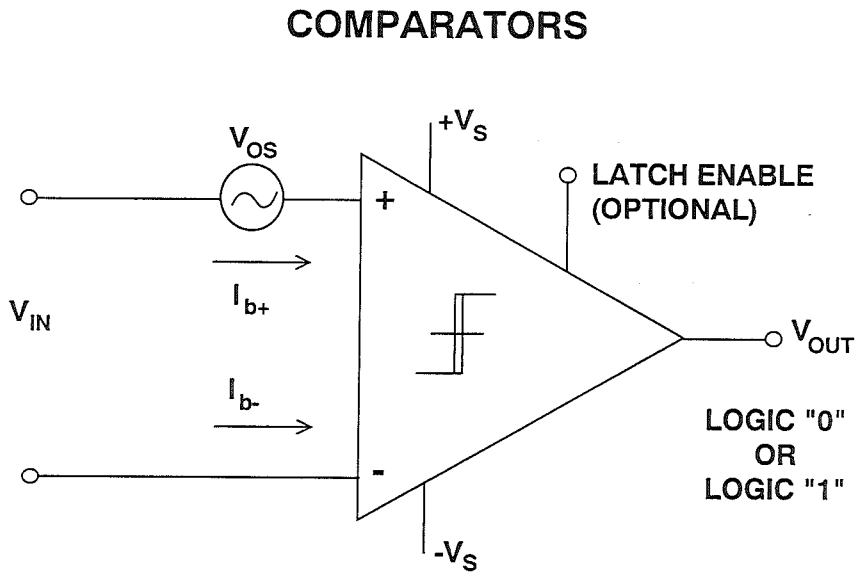


Figure 2.46

Most comparators have an internal latch. The latch-enable signal has two states: *compare* (track) and *latch* (hold). When the latch-enable signal is in the compare state, the comparator output continuously responds to the sign of the net differential input signal. When the latch-enable signal transitions to the latch state, the comparator output goes to either a logic "1" or a logic "0", depending on the sign of the differential input signal at the instant of the transition (at this point, we are neglecting the setup and hold-time, as well as the output propagation delay associated with the latch-enable function). Even though many comparators have a latch-enable function, they are often operated only in the compare mode.

Comparator DC specifications are similar to those of op amps: input offset voltage, input bias current, offset and drift, common-mode input range, gain, CMR, and PSR. Standard logic-related DC, timing and interface specs are associated with the comparator outputs.

KEY COMPARATOR SPECIFICATIONS

- DC:
  - Input Offset Voltage, Input Bias Current
  - Gain (Open-Loop)
  - Common-Mode Input RangeGain
  - Common Mode Rejection (CMR)
  - Power Supply Rejection (PSR)
  - Hysteresis
  - Output Logic Levels
  - Maximum Differential and Common-Mode Inputs
- AC:
  - Propagation Delay
  - Propagation Delay Dispersion
  - Output Logic Rise and Fall Time
  - Latch-Enable Delay to Output High and Low
  - Minimum Latch-Enable Pulse Width
  - Latch-Enable Input Setup and Hold Time

Figure 2.47

The addition of hysteresis to a comparator's transfer function is often useful in a noisy environment, or where it is undesirable for the comparator to toggle continuously between states when the input signal is at or near the switching threshold. The transfer function for a comparator with hysteresis is shown in Figure 2.48.

COMPARATOR HYSTERESIS

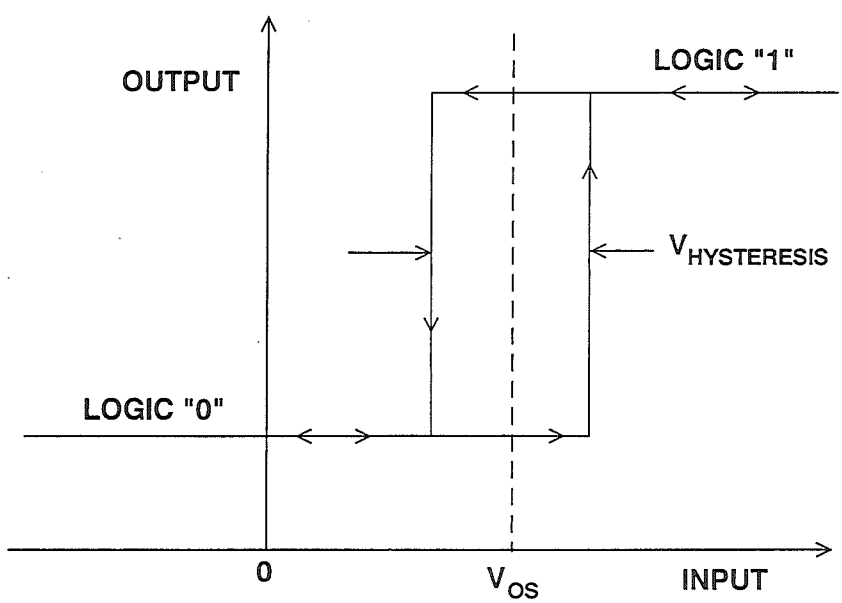


Figure 2.48

If the input voltage approaches the switching threshold (V_{OS}) from the negative direction, the comparator will switch from a "0" to a "1" when the input crosses $V_{OS}+V_H/2$. The "new" switching threshold now becomes $V_{OS}-V_H/2$. The comparator output will remain in a "1" state until the threshold $V_{OS}-V_H/2$ is crossed, coming from the positive direction. Input noise centered around V_{OS} will not cause the comparator to switch states unless it exceeds the region bounded by $V_{OS}\pm V_H/2$.

The key comparator AC specification is *propagation delay*: it is the time required for the output to reach the 50% point of a transition, after the differential input signal crosses the offset voltage - when driven by a square wave (typically 100mV in amplitude) to a prescribed value of input overdrive (usually 5mV or 10mV).

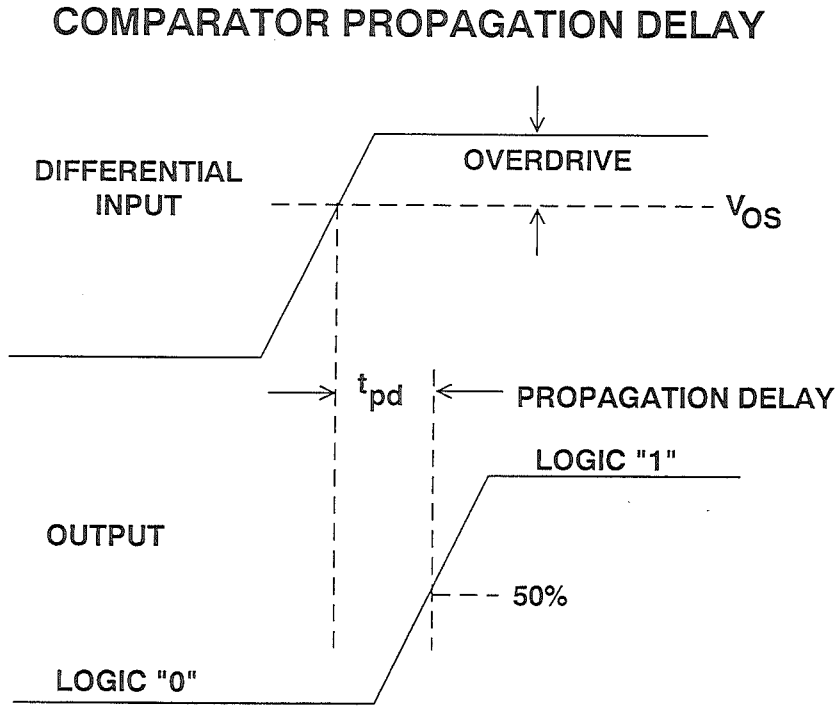


Figure 2.49

The propagation delay in practical comparators decreases somewhat as the input overdrive is increased. This variation in propagation delay as a function of overdrive is called *dispersion*. The effects of dispersion are illustrated in the ATE application shown in Figure 2.51, where the ECL gate under test (DUT) is being tested for output logic risetime. The comparator threshold is first set to –1.7V (10% point). The programmable delay,T2, is adjusted until the output of the D flip-flop is toggling equally between the "1" and "0" output states. The comparator threshold is then set to –0.9V (90% point), and the programmable delay is changed until the D flip-flop is again toggling equally between the "1" and "0" output states. The change in T2 between the two measurements corresponds to the DUT output logic risetime. Comparator dispersion will cause a corresponding risetime measurement error due to the two different overdrive conditions required to perform the 10% and 90% measurement. Fast comparators for ATE applications typically have dispersions less than 100ps.

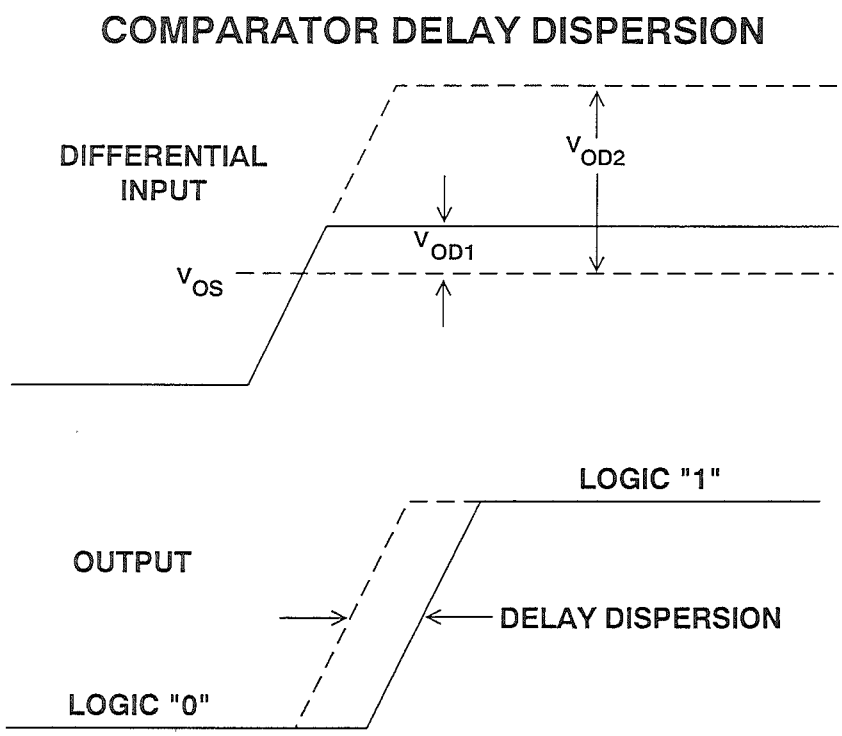


Figure 2.50

RISETIME MEASUREMENT USING COMPARATOR IN AN ATE SYSTEM

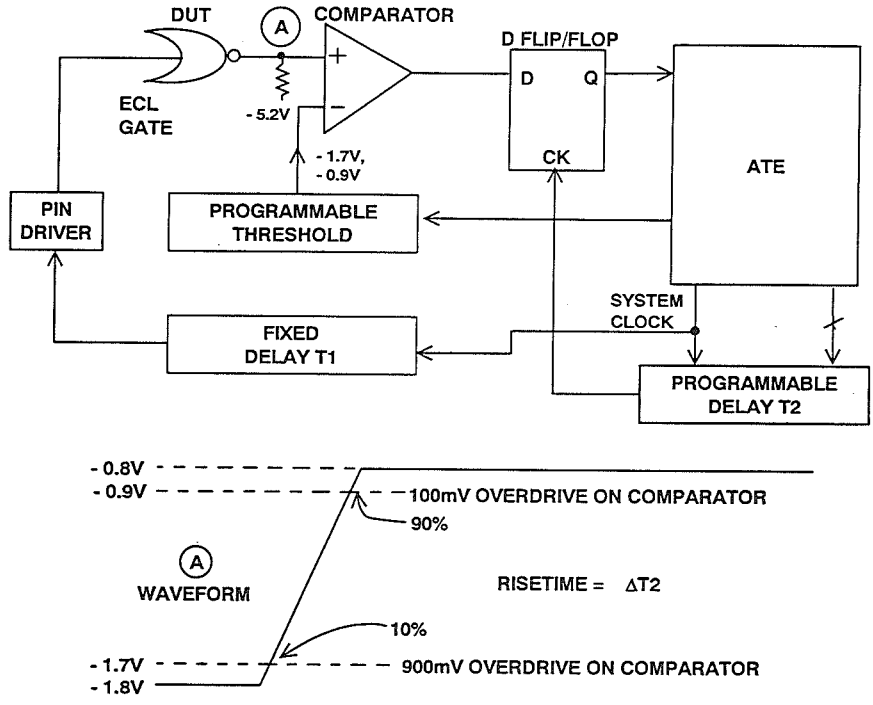


Figure 2.51

COMPARATOR/RAMP DELAY GENERATOR

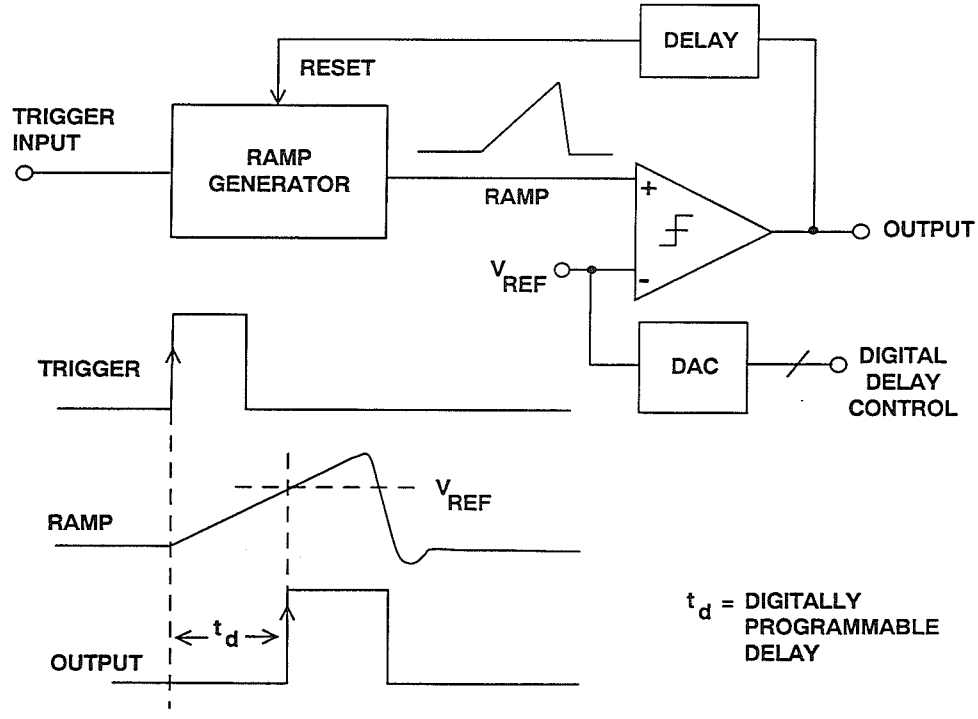


Figure 2.52

A comparator may be used for precise time delay generation if one of its inputs is driven by a ramp voltage (Figure 2.52). The steadily increasing (or decreasing) ramp is applied to the comparator, and its output will change state when its reference level is crossed. The comparator is also an important element of pulse-width modulators, peak detectors, delay generators, time-to-digital converters, and microprocessor supervisory circuits.

Window comparators make use of two comparators with different reference voltages and a common input voltage. The comparators are connected to logic in such a way that the final output logic level is asserted when the input signal falls between the two reference voltages (Figure 2.53). This circuit may be used with fast comparators to make accurate settling time measurements.

WINDOW COMPARATOR CIRCUIT

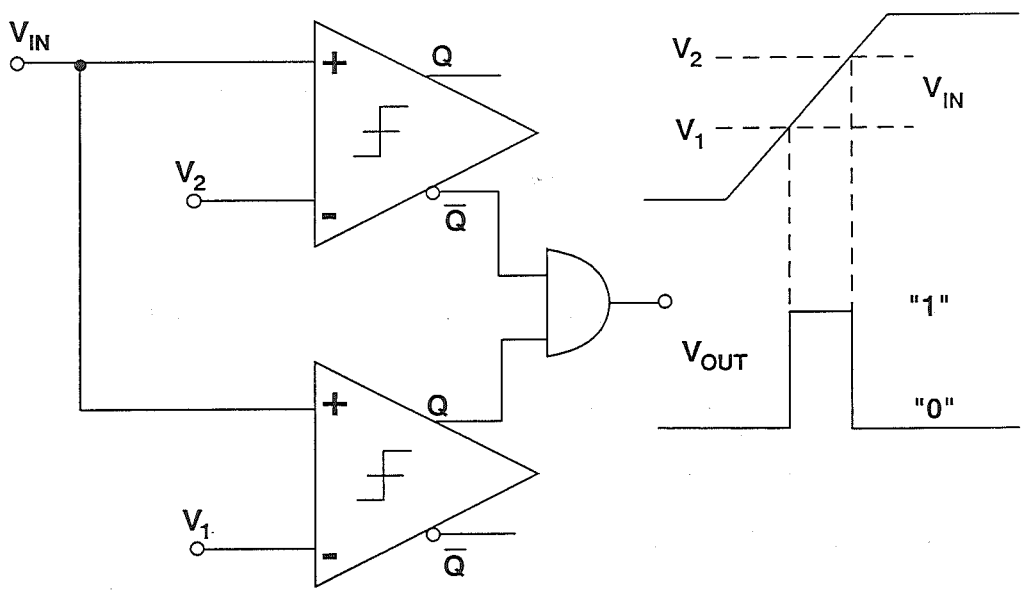


Figure 2.53

The comparator internal latch-enable function is particularly useful in ADC applications because it allows the comparator decision to be recorded *at a known instant of time*. Flash converters make use of this concept and are constructed of many parallel comparators which share a common latch-enable line. Typical timing associated with the latch-enable function is shown in Figure 2.54. The delay between the assertion of latch-enable and the 50% point of the output logic swing is referred to as *latch-enable to output delay*. It may be different for positive and negative-going outputs. The other key specification associated with the latch-enable function is the minimum allowable latch-enable pulse width. This specification determines the maximum frequency at which the comparator can be strobed.

LATCH-ENABLE TIMING

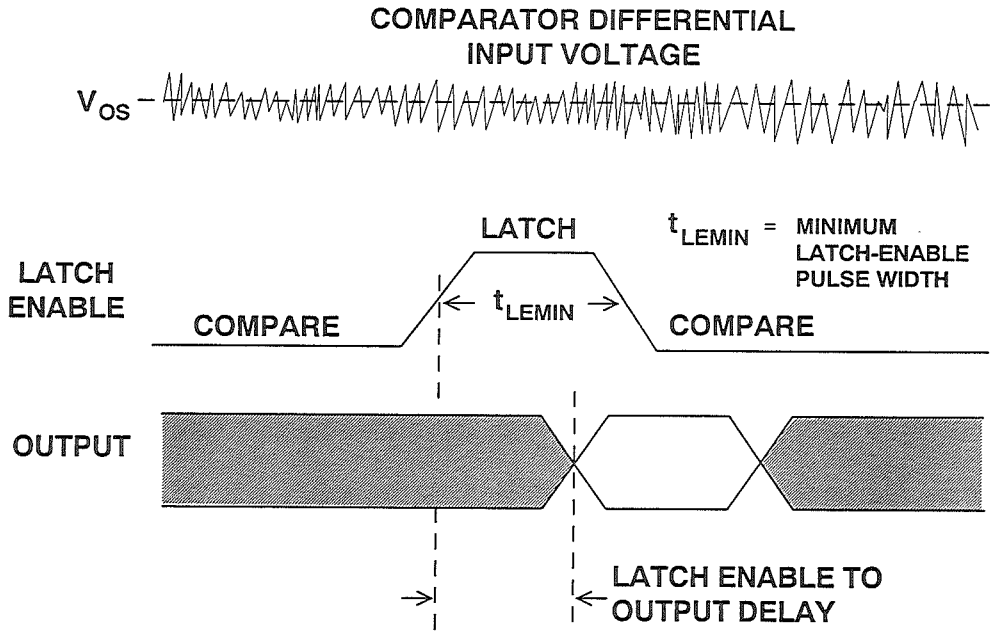


Figure 2.54

Fast comparators are somewhat difficult to apply because of their high gain and bandwidth. Proper application of high speed layout, grounding, decoupling, and signal routing is mandatory when using comparators. The biggest problem is their tendency to oscillate when the input signal is very near to or equal to the switching threshold. Hysteresis and the use of a narrow latch-enable pulse will generally help this condition. TTL comparators are more likely to oscillate than ECL ones because of their large output swings and fast edges, often combined with power supply current spikes as the output changes state.

REDUCING COMPARATOR OSCILLATION

- Use Good High Frequency Techniques:
  - Signal Routing
  - Grounding (Using Ground Plane)
  - Decoupling (HF and LF)
  - No Sockets
- Use Narrow Latch-Enable Strobe
- Hysteresis

Figure 2.55

REFERENCES

1. Daniel H. Sheingold, Editor, **Transducer Interfacing Handbook**, Analog Devices, Inc., 1981.

2. C. Kitchin and L. Counts, **Instrumentation Amplifier Applications Guide**, Analog, Devices, Inc., 1991.

3. **Amplifier Applications Guide**, Analog Devices, Inc., 1992.

4. **System Applications Guide**, Analog Devices, Inc., 1993.