SWITCHES & MUXES

ANALOG SWITCHES AND MULTIPLEXERS

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2. Analog Switch Technologies/Processes
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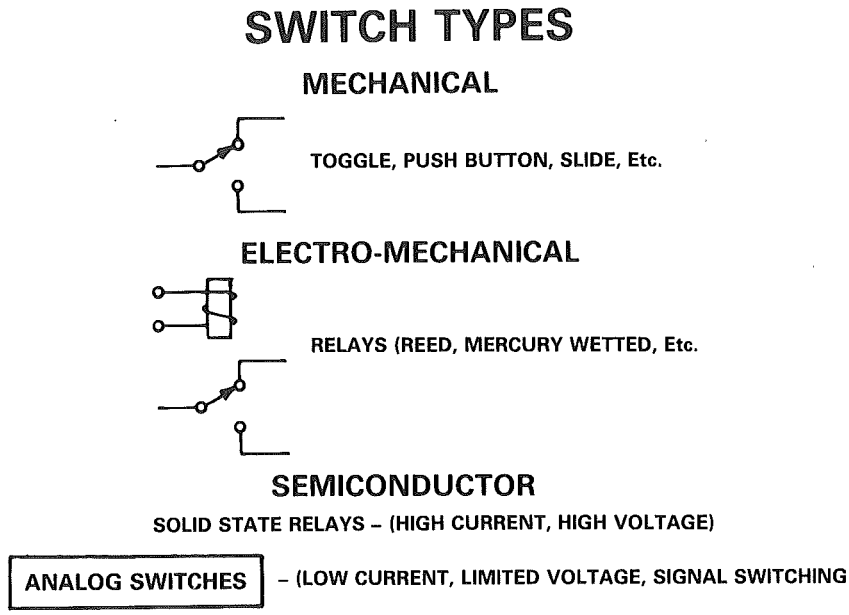
TYPES OF SWITCHES

The switching of analog signals is an essential function in a wide range of applications. There are a variety of switch types available to choose from.

The simplest of these is the mechanical switch. This offers the good electrical characteristics of low on-resistance and high off-isolation but cannot be controlled remotely.

The relay is an electro-mechanical device which offers the desireable electrical features of the mechanical switch plus remote control. It is used in different forms for both power control and analog signal switching. However the relay suffers from a number of problems which precludes its use in many applications. Principal among these are poor reliability, limited number of switch operations, deterioration of switch specifications with time, large size and weight, high power consumption and logic incompatibility.



Semiconductor switches avoid most of these problems at the cost of higher on-resistance and lower off-isolation than relays. The main types of semiconductor switch are 'Solid State Relays' and 'ANALOG SWITCHES'. By common useage within the electronics industry the term 'Analog Switch' has largely assumed the meaning '(semiconductor) analog switch', although relays are often still used to switch analog signals in specific applications. The solid state relay exhibits low on-resistance but poor isolation and is used mainly for power control applications.

SWITCH TYPES – ADVANTAGES AND DISADVANTAGES

TYPE	ADVANTAGE	DISADVANTAGE
MECHANICAL	• Low R_{ON} (<0.1Ω) • No control power or circuitry • High off isolation	• R_{ON} degrades with time • No remote control • Limited number of switch actions (life) • Very slow • Often large and heavy
ELECTRO-MECHANICAL	• Low R_{ON} • Remote control • High off isolation	• R_{ON} degrades with time • Exhibits "bounce" • Limited number of switch actions (life) • Slow • Often large and heavy • Not robust
SOLID-STATE RELAYS	• Low R_{ON} • High reliability • High voltage operation	• High leakage • Unsuitable for signal switching
ANALOG SWITCHES	• Unlimited life • Small Size • Low cost per channel • Low power consumption • Fast (<200ns) • No "bounce"	• High R_{ON} • Leakage limits dc isolation • Limited signal voltage • R_{ON} varies with supply and temperature • Parasitic capacitance limits ac isolation

Analog switches exhibit relatively high on-resistances—typically 10Ω to 500Ω depending on device type. The effect on system performance of these high resistances can be reduced to acceptable levels by buffering and other design techniques (see applications section). Bipolar transistors are rarely used as the signal switching elements in analog switches because they insert a base-emitter voltage drop into the signal path which is difficult to compensate for. Bipolar transistors are also unidirectional—they pass current in one direction only.

PROCESSES FOR SEMICONDUCTOR ANALOG SWITCHES

TECHNOLOGY	PRODUCT	COMMENTS
Hybrid JFET	N-Channel JFET and hybrid driver	• Very fast • R_{ON} <10Ω • Hybrid complexity and price
BIFET	P-Channel JFET and integrated driver	• Monolithic • R_{ON} rises near supply rail
CMOS	N- and P-Channel MOS FETs and integrated driver	• Lower power • Low cost • Wide signal range • Available junction isolated (JI) and diffusion isolated (DI)

ANALOG SWITCH TECHNOLOGIES & PROCESSES

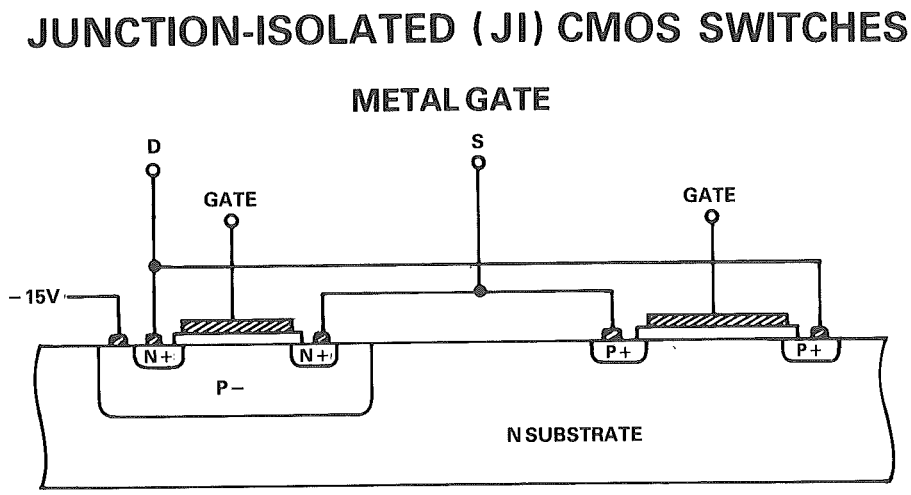
The two principal types of analog switches are CMOS and JFET with CMOS being by far the most popular. Both types are bidirectional and can thus handle bipolar input signals. JFET switches exhibit constant on-resistance over the useable signal range. However this signal range is less than the power supply range by an amount equal to the pinch-off voltage of the FETs.

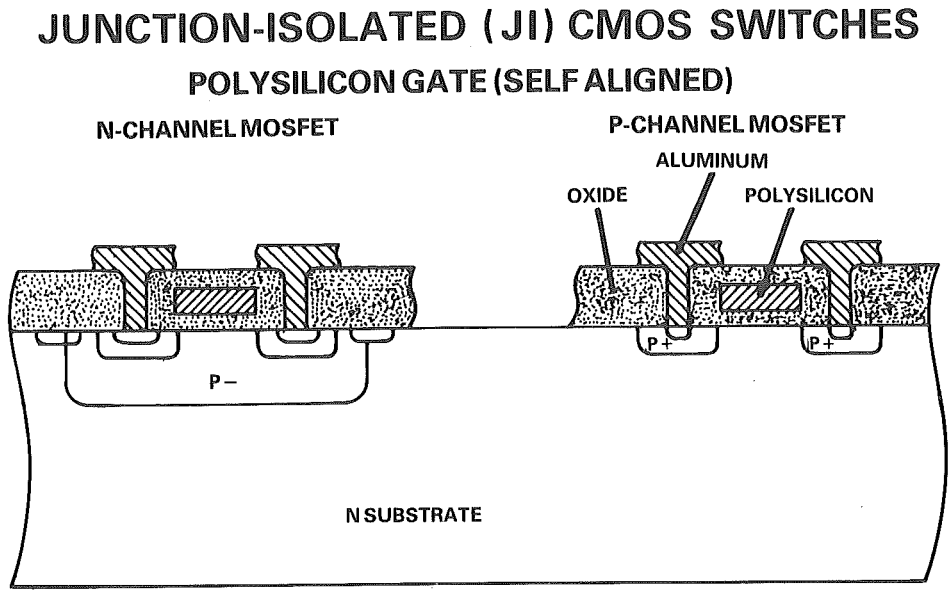
CMOS switches have a useable signal range which extends to the supply rails of the switch. They also use very little quiescent current. All the important parts of a fully integrated analog switch—fast logic interface, flexible level shifting and low leakage signal switches can easily be fabricated in CMOS. The problems associated with latch-up of first generation CMOS switches have been overcome and CMOS is now the technology of choice for analog switches.

CMOS wafer fabrication processes can be divided conveniently into two classes—Junction Isolated (JI) and Dielectrically Isolated (DI).

JUNCTION ISOLATED (JI) CMOS

Junction Isolation relies on reverse biased p-n junctions to maintain isolation between individual elements of the switch circuit. The early problems with JI associated with latch-up caused by parasitic SCR action have been eliminated by careful layout and other design techniques.





The latest JI processes include poly-silicon gates in place of previous metal gates for fabricating the individual MOSFETs. These poly-gates have the distinct advantage that their position can be accurately self-aligned relative to the source and drain regions. This inherent self alignment allows the minimum feature size of the process to be reduced considerably, thus cutting chip area, and it also significantly reduces the gate-source and gate-drain capacitances. These reductions in capacitance allow smaller propagation delays and better isolation performance to be achieved.

DIELECTRIC ISOLATION (DI) CMOS

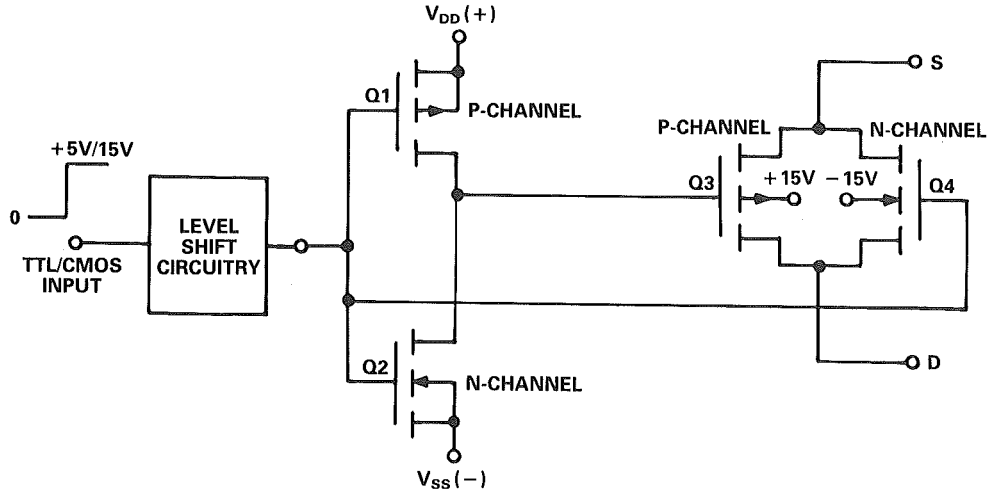
DI CMOS uses thin barriers of dielectric (usually silicon dioxide) to isolate the various chip elements. Forming of these dielectric barriers is expensive and pushes up the cost of the DI process. However DI can accommodate circuitry such as resistors and diodes which may be needed to protect the switch from excessive input overvoltages. These protection components often have to be added externally when using JI type switches.

The reverse biased junctions of JI, which have associated junction capacitances, contribute to the overall parasitic capacitance of the process. DI eleminates these contributions and thus exhibits lower parasitic capacitance.

SWITCH DESIGN AND PROTECTION

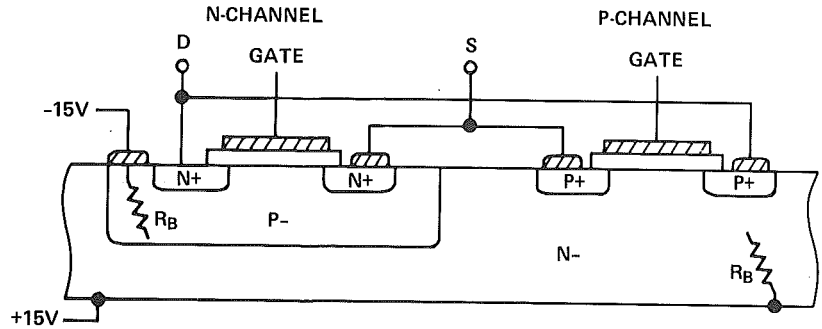
A typical CMOS analog switch IC design consists of a P-channel and an N-channel MOSFET connected in parallel to form a composite signal carrying switch. The gates of the P- and N-channel devices are driven in anti-phase by a push-pull CMOS stage which is in turn driven via level shifting circuitry from the input logic control voltage.

BASIC CMOS SWITCH



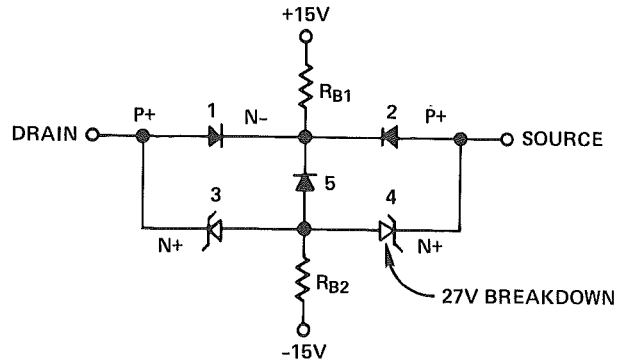
As previously mentioned, early JI CMOS switches suffered from one major drawback—they were prone to latch-up if a signal exceeded the supply voltage or if two signals applied to different switches on a single chip were greatly separated. The drawing below shows a cross section of a junction isolated CMOS switch.

CROSS SECTION OF JUNCTION-ISOLATED CMOS SWITCH



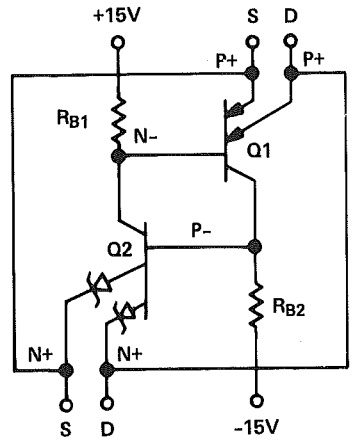
Note that the sources of both the N- and the P-channel devices, as well as the drains of both devices, are tied together. The substrate of the P-channel device (n-region) is tied to V+ while the substrate of the resistances RB are the bulk resistance from substrate to the supply voltages. An equivalent circuit can now be drawn, as shown below.

DIODE EQUIVALENT CIRCUIT OF CMOS SWITCHING ELEMENT



If the analog voltage at either the S or the D terminals exceeds the power supply voltages, the parasitic transistors formed by the various diode junctions shown above are placed into a forward bias mode. These parasitic NPN and PNP transistors form the SCR circuit shown below.

PARASITIC TRANSISTOR ACTION IN CMOS SWITCH



For example, consider the case of a SMALL transient positive overvoltage applied to the drain terminal of a CMOS switch. Since the base of Q1 is normally at V_{DD}, it will conduct when its emitter voltage exceeds V_{DD} by a V_{BE} drop. The collector current of Q1 will increase to a level limited only by the V_{SS} and V_{DD} current limitations. Since the metal interconnection to the power supply terminal is normally designed to handle only small currents, the high currents flowing in the SCR can cause device failure.

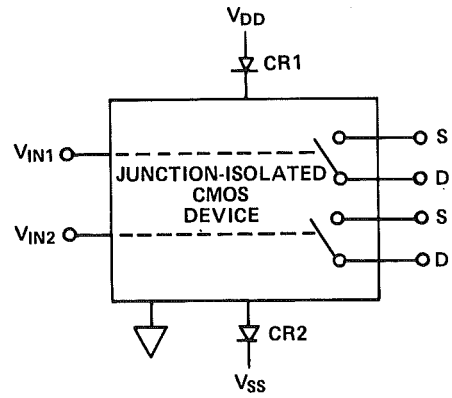
This analysis is also valid for S and D terminals between and two switches. Thus, due to the latching nature of the parasitic SCR, a small transient overvoltage causes permanent 'latch-up'.

Modern junction isolated CMOS switch designs avoid the latch-up problem by reducing the values of R_{B1} and R_{B2} by means of low substrate contact resistances and optimization of IC layout such that transistors Q1 and Q2 of the parasitic SCR cannot turn on, thus preventing latch-up.

Precautions external to the switch may need to be taken to protect junction isolated CMOS switches from long periods or high levels of signal overvoltage in excess of the supply voltage. The two methods most commonly used, supply line protection and input current limiting protection, are described below.

Normally, the outputs of operational amplifiers are used as the voltage sources feeding the S and D terminals so the currents cannot exceed their output current limitations. The op amps may even be powered from the same supply as the CMOS device, but it is still possible, though much less likely with modern JI switch designs, for transient induced currents to destroy the CMOS switch.

SUPPLY LINE PROTECTION



The above drawing illustrates a method of preventing the initial turn-on of the parasitic transistors. The diodes CR1 and CR2 are placed in series with the supply lines. If any S or D terminal exceeds either supply voltage CR1 or CR2 is reverse-biased and therefore no base drive is available to cause transistor turn-on. When this method is employed it is advised that each CMOS chip have its own protection diodes since if two switches use common protection diodes it is possible for the power supply current of one switch to furnish the required base current for parasitic transistors action on another device, even though the protection diode is reverse biased. The diodes used may be any general purpose device such as the 1N4148.

Even the diode protection scheme is not infalliable. The internal diodes 3 and 4 in the equivalent circuit have a 27-30V reverse breakdown while diodes 1 and 2 have a 40-50V breakdown. This means that if one of the terminals, say "S", has a potential above +12V (assuming V_{SS} = −15V), an avalanche current will run through the diode and R_{B2} to the −15V supply. Therefore the potential of the base of Q2 can be raised above the −15V line, turning on Q2, if the other terminal (emitter) is sufficiently negative. If +15V is applied to the terminal "S" (instead of +12V) then the potential on the base of Q2 will be −12V (because of the 27V zener), limiting potential on the other terminal to approximately −12.5V before Q2 turns on. The only way to protect against this condition is to have a 300-400Ω resistor in series with terminals "S" and "D" as shown below. This will prevent burn-out.

INPUT OVERVOLTAGE PROTECTION

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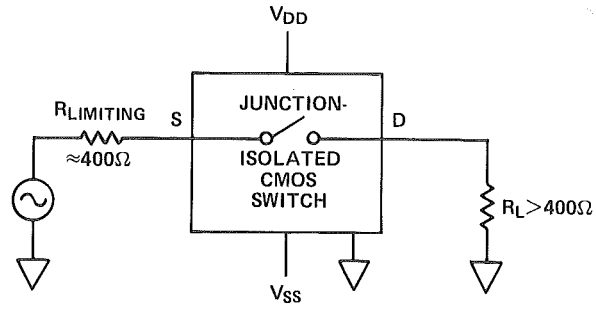
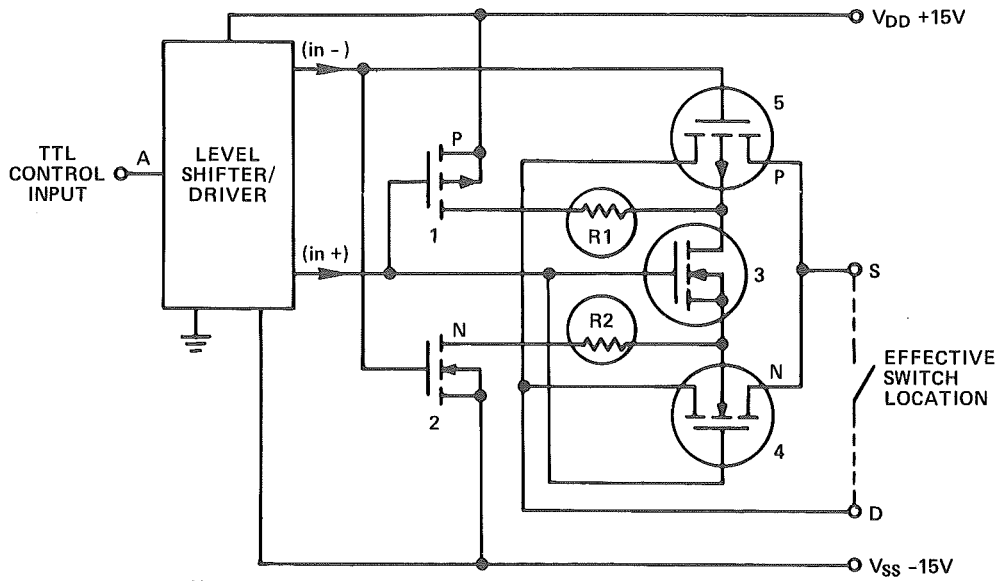


Unfortunately, the addition of this resistor increases the effective on-resistance of the switch.

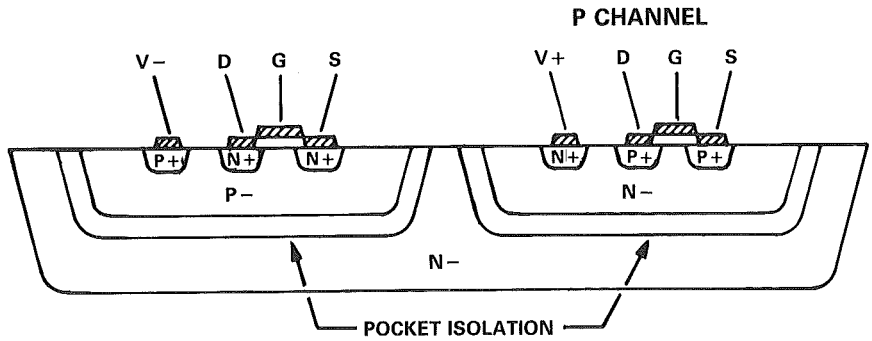
DI CMOS processing allows the switch designer to eliminate problems of latch-up. Internally protected against over-voltage DI CMOS switches retain, or improve on, all the features of the JI CMOS switch.

SCHEMATIC OF DI CMOS SWITCH



NOTE: CIRCLED DEVICES IN SEPARATE ISOLATED POCKETS.

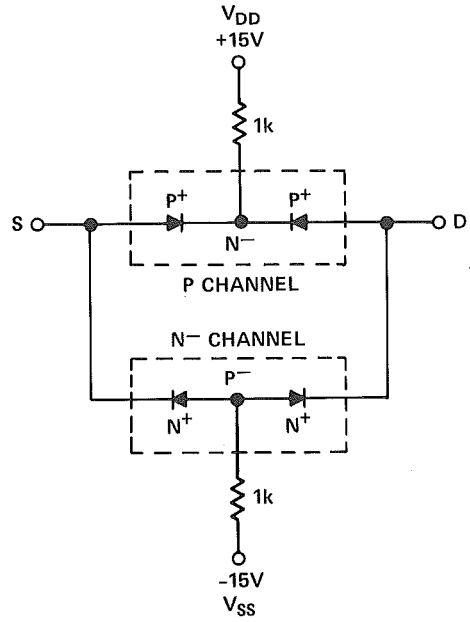
DIELECTRICALLY-ISOLATED CMOS SWITCHES ELIMINATES LATCH-UP PROBLEMS



DIELECTRIC-ISOLATION ELIMINATES THE HIGH BETA VERTICAL NPN AND THE LATERAL PNP. THIS ELIMINATES THE SCR PROBLEM.

Note from the above schematic that the signal-carrying FETs are located in isolated pockets, eliminating parasitic junctions. Also the protection resistors (R1 and R2) are NOT in series with the signal path. This novel protection arrangement provides protection for signals up to ±25V past the supply rails with no increase in resistance.

AD7590DI SERIES DIODE-EQUIVALENT CIRCUIT

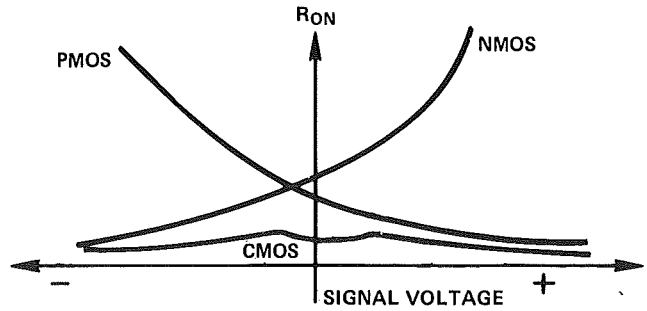


SWITCH SPECIFICATIONS

On resistance $R_{DS}(on)$ is a prime specification of an analog switch. Its presence can insert attenuation, distortion, gain error and noise into the signal path. Techniques for minimizing some of the effects of excessive on-resistance are discussed in the applications section which follows. The on-resistance of CMOS switches is modulated by signal level, and also by supply voltage, as a result of the characteristics of its internal components.

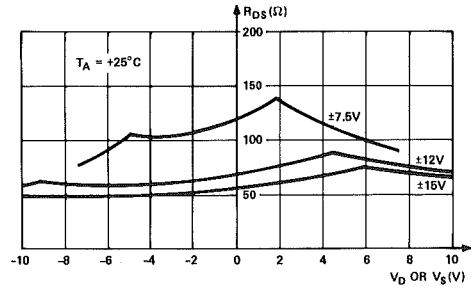
For a fixed applied gate voltage the PMOS transistor exhibits a decreasing on-resistance for an increase in signal voltage. Conversely the NMOS transistor exhibits an increasing on-resistance for an increase in signal voltage. By connecting a PMOS transistor in parallel with an NMOS transistor of suitable relative size, a combination is formed which exhibits a relatively small change in on-resistance for different values of signal voltage.

CMOS SWITCH R_{ON} CHARACTERISTICS

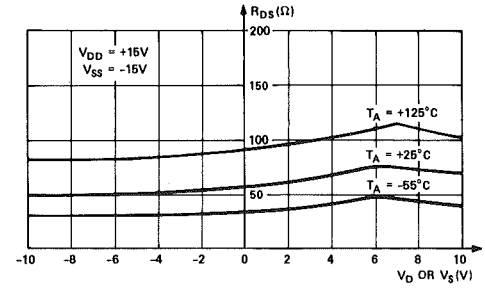


A drop in supply voltage causes a reduction in the enhancement of the two signal carrying transistors which increases their individual channel impedances. The on-resistance also has a positive temperature coefficient of approximately 0.5%/°C.

R_{DS} AS A FUNCTION OF SWITCH VOLTAGE V_D (V_S)



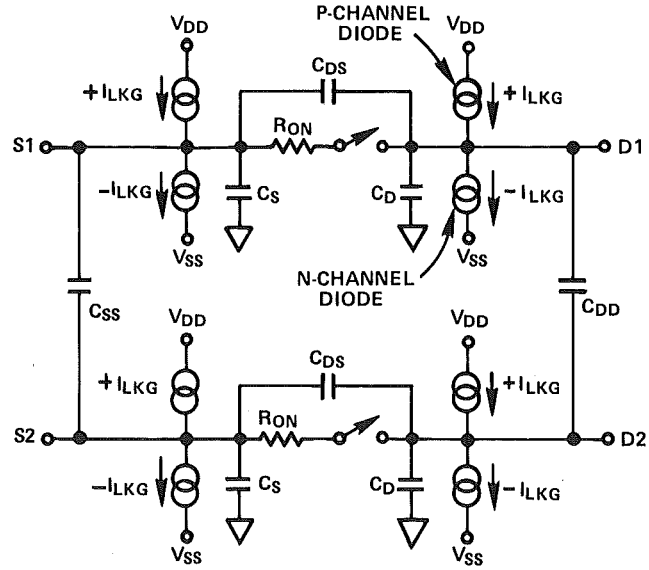
AT DIFFERENT POWER SUPPLIES



AT DIFFERENT TEMPERATURES

So far in this section we have only discussed switch on-resistance. Another dc specification which can introduce unacceptable errors into the user's system is leakage—which rises sharply with increase in temperature (silicon diode leakage doubles for every 10°C temperature increase)—and the high frequency performance of the switch is limited to a large extent by the effects of its parasitic capacitances. Both these error contributions are illustrated in the model below:

EQUIVALENT CIRCUIT OF TWO ADJACENT SWITCHES



Typical values for some of these specs are as follows:

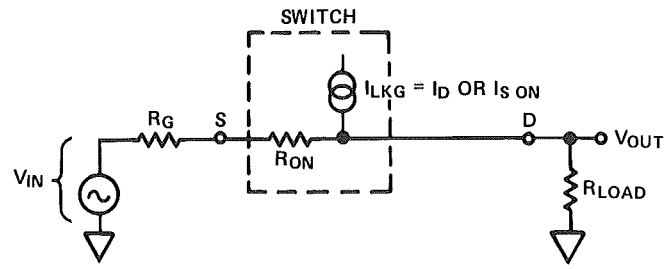
TYPICAL SWITCH SPECIFICATIONS (AD7590DI)

R_{ON}:	60Ω typ, 90Ω max
I_{LKG}:	0.5nA typ, 5nA max
C_{DS}:	1pF typ
C_D, C_S:	10pF typ (Off)
	30pF typ (On)
C_{DD}, C_{SS}:	0.5pF typ
t_{ON}, t_{OFF}:	170ns, 340ns

The on-resistance and leakage current specs determine low frequency signal transmission accuracy. Their effects can only be properly analyzed if the external source and load impedances are known.

A low frequency model of a switch in the "ON" condition is shown below. It is obviously desirable to have a very high value of R_{LOAD} to minimize voltage divider effects with R_{ON}. Furthermore, low values of R_G are desirable, since switch leakage current will flow through this resistance, causing another error.

MODEL OF SWITCH IN "ON" CONDITION



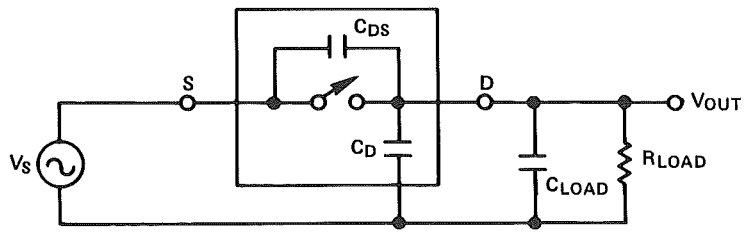
$$V_{OUT} = V_{IN}\left[\frac{R_{LOAD}}{R_G + R_{ON} + R_{LOAD}}\right] + I_{LKG}\left[\frac{R_{LOAD}(R_{ON} + R_G)}{R_G + R_{ON} + R_{LOAD}}\right]$$

If $R_G \rightarrow 0$,

$$V_{OUT} = V_{IN}\left[\frac{R_{LOAD}}{R_{LOAD} + R_{ON}}\right] + I_{LKG}\left[\frac{R_{LOAD}\,R_{ON}}{R_{LOAD} + R_{ON}}\right]$$

The primary concerns in using analog switches in ac applications are bandwidth and off isolation. These are not often specified on switch data sheets—with good reason. It is impossible for a manufacturer to test a switch for ac parameters without first knowing the load resistance and capacitance of the planned application circuit. The load resistance and capacitance directly affect the off-isolation of a switch, as is shown in the diagram below.

CIRCUIT MODEL FOR OFF ISOLATION



As an illustration of the effect of load impedance on isolation it is instructive to calculate the isolation, at 1MHz, or a fairly typical analog switch (having 0.5pF C_{DS} and 10pF C_{DOFF}) with two different loads.

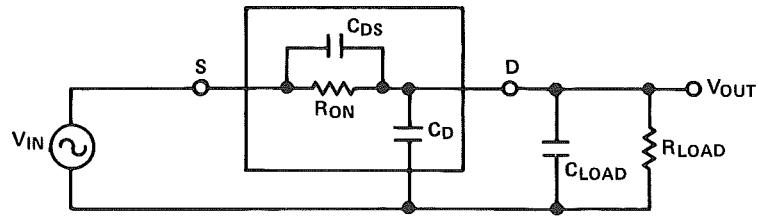
LOAD AFFECTS OFF ISOLATION

At 1MHz, C_{DS} = 1.0pF, C_D = 10pF:

If R_L = 1kΩ	If R_L = 10kΩ
C_L = 100pF	C_L = 10pF
Off Isolation is -48dB	Off Isolation is -31dB

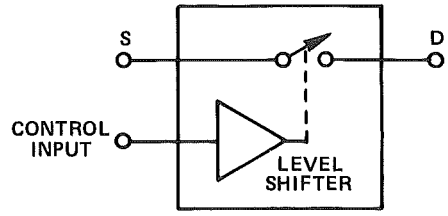
A similar analysis can be performed for the circuit model below in order to compute the available bandwidth, in the ON state, for a particular load.

CIRCUIT MODEL FOR BANDWIDTH ANALYSIS



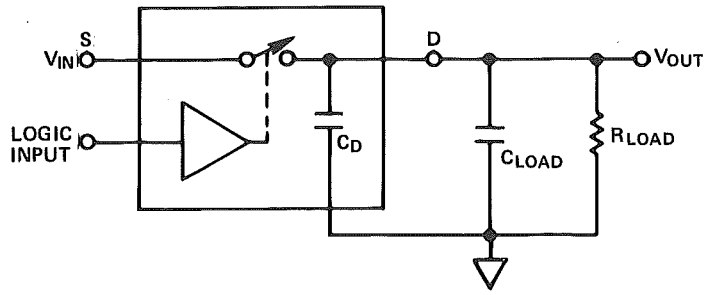
The turn-on and turn-off times are another pair of specifications which are important in analog switch applications. When a switch is commanded to change state there is a propagation delay in the level shifter/switch driver circuitry. These T_{ON} and T_{OFF} specifications are used to determine when a switch begins to operate, and whether multiple switches connected as a multiplexer will have make-before-break to break-before-make operation.

PROPAGATION DELAY IN ANALOG SWITCH



Propagation delay should not be confused with settling time. The settling time of a switch, like its isolation and bandwidth, is a function of its load impedance (resistive and reactive). When a switch changes state the settling time for its output to settle within a given error band may be determined from the model illustrated.

SETTLING TIME MODEL



$$\text{OFF-TO-ON: } t_{SETT} = t_{ON} + \frac{R_{ON}\,R_{LOAD}}{R_{ON}+R_{LOAD}}\,(C_{LOAD}+C_D)\,\text{-ln}\,\frac{\%\ \text{ERROR}}{100}$$

$$\text{ON-TO-OFF: } t_{SETT} = t_{OFF} + (R_{LOAD})\,(C_{LOAD}+C_D)\quad \text{-ln}\,\frac{\%\ \text{ERROR}}{100}$$

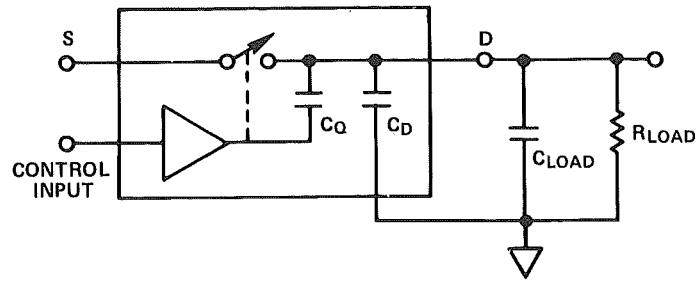
The ln(% error/100) term can be recognized as the number of time constants required (with a single pole response) to reach a particular error band.

One additional specification related to transitions in analog switches is charge injection. Charge injection is the result of capacitive coupling through the gates of FET switches. Its effect is to create a voltage step on any output capacitance according to the formula:

$\Delta V = Q_{INJ}/C_{OUT}$

This is particularly annoying in sample-and-hold amplifiers (SHAs) since it introduces an error between the sample-and-hold modes.

CHARGE INJECTION MODEL

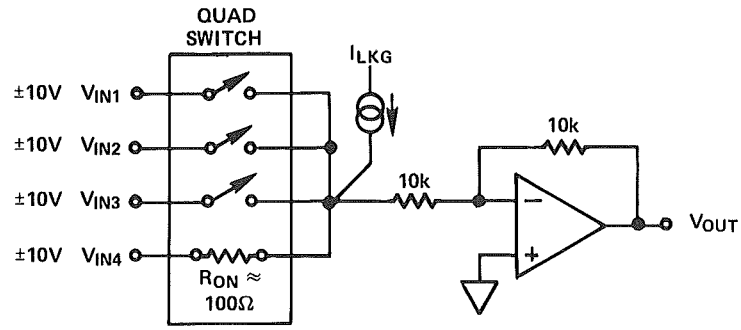


The resulting voltage pedestal error can be reduced, at the expense of settling time, by increasing the load capacitance. The AD7590DI switches feature typical charge injection of 40pF—which translates to a peak transient of 40mV with a 100pF load capacitor or 4mV with a 10,000pF capacitor. The length of the pulse depends on the load resistance.

APPLYING ANALOG SWITCHES

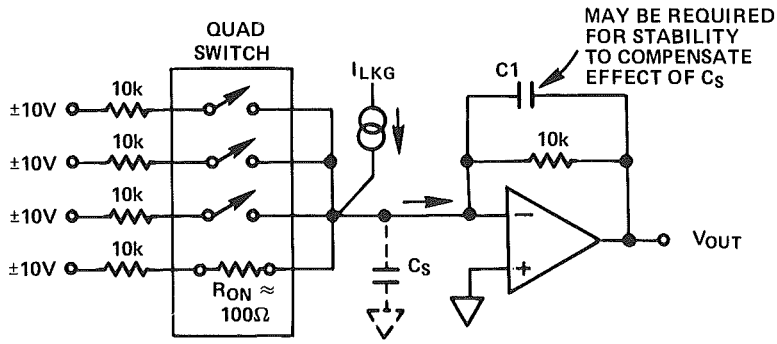
The most obvious application for an analog switch is to select one of several signals to be amplified. In the inverting amplifier shown below the resistance of the switch will obviously introduce a gain error.

UNITY-GAIN INVERTER WITH SWITCHED INPUT



Since CMOS switches' on resistance varies somewhat with signal voltage, as well as with temperature and supply variations, it is evident that this circuit will introduce nonlinearity. By placing the switch at the summing junction the voltage variation at the switch, and hence the nonlinearity, can be reduced—at the cost of an extra input resistor per channel.

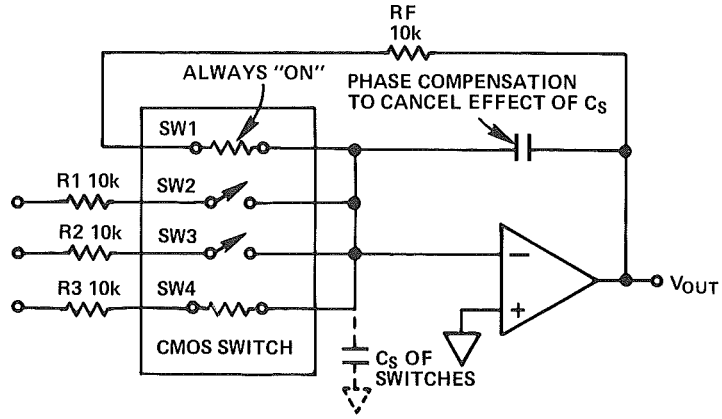
CONNECTING SWITCH AT THE SUMMING POINT



A disadvantage of this circuit is that the switch capacitance appears at the summing junction and may destabilize the amplifier. The feedback capacitor necessary to prevent this will limit overall bandwidth.

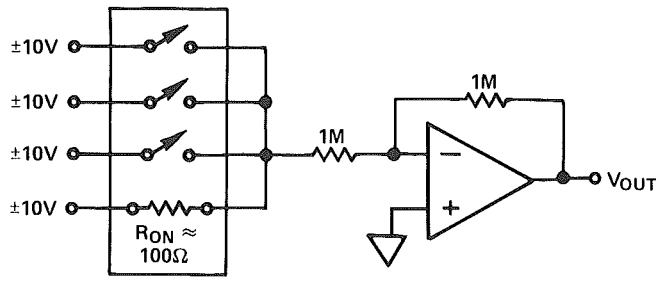
Variations of R_{ON} with temperature and supply may be compensated by connecting a closed analog switch, of the same type as is used in the multiplexer, in the feedback path. This will track the resistance of the multiplexer and reduce errors from these causes, but, of course, uses up one of the multiplexer channels and the problems of summing-point capacitance will remain.

SWITCH IN SERIES WITH FEEDBACK RESISTOR COMPENSATES GAIN



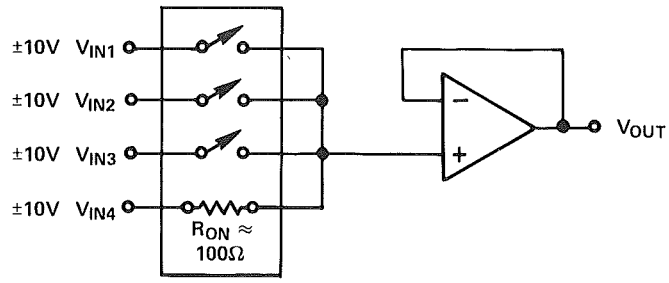
Of course the effect of switch resistance can be reduced by making the circuit resistances larger—at the cost of increased noise and of increased dc offsets due to switch leakage and amplifier bias current flowing in the extra resistance.

USING LARGER VALUES OF RESISTANCE



It is much better to follow a switch with a noninverting amplifier which raises the load impedance to a very high level. If an inverted output is required a separate inverter may follow it.

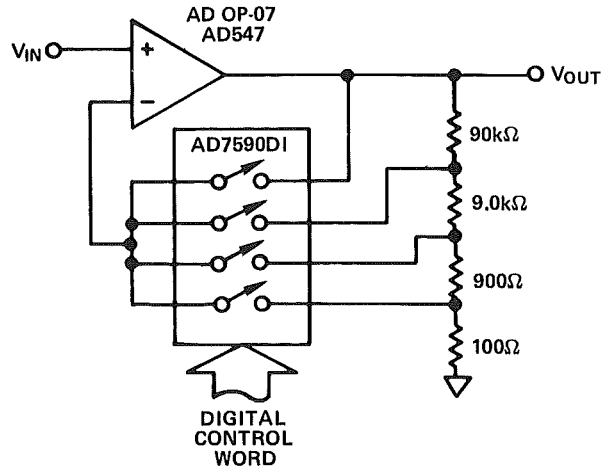
NONINVERTING SOLUTION



With CMOS switches all are open if the switch power is off, but with JFET (and this includes BIFET switches) they are all on—which can cause problems both for the switch and the signal sources connected to it.

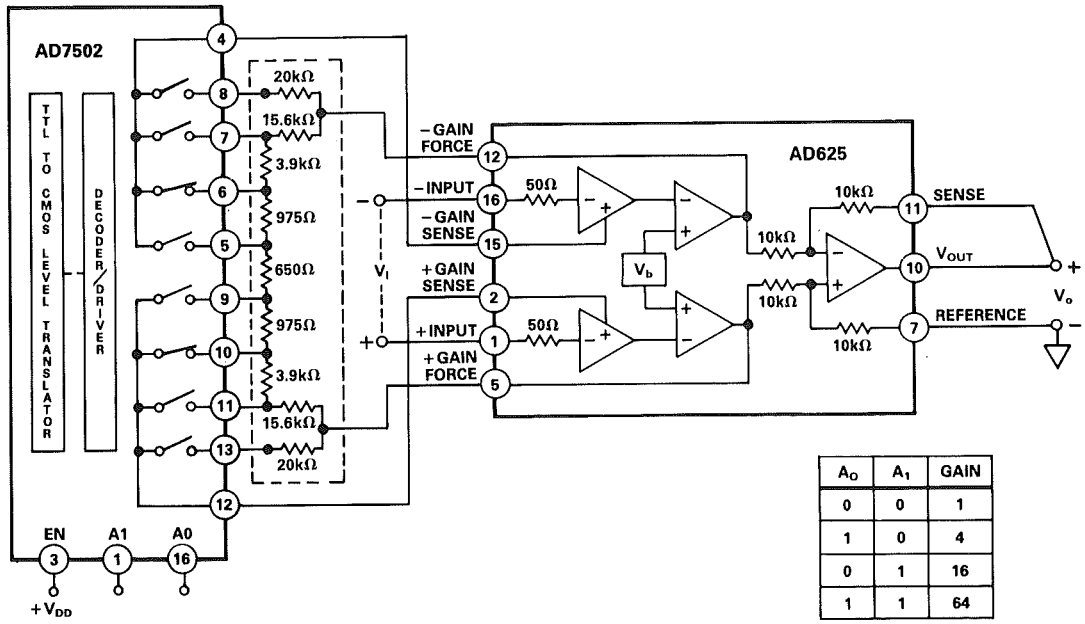
An analog switch may be used to switch the gain of an amplifier by selecting voltage taps on a resistive attenuator in the feedback path. This circuit is capable of high accuracy since only the amplifier bias current flows in the analog switch. The AD7590 is a good choice for such an application since it has make-before-break action, which prevents the amplifier from running open-loop during gain switching.

SWITCHED-GAIN AMPLIFIER



Early monolithic instrumentation amplifiers, such as the AD524 and AD624, were configured so that accurate gain switching required switches with R_{ON} of no more than a few milliohms. This is, of course, impossible to achieve with semiconductor analog switches. The AD625, however, was specifically designed so that its gain could be programmed with such switches and uses the principle shown in the diagram above—the feedback goes to a very high impedance and so the switch R_{ON} is unimportant.

THE AD625 INSTRUMENTATION AMPLIFIER, UNLIKE EARLIER TYPES, HAS BEEN DESIGNED TO ALLOW GAIN PROGRAMMING WITH ANALOG SWITCHES.



A_0	A_1	GAIN
0	0	1
1	0	4
0	1	16
1	1	64

Filter time constants can also be controlled by analog switches. In the circuit shown the low pass cutoff frequency is changed by selecting one of two capacitors. The circuit is useful in applications where a coarse reading is to be taken, and high-frequency noise can be tolerated, and a higher resolution reading must also be taken, where noise cannot be allowed. The technique is not limited to low-pass filters—any filter function may be adapted to this basic idea of switching capacitors to alter frequency response.

DIGITALLY CONTROLLED LOW-PASS FILTER