DATA ACQUISITION SYSTEMS

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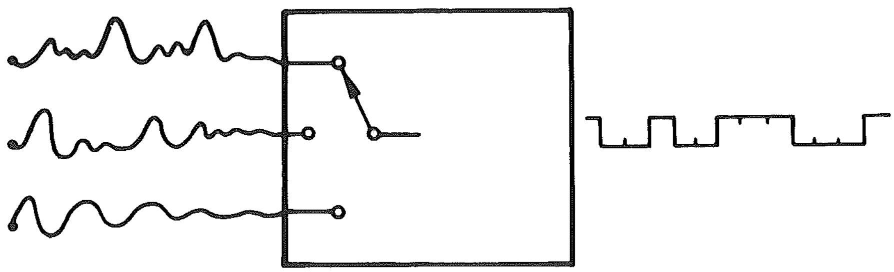
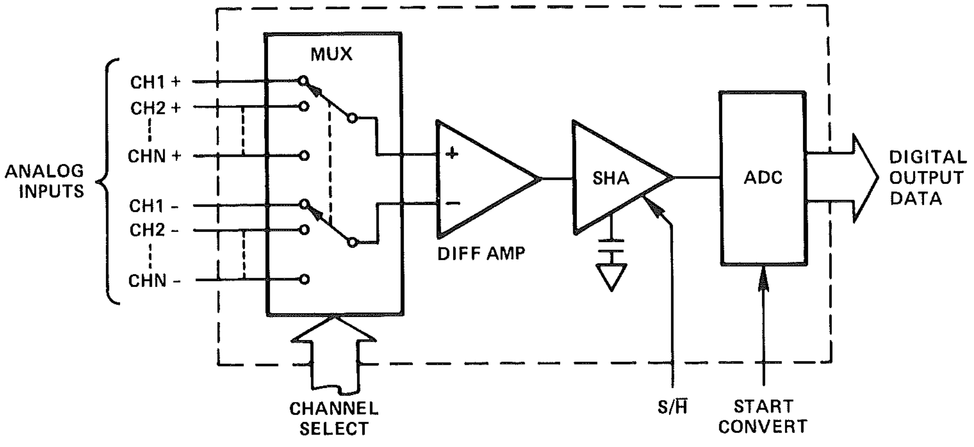


1. WHAT IS A DATA ACQUISITION SYSTEM?

Analog "real-world" voltage signals must be converted to a digital "word" form in order to communicate with a computer or microprocessor. Converting analog to digital signals is the essence of data acquisition.

A Data Acquisition System (DAS) may be defined as a circuit composed of an Analog-to-Digital Converter (ADC), preceded by appropriate multiplexing (if necessary), signal conditioning, and a sample-and-hold amplifier (SHA). A typical DAS block diagram is shown below.

GENERALIZED DATA ACQUISITION SYSTEM



Although system requirements will dictate the actual DAS characteristics, some basic rules do apply. Input impedance of the system should be high, and common-mode rejection should be as effective as possible. The A-to-D conversion must be accurate to the given resolution and speed required. The S/H amplifier must be selected and accounted for based on the desired system parameters.

DATA ACQUISITION SYSTEM REQUIREMENTS

- Multiple Input Channels
- High Input Impedance
- Single-Ended or Differential Operation
- Sample-Hold Function Included
- Maintain Signal Accuracy Commensurate with ADC
- Ease of Use

Each building block has certain performance characteristics. The multiplexer, for example, must have reasonably low "on" resistance, low leakage current, and a break-before-make operation. It is also desirable to include overvoltage protection, since many Data Aquisition Systems will encounter input signals which are outside the expected range.

DAS MUX REQUIREMENTS

- Low R_{ON}
- Low Leakage Current
- Overvoltage Protection
- Break-Before-Make Action

The differential amplifier (or single-ended buffer, if differential operation is not needed) should feature high common-mode rejection, low input bias current, low offset voltage, and sufficient linearity.

DAS DIFF AMP REQUIREMENTS

- Good CMR
- Low Bias Current
- Low Offset
- High Linearity

The sample-hold amplifier should have the charcteristics of low offset voltage, high linearity, fast acquisition and aperture times, and low sample-to-hold offset. Also, its associated hold capacitor should have sufficiently low dielectric absorption to prevent errors due to the "analog memory" effect.

DAS SHA REQUIREMENTS

- Low Offset Voltage
- Low S/H Offset
- High Speed
- Low D.A. Capacitor

The ADC requirements are, of course, dictated by system performance goals. Conversion speed becomes important in large multi-channel systems, since only one channel can be converted at any given time. ADC accuracy is important in any system, and when the DAS under consideration is to be interfaced to a microprocessor, easy interface connections are desirable.

DAS ADC REQUIREMENTS

- High Speed
- High Accuracy
- Easy Interface

A full data acquisition system may include additions such as the sensors which interface with the actual environment of interest (i.e., temperature, pressure, strain of materials, sound, atmospheric content). On the other side of the system is the digital data processing. Hardware interface with the designated processor is required to complete the task of data acquisition. In addition, hardware to implement control functions and calibration/error adjustment may be added to the system if needed.

2. APPLYING HYBRID TECHNOLOGY TO DAS CONSTRUCTION

Since each building block in a DAS has performance requirements which are best filled by different technologies, hybrid technology allows chips manufactured with incompatible technologies to be combined in a small, IC-size package.

ADVANTAGES OF HYBRID DAS CONSTRUCTION

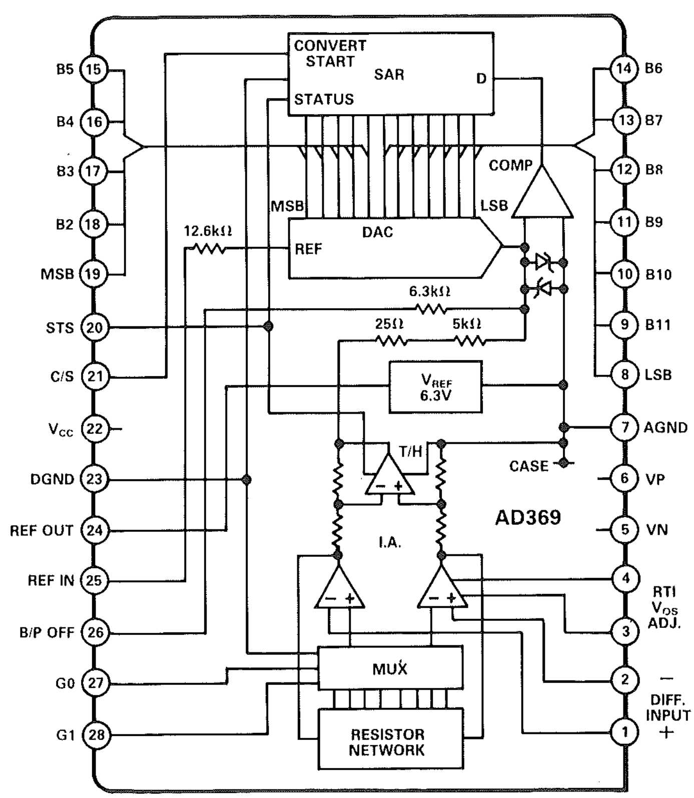
- Smaller Than Boards or Modules
- Can Use Multiple Technologies
- Low Cost
- Grounding/Decoupling Handled Internally

The AD369 is a good illustration of successful integration of a 12-bit DAS.

AD369 FEATURES

Includes: Programmable Gain Instrumentation Amplifier, Track and Hold Amplifier 12-Bit A/D Converter
Digitally Controlled Gain (1, 10, 100, 500)
50kHz Throughput Rate
Small Size: 28-Pin Metal Hermetic Double DIP
Guaranteed No Missing Codes Over Temperature
True 12-Bit Linear; Error ≤1/2LSB (B-Grade)
Unipolar or Bipolar Operation
Low Power: 775mW
Differential Input
Internal Hold Capacitor

AD369 BLOCK DIAGRAM



This hybrid 12-bit data acquisition system conditions and converts an analog signal into a 12-bit digital word. Evolution of this device was made possible by utilizing several of Analog Devices' monolithic ICs and encapsulating them in a space saving 28-pin metal hermetic package. The AD369 consists of a resistor network, multiplexer, instrumentation amplifier, and track-and-hold amplifier, the output of which drives a successive approximation analog-to-digital converter.

The AD7502 CMOS multiplexer and the thin-film resistor network form the gain switching network for the AD625 programmable instrumentation amplifier. By applying a binary address input to the TTL compatible G0 and G1 control lines, gains of 1, 10, 100, and 500 are realized. As shown in the table below, the AD369 accepts full-scale voltage ranges of 10, 1, 100mV, and 20mV corresponding to gains of 1, 10, 100, and 500 respectively. With a gain of 500, full-scale range of the device is 20mV corresponding to 4.88μV per LSB.

INPUT VOLTAGE RANGE SELECTION

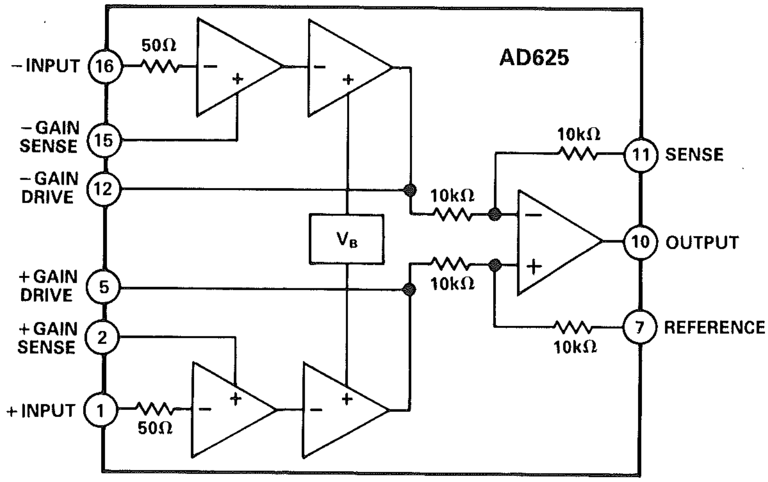
Gain Code		Programmable Gain Amplifier	Analog Input Voltage Range				One Least Significant Bit (LSB) Value
G0	G1	Gain	Unipolar		Bipolar		
0	0	1	0	+10V	−5V	+5V	2.44mV
0	1	10	0	+1V	−0.5V	+0.5V	0.24mV
1	0	100	0	+100mV	−50mV	+50mV	24.4μV
1	1	500	0	+20mV	−10mV	+10mV	4.88μV

The onboard thin-film resistor network has several advantages over discrete resistors. It not only minimizes P.C. board space but also enhances gain accuracy. Through the use of laser wafer trimming, these resistors can be matched to within 0.005%. With respect to the 0.02% inherent gain error of the AD625, the contribution of gain error due to the resistor network is negligible. Compared with discrete metal film resistors with 1% matching or resistor network packs with at best 0.015% matching, there is a definite advantage to using thin-film resistors when considering performance and cost.

Temperature effects also contribute to gain error. Using discrete resistors, thermal gradients in conjunction with mismatched temperature coefficients must be considered when the ambient temperature deviates from 25°C. For example, based upon an ambient temperature of 25° rising to 85°, and using discrete resistors with a typical T.C. of 50ppm/°C, an error of 3000ppm occurs. This error combines with the gain T.C. of 5ppm/°C for the AD625 to yield a total gain error of 3300ppm disregarding the effects of T.C. matching. Alternatively, the AD369's thin-film resistor network with T.C. of 25ppm/°C effectively reduces gain error by 1/2. In addition, the excellent T.C. matching of the thin-film resistors (5ppm/°C) further reduces gain error.

The nucleus of the analog section of the AD369 is the AD625 instrumentation amplifier depicted below.

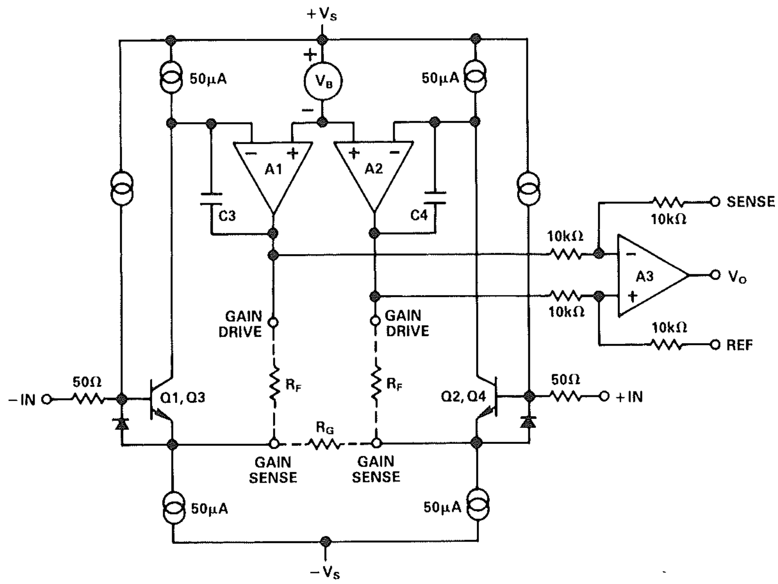
AD625 INSTRUMENTATION AMPLIFIER



This monolithic instrumentation amplifier is based on a modification of the classic three-op-amp design. Referring to the preamp section (Q1-Q4) provides additional gain to A1 and A2. Feedback from the outputs of these amplifiers maintains the collector currents of Q1-Q4 constant. Thus, the input voltage appears across R_G, the gain setting resistor. As a result, a differential voltage is produced at the outputs of A1 and A2 which is given by the gain ($2R_F/R_G+1$) times the differential portion of the input voltage. A3 configured as a unity gain subtractor, develops a single-ended output (V_{OUT}) referred to the potential at the reference pin and free from common-mode signals.

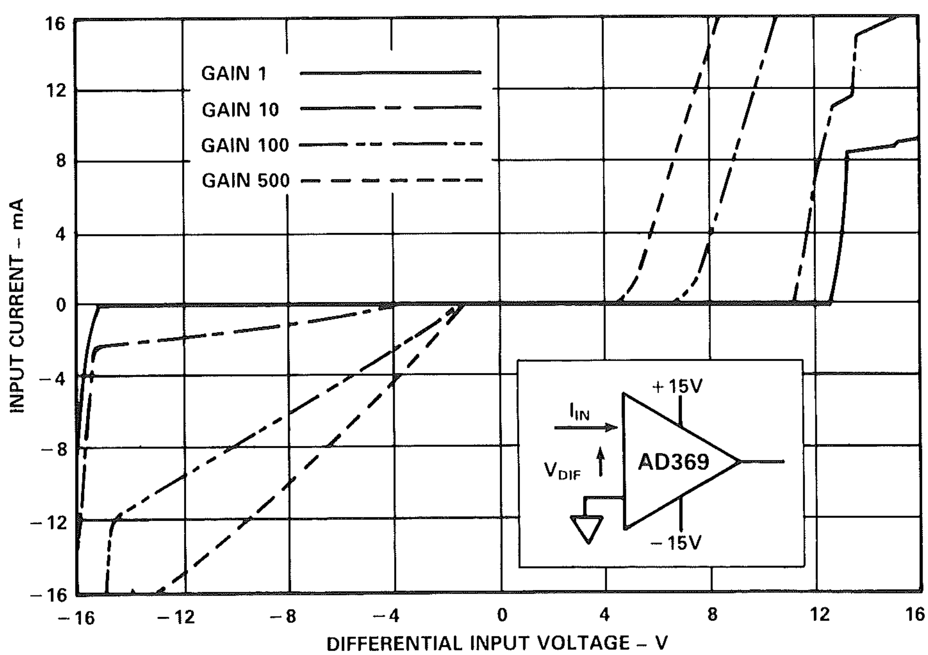
Resistor R_G determines the transconductance of the input preamp stage. Decreasing R_G for larger gain increases the transconductance. With this design, a very high open loop gain of 3×10^8 at gain of 500 is developed. In addition, the gain-bandwidth product, determined by C3, C4 and the input transconductance, increases with gain to enhance frequency response. Moreover, input voltage noise, a critical parameter in a data acquisition system, is reduced to $40nV/\sqrt{Hz}$ being determined by the collector currents of Q1-Q4.

SIMPLIFIED CIRCUIT OF THE AD625



In many applications, the DAS front end will be exposed to input voltages that exceed the linear range of operation for the in-amp. Some form of input protection is required to limit input current to less than 20mA and to prevent the input voltage from exceeding either supply by one V_{BE}. Under differential overload conditions, ($R_G + 100\Omega$) appears in series with two diode drops (1.2V) between the plus and minus inputs in either direction. With no external protection at gain of 500, the maximum continuous overload voltage is approximately 2.5V.

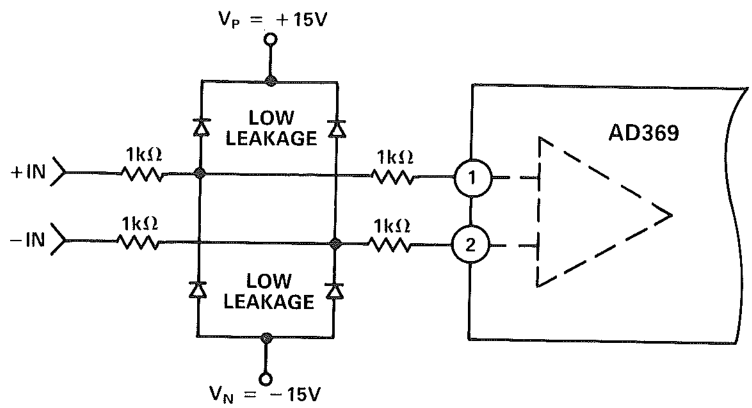
INPUT CURRENT VS. DIFFERENTIAL INPUT VOLTAGE WITHOUT INPUT PROTECTION



1kΩ resistors in series with each input would safely limit thecurrent for input voltages in the range of $V_P = +15$ to $V_N = -15V$. The figure below shows the external components necessary to protect the AD369 regardless of gain. The four low leakage diodes limit the differential overload voltage to ±0.6V when the input voltages exceed the supplies. Input protection, however, is at the expense of degraded noise performance. The four 1kΩ resistors will degrade the noise performance to:

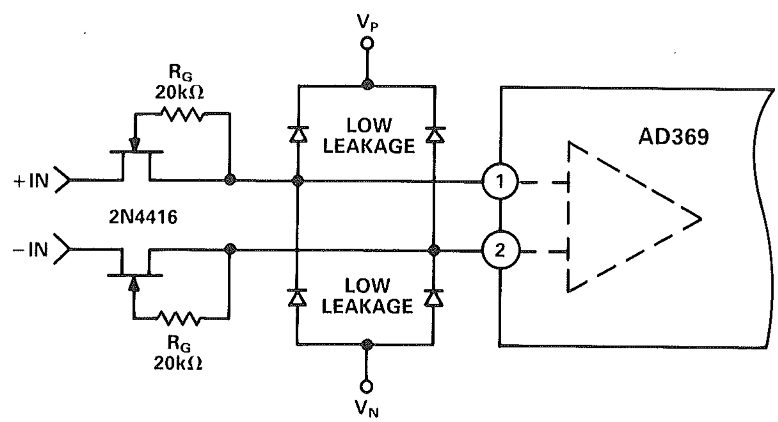
$$\sqrt{4KTR + (4nV/\sqrt{Hz})**2} = 7.9nV/\sqrt{Hz}$$

INPUT PROTECTION CIRCUIT FOR AD369

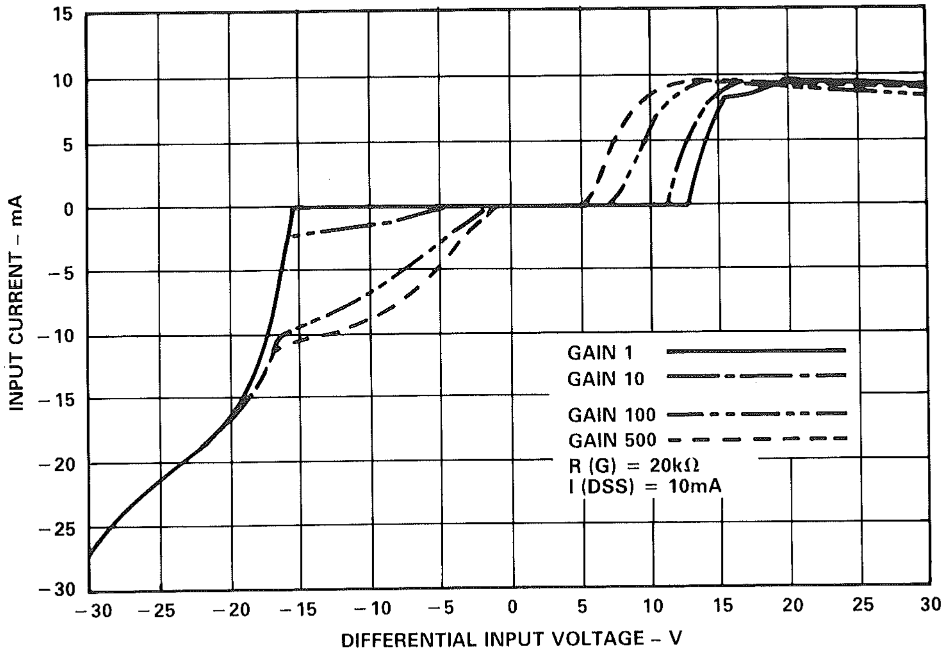


An alternate approach is to replace the resistors with low-cost FETs. FETs such as the 2N4416 with low I_{DSS} (9mA) and low on-resistance (170Ω) should be used. The 20kΩ resistor, in series with the gate, limits the reverse I_{DSS} current without introducing noise. Typical noise performance with this FET is $5.2nV/\sqrt{Hz}$.

LOW NOISE INPUT PROTECTION CIRCUIT FOR AD369

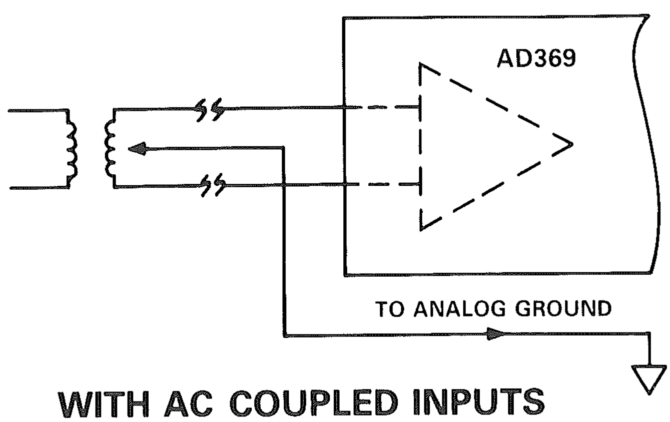


AD369
INPUT PROTECTION WITH 2N4416 FETs AND FD333 CLAMPING DIODES

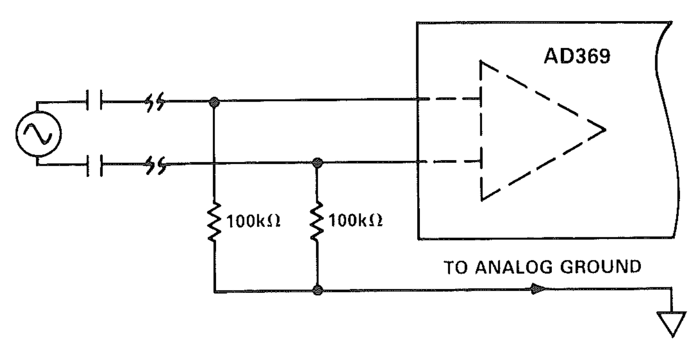


The AD369 DAS requires a direct return path for the input bias currents of the PGA input transistors. Failure to provide this path results in charging stray capacitances which appear as output drift or saturation. Therefore floating sources such as transformer coupled inputs must be returned to ground. AC coupled inputs require a different approach. The two 100kΩ resistors, however, do produce an offset voltage since input offset current flows through these resistors. This input offset voltage is RTI (i.e., referred to input) and after multiplication by gain contributes considerably to system error.

GROUND RETURNS FOR BIAS CURRENTS WITH TRANSFORMER COUPLED INPUT

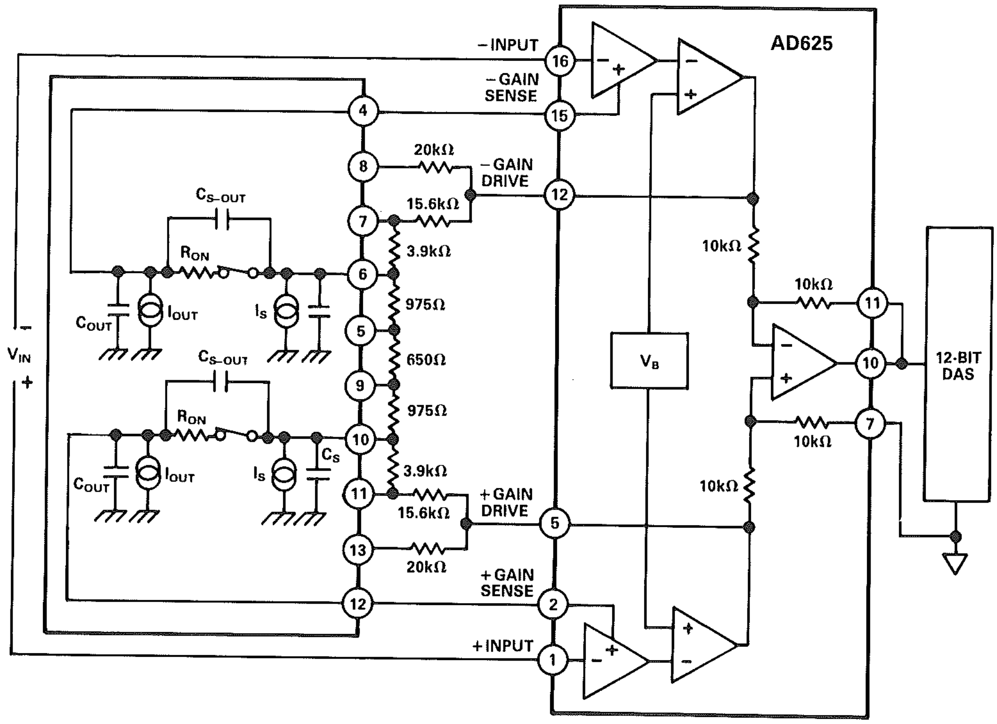


WITH AC COUPLED INPUTS



Historically, the major problem in gain switching amplifiers has been the on-resistance (R_{ON}) of the multiplexer. Since this resistance is in series with the gain setting resistor R_G, additional gain error and drift will occur. However, the AD625 incorporates gain drive and sensing thereby removing the multiplexer's on-resistance from the signal path. As evident from Table II, the total contribution of error at gain of 500 due to multiplexer on-resistance and leakage current is 10.21μV appearing as an input offset voltage. Nulling of offset is achieved with a 10kΩ potentiometer connected between Pin 3, Pin 4 and the positive supply.

SPGA WITH MULTIPLEXER ERROR SOURCES



Induced Error	AD625C	Specifications AD7502KN	Calculation	Voltage Offset Induced RTI
RTI Offset Voltage	Gain Sense Offset Current 40nA	Switch Resistance 170Ω	40nA × 170Ω = 6.8μV	6.8μV
RTI Offset Voltage	Gain Sense Current 60nA	Differential Switch Resistance 6.8Ω	60nA × 6.8Ω = 0.41μV	0.41μV
RTO Offset Voltage	Feedback Resistance 20kΩ	Differential Leakage Current (I_S) +0.2nA −0.2nA	2(0.2nA × 20kΩ) = 8μV/16	0.5μV
RTO Offset Voltage	Feedback Resistance 20kΩ	Differential Leakage Current (I_{OUT}) +1nA −1nA	2(1nA × 20kΩ) = 40μV/16	2.5μV

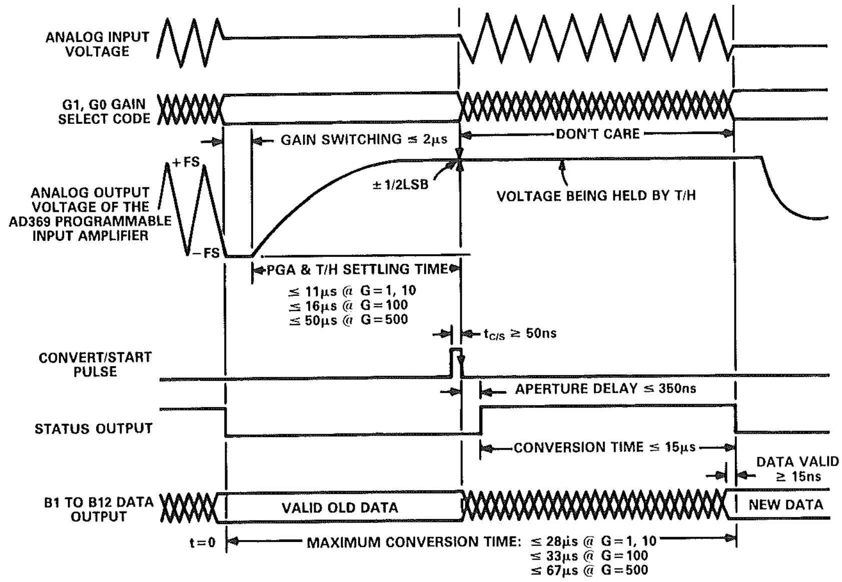
AD369 SYSTEM TIMING SPECIFICATIONS

To perform data acquisition with the AD369, the user must first select the amplifier gain. This is accomplished by entering a two-bit binary word which serves as the gain code. After the correct code is entered, a maximum switching time period of 2μs will elapse and the output stage of the instrumentation amplifier will begin to settle. Settling time for the PGA is dependant on gain; the maximum time being in the gain of 500 mode.

The Convert-Start (C/S) pulse may be submitted after the gain settling time has elapsed. The C/S pulse must be a minimum of 50ns wide; the falling edge initiates the conversion process and, after the SHA aperture delay time of 350ns maximum, the Status output goes high. Since the amplifier settling time is much greater than the SHA acquisition time, the acquisition time of the SHA has no effect on the timing on the first conversion. Conversion time from the falling edge of the C/S pulse is 15μs, maximum.

A low output on the status line indicates a completed conversion; the SHA now returns to the tracking mode. The digital data is valid at the output for at least 15ns prior to the falling edge of the Status pulse. This gives sufficient set-up time at the output to assure accurate data transmission to an external latch if immediate extraction (triggered by falling edge of the Status pulse) is desired. This feature of the DAS enables the user to maximize throughput rates when using the AD369 under microprocessor control. Data is valid at the output until the next falling edge of a C/S pulse. A timing diagram for the first conversion is shown below.

AD369 TIMING DIAGRAM WITHOUT PIPELINING

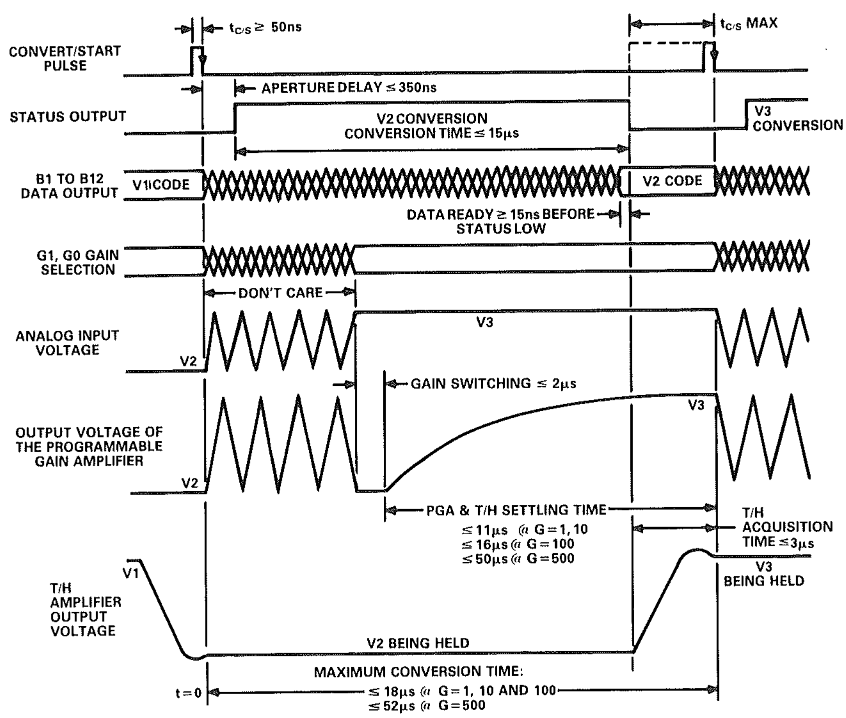


DAS throughput rates are maximized by "pipelining" the acquisition process, as shown below. As soon as a conversion has been initiated by a falling edge of the C/S pulse, the system develops into a "don't care" state and a new set of conditions may be imposed. The figure shows the timing when a new gain is selected after the falling edge of the C/S pulse. A new voltage begins to settle at the output of the PGA no more than 2μs later. Since the conversion has already begun, the amplifier settling time occurs concurrently with the previous A-to-D conversion.

At gains of 1 and 10, the output of the amplifier will settle before the conversion time. In these cases, once the status output goes low indicating a completed previous conversion and the SHA goes into the tracking mode, the user must allow a maximum of 3μs acquisition time before the next falling edge of the C/S pulse can be submitted.

In the gain 100 and 500 modes, the settling time is long enough such that by the time the proper time has elapsed for settling, the SHA acquisition time will already be accounted for (t_{ACQ} and t_S are added "RMS").

AD369 TIMING DIAGRAM WITH PIPELINING



NOISE CONSIDERATIONS

Assuming normally distributed or white noise, the rms noise voltage E_N of a system is a function of its noise bandwidth BW_N. The correlation between $-3dB$ bandwidth (BW) and BW_N is dependant upon the frequency response of the system under consideration.

For a 6dB/octave (one-pole) filter, the ratio is $\pi/2 = 1.57$. For a "brick wall" filter, it is one. The noise correlation is $E_N = e_n\sqrt{BW_N}$, where e_N is the noise density ($nV/\sqrt{Hz}$).

The noise of the input signal must also be added to the noise of the DAS. Again, in calculating the rms noise contribution of the signal, the BW_N of the source must be considered. If not filter limited before the AD369 input, the BW_N of the PGA must be used, which is about $\pi/2$ times its $-3dB$ bandwidth, assuming the one-pole roll-off.

Input protection resistors will also contribute to the total system noise. The rms noise voltage of a 1kΩ resistor over a noise bandwidth of 1Hz is 4nV. So, the noise voltage of a resistor, R(kΩ) and a noise bandwidth, BW_N(Hz) is: $E_N(R) = 4nV\sqrt{R \times BW_N}$.

The total system rms noise is given by the equation:

$$E_N(\text{system}) = \sqrt{E_N(AD369)^2 + [G \times E_N(R_{IN})]^2 + [G \times E_N(\text{sig})]^2}$$

Once the system rms noise value is known, the probability of the peak-to-peak value of the noise exceeding an LSB is given to Table III.

PROBABILITY OF NOISE EXCEEDING ONE LSB

LSB/E_N	Probability
1.0	62.0%
2.0	32.0%
3.0	13.0%
4.0	4.6%
5.0	1.2%
5.15	1.0%
6.0	0.27%
6.6	0.10%

ERRORS DUE TO SYSTEM BANDWIDTH LIMITATIONS

There will be applications in which the AD369 is used to digitize sinusoids. The overall bandwidth of the AD369 is limited by the input stage of the instrumentation amplifier. The 3-dB bandwidth will vary according to which gain mode is chosen. In the $G=1$ mode, the DAS has a 3-dB roll-off at 1MHz. For $G=500$ operation, the value drops to 40kHz.

A data acquisition system with 12 bits of resolution will incur errors in precision due to frequency response limitations well before the 3-dB point. An extreme example is where an error of one LSB occurs. This frequency can be derived by using the equation of the absolute value of output to input voltage for the PGA:

$$|V_O/V_I = G/|(1 + jf/f_A)| = G/[1 + (f/f_A)^2]^{.5},$$

where f_A is the 3-dB point and f is the input frequency. The amplifier frequency response is assumed to be a single-pole roll-off. Substituting 4095/4096 (FS = 10V) for V_O/V_I and solving for f(LSB) yields:

$$f(LSB) = f_A/45.25$$

The PGA will have reached the limits of 12-bit precision for signal frequencies of f(LSB). The frequency can be doubled for every two bits of precision sacrificed:

$$f(3LSBs) = 2{*}f_A/45.25,\ f(5LSBs) = 4{*}f_A/45.25,\ \text{etc.}$$

From a total system accuracy viewpoint, this degree of dynamic precision is usually not required. For example, one LSB of roll-off in a 12-bit system is $-0.002dB$ from a full-scale input of 10V. Nevertheless, the concept is valid and should be kept in mind when converting time-varying signals.

"BUILD" VS. "BUY"

While it is clear that a system such as the one depicted earlier can be constructed from its individual components, the "build" vs. "buy" should consider the following trade-offs:

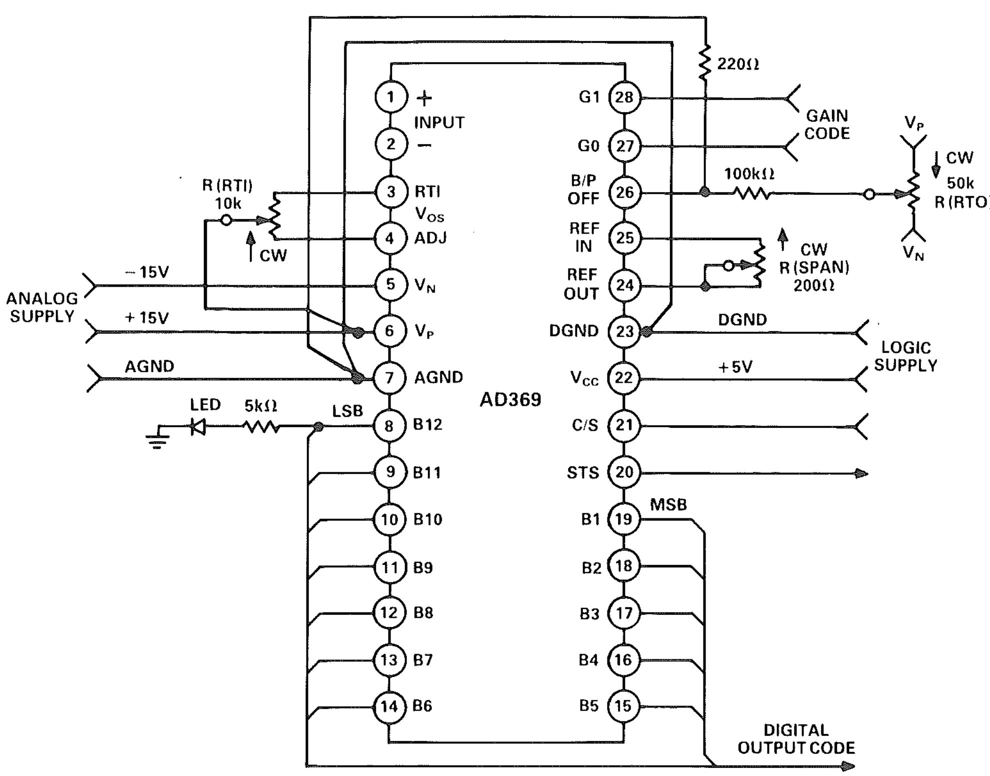
"BUILD" VS. "BUY" FOR N-CHANNEL DAS

	"BUILD"	"BUY"
Cost Per Channel	**Lower for N<3**	**Lower for N≥3**
Board Space Needed	**Less for N<3**	**Less for N≥3**
Guaranteed Specs?	**No**	**Yes**
Layout Problems	**Considerable**	**Few**
Nonrecoverable Engineering Cost (NRE)	**Higher**	**Lower**

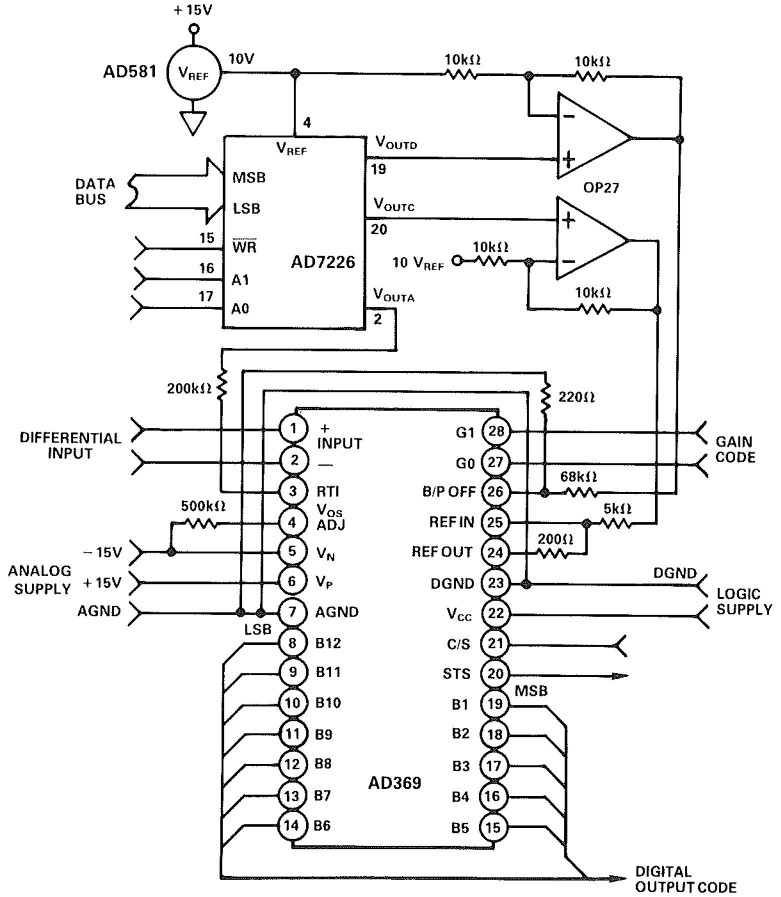
APPLYING THE AD369

Although the AD369 may be trimmed for gain and offset with three potentiometers, this process may be automated. The three potentiometers are replaced with an AD7226 Quad 8-bit CMOS DAC using only three of the DACs. Using this system, the gain and offset error of the AD369 may now be corrected under digital control. Once the three 8-bit words are determined, they may be stored in memory for auto-calibration in the field. Temperature offsets may be cancelled by using an AD590. Temperature Transducer. The ambient temperature is measured and based upon this temperature, a microprocessor then addresses three locations in memory which hold the 8-bit word values for proper trimming.

AD369 IN THE UNIPOLAR MODE WITH RTI V_{OS}, RTO V_{OS} AND SPAN TRIMPOTS

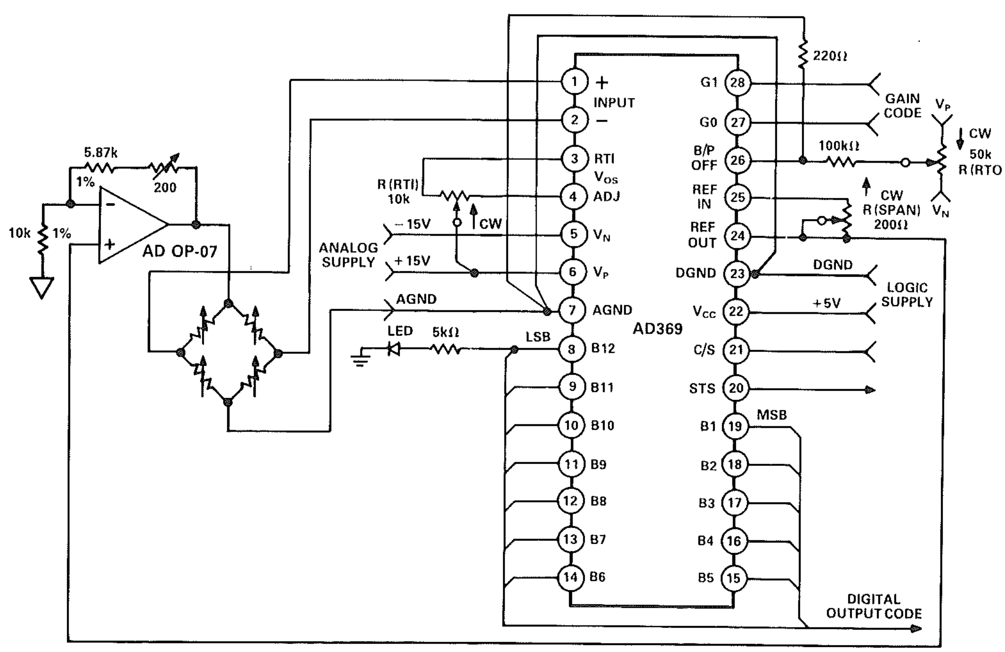


AD369 IN THE UNIPOLAR MODE WITH D/A CIRCUIT REPLACING TRIMPOTS



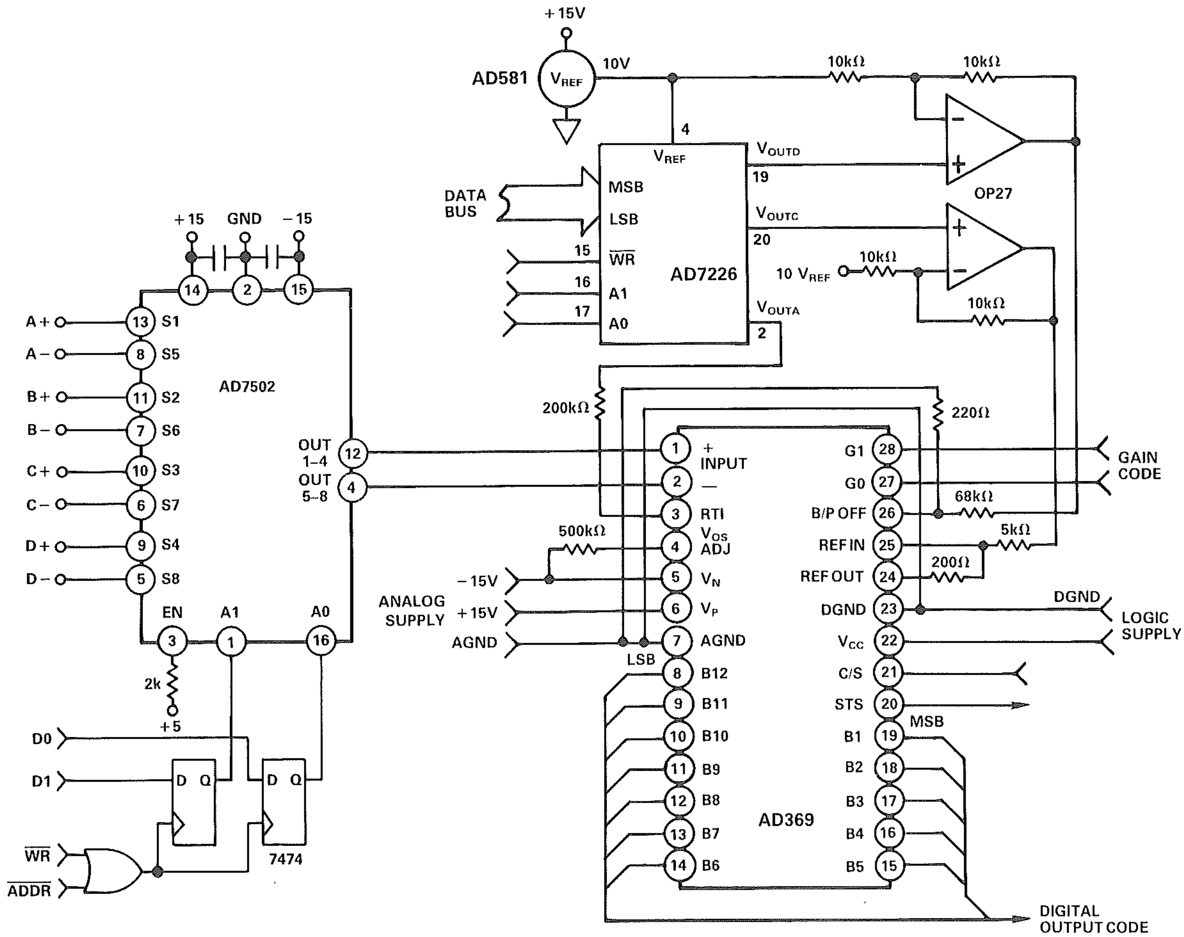
The AD369 is easily interfaced to a load cell. In the circuit shown, the AD369 6.3V internal voltage reference is applied to a noninverting gain stage of 1.6 to deliver 10V across the load cell. The cell's output will be 20mV for a force of 10kg. With the AD369 set to gain of 500, the resolution will be 2.44 grams per LSB over the 10kg range.

LOAD CELL INTERFACE TO AD369



Most data acquisition systems require measurement of several analog signals. Moreover, the system must be capable of handling a wide dynamic input range. An AD7502 Dual 4-Channel MUX will multiplex four differential signals to the AD369. The decoded address is OR'ed with the microprocessor's write strobe to latch the flip-flop. A write cycle to the AD7502 address latches the 2LSBs of the data word selecting the proper channel prior to conversion.

MULTIPLEXED ANALOG INPUTS TO AD369



HIGH THROUGHPUT SYSTEMS

High throughput data aquisition systems have three basic requirements on system dynamics. The programmable gain amplifier must settle fast to the required percent of accuracy. The sample-and-hold must exhibit fast acquisition and maintain low droop and feedthrough. The high-speed A/D converter must ensure no missing codes. In addition, the dc specifications of all components must meet the desired accuracy.

HIGH THROUGHPUT SYSTEM REQUIREMENTS

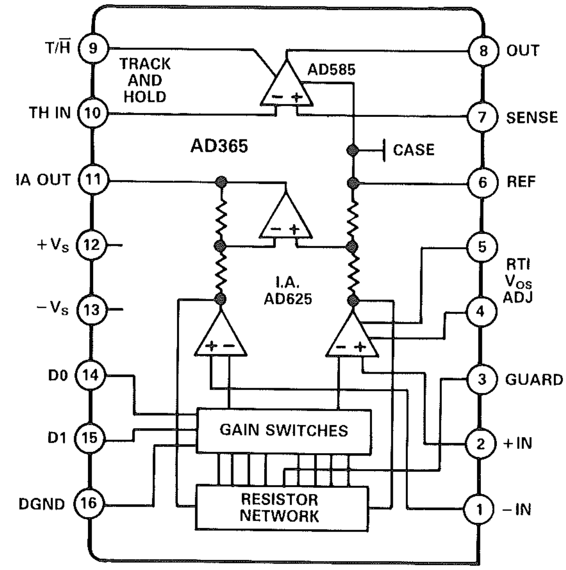
P.G.A.	• Fast Settling • Fast Gain Switching • Fast Overdrive Recovery • Low Noise
Sample-and-Hold	• Fast Acquisition • Low Droop • Low Feedthrough
A/D	• Fast Conversion • No Missing Codes • Easily Interfaced to Microprocessor

In many systems the conversion time will dominate the throughput. The fast acquisition time of the AD365, when used with a high-speed A/D converter, allows accurate digitization of high-frequency signals and high throughput rates in multichannel data acquisition systems. The AD365 can be used with a number of different A/D converters to achieve high throughput rates. The figures below show the use of an AD365 with the AD578 and AD574A.

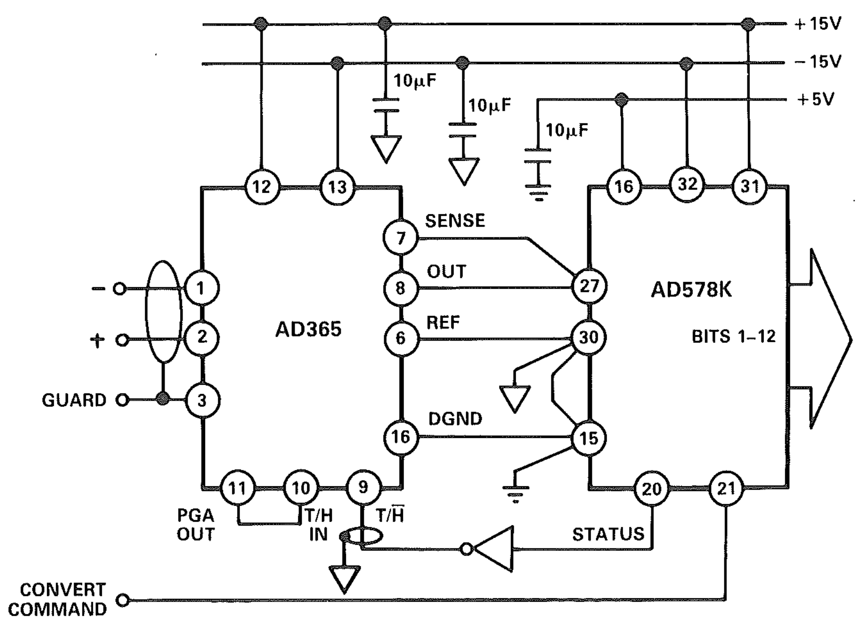
AD365 FEATURES

Software Programmable Gain (1, 10, 100, 500)
Low Input Noise (0.2μV p-p)
Low Gain Error (0.05% max)
Low Nonlinearity (0.005% max)
Low Gain Drift (10ppm/°C max)
Low Offset Drift (2μV/°C RTI max)
Fast Settling (15μs @ Gain 100)
Small 16-Pin Metal DIP

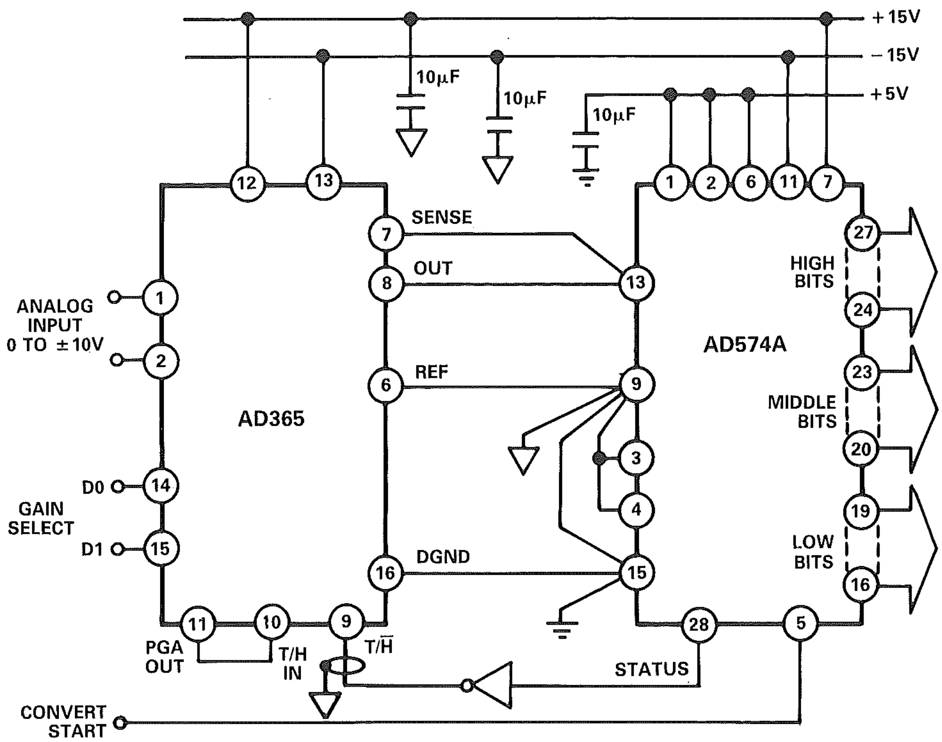
AD365 FUNCTIONAL DIAGRAM



A/D CONVERSION SYSTEM, 117.6kHz THROUGHPUT 58.8kHz MAX SIGNAL INPUT



12-BIT A/D CONVERSION SYSTEM, 26.3kHz THROUGHPUT RATE, 13.1kHz MAX SIGNAL INPUT



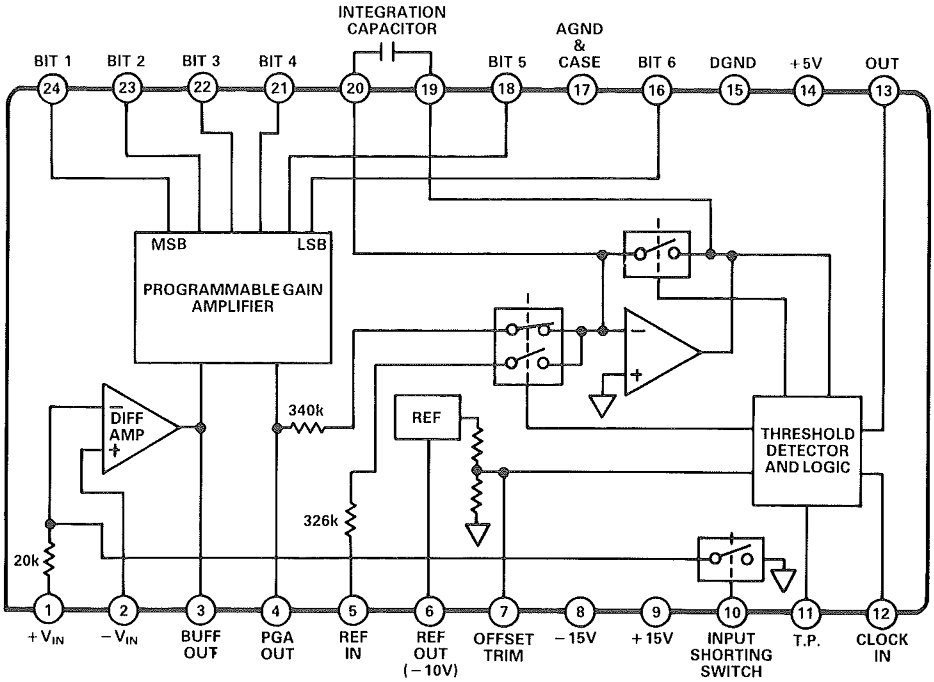
HIGH-RESOLUTION DATA ACQUISITION SYSTEM

Slow, time varying, low-level signals from pressure transducers and thermocouples often require a DAS with greater than 12 bits of resolution. Moreover, the wide dynamic range of output voltages from such sensors necessitates a programmable gain amplifier to drive the A/D converter. Using the dual slope integrating conversion technique, the AD367 provides a building block for any high-resolution system. Its input stage is programmed via a 6-bit digital code to accommodate an input range of 0.417 to 10V. The AD367 output is a pulse width whose duration is proportional to the input voltage and the gain selected. The active-low output pulse is used to gate a separate counter which accumulates pulses from a high-speed clock. This partition of the analog-to-digital conversion function into analog processing section and digital counting greatly reduces the potential for crosstalk between the noisy digital function and the low-level signal processing performed by the analog front end. This preserves the inherent rejection of high frequency normal mode noise that is a prime advantage of the dual slope conversion technique.

AD367 FEATURES

Differential Input – Programmable Gain Amplifier
6 Bit (1 of 64) Gain Control
Internal −10V Reference
15 Bit Integral Nonlinearity
±305μV Resolution
10ms Conversion Time
External Integration Capacitor
Programmable Conversion Time

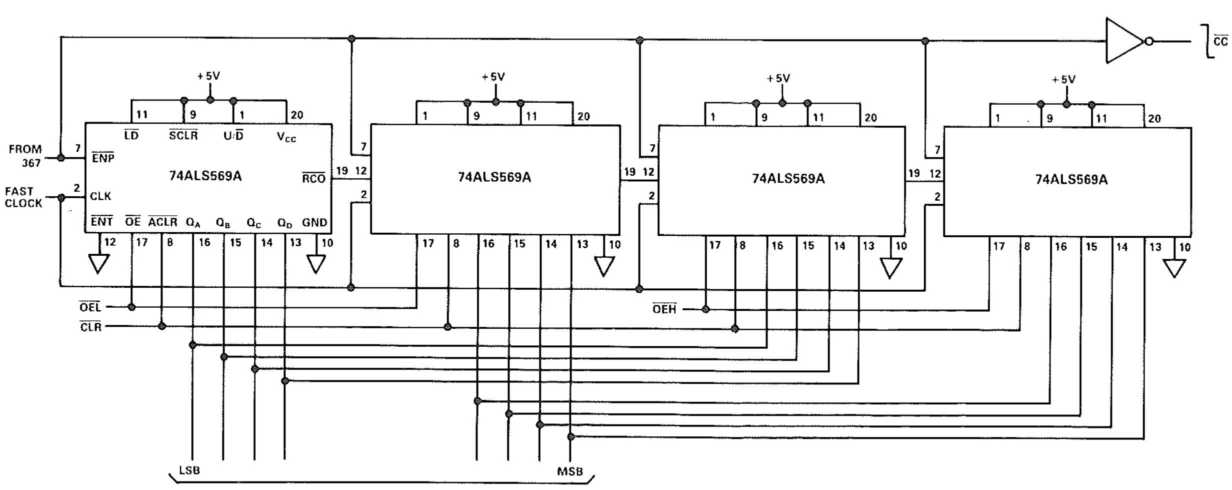
AD367 FUNCTIONAL BLOCK DIAGRAM



ADVANTAGES OF DUAL-SLOPE INTEGRATION

Conversion accuracy is independent of the length of the clock period and the integrating capacitance. Theoretical accuracy depends only on the absolute value of the reference and the stability of the clock. Even changes in other components such as the comparator input offset voltage have no effect as long as they do not change during a conversion. Differential nonlinearity is excellent since the technique is analog and inherently free from discontinuities.

GENERAL COUNTER SCHEMES 8-BIT BUS



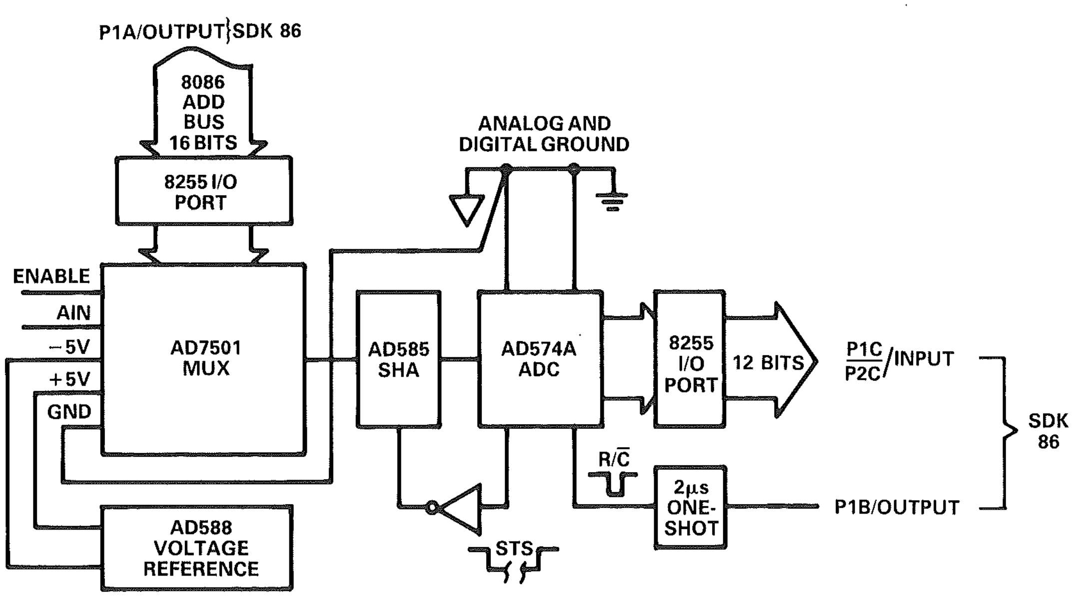
SOFTWARE AUTO CALIBRATION

The Analog Devices monolithic high-precision voltage reference, AD588, just recently introduced into the marketplace, is already setting the standard for other references to follow boasting an initial untrimmed error of 1mV, a maximum guaranteed temperature drift coefficient of 1.5 parts per million per °C and offering industry's favorite voltages of ±5V. The AD588 does indeed offer a practical and economical solution to the question "Where do I get a precision 10V reference at a reasonable price?"

The AD588 at present has sufficiently stable and absolute attributes allowing it to be used as a system reference voltage. Additionally, the attractive price of the AD588 allows the device to be used in local applications such as an on-board reference for data acquisition systems.

Data acquisition systems are generally used to monitor a number of electrical signals whose voltage values represent a physical parameter such as temperature or pressure. The AD588, being a precision voltage reference, can be used as a measuring stick to gage the absolute value of the unknown voltage from which the precise temperature or pressure can be determined. The measurement and quantification of the unknown is achieved by comparing the difference between the reference signal and the unknown signal, and correcting the unknown signal based upon the measured value of the reference signal. This is accomplished effectively in microprocessor based systems and is known as autocalibration. In the data acquisition system, for example, numerous errors such as multiplexer signal path leakage, sample-to-hold offset voltage and the offset and gain error associated with the analog-to-digital converter can be compensated. The principle involved is simply to measure and preserve voltage values as a result of stimulating the system with a known, stable reference voltage, signal ground, and the voltage representing a parametric value. The preserved values represent the absolute values plus system errors, which can be factored out mathematically. This autocalibration technique is accomplished using the AD588 reference in conjunction with an Intel 8086 microprocessor based system. Attached is a flow chart and an assembly language program describing the sequence of events for the autocalibration of a data acquisition system.

MICROPROCESSOR CONTROLLED DATA ACQUISITION SYSTEM WITH AUTO CAL



AUTOCALIBRATION SOFTWARE ROUTINE FOR SDK-86

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1571:0100   0100       FC      CLD
1571:0101   BF0005     MOV     DI,0500
1571:0104   B80400     MOV     AX,0004
1571:0107   A30003     MOV     [0300],AX
1571:010A   B080       MOV     AL,80
1571:010C   BAFFFF     MOV     DX,FFFF
1571:010F   EE         OUT     DX,AL
1571:0110   BAF9FF     MOV     DX,FFF9
1571:0113   A10003     MOV     AX,[0300]
1571:0116   EE         OUT     DX,AL
1571:0117   BAFBFF     MOV     DX,FFFB
1571:011A   BOFF       MOV     AL,FF
1571:011C   EE         OUT     DX,AL
1571:011D   F6D0       NOT     AL
1571:011F   EE         OUT     DX,AL
1571:0120   90         NOP
1571:0121   90         NOP
1571:0122   90         NOP
1571:0123   B80900     MOV     AX,0009
1571:0126   48         DEC     AX
1571:0127   75FD       JNZ     0126
1571:0129   B89B9B     MOV     AX,9B9B
1571:012C   BAFEFF     MOV     DX,FFFE
1571:012F   EF         OUT     DX,AX
1571:0130   BAFCFF     MOV     DX,FFFC
1571:0133   ED         IN      AX,DX
1571:0134   AB         STOSW
1571:0135   B80000     MOV     AX,0000
1571:0138   A10003     MOV     AX,[0300]
1571:013B   48         DEC     AX
1571:013C   75C9       JNZ     0107
1571:013E   90         NOP
1571:013F   90         NOP
1571:0140   90         NOP
1571:0141   B80008     MOV     AX,0800
1571:0144   A30006     MOV     [0600],AX
1571:0147   F8         CLC
1571:0148   A10405     MOV     AX,[0504]
1571:014B   8B1E0006   MOV     BX,[0600]
1571:014F   2BC3       SUB     AX,BX
1571:0151   730A       JNB     015D
1571:0153   A10405     MOV     AX,[0504]
1571:0156   8B1E0006   MOV     BX,[0600]
1571:015A   93         XCHG    BX,AX
1571:015B   2BC3       SUB     AX,BX
1571:015D   90         NOP
1571:015E   A30406     MOV     [0604],AX
1571:0161   90         NOP
1571:0162   F8         CLC
1571:0163   90         NOP
1571:0164   90         NOP
1571:0165   90         NOP
1571:0166   90         NOP
1571:0167   90         NOP
1571:0168   90         NOP
1571:0169   90         NOP
1571:016A   90         NOP
1571:016B   90         NOP
1571:016C   90         NOP
1571:016D   90         NOP
1571:016E   A10405     MOV     AX,[0504]
1571:0171   8B1E0006   MOV     BX,[0600]
1571:0175   2BC3       SUB     AX,BX
1571:0177   7210       JB      0189
1571:0179   A10605     MOV     AX,[0506]
1571:017C   8B1E0406   MOV     BX,[0604]
1571:0180   2BC3       SUB     AX,BX
1571:0182   A30805     MOV     [0508],AX
1571:0185   90         NOP
1571:0186   90         NOP
1571:0187   EBOF       JMP     0198
1571:0189   90         NOP
1571:018A   90         NOP
1571:018B   A10605     MOV     AX,[0506]
1571:018E   8B1E0406   MOV     BX,[0604]
1571:0192   03C3       ADD     AX,BX
1571:0194   A30805     MOV     [0508],AX
1571:0197   90         NOP
1571:0198   90         NOP
1571:0199   90         NOP
1571:019A   90         NOP
1571:019B   90         NOP
1571:019C   A10005     MOV     AX,[0500]
1571:019F   8B1E0205   MOV     BX,[0502]
1571:01A3   2BC3       SUB     AX,BX
1571:01A5   A30606     MOV     [0606],AX
1571:01A8   A10805     MOV     AX,[0508]
1571:01AB   8B1E0006   MOV     BX,[0600]
1571:01AF   F7E3       MUL     BX
1571:01B1   8B1E0606   MOV     BX,[0606]
1571:01B5   F7F3       DIV     BX
1571:01B7   A30806     MOV     [0608],AX
1571:01BA   92         XCHG    DX,AX
1571:01BB   A31006     MOV     [0610],AX
1571:01BE   B80200     MOV     AX,0002
1571:01C1   A31206     MOV     [0612],AX
1571:01C4   B80100     MOV     AX,0001
1571:01C7   A31406     MOV     [0614],AX
1571:01CA   BA0000     MOV     DX,0000
1571:01CD   A10606     MOV     AX,[0606]
1571:01D0   8B1E1206   MOV     BX,[0612]
1571:01D4   F7F3       DIV     BX
1571:01D6   A31606     MOV     [0616],AX
1571:01D9   8B1E1006   MOV     BX,[0610]
1571:01DD   F8         CLC
1571:01DE   2BC3       SUB     AX,BX
1571:01E0   730D       JNB     01EF
1571:01E2   8B1E0806   MOV     BX,[0608]
1571:01E6   A11406     MOV     AX,[0614]
1571:01E9   03C3       ADD     AX,BX
1571:01EB   A30806     MOV     [0608],AX
1571:01EE   90         NOP
1571:01EF   90         NOP
1571:01F0   90         NOP
1571:01F1   F4         HLT
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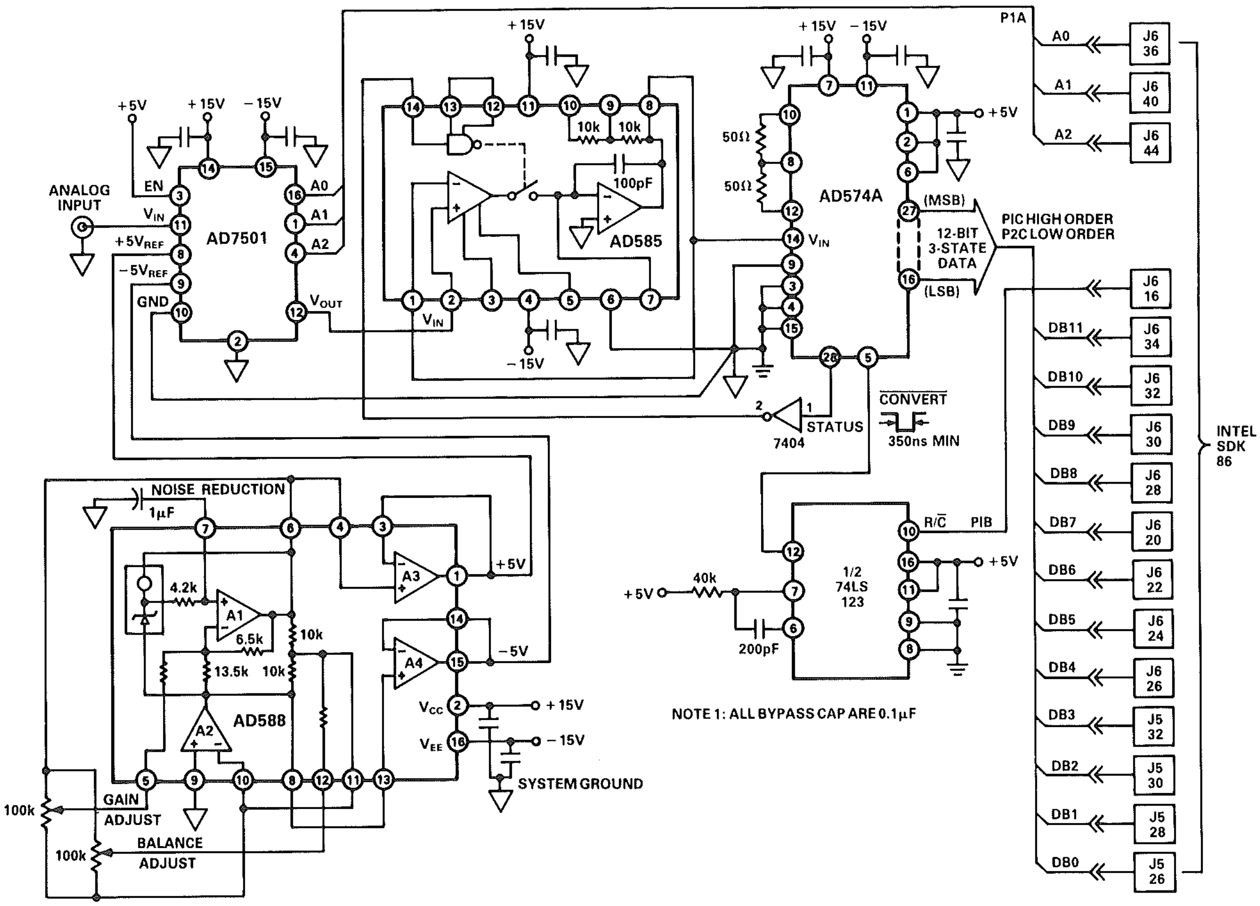
AD574A AUTO CAL USING THE AD588 VOLTAGE REFERENCE



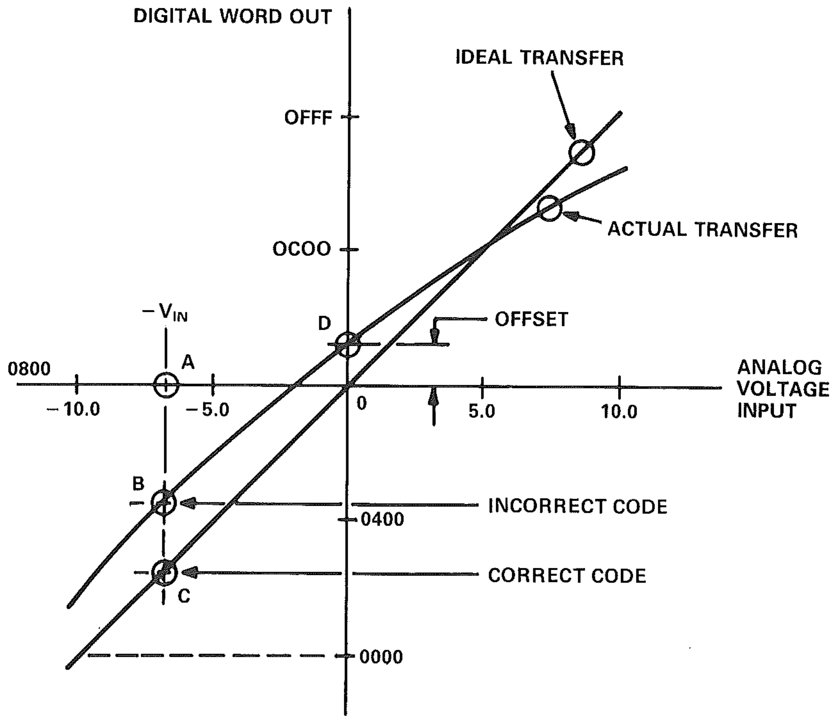
AD588 AUTOCALIBRATION MEMORY ASSIGNMENTS

The autocal program is structured such that various memory locations are used for analog inputs, temporary storage resulting from in-programming computations, constants, and the final result. Below is a table to describe the memory locations' contents.

MEMORY LOCATION	DESCRIPTION	VALUE
0500	+5.0V REFERENCE	0C00
0300	SEQUENCE VALUE	4, 3, 2, 1, 0,
0600	0C00 − 0400 = 0800	0800
0602	A LARGE NUMBER	FFFF
0604	MAGNITUDE OF OFFSET	0000
0502	−5.0 VOLT REFERENCE	0400
0606	0500 − 0502 = 0800	0800
0504	ANALOG GROUND	0800
0506	ANALOG SIGNAL	000 − FFF
0608	FINAL ANSWER	000 − FFF
0508	ANALOG SIGNAL OFFSET CORRECTED	
0610	REMAINDER	0600
0612	#2	0002
0614	#1	0001
0606	DELTA M12	0800
0616	(DELTA M12)/2	0400

Prior to elaborating on the software per se, it is instructive to review the figure below describing graphically the concept of analog-to-digital conversion. Note the ideal transfer curve passes through the origin and is without offset. This ideal transfer curve may be considered mathematically as a straight line curve of the form $Y = mX + b$ where the slope "m" is unity and the "Y" intercept "b" is zero as the curve passes through the origin and hence must be zero. The slope of the ideal transfer curve being one demands that the digital output word have a one-to-one correspondence with the input analog value. The actual transfer curve, however, is indeed different from the ideal. Considering the actual transfer curve with respect to the $Y = mX + b$ analogy, it is obvious the slope "m" is not unity or even constant but is nonlinear, and the "Y" intercept is not zero but some value called "offset". Further note that the set up is for an output in offset binary to accommodate negative input voltages. Point A represents a minus input voltage. The corresponding digital code is represented by point C. Point B represents an incorrect output code. The purpose of the autocalibration technique is to correct for the deficiencies of the actual curve (Point B), and make the system respond as if it were ideal (Point B).

ADC TRANSFER FUNCTION



The autocal program is written in five individual sections described briefly as follows: this sectioning of the autocal program was done to assist in debugging.

Section One

This section moves data into RAM; the programming is established for a minimum configuration and samples +5V (reference), −5V (reference), analog ground, and the analog signal of interest by defining the I/O ports, selecting appropriate MUX channels, starting conversions, and reading data.

Section Two

Section two computes the magnitude of the offset, delta, which is the difference between the digital output code for 0V input and the ideal digital code for a 0V input. The ideal condition would be to have offset equal to zero.

Section Three

Section three describes initial phases of signal correction and corrects the analog input signal by subtracting the offset error term. It should be pointed out that the corrections are done through math manipulations and not through fancy analog circuit tricks.

Section Four

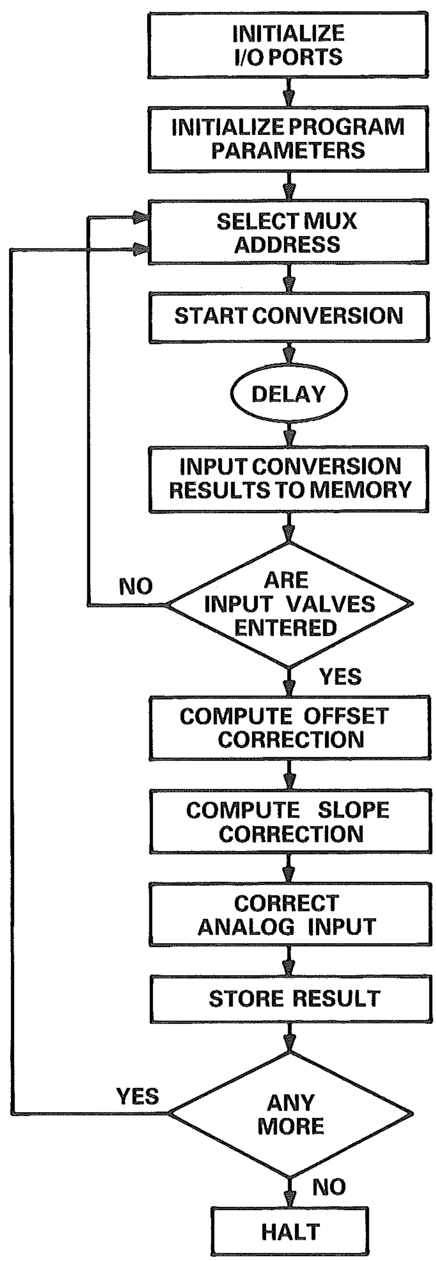
Section four computes the slope of the data acquisition system, and applies a slope correction factor to the offset corrected signal. The ideal slope is one and simply means the digital output word has a one-to-one relationship with the analog input signal. The slope correction factor is the inverse of the actual transfer slope. The actual transfer slope is calculated by first finding the difference between the digital codes corresponding to +5V (reference) and −5V (reference), and dividing this difference by the ideal code corresponding to ten.

Section Five

Since part of this routine requires mathematical division a rounding error exists, and this fifth part of the program modifies the result to account for any rounding error.

Results

The results were encouraging. Not only did the autocal technique eliminate the need for trimming the AD574ASD to achieve ±1LSB performance, the autocal technique also maintained 1LSB performance as the AD574ASD's temperature was varied between −55°C and +125°C.



HIGH-PERFORMANCE A/D CONVERTERS

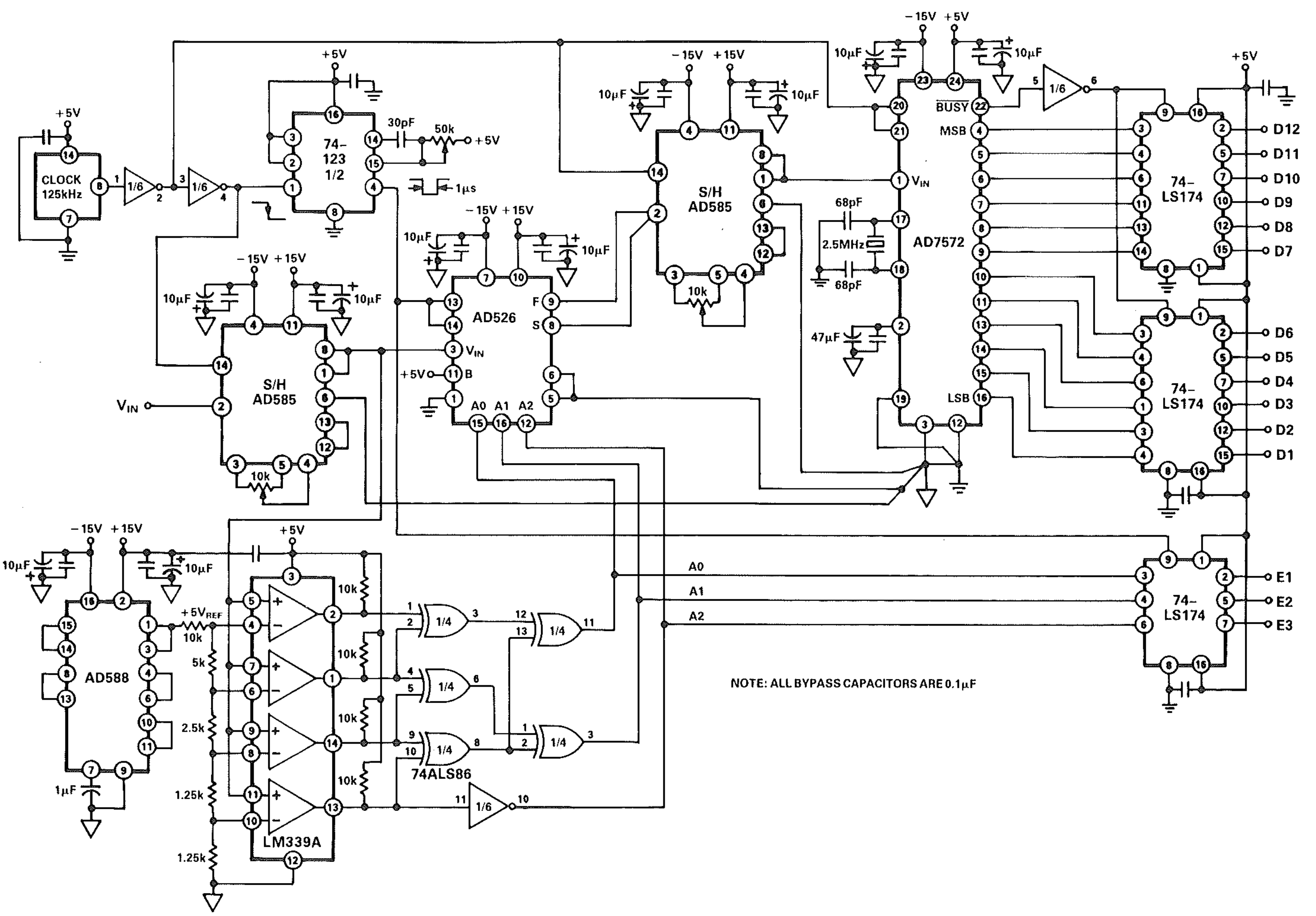
FLOATING POINT CONVERSION

High-resolution converters are used in systems to obtain high accuracy, improve the system resolution, or increase the dynamic range. There are a number of high-resolution converters available in the market with a throughput rate of 66.6kHz that can be purchased as a single component. However, in order to achieve higher throughput rates, alternative conversion techniques must be employed. A floating point A/D converter improves both the throughput rate and the dynamic range of a system by utilizing a low resolution, high-speed A/D converter, and acquiring data in two parts. In a floating point A/D converter the output data is presented as a 16-bit word, the lower 12 bits from the A/D form the mantissa and the upper 4 bits from the digital signal used to set the gain form the exponent. In the figure, an AD526 programmable gain amplifier, in conjunction with the comparator circuit, scales the input signal to a range between half scale and full scale for the maximum usable resolution.

The dynamic range of a converter is the ratio of the full-scale input range to the smallest signal the converter can detect which is the LSB value. With a floating point A/D converter, the smallest value of the LSB corresponds to the value of the LSB of the converter when the PGA is programmed for its highest gain. The floating point A/D converter has a full-scale range of 5V, a maximum gain of 16V/V from the AD526 and a 12-bit A/D converter, this corresponds to: LSB = FSR/(GAIN * 2N), LSB = (5V/[16 * 4096]) OR 76μV. The dynamic range in dBs is based on the log of the product of the amplifier gain and the converter's dynamic range. In the figure, the dynamic range is 96dB (20 LOG $[2^{12} * 2^4]$).

The floating point A/D converter achieves its high throughput rate of 125kHz by overlapping the acquisition time of the first sample/hold amplifier and settling time of the AD526 with the conversion time of the A/D converter. This conversion technique relies on the fast-settling characteristics of the AD526 after the flash autoranging (comparator) circuit quantizes the input signal. The 16-bit (LSB = 1 part in 65536) converter diagrammed in the figure consists of a pair of sample/hold amplifiers (the AD585s), flash converter, a five-range programmable gain amplifier (the AD526), and a fast 12-bit A/D converter (the AD7572). The first sample/hold

FLOATING POINT ADC
125kHz SAMPLE RATE



amplifier holds the signal for the flash autoranger, which determines which binary quantum the input falls within, relative to full scale. Once the AD526 has settled to the appropriate level then the second sample/hold amplifier can be put into hold which holds the amplified signal while the AD7572 performs its conversion routine. The acquisition time for the AD585 is 3μs and the conversion time for the AD7572 is 5μs for a total of 8μs or 125kHz. A 16-bit register holds the 3-bit output from the flash autoranger and the 12-bit output of the AD7572.

HIGH-ACCURACY A/D CONVERTERS

Very high-accuracy and high resolution floating point A/D converters can be achieved by the incorporation of offset and gain calibration routines. There are two techniques commonly used for calibration, a hardware circuit as shown in the figure and/or a software routine. In this application, the microprocessor is functioning as the autoranging circuit, requiring software overhead. Therefore, a hardware calibration technique was applied which reduces the software burden. In this floating point design the software is used to set the gain of the AD526, requiring multiple conversions from the AD574. In operation, the signal is converted, and if the MSB is not equal to a logical 1, the gain is increased by a number of binary steps, up to the maximum gain. This maximizes the full-scale range of the conversion process and insures a wide dynamic range.

The calibration technique uses two point correction, offset and gain. The hardware is simplified by the use of programmable magnitude comparators the 74ALS528, an 74ALS528 can be "burned" for particular code. The 74ALS528 will then produce a low going pulse when the conversion result and the programmed code are equal. In order to prevent under or over range hunting during the calibration process, the equivalent offset and gain codes are different from the endpoint codes. A calibration cycle consists of selecting whether offset or gain is to be calibrated, then selecting the appropriate multiplexer channel to apply the reference voltage to the signal channel. Once the operation has been initiated, the counter, a 74ALS869, drives the D/A converter in a linear fashion, providing a small correction voltage to either the gain or offset trim points. The output of the A/D converter is then compared to the value preset in the 74ALS528 to determine a match. Once a match is detected then the counter is stopped and the code at the D/A converter is latched until the next calibration cycle. Calibration cycles are under the control of the microprocessor in this application and should be implemented only during periods of converter inactivity.

HIGH-ACCURACY A/D CONVERTER