

APPENDIX A

SECTION I

READS AND PUTS DATA INTO MEMORY LOCATION [0500], [0502], [0504], [0506]

PROGRAM MEMORY	MNEMONIC	BINARY CODE	HEX CODE	DESCRIPTION/ COMMENTS
0100	DF = 0 CLEAR DIR FLAG	CLD	FC	SET CLEAR DIRECTION FLAG TO "0"
0101	MOV I TO DI	MOV 500→DI	BF	MOV IMM TO DI FOR INITIAL DATA LOCATION
0102			00	MEMORY LOCATIONS FOR ANALOG INPUT SIGNALS
0103			05	
0104	MOV IMM TO AX	MOV	B8	MOV TO [AX] 0004
0105			04	
0106			00	
0107	MOV AX TO M1 0004→0300	MOV AX ₁ [0300]	A3	MOV [AX] TO 0300
0108			00	
0109			03	
010A	MOV IMM TO AL		B0	MOV TO AL THE FOLLOWING NUMBER
010B			80	THIS DEFINES P1 AS AN AN OUTPUT PORT
010C	MOV IMM TO DX	MOV FFFF→DX	BA	MOV TO THE [DX]
010D			FF	INITIALIZE FOR OUTPUT PORT
010E			FF	PG 3-16
010F	OUT DX, AX		EE	THE [DX] REGISTER IS A POINTER FOR THE AL INSTRUCTION
0110	MOV IMM TO DX	MOV TO DX	BA	
0111			F9	LOCATION FOR DATA OUT
0112			FF	LOCATION FOR DATA OUT
0113	MOV [0300]→AX		A1	MOV [0300]→ [AX]
0114			00	
0115			03	

SECTION I (Continued)

PROGRAM MEMORY	MNEMONIC	BINARY CODE	HEX CODE	DESCRIPTION/ COMMENTS
0116	OUT DX		EE	OUTPUT AL TO DIA
0117	MOV IMM TO DX		BA	LOCATION FOR DATA OUT
0118			FB	LOCATION FOR DATA OUT
0119			FF	Pg 4-8
011A	MOV IMM TO AL		B0	MOV TO AL FF
011B			FF	NUMBER FF TO AL
011C	OUT DX		EE	OUTPUT AL TO PIB
011D	NOT AL		F6	INVERT AL
011E			D0	
011F	OUT DX		EE	OUTPUT AL TO PIB
0120	NOP		90	NO OPERATION
0121	NOP		90	NO OPERATION
0122	NOP		90	NO OPERATION
0123	MOV IMM TO AX		B8	MOV IMM TO AX
0124			09	NUMBER INTO
0125			00	ACCUMULATOR
0126	DEC AX		48	DECREMENT AX
0127	JNZ		75	JUMP NOT ZERO
0128			FD	FD = FF-02
0129	MOV IMM TO AX		B8	MOV IMM TO AX
012A			9B	THIS WORD DEFINES P2/P1 AS AN INPUT PORT
012B			9B	
012C	MOV IMM TO DX		BA	MOV TO THE DX REGISTER THE FOLLOWING NUMBER
012D			FE	PORT ADDRESS PG 3-16
012E			FF	PORT ADDRESS PG 3-16
012F	OUT AX, DX		EF	THE DX REGISTER ACTS AS A POINTER FOR THE AX REGISTER
0130	MOV IMM TO DX		BA	MOV TO DX THE FOLLOWING NUMBER FFFC
0131			FC	THIS NUMBER DEFINES THE PORT INPUT ADDRESS
0132			FF	
0133	IN DX		ED	THE CONTENTS OF STORE DATA AT DI (0500) INDEXES THE DI ONE
0134	STDS W		AB	
0135			B8	MOV IMM TO AX
0136			00	PLACE ALL ZEROS INTO ACCUMULATOR
0137			00	

SECTION I (Continued)

PROGRAM MEMORY	MNEMONIC	BINARY CODE	HEX CODE	DESCRIPTION/ COMMENTS
0138	MOV [0300]→AX		AX	MOV [0300] → AX
0139			00	THE CONTENTS OF MEMORY LOCATION [0300] ARE LOADED INTO THE ACCUMULATOR
013A			03	
013B	DEC AX		48	DECREMENT AX REDUCE AX BY ONE
013C	JNZ		75	JUMP NOT ZERO
013D			C9	THIS MANY BACK (FF – XX) = C9
013E	JUMP UNCONDITIONAL	EB	EB	JUMP ON ANYTHING
			90	NO OP
013F			C1	THIS MUCH
			90	NO OP
0140			F4	STOP
			90	NO OP

SECTION II

COMPUTES OFFSET AND STORES IN [06??]

PROGRAM MEMORY	MNEMONIC	BINARY CODE	HEX CODE	DESCRIPTION/ COMMENTS
0141	MOV IMM TO AX		B8	MOV IMM TO AX
0142			00	000 – 0400 = 0800
0143			08	000 – 0400 = 0800
0144	MOV AX→[0600]		A3	MOV AX → [0600]
0145			00	MEMORY LOCATION
0146			06	FOR (0800)
0147			F8	CLEAR CARRY FLAG
0148			A1	MOV [0504] → AX
0149			04	MEMORY LOCATION FOR
014A			05	ANALOG GROUND ≈0800 ± 2
014B			8B	MOV [0600] → BX
014C			1E	MOV [0600] → BX
014D			00	MEMORY LOCATION
014E			06	FOR 0800
014F			2B	
0150			C3	AX – BX = AX
0151			73	JUMP IF CF = 0
0152			0A	← THIS MANY
0153			A1	MOV [0504] → AX
0154			04	MEMORY LOCATION FOR
0155			05	ANALOG GROUND 0800 ± 3
0156			8B	MOV [0600] = BX
0157			1E	
0158			00	MEMORY LOCATION [0600]
0159			06	[0600] CONTAINS NUMBER 0800
015A			93	SWAP AX → ← BX
015B			2B	AX – BX = AX
015C			C3	AX – BX = AX
015D			90	NO OP
015E			A3	MOV AX → [0604]
015F			04	MEMORY LOCATION
0160			06	Δ OFFSET
0161			F4	HALT
			90	NO OP

SECTION III

TAKES [0604] (OFFSET 1), COMPARES GROV REFERENCE AND COMPUTES AIN¹
 AIN¹ = AIN ± OFFSET

PROGRAM MEMORY	MNEMONIC	BINARY CODE	HEX CODE	DESCRIPTION/ COMMENTS
0162			F8	CLEAR CARRY FLAG
0163			90	NO OP
0164			90	NO OP
0165			90	NO OP
0166			90	NO OP
0167			90	NO OP
0168				NO OP
0169			90	NO OP
016A			90	NO OP
016B			90	NO OP
016C			90	NO OP
016D			90	NO OP
016E			A1	MOV [0504] → <u>AX</u>
016F			04	LOCATION FOR ANALOG GROUND
0170			05	
0171			8B	MOV [0600] → <u>BX</u>
0172			1E	MOV [0600] → <u>BX</u>
0173			00	LOCATION FOR 0800
0174			06	LOCATION FOR 0800
0175			2B	<u>AX</u> - <u>BX</u> = <u>AX</u>
0176			C3	<u>AX</u> - <u>BX</u> = <u>AX</u>
0177			72	JUMP IF CF → 1
0178			10	← THIS MANY
0179			A1	MOV [0506] → <u>AX</u>
017A			06	LOCATION FOR AIN
017B			05	LOCATION FOR AIN
017C			8B	MOV [0604] → <u>BX</u>
017D			1E	[0604] → DELTA
017E			04	MEMORY LOCATION FOR DELTA OFFSET
017F			06	
0180			2B	<u>AX</u> = <u>AX</u> - <u>BX</u>
0181			C3	<u>AX</u> = <u>AX</u> - <u>BX</u>
0182			A3	MOV <u>AX</u> → [0508]
0183			08	AIN ¹
0184			05	AIN ¹
0185			90	NO OP
0186			90	NO OP
0187			EB	JUMP UNCONDITIONAL
0188			OF	THIS MANY

SECTION III (Continued)

PROGRAM MEMORY	MNEMONIC	BINARY CODE	HEX CODE	DESCRIPTION/ COMMENTS
0189			90	
018A			90	
018B			A1	MOV [0506] → AX
018C			06	MEM LOCATION FOR AIN
018D			05	
018E			8B	MOV [0604] → BX
018F			1E	
0190			04	MEMORY LOCATION FOR DELTA
0191			06	
0192			03	AX = AX + BX
0193			C3	AX = AX + BX
0194			A3	MOV AX → [0508]
0195			08	
0196			05	AIN ¹
0197			90	NO OP
0198			90	NO OP
0199			90	NO OP
019A			90	NO OP
019B			F4	NO OP
			90	

Section IV

COMPUTES THE VALUE FOR THE ANALOG INPUT BY CORRECTING SLOPE

PROGRAM MEMORY	MNEMONIC	BINARY CODE	HEX CODE	DESCRIPTION/ COMMENTS
019C			A1	MOV [0500] → AX $V_{REF} + \approx 0C00$
019D			00	MEMORY LOCATION
019E			05	MEMORY LOCATION
019F			8B	MOV [0502] → BX $V_{REF} - \approx 0400$
01A0			1E	
01A1			02	MEMORY LOCATION
01A2			05	FOR $-5V_{REF} \approx 0400$
01A3			2B	AX - BX = AX
01A4			C3	
01A5			A3	MOV AX → [0606]
01A6			06	THIS IS THE LOCATION
01A7			06	FOR $\Delta M12$
01A8			A1	MOV AIN ¹ [0508] → AX
01A9			08	MEMORY LOCATION FOR
01AA			05	CORRECTED ANALOG SIGNAL
01AB			8B	MOV [0600] → BX
01AC			1E	MOV [0600] → BX
01AD			00	MEMORY LOCATION
01AE			06	FOR 0800
01AF			F7	MULT AX BY BX
01B0			E3	STORE RESULTS IN DX AX
01B1			8B	MOV [0606] (DM12) → BX
01B2			1E	MOV [0606] (DM12) → BX
01B3			06	
01B4			06	LOCATION FOR DM12
01B5			F7	DIVIDE DX AX
01B6			F3	BY BX = AX BX
01B7			A3	MOV AX → [0608]
01B8			08	LOCATION FOR FINAL
01B9			06	ANSWER

Section V

MODIFIES ANSWER TO ACCOUNT FOR ROUNDING ERRORS

PROGRAM MEMORY	MNEMONIC	BINARY CODE	HEX CODE	DESCRIPTION/ COMMENTS
01BA			92	SWAP $\boxed{AX}$ $\rightarrow$ $\leftarrow \boxed{DX}$
01BB			A3	MOV $\boxed{AX}$ $\rightarrow$ [0610]
01BC			10	LOCATION FOR REMAINDER
01BD			06	LOCATION FOR REMAINDER
01BE			B8	MOV IMM TO $\boxed{AX}$
01BF			02	NUMBER 2
01C0			00	NUMBER 2
01C1			A3	MOV $\boxed{AX}$ $\rightarrow$ [0612]
01C2			12	LOCATION FOR #2
01C3			06	LOCATION FOR #2
01C4			B8	MOV IMM TO $\boxed{AX}$
01C5			01	#1
01C6			00	#1
01C7			A3	MOV $\boxed{AX}$ $\rightarrow$ [0614]
01C8			14	LOCATION FOR 0001
0109			06	LOCATION FOR 0001
01CA			BA	MOV IMM $\rightarrow$ $\boxed{DX}$
01CB			00	#0000
01CC			00	#0000
01CD			A1	MOV [0606] $\rightarrow$ $\boxed{AX}$
01CE			06	MEMORY LOCATION
01CF			06	MEMORY LOCATION
01D0			8B	MOV [0612] $\rightarrow$ $\boxed{BX}$
01D1			1E	
01D2			12	MEMORY LOCATION FOR #2 (0002)
01D3			06	
01D4			F7	DIV $\boxed{DX}$ $\boxed{AX}$
01D5			F3	BY $\boxed{BX}$ = $\boxed{AX}$ $\boxed{DX}$
01D6			A3	MOV $\boxed{AX}$ $\rightarrow$ [0616]
01D7			16	$\frac{\Delta M12}{2} \approx 0400$
01D8			06	$\frac{\Delta M12}{2} \approx 0400$
01D9			8B	MOV [0610] $\rightarrow$ $\boxed{BX}$
01DA			1E	
01DB			10	LOCATION OF REMAINDER
01DC			06	LOCATION OF REMAINDER
01DD			F8	CLEAR CARRY FLAG
01DE			2B	$\boxed{AX} - \boxed{BX} = \boxed{AX}$
01DF			C3	

SECTION V (Continued)

PROGRAM MEMORY	MNEMONIC	BINARY CODE	HEX CODE	DESCRIPTION/ COMMENTS
01E0			73	JUMP IF CF = 0
01E1			0D	← THIS MANY
01E2			8B	MOV [0608] → BOX
01E3			1E	
01E4			08	LOCATION OF ANSWER
01E5			06	LOCATION OF ANSWER
01E6			A1	MOV [0614] → AX
01E7			14	NUMBER 0001 LOCATION
01E8			06	NUMBER 0001 LOCATION
01E9			03	AX + BOX = AX
01EA			C3	
01EB			A3	MOV AX → 0608
01EC			08	MEMORY LOCATION FOR ANSWER
01ED			06	
01EE			90	NO OP
01EF			90	NO OP
01F0			90	NO OP
01F1			F4	HALT

APPENDIX B

BINARY BIT WEIGHTS OR RESOLUTION

BIT	2^{-n}	$1/2^n$ (Fraction)	"dB"	$1/2^n$ (Decimal)	%	ppm
FS	2^0	1	0	1.0	100	1,000,000
MSB	2^{-1}	1/2	-6	0.5	50.	500,000
2	2^{-2}	1/4	-12	0.25	25	250,000
3	2^{-3}	1/8	-18.1	0.125	12.5	125,000
4	2^{-4}	1/16	-24.1	0.0625	6.2	62,500
5	2^{-5}	1/32	-30.1	0.03125	3.1	31,250
6	2^{-6}	1/64	-36.1	0.015625	1.6	15,625
7	2^{-7}	1/128	-42.1	0.007812	0.8	7,812
8	2^{-8}	1/256	-48.2	0.003906	0.4	3,906
9	2^{-9}	1/512	-54.2	0.001953	0.2	1,953
10	2^{-10}	1/1,024	-60.2	0.0009766	0.1	977
11	2^{-11}	1/2,048	-66.2	0.00048828	0.05	488
12	2^{-12}	1/4,096	-72.2	0.00024414	0.024	244
13	2^{-13}	1/8,192	-78.3	0.00012207	0.012	122
14	2^{-14}	1/16,384	-84.3	0.000061035	0.006	61
15	2^{-15}	1/32,768	-90.3	0.0000305176	0.003	31
16	2^{-16}	1/65,536	-96.3	0.0000152588	0.0015	15
17	2^{-17}	1/131,072	-102.3	0.00000762939	0.0008	7.6
18	2^{-18}	1/262,144	-108.4	0.000003814697	0.0004	3.8
19	2^{-19}	1/524,288	-114.4	0.000001907349	0.0002	1.9
20	2^{-20}	1/1,048,576	-120.4	0.0000009536743	0.0001	0.95

APPENDIX C

STANDARD VALUE DECADE FOR 1% DECADE FOR 1% FILM RESISTORS

Ohms*

10.0	14.7	21.5	31.6	46.4	68.1
10.2	15.0	22.1	32.4	47.5	69.8
10.5	15.4	22.6	33.2	48.7	71.5
10.7	15.8	23.2	34.0	49.9	73.2
11.0	16.2	23.7	34.8	51.1	75.0
11.3	16.5	24.3	35.7	52.3	76.8
11.5	16.9	24.9	36.5	53.6	78.7
11.8	17.4	25.5	37.4	54.9	80.6
12.1	17.8	26.1	38.3	56.2	82.5
12.4	18.2	26.7	39.2	57.6	84.5
12.7	18.7	27.4	40.2	59.0	86.6
13.0	19.1	28.0	41.2	60.4	88.7
13.3	19.6	28.7	42.2	61.9	90.9
13.7	20.0	29.4	43.2	63.4	93.1
14.0	20.5	30.1	44.2	64.9	95.3
14.3	21.0	30.9	45.2	66.5	97.6

*Standard resistance values are obtained from the decade by multiplying by powers of 10. Ex.: 13.3 can be 13.3, 133, 1.33K, 13.3K, 133K, or 1.33MΩ.

APPENDIX D

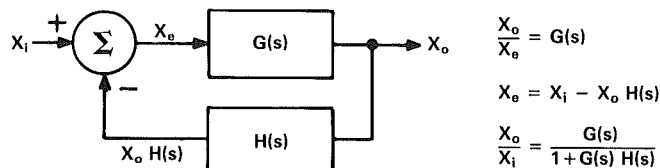
NEGATIVE FEEDBACK TECHNIQUES

The concept of negative feedback is of considerable importance in the design of electronic systems. Negative feedback techniques allow the electronic designer to be more accurate in the prediction and control of the performance of his systems, and to achieve that control by the use of stable well-characterized passive elements such as resistors, capacitors and, sometimes, inductors.

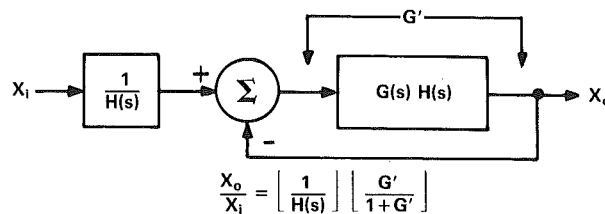
In all feedback controlled systems a signal derived from the system output is applied to a summing point where it is added to the original input signal and applied to an amplifier which drives the system output. The system is thereby stabilized. It should be clearly understood that negative feedback is a general physical concept which applies to systems of all types, not merely electronic ones, even though negative feedback in electronic systems is the only type that will be discussed in this seminar. Negative feedback techniques can be used in electronic systems to stabilize gain, bandwidth, impedance levels, velocity, position, or any physical parameter which can be converted to an electrical signal to be fed into the summing point.

A generalized diagram of a negative feedback system is shown in the diagram, as is a restructured version of the same system which has been redrawn to demonstrate more clearly how a negative feedback network works. (The feedback need not actually be negative—positive feedback systems are equally possible but are of more limited use, although the same analyses work for them.)

GENERALIZED FEEDBACK NETWORK



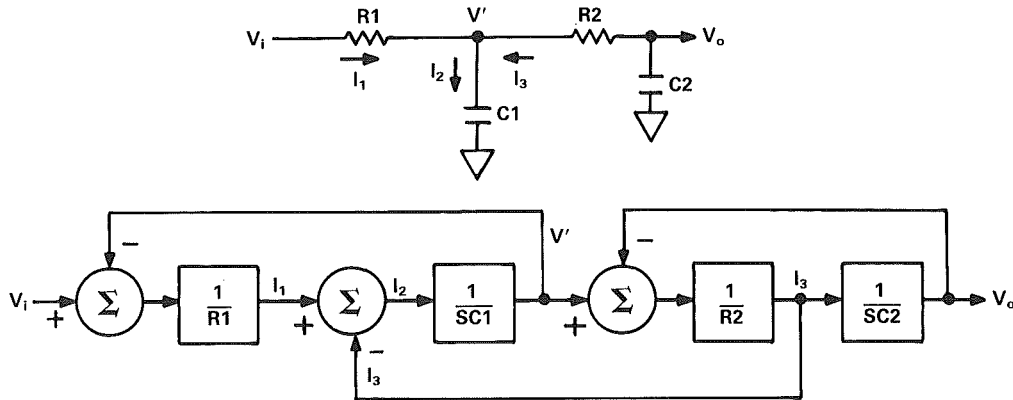
RESTRUCTURED FORM OF GENERALIZED FEEDBACK NETWORK



Consider the diagram. For large values of the product $G(s)H(s)$ the ratio X_o/X_i approaches a value of $1/[H(s)]$, indicating a distinct advantage of a negative feedback system: if the open loop gain is sufficiently large the system gain is determined by feedback and the open loop gain does not significantly affect it.

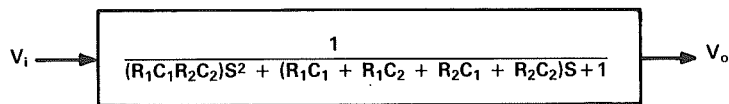
Electronic feedback systems can have voltage feedback, current feedback or both.

RESISTOR CAPACITOR NETWORK AND EQUIVALENT FEEDBACK MODEL



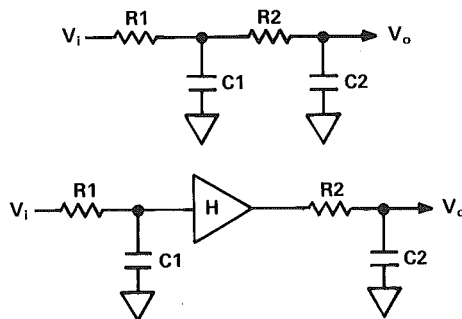
Even resistors—capacitor networks maybe modelled as a feedback network or control system. The system shown illustrates both voltage and current feedback and each element in the circuit represents a stand alone transfer function. Some simple mathematical manipulation can reduce the complex form to a simple block.

EQUIVALENT RESISTOR CAPACITOR NETWORK REDUCED TO A SINGLE BLOCK

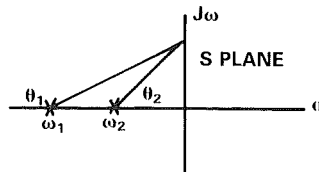


Control system analysis is a convenient means of describing many physical occurrences which we take for granted. Consider walking around with closed eyes—this represents a system with minimal negative feedback. At best one would have to move slowly and unless guided it would be quite difficult not to stumble into obstacles. Even with sight there are limitations upon the speed with which one could negotiate obstacles. This speed limitations may be regarded as the system frequency response and is directly related to the mechanics of the system. Practically speaking the frequency response is a measure of how quickly the system can respond to changes at the input.

ISOLATION BETWEEN STAGES SIMPLIFIES ANALYSIS



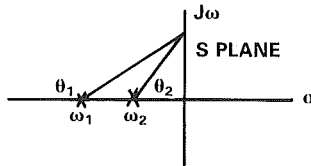
ISOLATION/NONISOLATION COMPARISON



$$\omega_1 = \frac{-(R_1C_1 + R_1C_2 + R_2C_1 + R_2C_2) + \sqrt{(R_1C_1 + R_1C_2 + R_2C_1)^2 - 4(R_1C_1R_2C_2)}}{2(R_1C_1R_2C_2)}$$

$$\omega_2 = \frac{-(R_1C_1 + R_1C_2 + R_2C_1 + R_2C_2) - \sqrt{(R_1C_1 + R_1C_2 + R_2C_1)^2 - 4(R_1C_1R_2C_2)}}{2(R_1C_1R_2C_2)}$$

NONISOLATED



$$\omega_1 = \frac{1}{R_1C_1}$$

$$\omega_2 = \frac{1}{R_2C_2}$$

ISOLATED

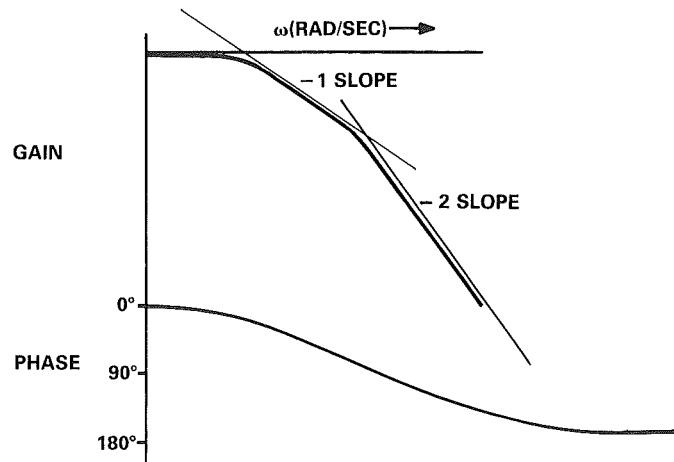
Obviously a single capacitor resistor circuit is easier to analyze than a cascaded dual capacitor resistor network for there is no interaction between the networks. But the two-resistor two-capacitor network is quite easy to analyze provided an isolation stage is placed between the circuits. Clearly each network has two poles, but in the nonisolated case repositioning one pole causes a shift in the location of the other. However, irrespective of the circuit topology the output phase is equal to the sum of θ_1 and θ_2 . The pole zero representation is a convenient method to visualize the phase response as the input frequency is varied. The pole zero diagram does not give much insight with regard to the absolute magnitude of the response, however, and Bode plot, or gain magnitude phase plot, is necessary. Consider again the resistor capacitor network resulting in two poles located at ω_1 and ω_2 whose values are 300 and 900 radians per second respectively. At low frequencies the phase shift approaches zero and at high frequencies the phase shift approaches zero and at high frequencies it approaches 180° . The fundamental equation for this response is:

$$\theta_T = \theta_1 + \theta_2$$

$$\theta_T = \tan^{-1} \omega/\omega_1 + \tan^{-1} \omega/\omega_2$$

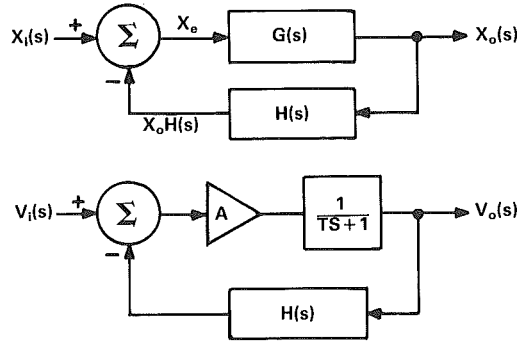
This response is consistent with the one implied by the pole zero diagram.

GAIN MAGNITUDE/FREQUENCY & PHASE/FREQUENCY PLOTS FOR 2 RESISTOR/2 CAPACITOR LOW PASS FILTER



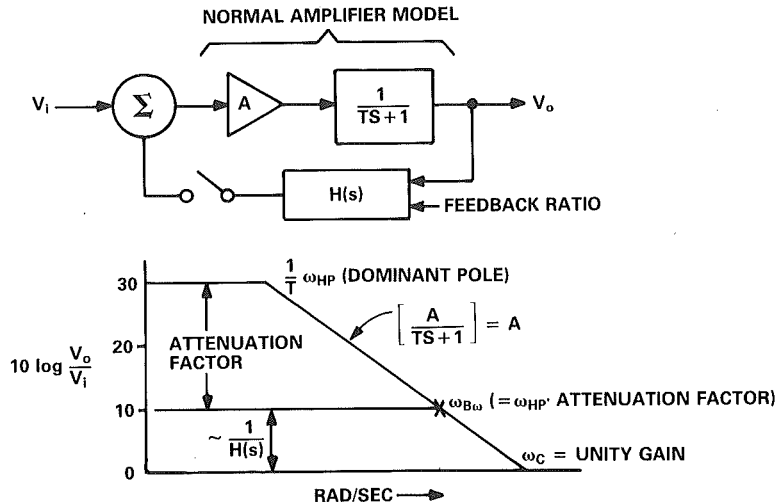
The resistor-capacitor network is referred to as a passive network because no external power is required to make it function. There is no amplification and the network is not capable of increasing power levels of its own. Any of the amplifier types that we discussed earlier may be used in a feedback system to increase power levels or provide isolation between the input and output. At present, however, we shall use a voltage amplifier in our examples since today op amps are the commonest type of amplifier to be used in such systems.

GENERAL FORM OF FEEDBACK NETWORK AND AN AMPLIFIER CASCADED WITH A LOW PASS STRUCTURE



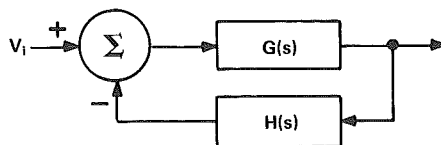
A voltage amplifier followed by a low pass filter is a reasonable first order approximation to a voltage amplifier with a dominant pole. The dominant pole is the major element in determining the frequency response of the system. The gain magnitude plot of the amplifier and low pass filter is similar to that of a low pass filter on its own except that the amplifier system has gain.

GAIN MAGNITUDE PLOT FOR AN IDEAL VOLTAGE AMPLIFIER WITH GAIN "A" AND CASCADED LOW PASS FILTER



This type of response is typical for operational amplifiers that are internally compensated. The system is stable for all values of attenuation factor (stable for unity gain). The stability factor can be determined if the gain magnitude and feedback ratio $H(s)$ are known. The feedback ratio is shown as $H(s)$ for "H" and is generally frequency dependent. For the system to be stable the product $G(s)H(s)$ should be less than unity when the phase-shift is 180° . If at any frequency the product $G(s)H(s)$ is greater than unity at 180° phase-shift the system will be unstable and oscillate. (Don't tell marketing—they'll want to offer it as an option.)

CONTROL SYSTEM STABILITY REQUIREMENT



FOR STABLE OPERATION $G(s)H(s) < 1$ at 180° PHASE SHIFT

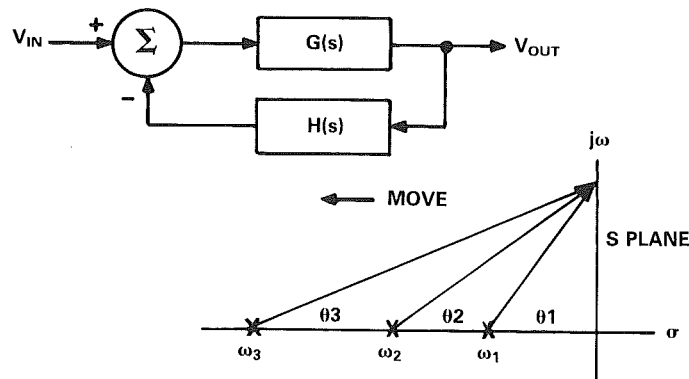
As an example consider an amplifier with a low frequency gain $A_O = -1000$ and poles f_1 , f_2 and f_3 located at 50kHz, 1MHz and 2MHz respectively. Is this amplifier stable for $H(s) = -0.005$ and $H(s) = -0.02$?

EXAMPLE 1

$$A_O = -10^3 \text{ V/V}, \omega_1 = 0.5 \times 10^6 \text{ r/s}, \omega_2 = 1.0 \times 10^6 \text{ r/s}$$

$$\omega_3 = 2.0 \times 10^6 \text{ r/s}$$

$$H(s) = -0.003, -0.02$$



FOR STABILITY $G(s) H(s) < 1.0$ 1180°

$\therefore$ AT WHAT FREQUENCY DOES $\theta_1 + \theta_2 + \theta_3 = 180^\circ$

$$A(f) = \frac{A_O}{\left(1 + \frac{j\omega}{\omega_1}\right) \left(1 + \frac{j\omega}{\omega_2}\right) \left(1 + \frac{j\omega}{\omega_3}\right)} =$$

$$A(f) = - \frac{10^3}{\left(1 + \frac{j\omega}{0.5 \times 10^6}\right) \left(1 + \frac{j\omega}{1 \times 10^6}\right) \left(1 + \frac{j\omega}{2 \times 10^6}\right)} =$$

A pole zero diagram will help get started on the problem by displaying the output phase variation as a function of frequency. Additionally, setting up an equation for the gain will allow us to find the frequency for which the output phase is 180° . For this problem it is only necessary to plot the loop gain $G(s)H(s)$ and obtain a root locus since all that is of interest is whether or not stability exists for two values of $H(s)$.

EXAMPLE 1 (CONTINUED)

$$A(f) = \frac{A_O}{(1 - 3.5f^2) + j(3.5f - f^3)}$$

FOR $180^\circ \text{ Im}[A(f)] = 0$

$$\therefore 3.5f - f^3 = 0 = 3.5 - f^2$$

$$f^2 = 3.5, f = 1.87 \text{ MHz}$$

$$A(f) = \frac{-10^3}{[1 - (3.5)(1.87)^2]} = 88.97 \text{ V/V}$$

$\theta = 180$

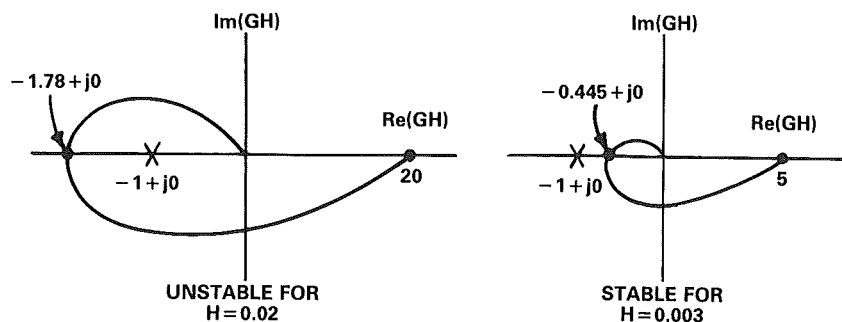
AGAIN $GH < 1 < 180^\circ$

FOR $H = -0.005$

$$GH = (88.97)(0.005) = -0.445 \text{ STABLE}$$

FOR $H = -0.02$

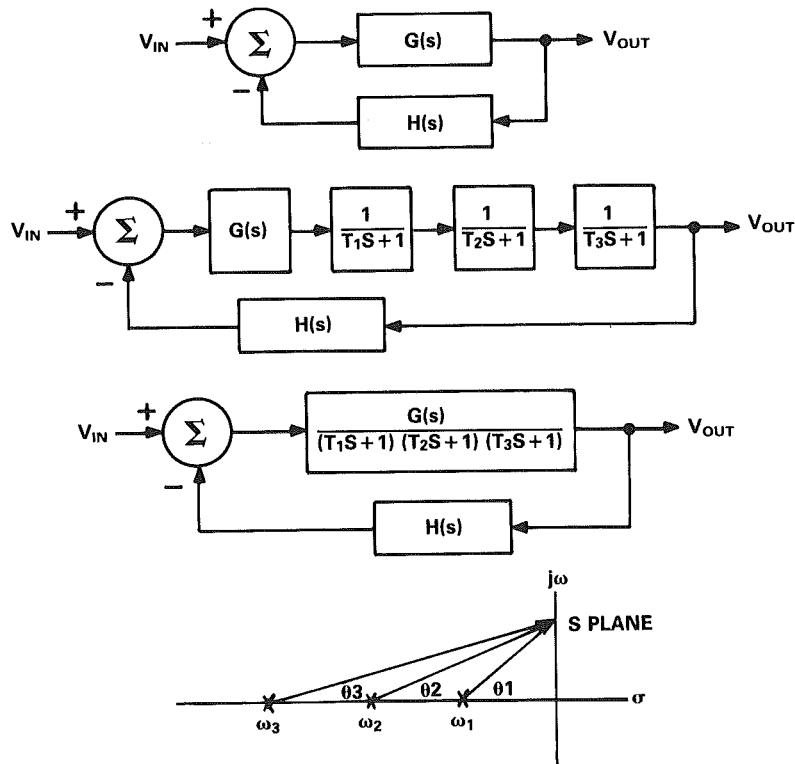
$$GH = (88.97)(0.02) = -1.78 \text{ UNSTABLE}$$



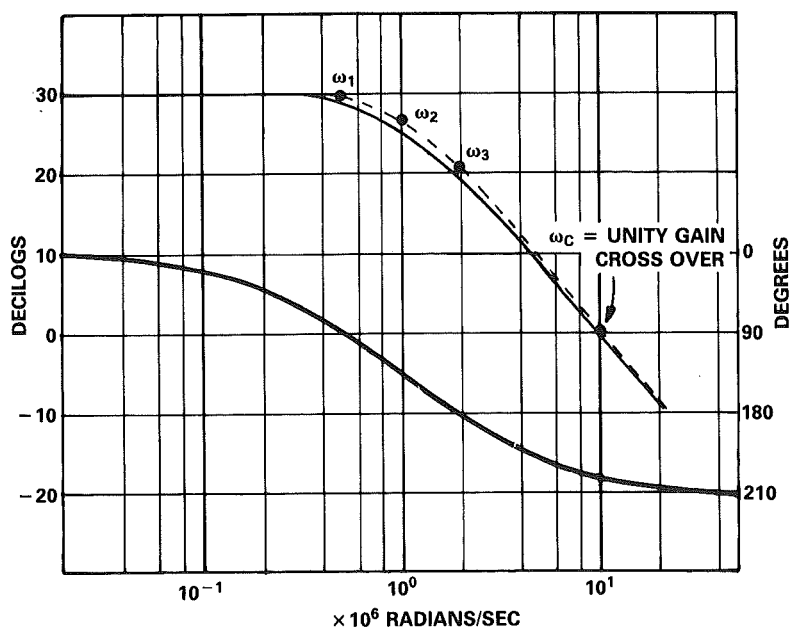
A combination of analytical and graphical techniques considerably assists the development of insight into a problem. In this case it can be seen that for an $H(s)$ of 0.02 the amplifier is unstable and for an $H(s)$ of 0.005 it is stable.

EXAMPLE 2

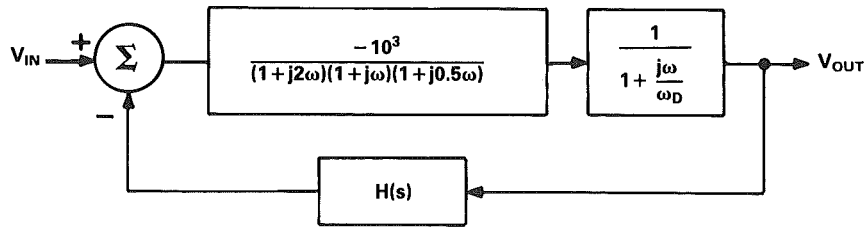
$$A_0 = -10^3 \text{ V/V}, \omega_1 = 0.5 \times 10^6 \text{ r/s}, \omega_2 = 1.0 \times 10^6 \text{ r/s}, \omega_3 = 2.0 \times 10^6 \text{ r/s}$$



The amplifier gain magnitude and phase response is plotted. The Bode plot reveals that the gain at a phase shift of 180° is in agreement with the computed value of 89 V/V . From both the root locus plot and the Bode plot it is obvious that the amplifier cannot be used in a system where the closed loop gain is less than 89 V/V . However, at a gain of 89 V/V the amplifier bandwidth is approximately 318 kHz . The location of the poles at ω_1 , ω_2 and ω_3 are inherent in the design. It is possible, however, to add a dominant pole to the amplifier such that it will be stable for all closed loop gains. The disadvantage of doing this is that the bandwidth is reduced.

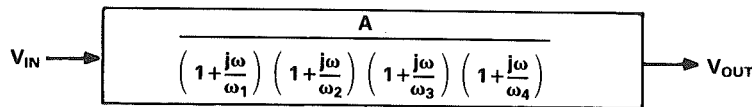


ω_D REPRESENTS A DOMINANT POLE. WHERE SHOULD IT BE FOR AN AMPLIFIER TO BE STABLE FOR ALL VALUES OF (H)?



The purpose of adding the dominant pole is to assure the stability of the amplifier for all values of the feedback ratio "H"—the largest practical value is "1" when the full output signal is fed back to the input. For stability, the product $G(s)H(s)$ must be less than unity at 180° . The attenuation (negative gain) at 180° phase shift is known as the "gain margin" of the amplifier and is usually expressed in dB—similarly the difference between the phase shift at unity gain and 180° is known as the phase margin and is expressed in degrees. For practical purposes a gain margin 6dB and a phase margin of 35° are reasonable values which represent a compromise between excessive overshoot and mushiness in the loop response.

SOLVING EXPLICITLY FOR ω_D IN A SYSTEM WITH GREATER THAN THREE POLES IS CUMBERSOME AND TIME CONSUMING.



$$\frac{V_{OUT}}{V_{IN}} = 1 \angle 180^\circ = 1 \pm j0.0$$

Using a combination of analytical and graphical techniques the dominant pole is located at approximately 0.0005 rad/sec. The phase is plotted and for an open loop gain of unity or 0dB the open loop phase shift is just about 180° .

