SECTION 7

HIGH SPEED HARDWARE DESIGN TECHNIQUES

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ANALOG CIRCUIT SIMULATION

Walt Kester, Joe Buxton

In recent years there has been much pressure placed on system designers to verify their designs with computer simulations before committing to actual printed circuit board layouts and hardware. Simulating complex digital designs is extremely beneficial, and very often, the prototype phase can be eliminated entirely. However, bypassing the prototype phase in high-speed/high-performance analog or mixed-signal circuit designs can be risky for a number of reasons.

For the purposes of this discussion, an *analog* circuit is any circuit which uses ICs such as op amps, instrumentation amps, programmable gain amps (PGAs), voltage controlled amps (VCAs), log amps, mixers, analog multipliers, etc. A *mixed-signal* circuit is an A/D converter (ADC), D/A converter (DAC), or combinations of these in conjunction with some amount of digital signal processing which may or may not be on the same IC as the converters.

Consider a typical IC operational amplifier. It may contain some 20-40 transistors, almost as many resistors, and a few capacitors. A complete SPICE (Simulation Program with Integrated Circuit Emphasis, see Reference 1) model will contain all these components, and probably a few of the more important parasitic capacitances and spurious diodes formed by the various junctions in the op-amp chip. For high-speed ICs, the package and wirebond parasitics may also be included. This is the type of model that the IC designer uses to optimize the device during the design phase and is typically run on a CAD workstation. Because it is a detailed model, it will be referred to as a *micromodel*. In simulations, such a model will behave very much like the actual op-amp, but not exactly.

The IC designer uses transistor and other device models based on the actual process upon which the component is fabricated. Semiconductor manufacturers invest considerable time and money developing and refining these device models so that the IC designers can have a high degree of confidence that the first silicon will work and that mask changes (costing additional time and money) required for the final manufactured product are minimized.

However, these *device* models are not published, neither are the IC *micromodels*, as they contain proprietary information which would be of use to other semiconductor companies who might wish to copy or improve on the design. It would also take far too long for a simulation of a system containing several ICs (each represented by its own micromodel) to reach a useful result. SPICE micromodels of analog ICs often

fail to converge (especially under transient conditions), and multiple IC circuits make this a greater possibility.

For these reasons, the SPICE models of analog circuits published by manufacturers or software companies are *macromodels* (as opposed to *micromodels*), which simulate the major features of the component, but lack fine detail. Most manufacturers of linear ICs (including Analog Devices) provide these macromodels for components such as operational amplifiers, analog multipliers, references, etc. (Reference 2 and 3). These models represent *approximations* to the actual circuit, and parasitic effects such as package capacitance and inductance and PC board layout are rarely included. The models are designed to work with various versions of SPICE simulation programs such as PSpice® (Reference 4) and run on workstations or personal computers. The models are simple enough so that circuits using multiple ICs can be simulated in a reasonable amount of computation time and with good certainty of convergence. Consequently, SPICE modeling does not always reproduce the exact performance of a circuit and should always be verified experimentally using a carefully built prototype.

Finally, there are mixed-signal ICs such as A/D and D/A converters which have *no* SPICE models, or if they exist, the models do not simulate dynamic performance (Signal-to-noise, effective bits, etc.), and prototypes of circuits using them should always be built.

SPICE SIMULATIONS: MACROMODEL OR MICROMODEL?

	METHODOLOGY	ADVANTAGES	DISADVANTAGES
MACROMODEL	Ideal Elements Model the Device Behavior	Fast Simulation Time, Easy to Modify	May Not Model All Characteristics
MICROMODEL	Fully Characterized Transistor Level	Most Complete Model	Slow Simulation, Difficulty in Convergence Not Available to Customers

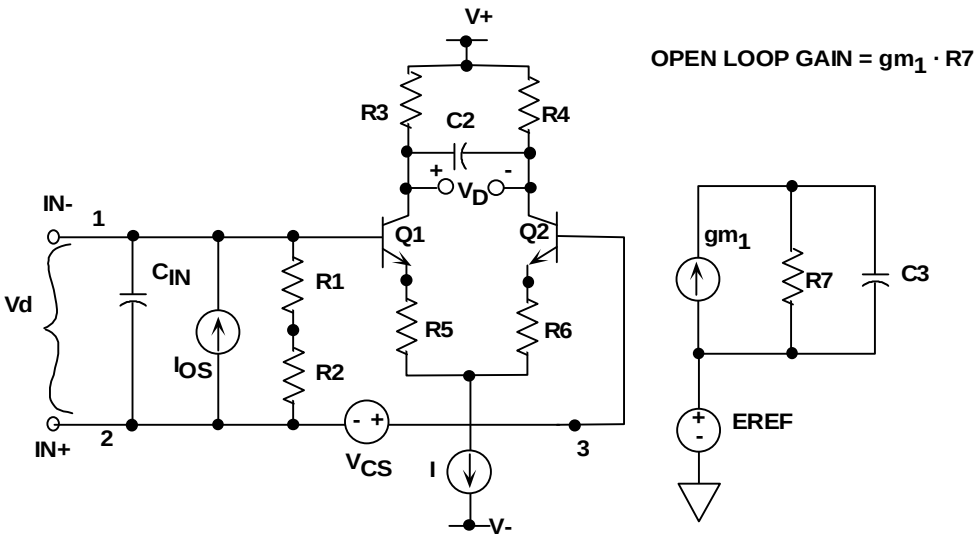
The ADSpice Model

The ADSpice model was developed to advance the state-of-the-art in op amp macromodelling and provide a tool for designers to simulate accurately their circuits. Previously, the dominant model architecture was the Boyle model (Reference 3). However, this model was developed over 20 years ago and does not accurately model many of today's higher speed amplifiers. The primary reason for this is that the Boyle model has only two frequency shaping poles and no zeroes. In contrast, the

ADSpice model has an open architecture that allows for unlimited poles and zeroes, leading to much more accurate AC and transient responses.

The ADSpice model is comprised of three main portions: the input and gain stage, the pole/zero stages, and the output stage. The input stage shown in Figure 7.2 uses the only two transistors in the entire model. These are needed to model properly an op amp's differential input stage characteristics. Although the example here uses NPN transistors, the input stage can easily be modified to include PNP, JFET, or CMOS devices. The rest of the input stage uses simple SPICE elements such as resistors, capacitors, and controlled sources.

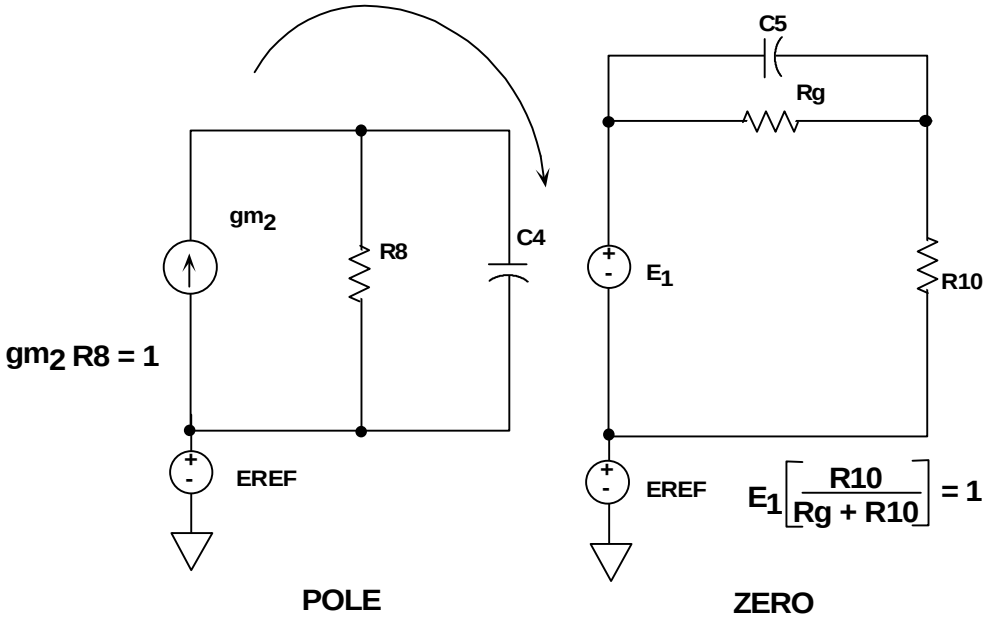
ADSpice INPUT AND GAIN STAGE MODEL



An example of a controlled source is gm_1 in the gain stage, which is a voltage controlled current source. It senses the differential collector voltage from the input stage and converts that to a current. When the current flows through R7, a single-ended voltage is produced. By making the product of gm_1 and R7 equal to the open loop gain, the entire open-loop gain is produced in the gain stage, which means that all other stages are set to unity gain. This leads to significant flexibility in adding and deleting stages.

Following the gain stage are an unlimited number of pole / zero stages and their combinations. The typical topology of these stages is shown in Figure 7.3, which is similar to the gain stage. The main difference is that now the product of gm_2 times R8 is equal to unity. The pole or zero frequency is set by the parallel combination of the resistor and capacitor, R8-C4 for the pole and Rg-C5 for the zero. Because these stages are unity gain, any number of them can be added or deleted without affecting the low frequency response of the model. Instead, the high frequency gain and phase response can be tailored to match accurately the actual amplifier's response. The benefits are especially apparent in closed loop pulse response and stability analysis.

POLE AND ZERO STAGE



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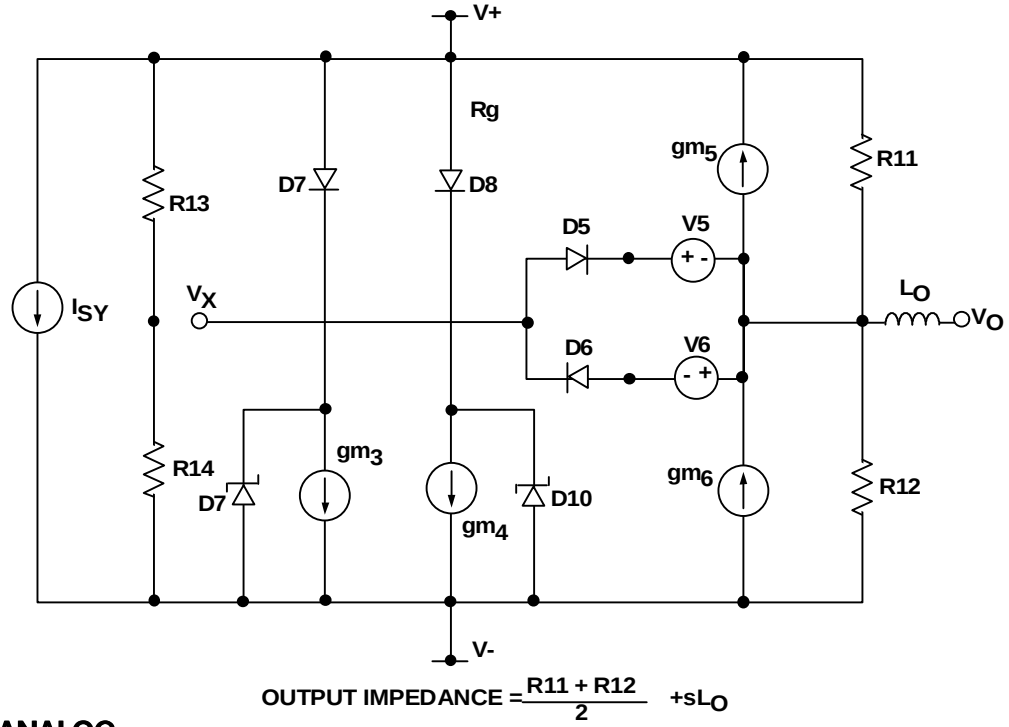
7.3

The output stage in Figure 7.4 not only models the open loop output impedance at DC but with the inclusion of an inductor also models the rise in impedance at high frequencies. Additionally, the output current is correctly reflected in the supply currents. This is a significant improvement over the Boyle model because now the power consumption of the circuit under load can be analyzed accurately. Furthermore, circuits that use the supply currents for feedback can also be simulated.



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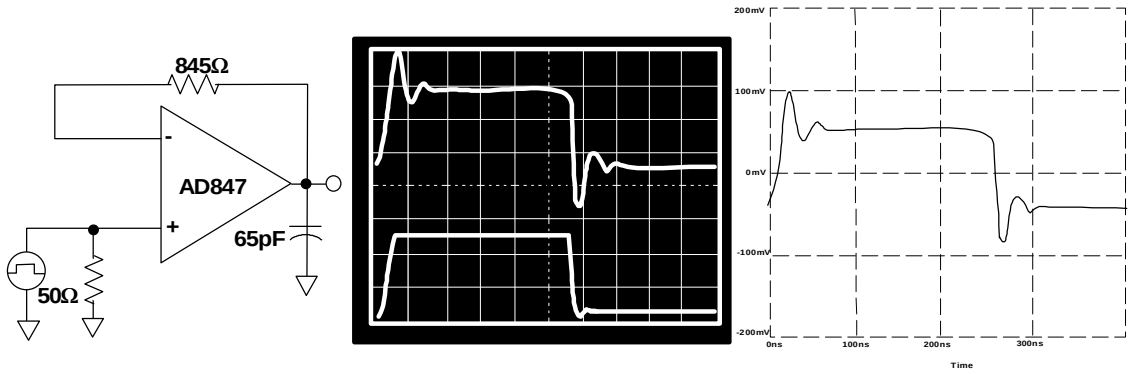
As an illustration of using the ADSpice model to predict circuit performance, the AD847 op amp (50MHz unity gain-bandwidth product) output was loaded in a 65pF capacitor and the response measured (both in ADSpice and in the circuit). The results shown in Figure 7.5 illustrate good correlation between the simulated and the actual response. As an additional example, extra parasitic capacitances were added as shown in Figure 7.6, and the simulated and actual responses compared. Again, note the excellent general agreement.

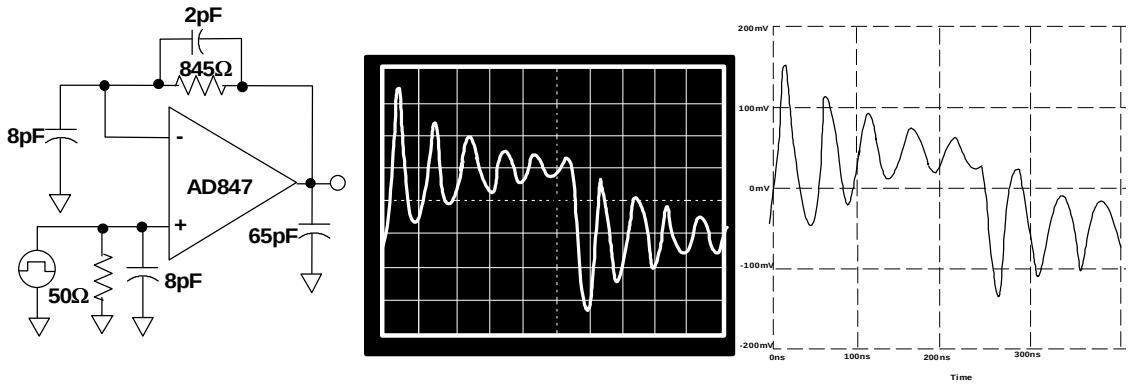
AD847 PULSE RESPONSE



(A) (B) (C)

Properly laid out PC board and simulation agree closely

PC BOARD PARASITICS WILL ALTER THE RESULTS



(A) (B) (C)

- **Parasitic capacitances worsen the circuit's response**
- **Properly modelling the parasitics in SPICE yields good results**

Other Features of ADSpice Models

In addition to offering models of op amps (both voltage and current feedback), which allow simulation of AC and DC performance, Analog Devices has included noise in many of its amplifier models. The capability to model a circuit's noise performance in SPICE can be appreciated by anyone who has tried to analyze noise by hand. A

complete analysis is a very involved and tedious task which requires calculating all the individual noise contributors and reflecting them to the input or output. The procedure is further complicated by the fact that noise gain is generally a function of frequency and can significantly affect results if not carefully considered.

To greatly simplify this task, the ADSpice model was enhanced to include noise generators which accurately predict the broadband and 1/f noise of the actual amplifier. Noise is currently modeled in a number of ADI op amps, variable gain amplifiers, and voltage references. For further discussion on the noise model details, see Reference 2.

In addition to amplifiers, ADSpice models exist for instrumentation amplifiers, analog multipliers, voltage references, analog switches, multiplexers, matched transistors, and buffers. A complete set of ADSpice models is available from Analog Devices upon request.

ADSpice will give good approximations to actual performance, if used correctly. However, the user must include the external components and parasitics which may affect the device performance in the circuit. This becomes a difficult task at frequencies much above 100MHz, and caution must be used in interpreting the simulation results. There is no substitute for prototyping at these frequencies.

While pulse and frequency response can be successfully simulated using the ADSpice models, distortion performance cannot be predicted since non-linear effects are not included in the models. As mentioned previously, models for ADCs and DACs are not available due to the difficulty in modeling their AC performance.

SUMMARY: ADSpice FEATURES

- **Transistor-Level Input Stage Model**
- **Unlimited Poles and Zeros**
- **Noise is Included in Some Models**
- **Distortion is not Modeled**
- **Over 500 Models Exist for:**
  - **Amplifiers**
  - **Instrumentation Amplifiers**
  - **Analog Multipliers**
  - **Voltage References**
  - **VCAs**
  - **Multiplexers and Switches**
- **But There is no Substitute for a Good Prototype!!**

PROTOTYPING TECHNIQUES
James Bryant, Walt Kester

The basic principle of a breadboard or prototype is that it is a *temporary* structure, designed to test the performance of a circuit or system, and must therefore be easy to modify.

There are many commercial prototyping systems, but almost all of them are designed to facilitate the prototyping of *digital* systems, where noise immunities are hundreds of millivolts or more. Non copper-clad Matrix board, Vectorboard, wire-wrap, and plug-in breadboard systems are, without exception, unsuitable for high performance or high frequency analog prototyping because their resistance, inductance, and capacitance are too high. Even the use of standard IC sockets is inadvisable in many prototyping applications.

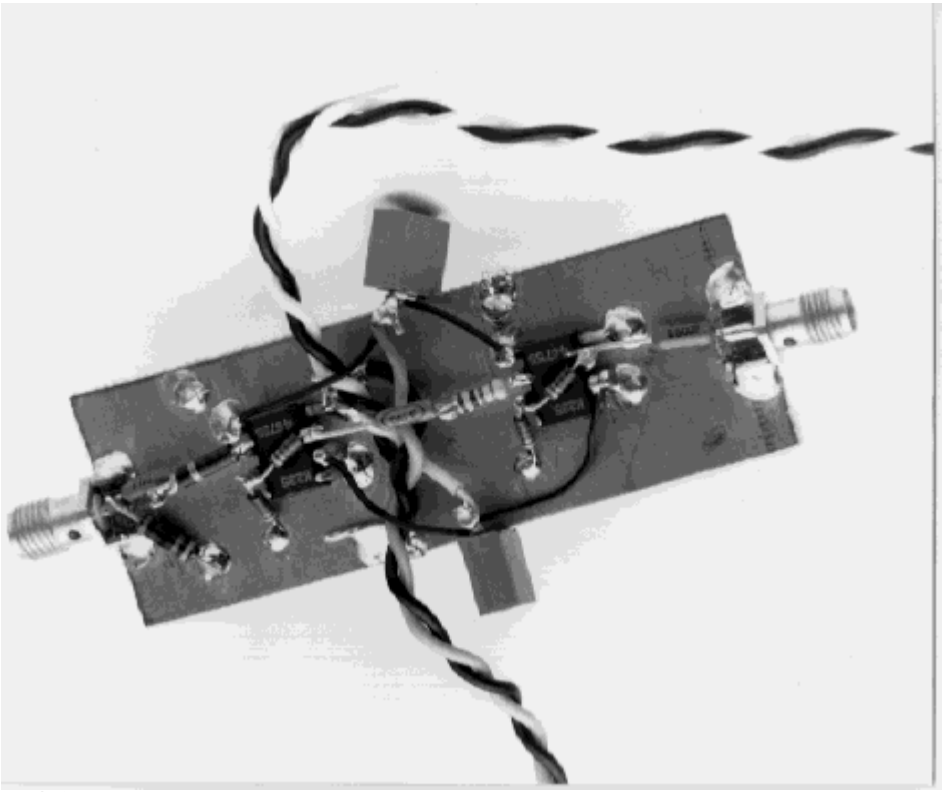
An important consideration in selecting a prototyping method is the requirement for a large-area ground plane. This is required for high frequency circuits as well as low speed precision circuits, especially when prototyping circuits involving ADCs or DACs. The differentiation between *high-speed* and *high-precision* mixed-signal circuits is difficult to make. For example, 16+ bit ADCs (and DACs) may operate on high speed clocks (>10MHz) with rise and fall times of less than a few nanoseconds, while the effective throughput rate of the converters may be less than 100kSPS. Successful prototyping of these circuits requires that equal attention be given to good high-speed and high-precision circuit techniques.

The simplest technique for analog prototyping uses a solid copper-clad board as a ground plane (Reference 5 and 6). The ground pins of the ICs are soldered directly to the plane, and the other components are wired together above it. This allows HF decoupling paths to be very short indeed. All lead lengths should be as short as possible, and signal routing should separate high-level and low-level signals. Connection wires should be located close to the surface of the board to minimize the possibility of stray inductive coupling. In most cases, 18-gauge or larger insulated wire should be used. Parallel runs should not be "bundled" because of possible coupling. Ideally the layout (at least the relative placement of the components on the board) should be similar to the layout to be used on the final PCB. This approach is often referred to as *deadbug prototyping* because the ICs are often mounted upside down with their leads up in the air (with the exception of the ground pins, which are bent over and soldered directly to the ground plane). The upside-down ICs look like deceased insects, hence the name.

Figure 7.8 shows a hand-wired breadboard using two high speed op amps which gives excellent performance in spite of its lack of esthetic appeal. The IC op amps are mounted upside down on the copper board with the leads bent over. The signals are connected with short point-to-point wiring. The characteristic impedance of a wire over a ground plane is about 120Ω, although this may vary as much as ±40% depending on the distance from the plane. The decoupling capacitors are connected directly from the op amp power pins to the copper-clad ground plane. When working at frequencies of several hundred MHz, it is a good idea to use only one side of the board for ground. Many people drill holes in the board and connect both sides together with short pieces of wire soldered to both sides of the board. If care is not

taken, however, this may result in unexpected ground loops between the two sides of the board, especially at RF frequencies.

"DEADBUG" PROTOTYPE



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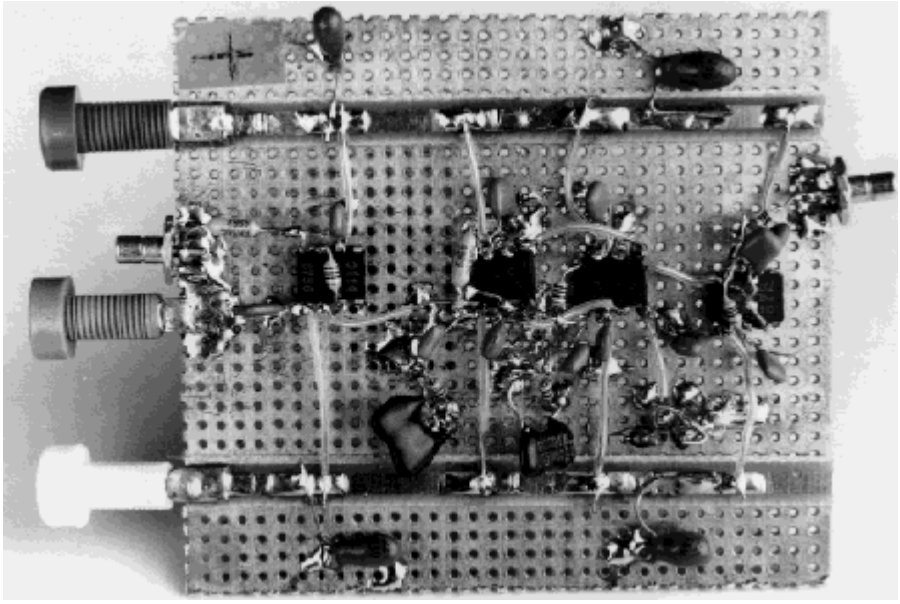
Pieces of copper-clad board may be soldered at right angles to the main ground plane to provide screening, or circuitry may be constructed on both sides of the board (with connections through holes) with the board itself providing screening. In this case, the board will need standoffs at the corners to protect the components on the underside from being crushed.

When the components of a breadboard of this type are wired point-to-point in the air (a type of construction strongly advocated by Robert A. Pease of National Semiconductor (Reference 6) and sometimes known as "bird's nest" construction) there is always the risk of the circuitry being crushed and resulting short-circuits. Also, if the circuitry rises high above the ground plane, the screening effect of the ground plane is diminished, and interaction between different parts of the circuit is more likely. Nevertheless, the technique is very practical and widely used because the circuit may easily be modified (assuming the person doing the modifications is adept at using a soldering iron, solder-wick, and a solder-sucker).

Another prototype breadboard is shown in Figure 7.9. The single-sided copper-clad board has pre-drilled holes on 0.1" centers (Reference 7). Power busses are at the top and bottom of the board. The decoupling capacitors are used on the power pins of each IC. Because of the loss of copper area due to the pre-drilled holes, this technique does not provide as low a ground impedance as a completely covered copper-clad board.

"DEADBUG" PROTOTYPE USING PRE-DRILLED SINGLE-SIDED COPPER-CLAD BOARD



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7.9

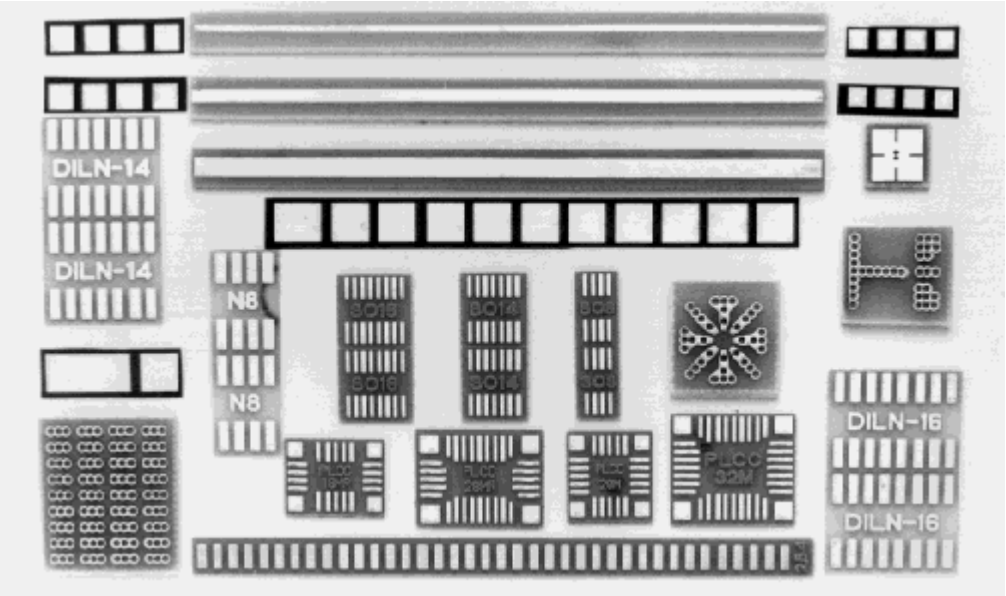
In a variation of this technique, the ICs and other components are mounted on the non-copper-clad side of the board. The holes are used as vias, and the point-to-point wiring is done on the copper-clad side of the board. The copper surrounding each hole used for a via must be drilled out to prevent shorting. This approach requires that all IC pins be on 0.1" centers. Low profile sockets can be used for low frequency circuits, and the socket pins allow easy point-to-point wiring.

There is a commercial breadboarding system which has most of the advantages of the above techniques (robust ground, screening, ease of circuit alteration, low capacitance and low inductance) and several additional advantages: it is rigid, components are close to the ground plane, and where necessary, node capacitances and line impedances can be calculated easily. This system is made by Wainwright Instruments and is available in Europe as "Mini-Mount" and in the USA (where the trademark "Mini-Mount" is the property of another company) as "Solder-Mount" (Reference 8).

Solder-Mount consists of small pieces of PCB with etched patterns on one side and contact adhesive on the other. These pieces are stuck to the ground plane, and components are soldered to them. They are available in a wide variety of patterns, including ready-made pads for IC packages of all sizes from 8-pin SOICs to 64-pin DILs, strips with solder pads at intervals (which intervals range from 0.040" to 0.25", the range includes strips with 0.1" pad spacing which may be used to mount DIL devices), strips with conductors of the correct width to form microstrip transmission lines (50Ω, 60Ω, 75Ω or 100Ω) when mounted on the ground plane, and a variety of pads for mounting various other components. Self-adhesive tinned

copper strips and rectangles (LO-PADS) are also available as tie-points for connections. They have a relatively high capacitance to ground and therefore serve as low-inductance decoupling capacitors. They come in sheet form and may be cut with a knife or scissors. A few of the many types of Solder-Mount building-block components are shown in Figure 7.10.

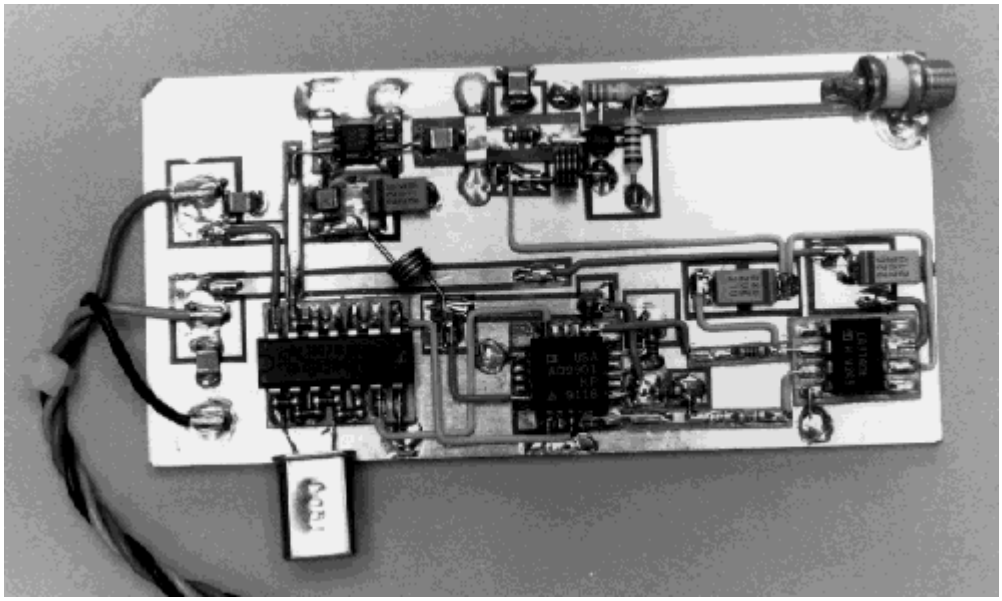
SAMPLES OF "SOLDER-MOUNT" COMPONENTS



The main advantage of Solder-Mount construction over "bird's nest" or "deadbug" is that the resulting circuit is far more rigid, and, if desired, may be made far smaller (the latest Solder-Mounts are for surface-mount devices and allow the construction of breadboards scarcely larger than the final PC board, although it is generally more convenient if the prototype is somewhat larger). Solder-Mount is sufficiently durable that it may be used for small quantity production as well as prototyping.

Figure 7.11 shows an example of a 2.5GHz phase-locked-loop prototype built with Solder-Mount. This is a high speed circuit, but the technique is equally suitable for the construction of high resolution low frequency analog circuitry. A particularly convenient feature of Solder-Mount at VHF is the ease with which it is possible to make a transmission line.

"SOLDER-MOUNT" PROTOTYPE



If a conductor runs over a ground plane, it forms a microstrip transmission line. The Solder-Mount components include strips which form microstrip lines when mounted on a ground plane (they are available with impedances of 50Ω, 60Ω, 75Ω, and 100Ω). These strips may be used as transmission lines, for impedance matching, or simply as power buses. (Glass fiber/epoxy PCB is somewhat lossy at VHF and UHF, but the losses will probably be tolerable if microstrip runs are short.)

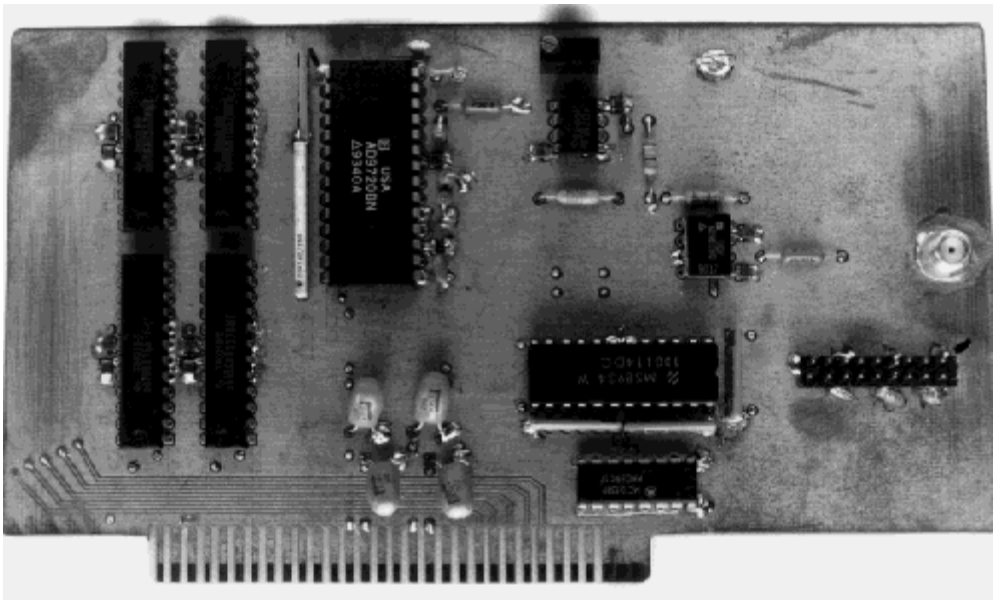
Both the "deadbug" and the "Solder-Mount" prototyping techniques become somewhat tedious for complex analog or mixed-signal circuits. Larger circuits are often better prototyped using more formal layout techniques.

An approach to prototyping more complex analog circuits is to actually lay out a double-sided board using CAD techniques. PC-based software layout packages offer ease of layout as well as schematic capture to verify connections (Reference 9). Although most layout software has some amount of auto-routing capability, this feature is best left to digital designs. After the components are placed in their desired positions, the interconnections should be routed manually following good analog layout guidelines. After the layout is complete, the software verifies the connections per the schematic diagram net list.

Many design engineers find that they can use CAD techniques to lay out simple boards themselves, or work closely with a layout person who has experience in analog circuit boards. The result is a pattern-generation tape (or Gerber file) which would normally be sent to a PCB manufacturing facility where the final board is made. Rather than use a PC board manufacturer, however, automatic drilling and milling machines are available which accept the PG tape directly (Reference 10). These systems produce single and double-sided circuit boards directly by drilling all holes and using a milling technique to remove copper and create insulation paths and finally, the finished board. The result is a board very similar to the final manufactured double-sided PC board, the chief exception being that there is no

"plated-through" hole capability, and any "vias" between the two layers of the board must be wired and soldered on both sides. Minimum trace widths of 25 mils (1 mil = 0.001") and 12 mil spacing between traces are standard, although smaller trace widths can be achieved with care. The minimum spacing between lines is dictated by the size of the milling bit, typically 10 to 12 mils. An example of such a prototype board is shown in Figure 7.12 (top view) and Figure 7.13 (bottom view).

"MILLED" PROTOTYPE - TOP VIEW



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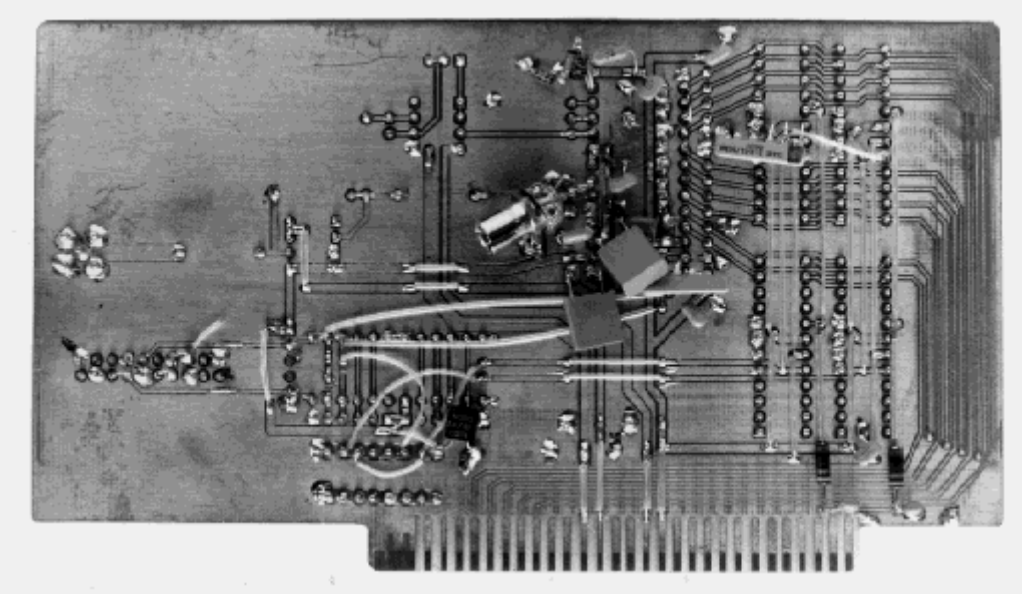
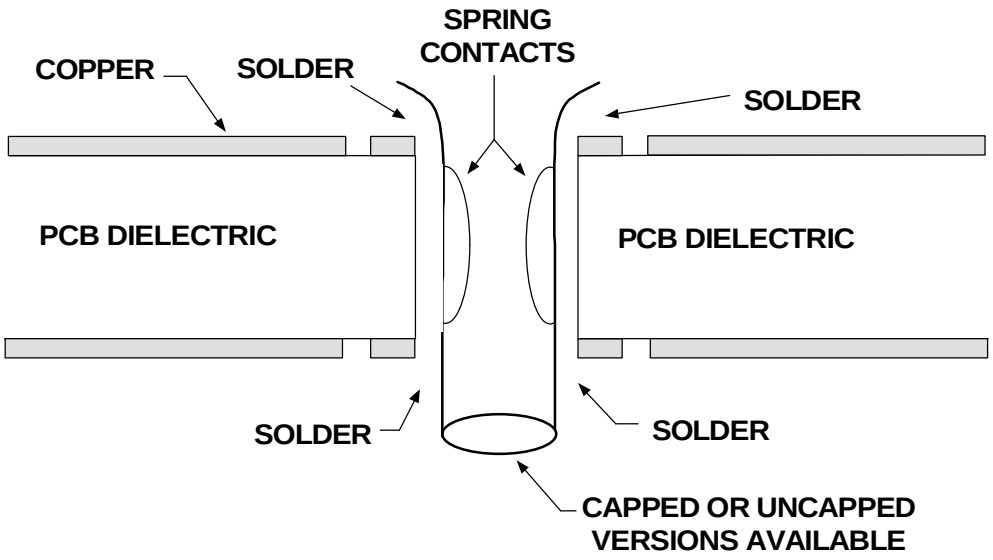
"MILLED" PROTOTYPE - BOTTOM VIEW



IC sockets can degrade the performance of high speed or high precision analog ICs. Although they make prototyping easier, even *low-profile* sockets often introduce enough parasitic capacitance and inductance to degrade the performance of the circuit. If sockets must be used in high speed circuits, an IC socket made of individual *pin sockets* (sometimes called *cage jacks*) mounted in the ground plane board may be acceptable (clear the copper, on both sides of the board, for about 0.5mm around each ungrounded pin socket and solder the grounded ones to ground on both sides of the board). Both capped and uncapped versions of these pin sockets are available (AMP part numbers 5-330808-3, and 5-330808-6, respectively). The pin sockets protrude through the board far enough to allow point-to-point wiring interconnections between them (see Figure 7.14).

The spring-loaded gold-plated contacts within the pin socket makes good electrical and mechanical connection to the IC pins. Multiple insertions, however, may degrade the performance of the pin socket. The uncapped versions allow the IC pins to extend out the bottom of the socket. After the prototype is functional and no further changes are to be made, the IC pins can be soldered directly to the bottom of the socket, thereby making a permanent and rugged connection.

PIN SOCKETS (CAGE JACKS) HAVE MINIMUM PARASITIC RESISTANCE, INDUCTANCE, AND CAPACITANCE



The prototyping techniques discussed so far have been limited to single or double-sided PC boards. Multilayer PC boards do not easily lend themselves to standard prototyping techniques. If multilayer board prototyping is required, one side of a double-sided board can be used for ground and the other side for power and signals. Point-to-point wiring can be used for additional runs which would normally be placed on the additional layers provided by a multi-layer board. However, it is difficult to control the impedance of the point-to-point wiring runs, and the high

frequency performance of a circuit prototyped in this manner may differ significantly from the final multilayer board.

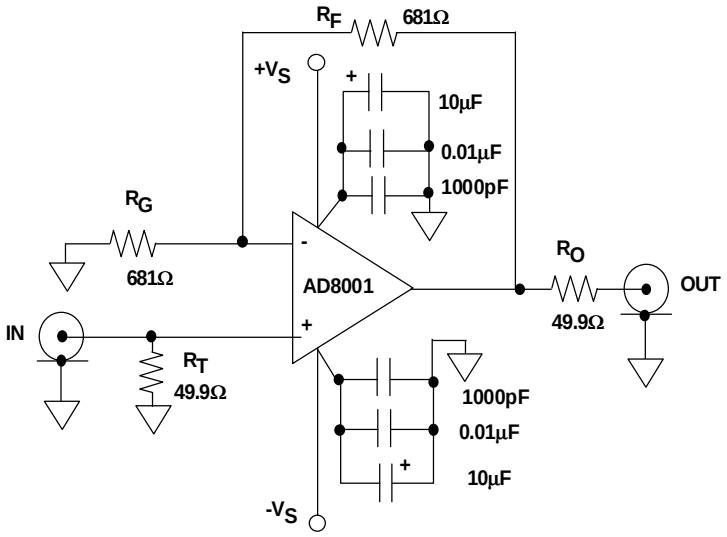
Other difficulties in prototyping may occur with op amps or other linear devices having bandwidths greater than a few hundred megahertz. Small variations in parasitic capacitance (<1pF) between the prototype and the final board may cause subtle differences in bandwidth and settling time. Oftentimes prototyping is done with DIP packages, when the final production package is an SOIC. This can account for differences between prototype and final PC board performance.

EVALUATION BOARDS
Walt Kester

Most manufacturers of analog ICs provide evaluation boards (usually at a nominal cost) which allow customers to evaluate products without constructing their own prototypes. Regardless of the product, the manufacturer has taken proper precautions regarding grounding, layout, and decoupling to ensure optimum device performance. The artwork or CAD file is usually made available free of charge, should the customer wish to copy the layout directly or make modifications to suit the application.

Figure 7.15 shows the schematic for the AD8001 (SOIC package) 800MHz op amp evaluation board. Figures 7.16 and 7.17, respectively, show the top and bottom side of the PCB. The amplifier is connected in the non-inverting mode. The top side (Figure 7.16) shows the top side of the SOIC package along with input and output SMA connectors. Notice that the ground plane is cut away around the SOIC in order to minimize parasitic capacitance. The bottom side of the board (Figure 7.17) shows the surface mount resistors and capacitors which comprise the op amp gain-setting and power supply decoupling circuits, respectively.

AD8001AR (SOIC) 800MHz OP AMP: NON-INVERTING MODE EVALUATION BOARD SCHEMATIC



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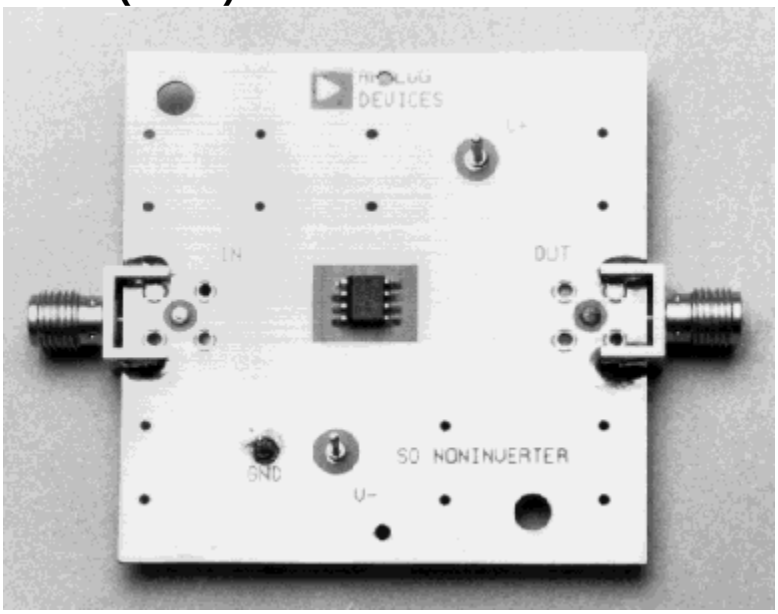
AD8001AR (SOIC) EVALUATION BOARD - TOP VIEW



ANALOG DEVICES

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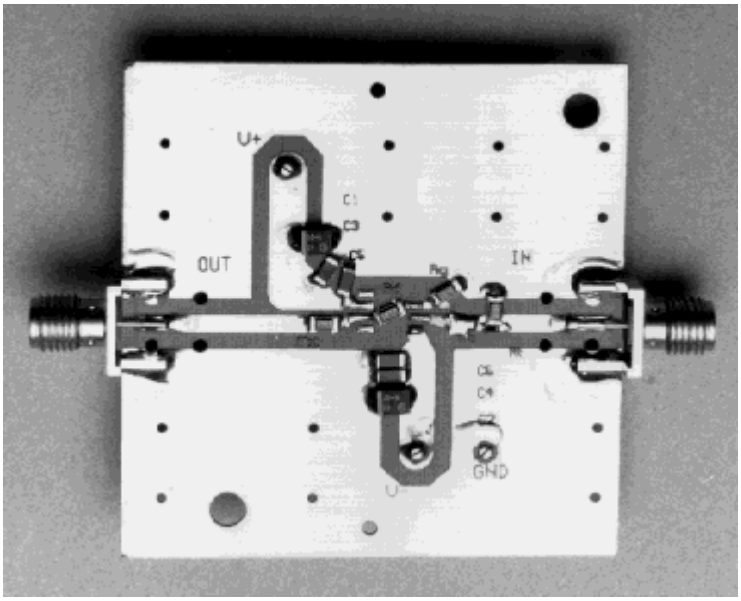
AD8001AR (SOIC) EVALUATION BOARD - BOTTOM VIEW



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In high speed/high precision ICs, special attention must be given to power supply decoupling. For example, fast slewing signals into relatively low impedance loads produce high speed transient currents at the power supply pins of an op amp. The transient currents, in turn, produce corresponding voltages across any parasitic impedance which may exist in the power supply traces. These voltages, in turn, may couple to the amplifier output because of the op amp's finite power supply rejection at high frequencies.

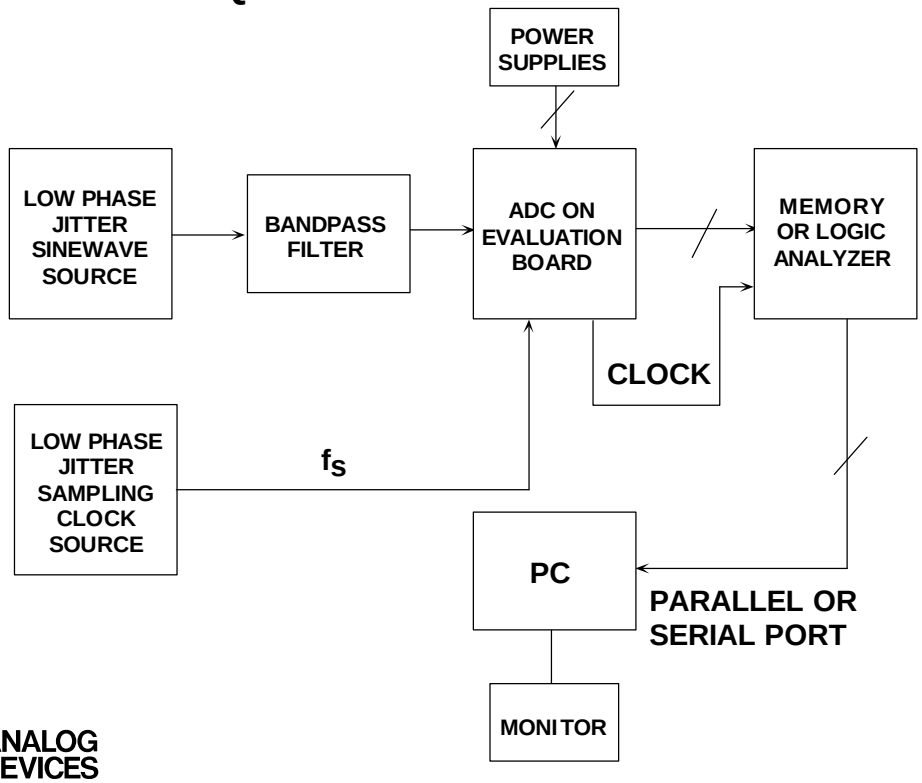
A three-capacitor decoupling scheme was chosen for the AD8001 evaluation board to ensure a low impedance path to ground at all transient frequencies. The highest frequency transients are shunted to ground by the 1000pF and the 0.01µF ceramic capacitors. These are located as close to the power supply pins as possible to minimize any series inductance and resistance. Because the devices are surface mount, there is minimum stray inductance and resistance in the path to the ground plane. The lower frequency transient currents are shunted to ground by the 10µF tantalum capacitors.

The input and output signal traces are of the AD8001 evaluation board are 50Ω microstrip transmission lines. Notice that there is considerable continuous ground plane area on both sides of the PCB. Plated-through holes connect the top and bottom side ground planes at several points in order to maintain low impedance ground continuity at high frequencies.

Evaluation boards can range from relatively simple ones (op amps, for example) to rather complex ones for mixed-signal ICs such as A/D converters. ADC evaluation boards often have on-board memory and DSPs for analyzing the ADC performance. Software is often provided with these more complex evaluation boards so that they can interface with a personal computer to perform complex signal analysis such as histogram and FFT testing.

Complete evaluations of ADCs requires the use of FFTs to fully characterize the devices AC performance. A typical test setup is shown in Figure 7.18. The manufacturer's evaluation board is used as a means for interfacing to the ADC. The evaluation board is designed to allow easy access to the ADC inputs and outputs while also providing a good layout (including all necessary references, buffer amplifiers, and decoupling). The evaluation board allows the ADC output data to be captured on a parallel output connector. Most ADC evaluation boards contain an on-board DAC which can be used to check the functionality of the ADC, but is somewhat limited in performing meaningful AC testing. A block diagram of the AD9042 (12-bits, 41MSPS) evaluation board is shown in Figure 7.19, and a photo in Figure 7.20.

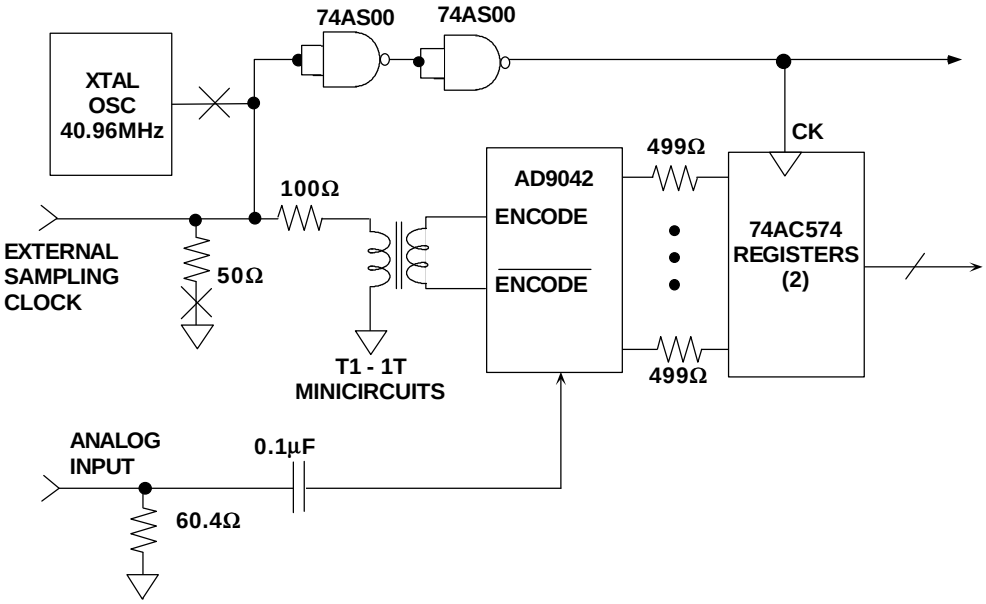
TEST SETUP REQUIRED TO EVALUATE HIGH SPEED ADCs



ANALOG DEVICES

7.18

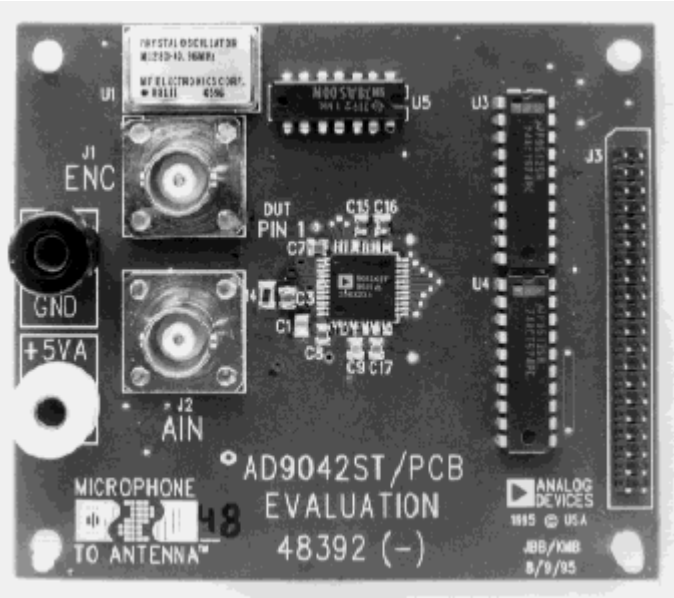
AD9042 12-BIT, 41MSPS ADC EVALUATION BOARD FUNCTIONAL DIAGRAM



ANALOG DEVICES

7.19

AD9042 EVALUATION BOARD - TOP VIEW



ANALOG DEVICES

7.20

The most complex part of the problem is usually designing the buffer memory module. A high speed logic analyzer is one method of capturing the ADC output data, and interfaces easily to the ADC evaluation board. Data from the logic analyzer can be loaded into a PC through either parallel or serial ports. Once the ADC data is inside the PC, software packages such as Mathcad can be used to perform the actual FFT.

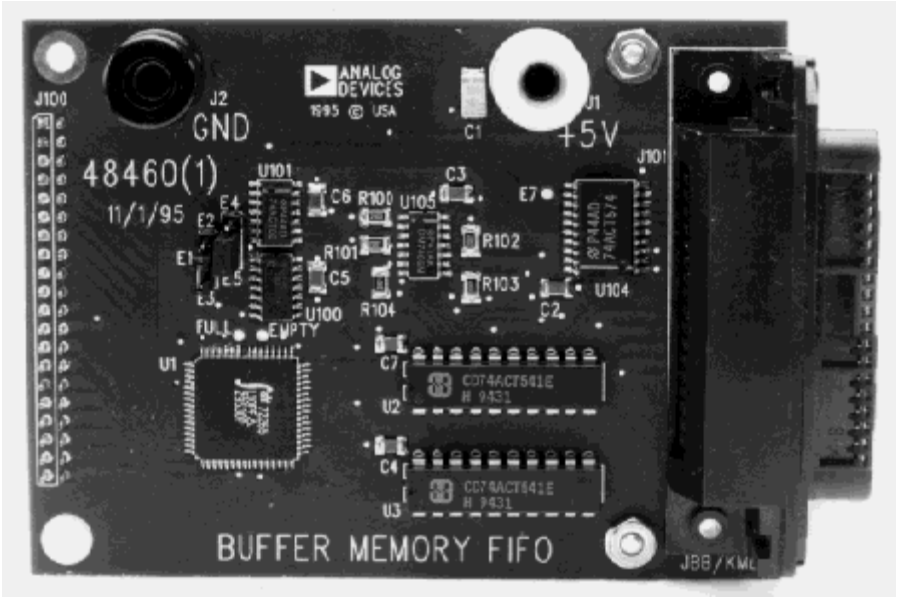
Another alternative is to use a commercially-available data acquisition module that plugs directly into a card slot of the PC. These modules come complete with FFT and other ADC test software, but are not easily portable from one PC to another and are generally difficult to interface with laptop computers.

Although fast and relatively low power memories (FIFOs) are available commercially, designing a buffer memory, the interfaces to the ADC and the PC, and the necessary software can be a time-consuming project. Analog Devices has designed a simple 16-bit by 16k deep 100MHz memory board (3 x 4 inches) and the necessary software to allow high speed ADC evaluation boards to interface directly with the parallel printer port of most PCs. The core of the memory design is the IDT72265 16k by 18-bit wide FIFO or alternately, the IDT72255 is an 8k pin compatible device which may be substituted if the deeper memory is not required.

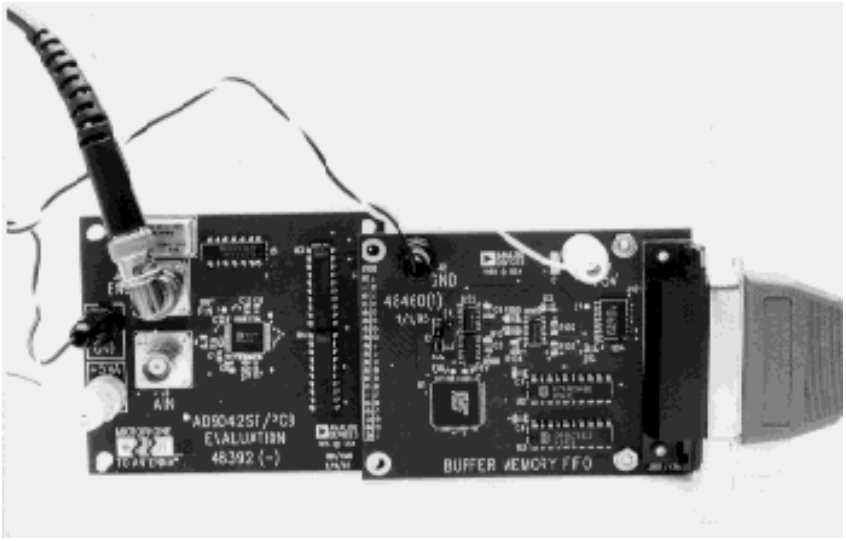
This FIFO chip features fully independent I/O ports that allow data to be loaded at up to 100MSPS and downloaded at the rate of a parallel printer port. Since the ports are independent, both can operate simultaneously, i.e., data may be read out while new data is being written. The chip takes care of all addressing, overhead and much of the hand-shaking for these operations. Included is circuitry that prevents unread data from being overwritten, eliminating the need for extensive write control circuitry.

A photograph of the *Fifo Memory* board is shown in Figure 7.21, and Figure 7.22 shows it connected to the AD9042 evaluation board.

BUFFER MEMORY FIFO BOARD - TOP VIEW

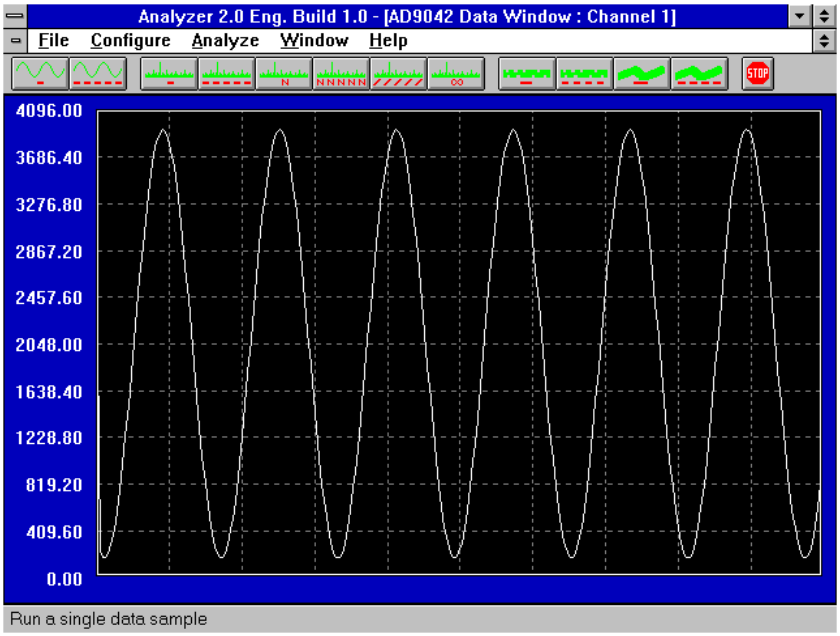


MEMORY BOARD / AD9042 EVALUATION BOARD

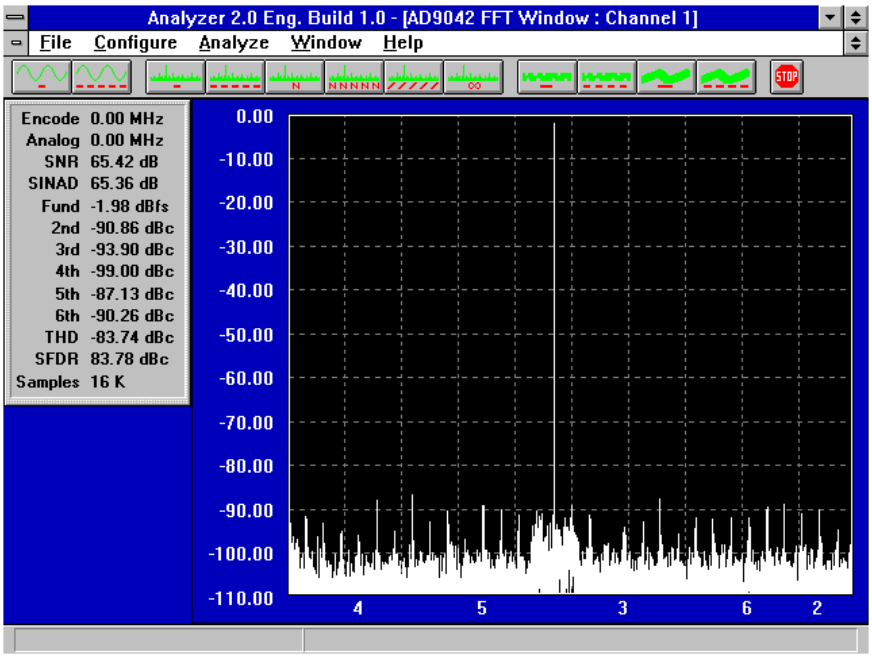


Using this hardware and Windows-based software to capture the ADC data, many testing possibilities exist. Figure 7.23 shown a time-domain plot of data captured using the fifo memory. Once the data is captured, FFT analysis (Figure 7.24) or DNL histograms (Figure 7.25) are easily generated.

DATA CAPTURE PC OUTPUT DISPLAY



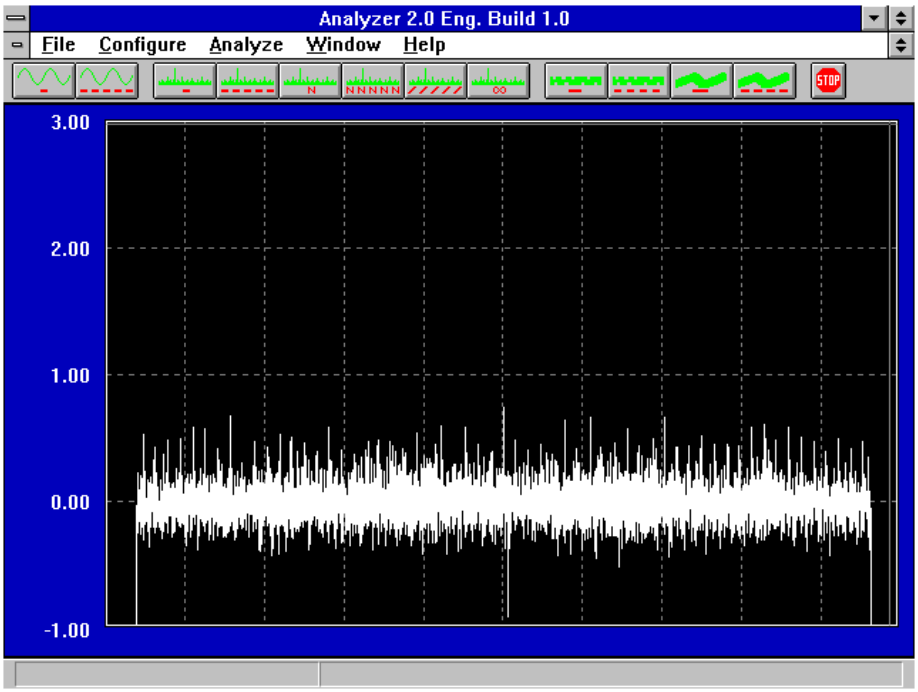
FFT OUTPUT



ANALOG DEVICES

7.24

DNL HISTOGRAM



ANALOG DEVICES

7.25

In summary, good analog designers utilize as many tools as possible to ensure that the final system design performs correctly. The first step is the intelligent use of IC macromodels, where available, to simulate the circuit. The second step is the construction of a prototype board to further verify the design and the simulation. The final PCB layout should be then be based on the prototype layout as much as possible.

Finally, evaluation boards can be extremely useful in evaluating new analog ICs, and allow designers to verify the IC performance with a minimum amount of effort. The layout of the components on the evaluation board can serve as a guide to both the prototype and the final PC board layout. Gerber files are generally available for all evaluation board layouts and may be obtained at no charge.

REFERENCES: SIMULATION, PROTOTYPING, AND EVALUATION BOARDS

1. Paolo Antognetti and Guiseppe Massobrio, Ed, **Semiconductor Device Modeling with SPICE**, McGraw Hill, 1988.

2. **Amplifier Applications Guide**, Section 13, Analog Devices, Inc., Norwood, MA, 1992.

3. Boyle, et al, *Macromodelling of Integrated Circuit Operational Amplifiers*, **IEEE Journal of Solid State Circuits**, Vol. SC-9, no.6, December 1974.

4. PSpice® Simulation software.
MicroSim Corporation, 20 Fairbanks, Irvine, CA 92718, 714-770-3022

5. Jim Williams, **High Speed Amplifier Techniques**, Linear Technology Application Note 47, August, 1991.

6. Robert A. Pease, **Troubleshooting Analog Circuits**, Butterworth-Heinemann, 1991.

7. Vector Electronic Company, 12460 Gladstone Ave., Sylmar, CA 91342, Tel. 818-365-9661, Fax. 818-365-5718.

8. Wainwright Instruments Inc., 69 Madison Ave., Telford, PA, 18969-1829, Tel. 215-723-4333, Fax. 215-723-4620.

   Wainwright Instruments GmbH, Widdersberger Strasse 14, DW-8138 Andechs-Frieding, Germany. Tel: +49-8152-3162, Fax: +49-8152-40525.

9. Schematic Capture and Layout Software:
   PADS Software, INC, 165 Forest St., Marlboro, MA, 01752 and ACCEL Technologies, Inc., 6825 Flanders Dr., San Diego, CA, 92121

10. Prototype Board Cutters:

    LPKF CAD/CAM Systems, Inc., 6190 Artic Dr, PO Box 6209, Beaverton, OR, 97005 and
    T-Tech, Inc., 5591-B New Peachtree Road, Atlanta, GA, 34341

11. Howard W. Johnson and Martin Graham, **High-Speed Digital Design**, PTR Prentice Hall, 1993.

12. **Practical Analog Design Techniques**, Analog Devices, 1995.